Load Store Unit

The Load Store Unit (LSU) has (by default) 4-inputs of which one can be selected for addressing and one as data input. All outputs are buffered and one of the (by default 2) outputs can be selected as the target register.

The LSU supports operations from both local (private to each LSU) and global (shared between LSUs). Currently all memories are considered to be single cycle but in the future an arbiter will be inserted between the global memory and the LSUs connected to it. This will also mean that we will have to implement some kind of stall signal.

On both the global and local memory the following operations can be performed:

- Load
- Store
- Load implicit
- Store implicit

Data Types

The LSU supports loading and storing multiple data types:

- DWORD (64-bit)
- WORD (32-bit)
- HWORD (16-bit)
- BYTE (8-bit)

However, the maximum supported width is equal to the datapath width (e.g. a 32-bit CGRA supports BYTE, HWORD and WORD).

Load and store

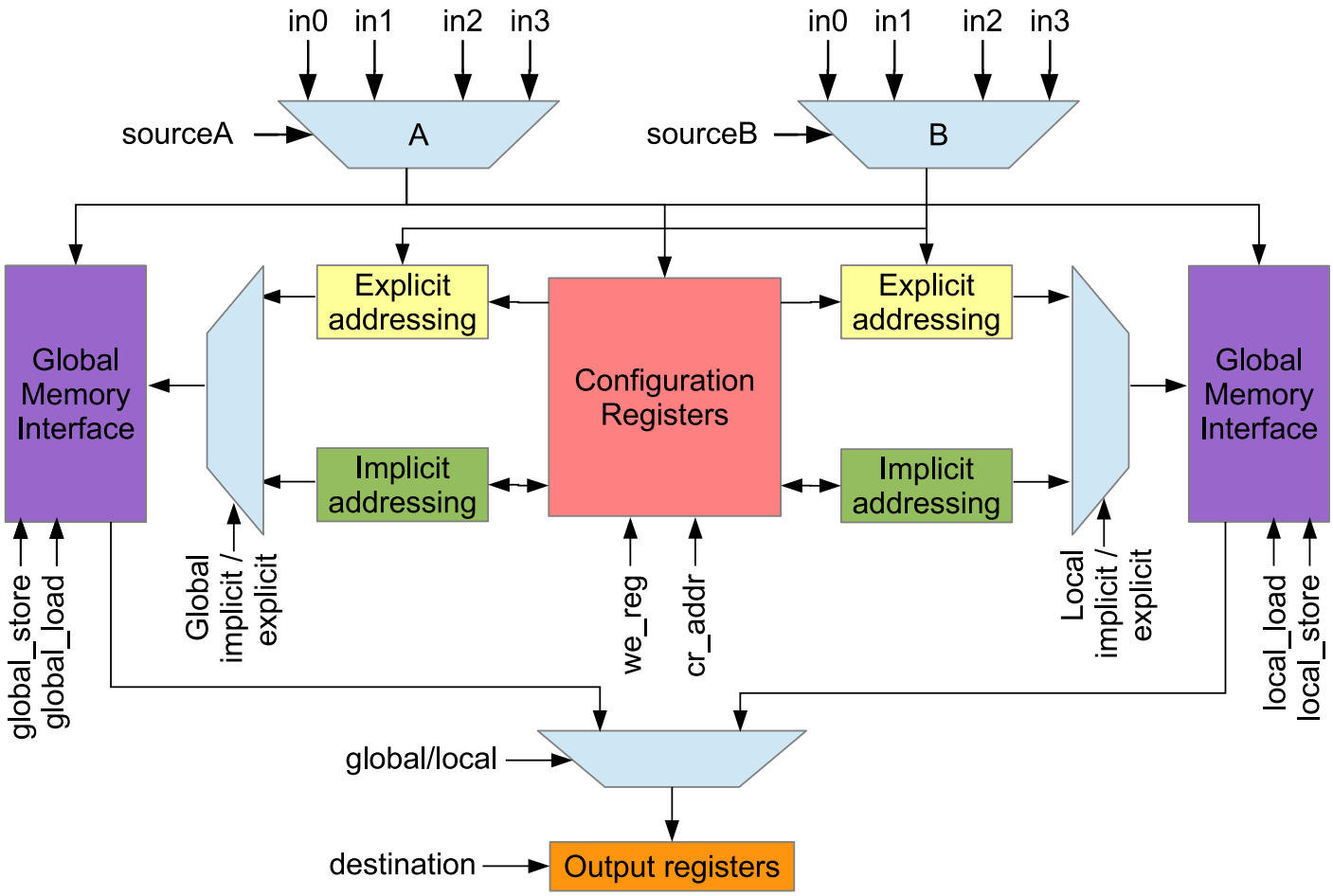
These operations take all their required information (address and data) from the inputs. Operand A is used for data and Operand B is used for addressing. Currently we consider the maximum address space of the local memory to be 16 bit and the address space of the global memory to be 32 bit. This means that e.g. a CGRA with a 8-bit data path cannot directly address all memory (both local and global) with addresses supplied from the data network. To overcome this, the LSU contains several configuration registers which also contain registers that hold the higher bytes/words of the addresses. The contents of these registers, together with the address supplied on the input will form the final memory address. With a 16-bit CGRA all local memory can be directly addressed and with a 32-bit CGRA all global memory can be directly addressed as well.

Implicit load and store

These operations use the configuration registers to implement some automatic address generation. The configuration registers allow to specify the start address and the stride. Each time an implicit operation is performed the address is incremented with the stride. This is done seperately for loads and stores and global and local accesses.
For the global memory the start address and the bytes for memory address extention (for 8-bit and 16-bit CGRAs) are shared, meaning that this address will increment with each implicit operation. For local memory the start address and memory address extention are separated.

Dual issue

Some operations that do not conflict with respect to input selection can be executed in parallel (e.g. a store on the local memory and a implicit load from the global memory). This allows for a higher memory bandwidth and for very efficient memory copy or shuffling. The operations that can be performed in parallel have a special instruction facilitating this (e.g. LGI_SLA), where the underscore denotes the simultaneous execution.



Picture source

LSU Configuration Registers

In order to overcome limitations related to data-path width and the width required to address the local- and global memories the Load Store Unit (LSU) has some configurtion registers. Additionally these registers can be used for implicit (automatically incrementing memory addresses) which allow parallel load and store operations.

The mapping of these configuration registers is as follows:

Register	Description
0	Start address for implicit local load operations (High byte in 8-bit datapath, not used for width larger than 8)
1	Start address for implicit local load operations (Low byte in 8-bit datapath)
2	Stride for implicit (local and global) load operations
3	Start address for implicit local store operations (High byte in 8-bit datapath, not used for width larger than 8)
4	Start address for implicit local store operations (Low byte in 8-bit datapath)
5	Stride for implicit (local and global) store operations
6	Global load address (also implicit counter) (byte 3 for W=8, unused for W=16, unused for W=32 and higher)
7	Global load address (byte 2 for W=8, unused for W=16, unused for W=32 and higher)
8	Global load address (byte 1 for W=8, word 1 for W=16, unused for

	W=32 and higher)
9	Global load address (byte 0 for W=8, word 0 for W=16, full for W=32 and higher)
10	Global store address (also implicit counter) (byte 3 for W=8, unused for W=16, unused for W=32 and higher)
11	Global store address (byte 2 for W=8, unused for W=16, unused for W=32 and higher)
12	Global store address (byte 1 for W=8, word 1 for W=16, unused for W=32 and higher)
13	Global store address (byte 0 for W=8, word 0 for W=16, full for W=32 and higher)
14	Local load address high byte (only for W=8)
15	Local store address high byte (only for W=8)