

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

ABSOLUTE MAXIMUM RATINGS

(All Voltages Are Referenced to Device Ground, Unless Otherwise Noted)

V _{CC}	+6V
EN1&2, EN3&4, EN, $\overline{\text{EN}}$	-0.3V to +6V
DI ₋	-0.3V to +6V
DO ₊ , DO ₋ (normal condition)	-0.3V to (V _{CC} + 0.3V)
DO ₊ , DO ₋ (power-off or three-state condition)	-0.3V to +6V
Driver Output Current per Pin	±150mA

Continuous Power Dissipation (T_A = +70°C)

16-Pin SO (derate 8.70mW/°C above +70°C)696mW

16-Pin TSSOP (derate 9.40mW/°C above +70°C)755mW

Operating Temperature Ranges

MAX303_EC_ 0°C to +70°C |

MAX303_EE_

 -40°C to +85°C |

Junction Temperature

 +150°C |

Storage Temperature Range

 -65°C to +160°C |

Lead Temperature (soldering, 10s)

 +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(3V ≤ V_{CC} ≤ 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER OUTPUT: DO₊, DO₋						
Differential Driver Output	V _{OD1}	R _L = 100Ω, Figure 1	2.0			V
	V _{OD2}	R _L = ∞, Figure 1			3.6	
	V _{OD3}	R _L = 3.9kΩ (for compliance with V.11), Figure 1			3.6	
Change in Differential Output Voltage	ΔV _{OD}	R _L = 100Ω (Note 2)	-0.4		+0.4	V
Driver Common-Mode Output Voltage	V _{OC}	R _L = 100Ω, Figure 1			3	V
Change in Common-Mode Voltage	ΔV _{OC}	R _L = 100Ω (Note 2)	-0.4		+0.4	V
Three-State Leakage Current	I _{OZ}	V _{OUT} = V _{CC} or GND, driver disabled			±10	μA
Output Leakage Current	I _{OFF}	V _{CC} = 0V, V _{OUT} = 3V or 6V			20	μA
Driver Output Short-Circuit Current	I _{SC}	V _{OUT} = 0V, V _{IN} = V _{CC} or GND (Note 3)	-150			mA
INPUTS: EN, $\overline{\text{EN}}$, EN1&2, EN3&4						
Input High Voltage	V _{IH}		2.0			V
Input Low Voltage	V _{IL}				0.4	V
Input Current	I _{LEAK}				±2	μA
Hot-Swap Driver Input Current	I _{HOTSWAP}	EN, $\overline{\text{EN}}$, EN1&2, EN3&4 (Note 4)			±200	μA
SUPPLY CURRENT						
Supply Current	I _{CC}	No load			100	μA
THERMAL PROTECTION						
Thermal-Shutdown Threshold	T _{SH}			160		°C
Thermal-Shutdown Hysteresis				10		°C
ESD Protection DO ₋		Human Body Model		±15		kV

2

MAXIM

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

MAX3030E-MAX3033E

SWITCHING CHARACTERISTICS—MAX3030E, MAX3032E

(3V ≤ V_{CC} ≤ 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay Low to High	t _{DPLH}	R _L = 100Ω, C _L = 50pF, Figures 2, 3		8	16	ns
Driver Propagation Delay High to Low	t _{DPHL}					
Differential Transition Time, Low to High	t _R	R _L = 100Ω, C _L = 50pF (10% to 90%), Figures 2, 3			10	ns
Differential Transition Time, High to Low	t _F					
Differential Skew (Same Channel) t _{DPLH} - t _{DPHL}	t _{SK1}	R _L = 100Ω, C _L = 50pF, V _{CC} = 3.3V			±2	ns
Skew Driver to Driver (Same Device)	t _{SK2}					
Skew Part to Part	t _{SK3}	R _L = 100Ω, C _L = 50pF, V _{CC} = 3.3V, ΔT _{MAX} = +5°C	20		5	ns
Maximum Data Rate						Mbps
Driver Enable to Output High	t _{DZH}	S2 closed, R _L = 500Ω, C _L = 50pF, Figures 4, 5			50	ns
Driver Enable to Output Low	t _{DZL}	S1 closed, R _L = 500Ω, C _L = 50pF, Figures 4, 5			50	ns
Driver Disable Time from Low	t _{DLZ}	S1 closed, R _L = 500Ω, C _L = 50pF, Figures 4, 5			50	ns
Driver Disable Time from High	t _{DHZ}	S2 closed, R _L = 500Ω, C _L = 50pF, Figures 4, 5			50	ns

SWITCHING CHARACTERISTICS—MAX3031E, MAX3033E

(3V ≤ V_{CC} ≤ 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay Low to High	t _{DPLH}	R _L = 100Ω, C _L = 50pF, Figures 2, 3		40	70	ns
Driver Propagation Delay High to Low	t _{DPHL}					
Differential Transition Time, Low to High	t _R	R _L = 100Ω, C _L = 50pF (10% to 90%), Figures 2, 3	15		50	ns
Differential Transition Time, High to Low	t _F					
Differential Skew (Same Channel) t _{DPLH} - t _{DPHL}	t _{SK1}	R _L = 100Ω, C _L = 50pF, V _{CC} = 3.3V			±10	ns
Skew Driver to Driver (Same Device)	t _{SK2}					

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

SWITCHING CHARACTERISTICS—MAX3031E, MAX3033E (continued)

($3V \leq V_{CC} \leq 3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Skew Part to Part	t_{SK3}	$R_L = 100\Omega$, $C_L = 50pF$, $V_{CC} = 3.3V$, $\Delta T_{MAX} = +5^\circ C$			18	ns
Maximum Data Rate			2			Mbps
Driver Enable to Output High	t_{DZH}	S2 closed, $R_L = 500\Omega$, $C_L = 50pF$, Figures 4, 5			100	ns
Driver Enable to Output Low	t_{DZL}	S1 closed, $R_L = 500\Omega$, $C_L = 50pF$, Figures 4, 5			100	ns
Driver Disable Time from Low	t_{DLZ}	S1 closed, $R_L = 500\Omega$, $C_L = 50pF$, Figures 4, 5			150	ns
Driver Disable Time from High	t_{DHZ}	S2 closed, $R_L = 500\Omega$, $C_L = 50pF$, Figures 4, 5			150	ns

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

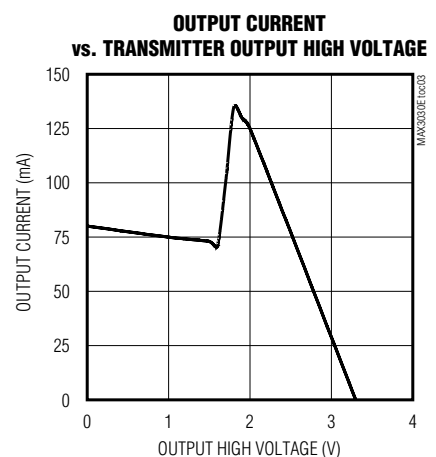
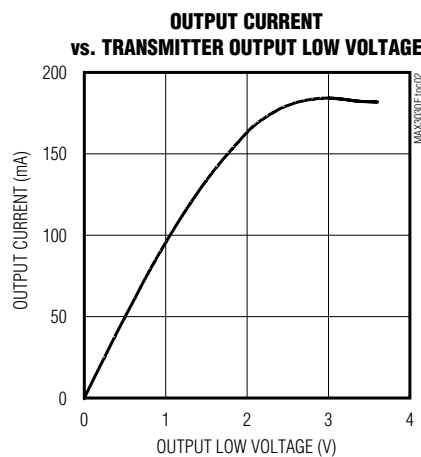
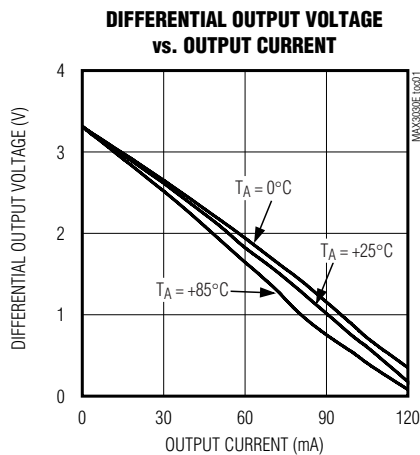
Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when DI changes state.

Note 3: Only one output shorted at a time.

Note 4: This input current is for the hot-swap enable (EN , \overline{EN}) inputs and is present until the first transition only. After the first transition, the input reverts to a standard high-impedance CMOS input with input current I_{LEAK} .

Typical Operating Characteristics

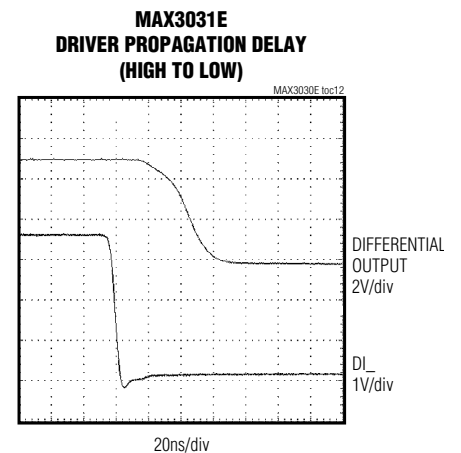
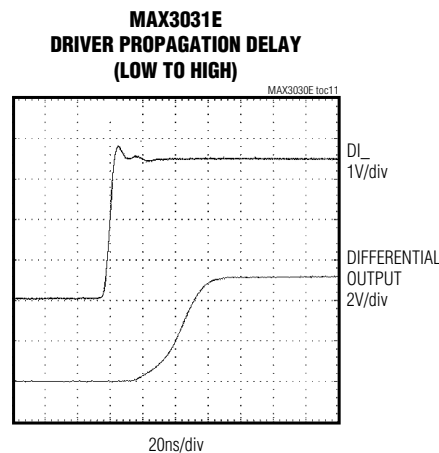
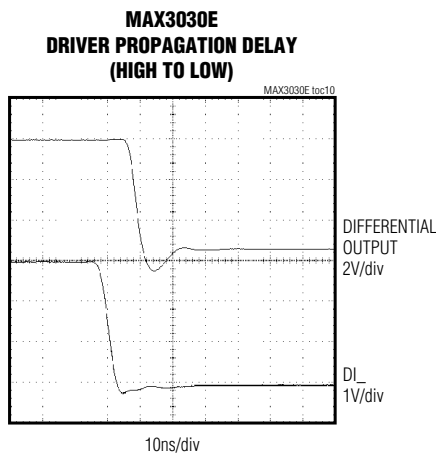
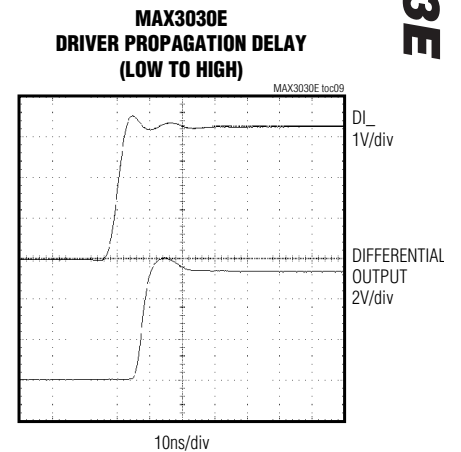
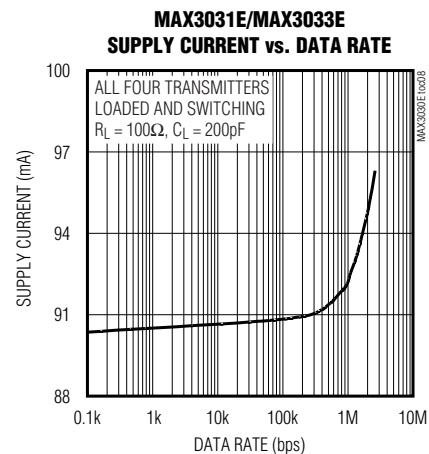
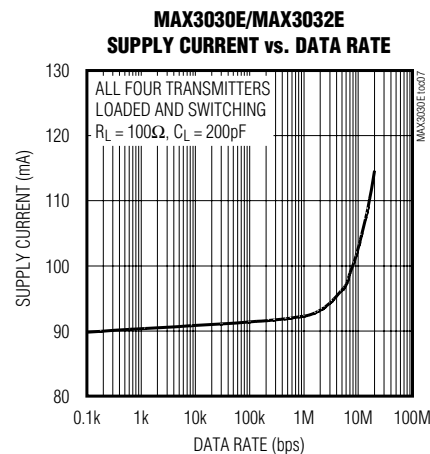
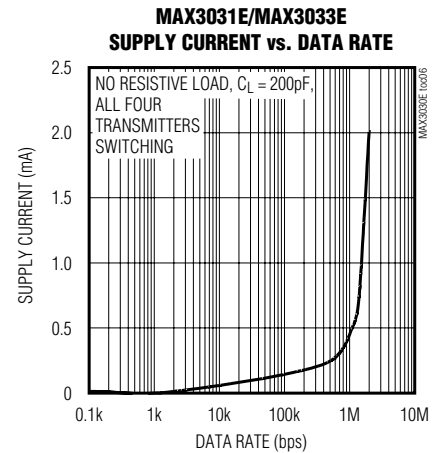
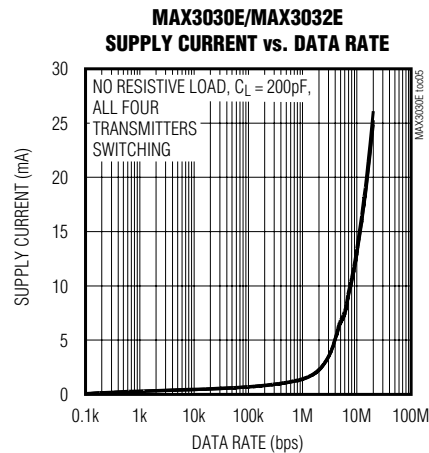
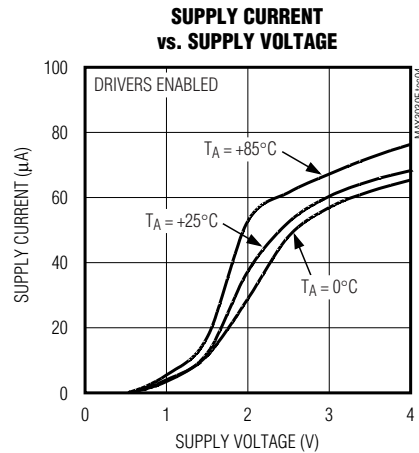
($V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.)



±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Typical Operating Characteristics (continued)

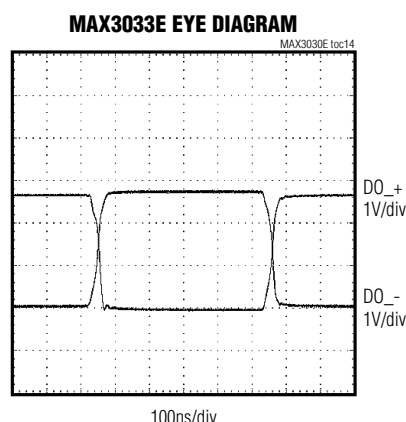
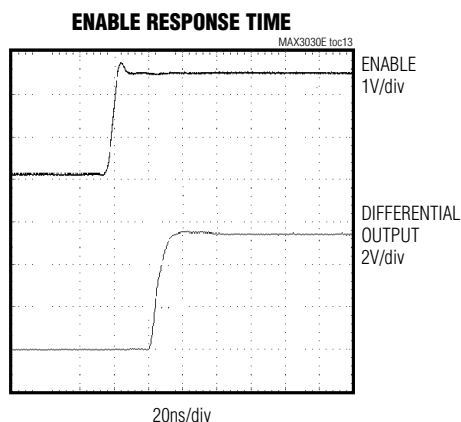
($V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.)



±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX3030E/ MAX3031E	MAX3032E/ MAX3033E		
1, 7, 9, 15	1, 7, 9, 15	DI1, DI2, DI3, DI4	Transmitter Inputs. When the corresponding transmitter is enabled, a low on DI _i forces the noninverting output low and inverting output high. Similarly, a high on DI _i forces noninverting output high and inverting output low.
2, 6, 10, 14	2, 6, 10, 14	DO1+, DO2+, DO3+, DO4+	Noninverting RS-422 Outputs
3, 5, 11, 13	3, 5, 11, 13	DO1-, DO2-, DO3-, DO4-	Inverting RS-422 Outputs
4	—	EN	Transmitter Enable Input: Active HIGH. Drive EN HIGH to enable all transmitters. When \overline{EN} is HIGH, drive EN LOW to disable (three-state) all the transmitters. The transmitter outputs are high impedance when disabled. EN is hot-swap protected (see the <i>Hot Swap</i> section).
8	8	GND	Ground
12	—	\overline{EN}	Transmitter Enable Input: Active LOW. Drive \overline{EN} LOW to enable all transmitters. When EN is LOW, drive \overline{EN} HIGH to disable all the transmitters. The transmitter outputs are high impedance when disabled. \overline{EN} is hot-swap protected (see the <i>Hot Swap</i> section).
—	4	EN1&2	Transmitter Enable Input for Channels 1 and 2. Drive EN1&2 HIGH to enable the corresponding transmitters. Drive EN1&2 LOW to disable the corresponding transmitters. The transmitter outputs are high impedance when disabled. EN1&2 is hot-swap protected (see the <i>Hot Swap</i> section).
—	12	EN3&4	Transmitter Enable Input for Channels 3 and 4. Drive EN3&4 HIGH to enable the corresponding transmitters. Drive EN3&4 LOW to disable the corresponding transmitters. The transmitter outputs are high impedance when disabled. EN3&4 is hot-swap protected (see the <i>Hot Swap</i> section).
16	16	V _{CC}	Positive Supply; $+3V \leq V_{CC} \leq +3.6V$. Bypass V _{CC} to GND with a 0.1μF capacitor.

MAX3030E-MAX3033E

The diagram illustrates the timing requirements for a differential signal. It shows three waveforms: DI , DO_- , and DO_+ . The DI signal is a square wave between 0V and 3V. The DO_- and DO_+ signals are differential signals with a common-mode voltage of V_0 . The setup time t_{DPLH} is the time from the DI signal falling to the DO_- signal reaching V_0 . The hold time t_{DPHL} is the time from the DI signal rising to the DO_+ signal reaching V_0 . The differential voltage V_{DIFF} is defined as $V_{DIFF} = V(DO_+) - V(DO_-)$. The rise time t_R and fall time t_F are shown for the V_{DIFF} signal, with 10% and 90% level markers. The skew t_{SKEW} is the difference between the setup and hold times: $t_{SKEW} = |t_{DPLH} - t_{DPHL}|$.

ENABLE SIGNAL IS ONE OF THE POSSIBLE
ENABLE CONFIGURATIONS (SEE TRUTH TABLE).

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The diagram shows a differential amplifier circuit. The non-inverting input (+) is connected to a voltage source V_{CC} through a resistor labeled DI . The inverting input (-) is connected to ground. The output of the amplifier is connected to two current sources, both labeled A , which are connected to ground. The output voltage is labeled DO_{-+} .

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Test Circuits and Timing Diagrams (continued)

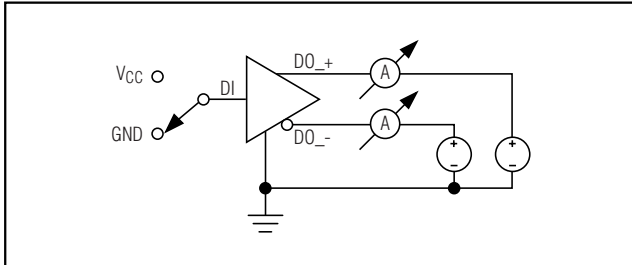


Figure 7. Power-Off Measurements

Detailed Description

The MAX3030E-MAX3033E are high-speed quad RS-422 transmitters designed for digital data transmission over balanced lines. They are designed to meet the requirements of TIA/EIA-422-B and ITU-T V.11. The MAX3030E-MAX3033E are available in two pinouts to be compatible with both the 26LS31 and SN75174 industry-standard devices. Both are offered in 20Mbps and 2Mbps baud rate. All versions feature a low-static current consumption ($I_{CC} < 100\mu A$) that makes them ideal for battery-powered and power-conscious applications. The 20Mbps version has a maximum propagation delay of 16ns and a part-to-part skew less than 5ns, allowing these devices to drive parallel data. The 2Mbps version is slow-rate-limited to reduce EMI and reduce reflections caused by improperly terminated cables.

Outputs have enhanced ESD protection providing ±15kV tolerance. All parts feature hot-swap capability that eliminates false transitions on the data cable during power-up or hot insertion.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation and power-down. After an ESD event, the MAX3030E-MAX3033E keep working without latchup. ESD protection can be tested in various ways; the

transmitter outputs of this product family are characterized for protection to ±15kV using the Human Body Model. Other ESD test methodologies include IEC10004-2 Contact Discharge and IEC1000-4-2 Air-Gap Discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

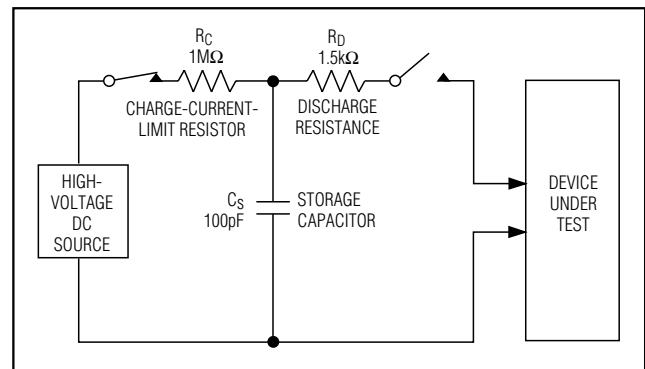


Figure 8. Human Body ESD Test Model

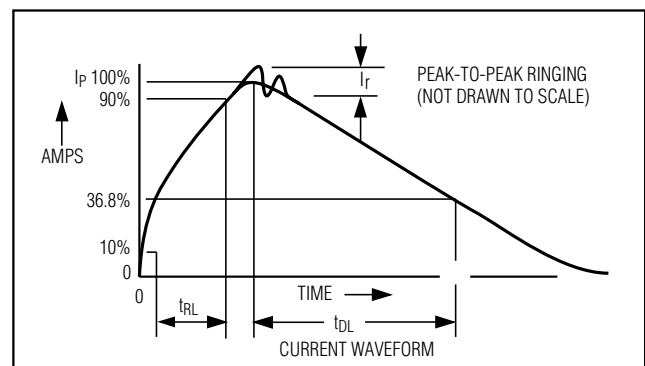


Figure 9. Human Body Current Waveform

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Hot Swap

When circuit boards are plugged into a “hot” backplane, there can be disturbances to the differential signal levels that could be detected by receivers connected to the transmission line. This erroneous data could cause data errors to an RS-422 system. To avoid this, the MAX3030E–MAX3033E have hot-swap capable inputs.

When a circuit board is plugged into a “hot” backplane, there is an interval during which the processor is going through its power-up sequence. During this time, the processor's output drivers are high impedance and are unable to drive the enable inputs of the MAX3030E–MAX3033E (EN, $\overline{\text{EN}}$, EN_) to defined logic levels. Leakage currents from these high-impedance drivers, of as much as 10 μA , could cause the enable inputs of the MAX3030E–MAX3033E to drift high or low. Additionally, parasitic capacitance of the circuit board could cause capacitive coupling of the enable inputs to either GND or VCC. These factors could cause the enable inputs of the MAX3030E–MAX3033E to drift to levels that may enable the transmitter outputs. To avoid this problem, the hot-swap input provides a method of holding the enable inputs of the MAX3030E–MAX3033E in the disabled state as VCC ramps up. This hot-swap input is able to overcome the leakage currents and parasitic capacitances that can pull the enable inputs to the enabled state.

Hot-Swap Input Circuitry

In the MAX3030E–MAX3033E, the enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 10). When VCC is ramping up from zero, an internal 6 μs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a 100 μA current sink, pull EN to GND through a 5.6k Ω resistor. M2 is designed to pull the EN input to the disabled state against an external parasitic capacitance of up to 100pF that is trying to enable the EN input. After 6 μs , the timer turns M2 off and M1 remains on, holding the EN input low against three-state output leakages that might enable EN. M1 remains on until an external source overcomes the required input

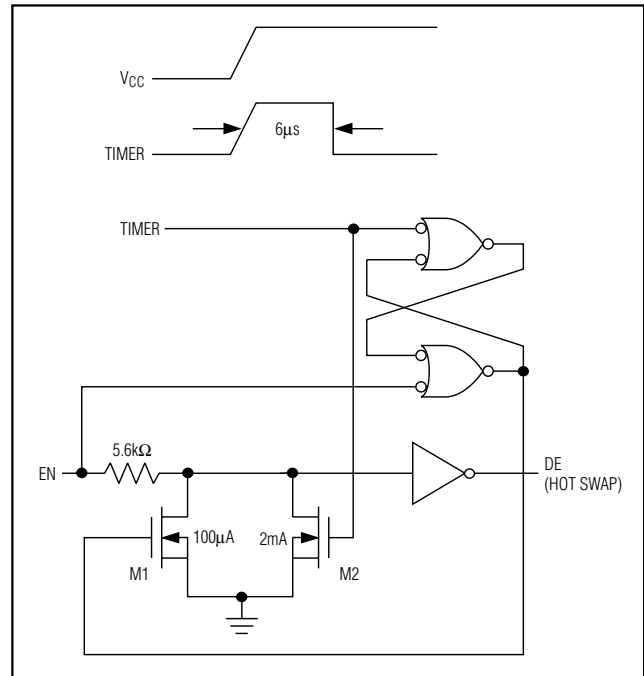


Figure 10. Simplified Structure of the Driver Enable Pin (EN)

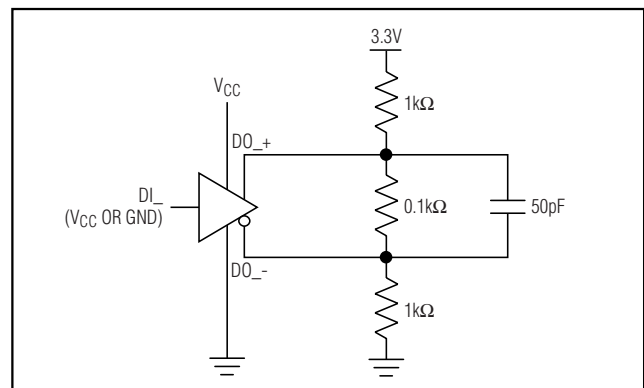


Figure 11. Differential Power-Up Glitch (Hot Swap)

current. At this time the SR latch resets and M1 turns off. When M1 turns off, EN reverts to a standard, high-impedance CMOS input. Whenever VCC drops below 1V, the hot-swap input is reset. The EN1&2 and EN3&4 input structures are identical to the EN input. For the $\overline{\text{EN}}$ input, there is a complementary circuit employing two PMOS devices pulling the $\overline{\text{EN}}$ input to VCC.

Hot-Swap Line Transient

The circuit of Figure 11 shows a typical offset termination used to guarantee a greater than 200mV offset when a line is not driven. The 50pF capacitor repre-

$\pm 15\text{kV}$ ESD-Protected, 3.3V Quad RS-422 Transmitters

sents the minimum parasitic capacitance that would exist in a typical application. In most cases, more capacitance exists in the system and reduces the magnitude of the glitch. During a “hot-swap” event when the driver is connected to the line and is powered up, the driver must not cause the differential signal to drop below 200mV (Figures 12 and 13).

Operation of Enable Pins

The MAX3030E-MAX3033E family has two enable-functional versions.

The MAX3030E/MAX3031E are compatible with 26LS31, where the two enable signals control all four transmitters (global enable).

The MAX3032E/MAX3033E are compatible with the SN75174. EN1&2 controls transmitters 1 and 2, and EN 3&4 controls transmitters 3 and 4 (dual enable).

Typical Applications

The MAX3030E-MAX3033E offer optimum performance when used with the MAX3094E/MAX3096 3.3V quad differential line receivers. Figure 14 shows a typical RS-422 connection for transmitting and receiving data.

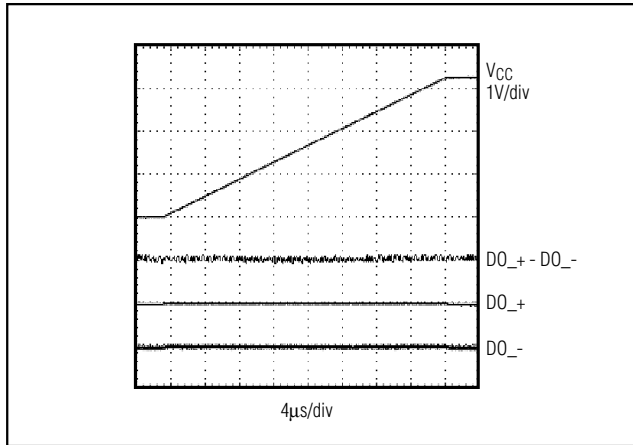


Figure 12. Differential Power-Up Glitch (0.1V/μs)

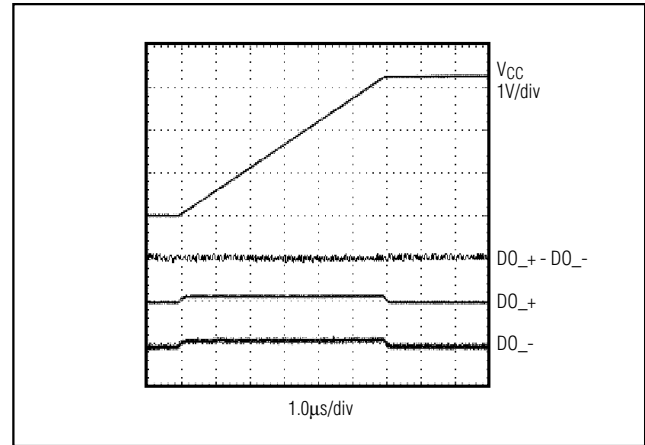


Figure 13. Differential Power-Up Glitch (1V/μs)

Table 1. MAX3030E/MAX3031E Transmitter Controls

EN	$\overline{\text{EN}}$	TX1	TX2	TX3	TX4	MODE
0	0	Active	Active	Active	Active	All transmitters active
0	1	High-Z	High-Z	High-Z	High-Z	All transmitters disabled
1	0	Active	Active	Active	Active	All transmitters active
1	1	Active	Active	Active	Active	All transmitters active

Table 2. MAX3032E/MAX3033E Transmitter Controls

EN1&2	EN3&4	TX1	TX2	TX3	TX4	MODE
0	0	High-Z	High-Z	High-Z	High-Z	All transmitters disabled
0	1	High-Z	High-Z	Active	Active	Tx 3 and 4 active
1	0	Active	Active	High-Z	High-Z	Tx 1 and 2 active
1	1	Active	Active	Active	Active	All transmitters active

$\pm 15\text{kV}$ ESD-Protected, 3.3V Quad RS-422 Transmitters

MAX3030E-MAX3033E

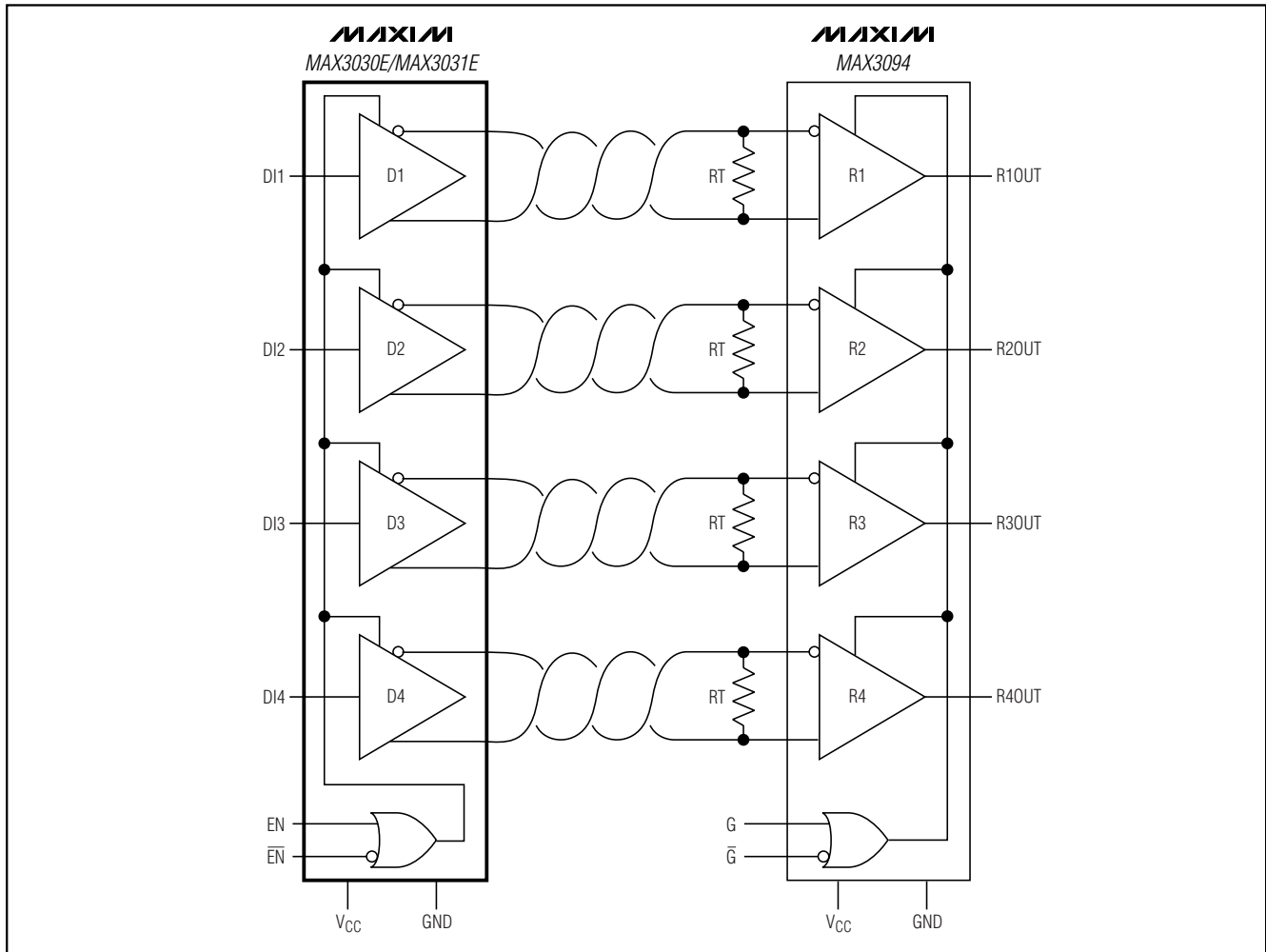


Figure 14. Typical Connection of a Quad Transmitter and Quad Receiver as a Pair

$\pm 15\text{kV}$ ESD-Protected, 3.3V Quad RS-422 Transmitters

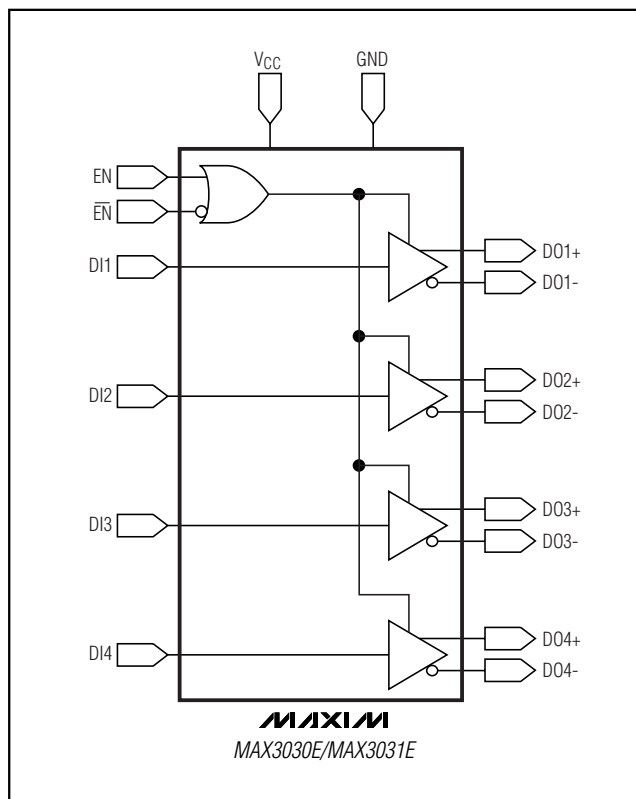


Figure 15. MAX3030E/MAX3031E Functional Diagram

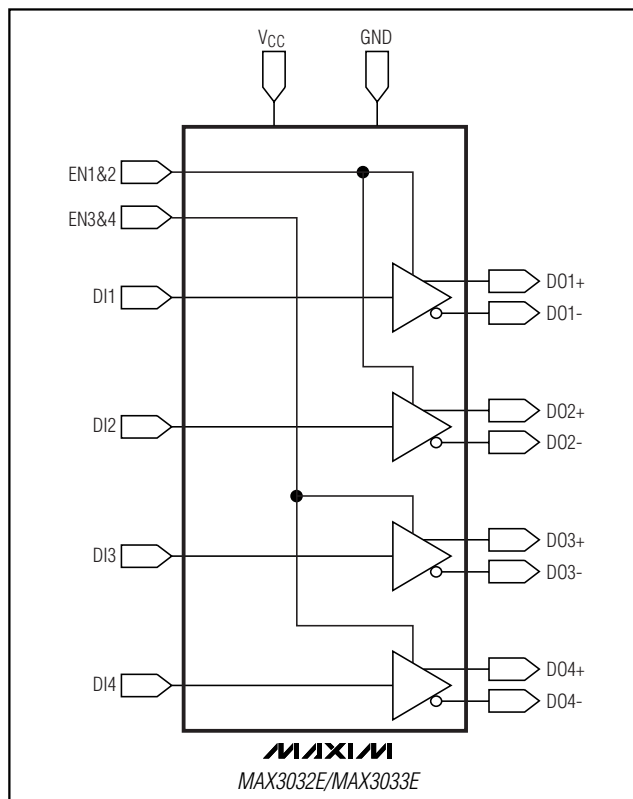


Figure 16. MAX3032E/MAX3033E Functional Diagram

Chip Information

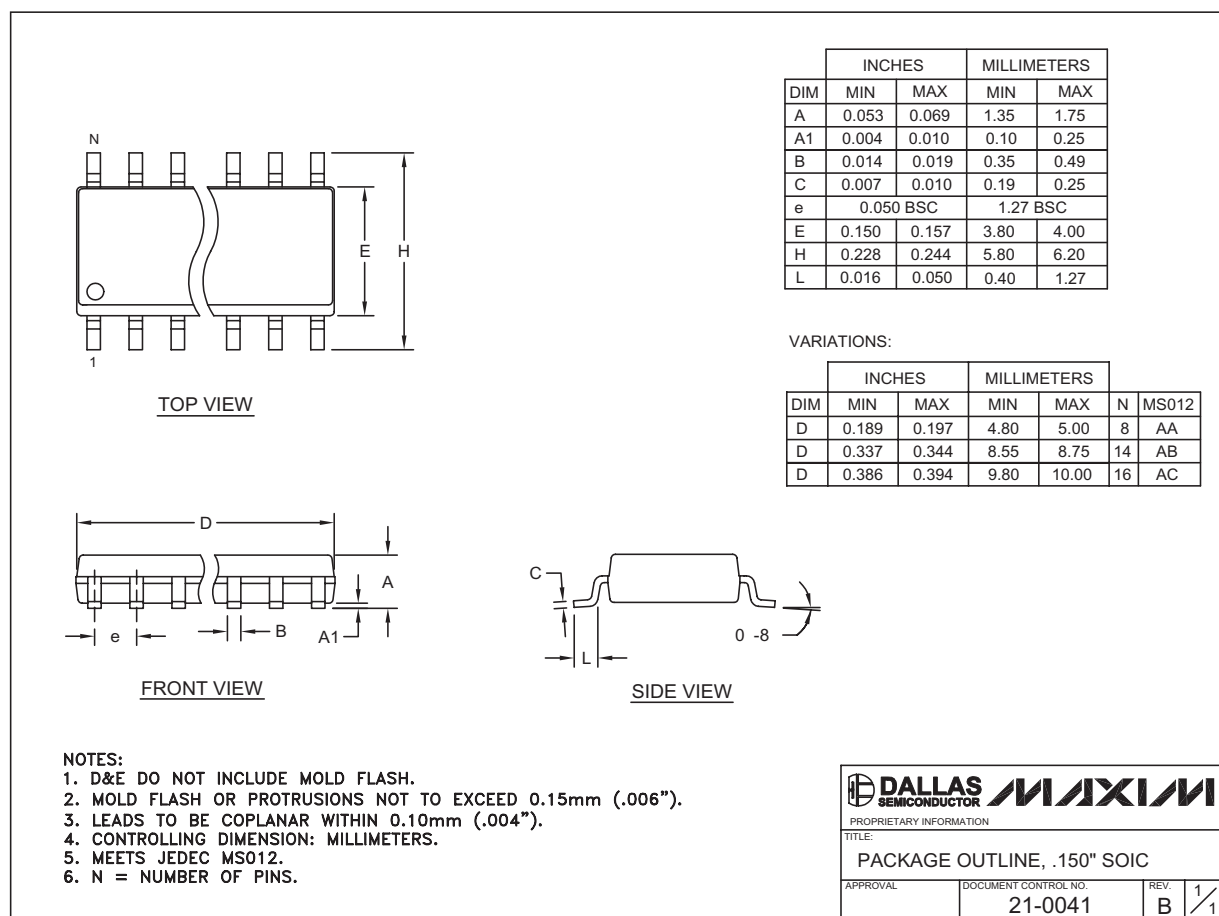
TRANSISTOR COUNT: 1050

PROCESS: BiCMOS

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



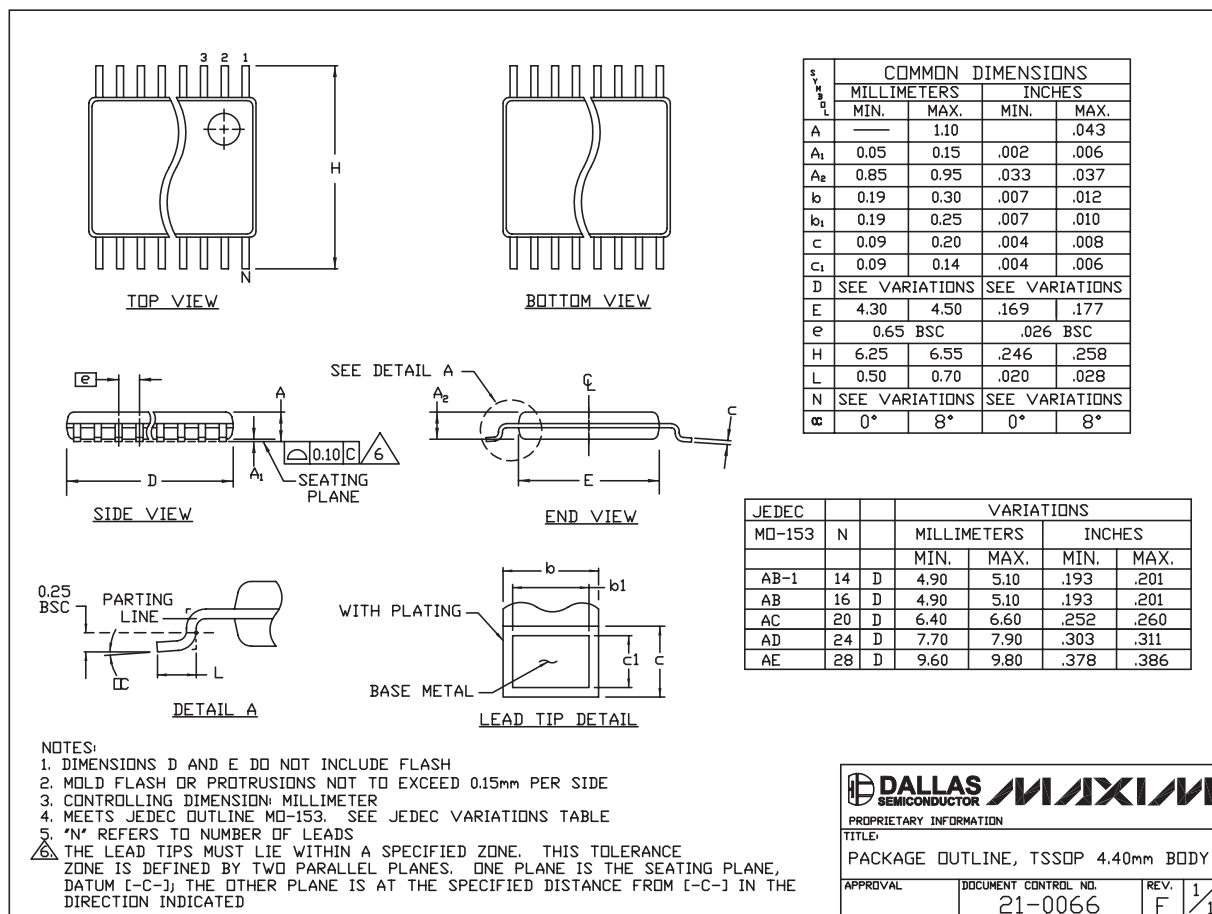
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MAX3030E-MAX3033E

±15kV ESD-Protected, 3.3V Quad RS-422 Transmitters

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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