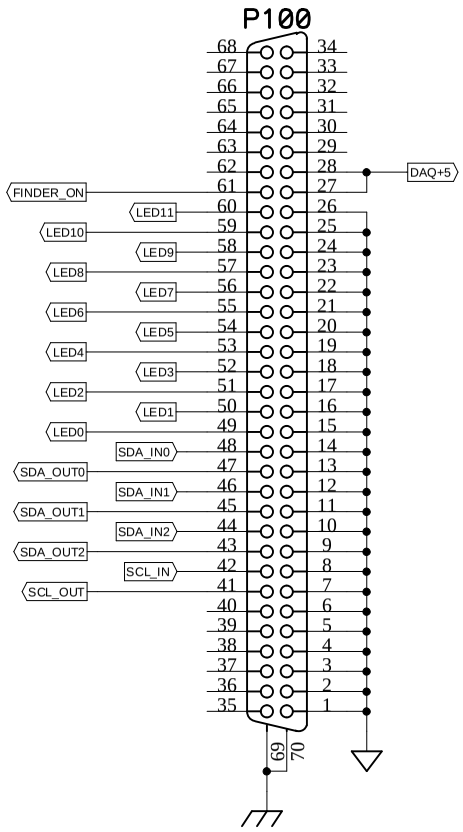
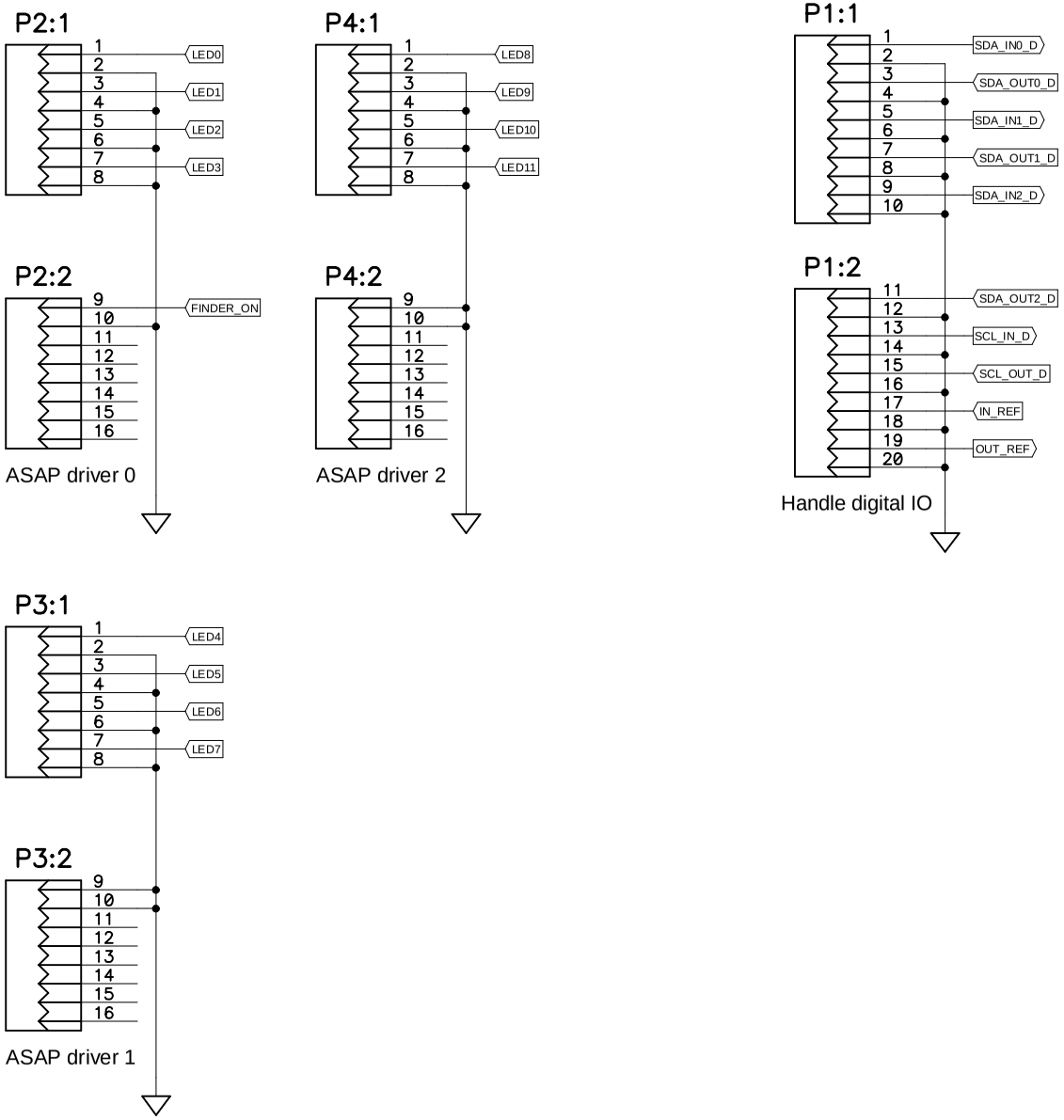
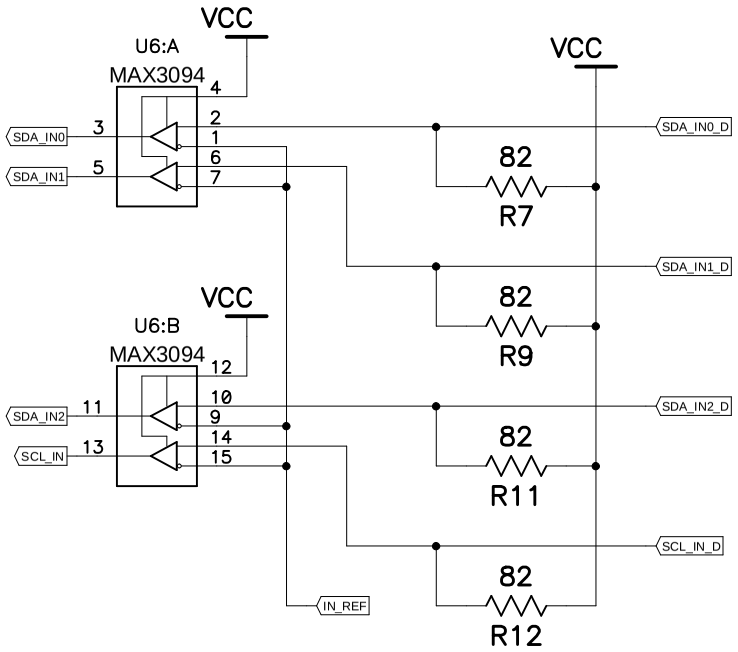
NI R-series RDIO



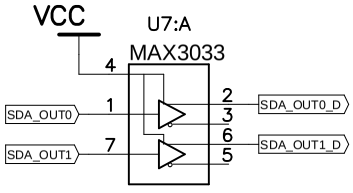
Title	Micron FPGA breakout: FPGA board connectors	
Size: A	Number	Rev: A
Date: Wed Feb 24, 2016		Drawn by: ram
Filename: fpga-breakout.sch		Sheet 1 of 4



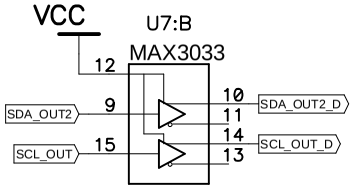
Title	Micron FPGA breakout: ASAP driver connectors		
Size A	Number		Rev A
Date	Wed Feb 24, 2016	Drawn by	ram
Filename	fpga-breakout.sch	Sheet	2 of 4

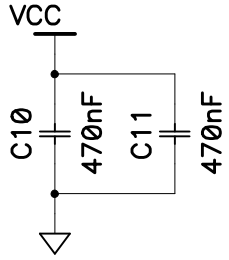


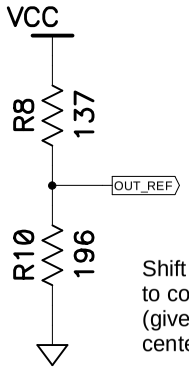
Lines are terminated to Vcc because this is the idle state.



The MAX3033 is slew rate limited to minimize reflections with imperfect impedance matching. 40 ns transition time typical.



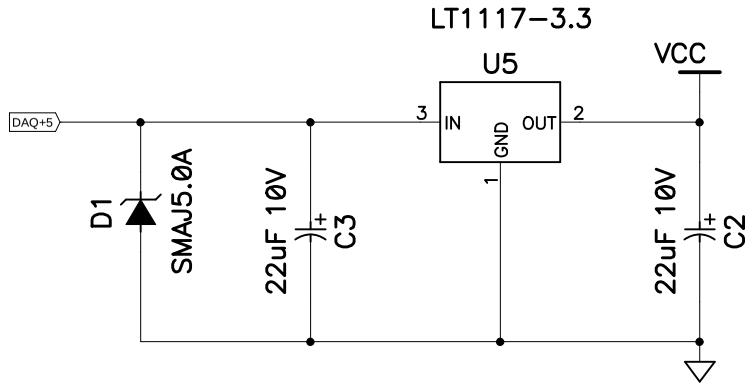


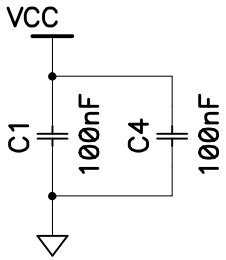


Shift ref level approx 300 mV positive to compensate for termination offset (given approx 10 ohm driver output resistance), centering threshold. R8 || R10 = Z0

These drivers are digital interface to the motor driver chips in the handle. The cable is too long for the I2C busses themselves to be routed over it, so a different electrical interface is used in the cable based on RS485. To save wires in the cable, and so the cable doesn't need to have a twisted-pair structure, we use a quasi-differential connection where all of the outgoing signals share a single negative reference at Vcc/2, and similarly all of the incoming signals have a single reference set at the handle end.
Compared to a normal differential connection this halves the noise margin because the differential swing is halved, and also degrades common mode rejection insofar as the interference experienced by the different wires will vary somewhat. It also forgoes the property of the complementary signal acting as a HF return.
All these compromises seem acceptable given that we are primarily concerned with external interference and not crosstalk, since all the digital signals are synchronized (and the LED drive is band-limited.) This also addresses the issue that there may be substantial voltage drops and ground bounce in the motor power return, making it problematic as a signal reference.

Title: Micron FPGA breakout: Line drivers		
Size: A	Number:	Rev: A
Date: Wed Feb 24, 2016		Drawn by: ram
Filename: fpga-breakout.sch		Sheet 3 of 4





Supply 3.3V to line drivers.

Title		
Size A	Number	Rev
Date		Drawn by
Filename		Sheet of