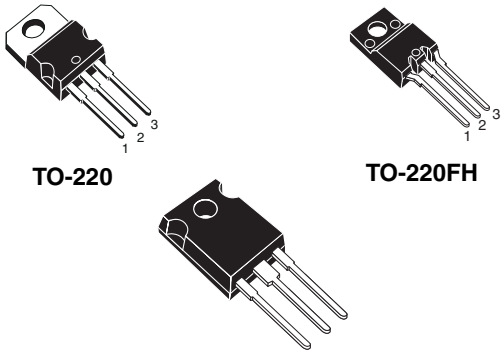
STFV3N150
STP3N150 - STW3N150

N-channel 1500V - 6Ω - 2.5A - TO-220 - TO-220FH - TO-247
Very high voltage PowerMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP3N150	1500V	< 9Ω	2.5A	140W
STFV3N150	1500V	< 9Ω	2.5A	30W
STW3N150	1500V	< 9Ω	2.5A	140W

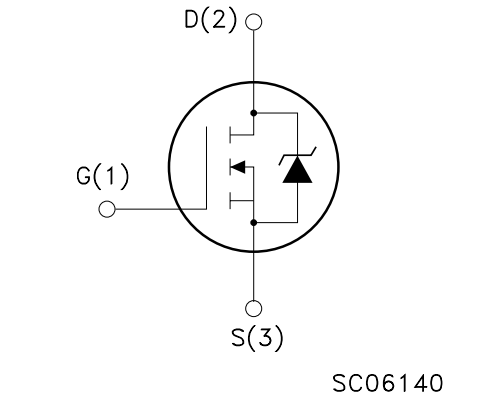
- 100% avalanche tested
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching



Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, unrivalled gate charge and switching characteristics.

Figure 1. Internal schematic diagram



Application

- Switching applications

Table 1. Device summary

Oder code	Marking	Package	Packaging
STP3N150	3N150	TO-220	Tube
STFV3N150	3N150	TO-220FH	Tube
STW3N150	3N150	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/TO-247	TO-220FH	
V_{DS}	Drain-source voltage (V_{GS} = 0)	1500		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	2.5	2.5 (1)	A
I_D	Drain current (continuous) at T_C = 100°C	1.6	1.6 (1)	A
I_{DM} (2)	Drain current (pulsed)	10	10 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	140	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T_C=25°C)	--	2500	V
	Derating factor	1.12	0.24	W/°C
T_j T_{stg}	Operating junction temperature Storage temperature	-50 to 150		°C

1. Limited by maximum temperature allowed
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	TO-220	TO-247	TO-220FH	Unit
Rthj-case	Thermal resistance junction-case Max	0.89		4.17	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	62.5	50	62.5	°C/W
T_j	Maximum lead temperature for soldering purpose	300			°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	450	mJ

2 Electrical characteristics

(T_{case} =25°C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} = 0	1500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125°C				10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 1.3A		6	9	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 30V, I_D = 1.3A		2.6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		939 102 13.2		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS}=0V to 1200, V_{GS} = 0		100		pF
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		4		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 1200V, I_D = 2.5A, V_{GS} = 10V *(see Figure 19)*		29.3 4.6 17		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 750V, I_D = 1.25A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 18)*		24 47 45 61		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				2.5 10	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 2.5A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2.5A, di/dt = 100A/µs V_{DD}= 60V Tj = 25°C *(see Figure 20)*		410 2.4 11.7		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2.5A, di/dt = 100A/µs V_{DD}= 60V Tj = 150°C *(see Figure 20)*		540 3.3 12.3		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

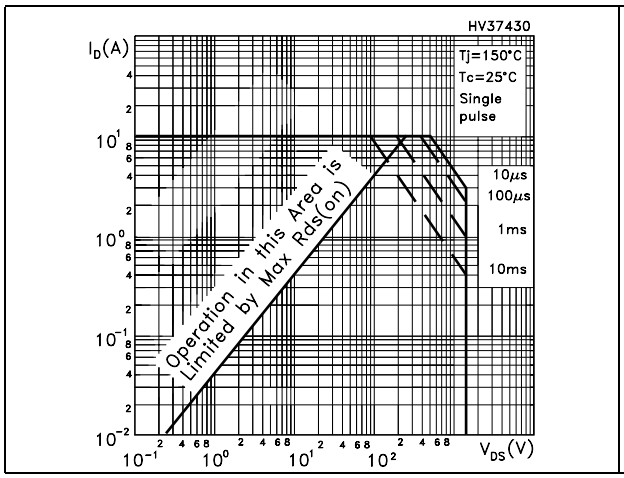


Figure 3. Thermal impedance for TO-220

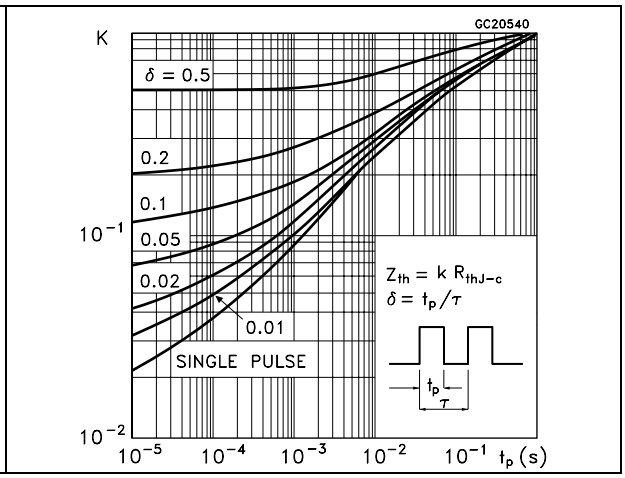


Figure 4. Safe operating area for TO-220FH

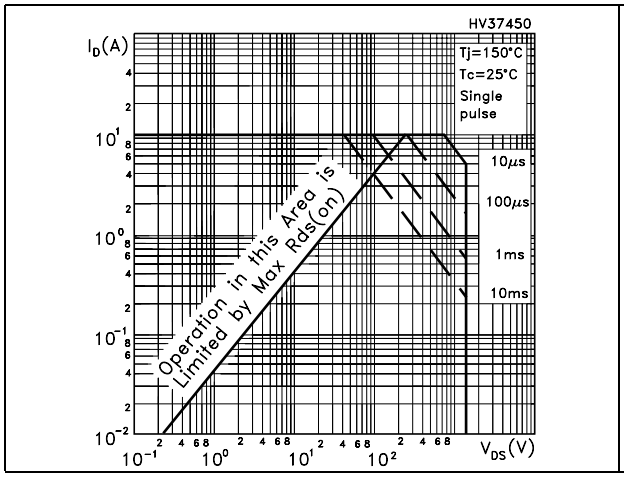


Figure 5. Thermal impedance for TO-220FH

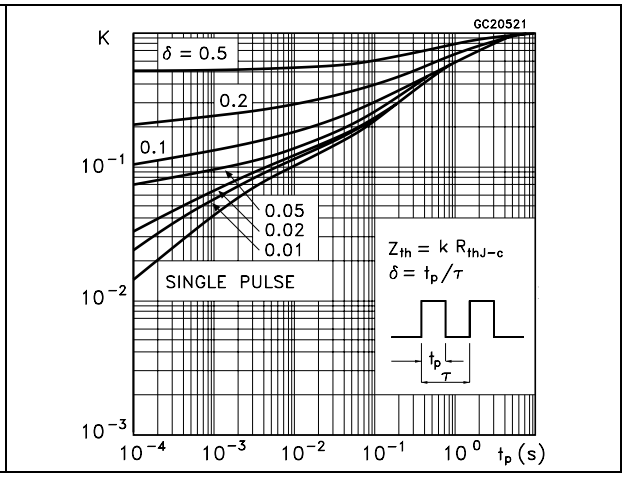


Figure 6. Safe operating area for TO-247

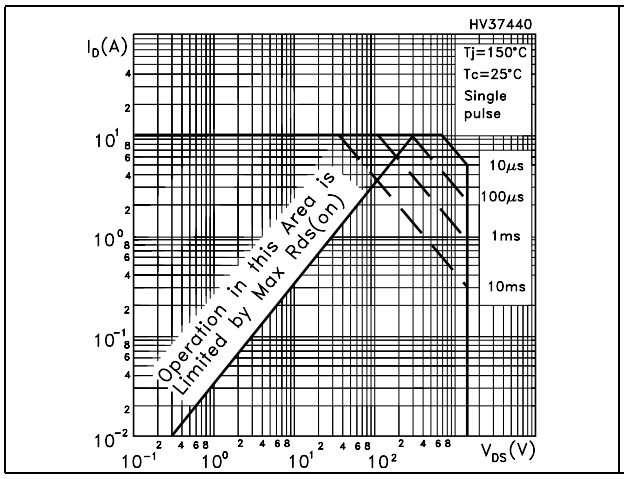


Figure 7. Thermal impedance for TO-247

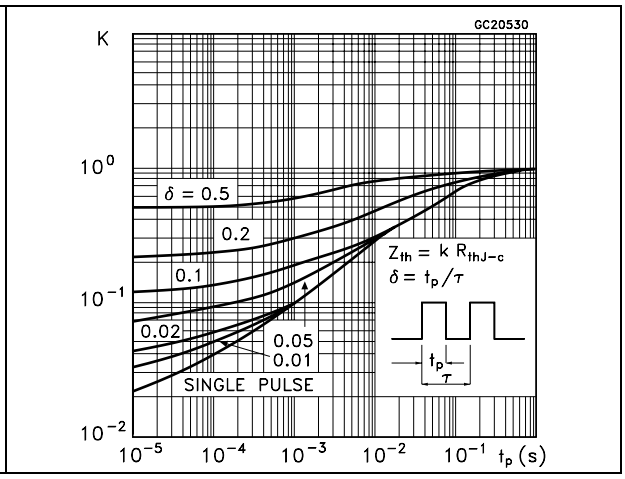


Figure 8. Output characteristics

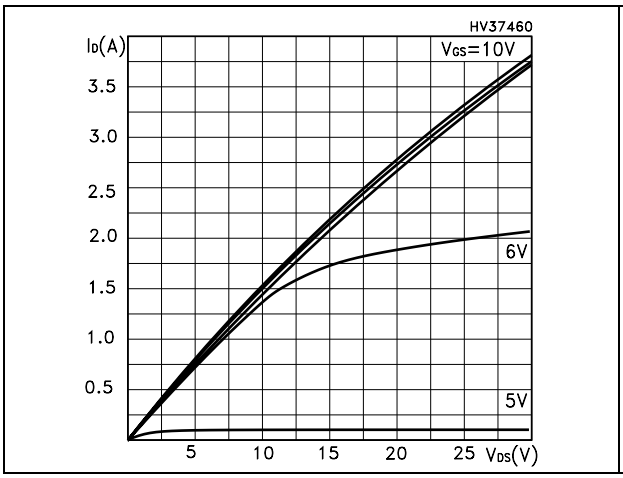


Figure 9. Transfer characteristics

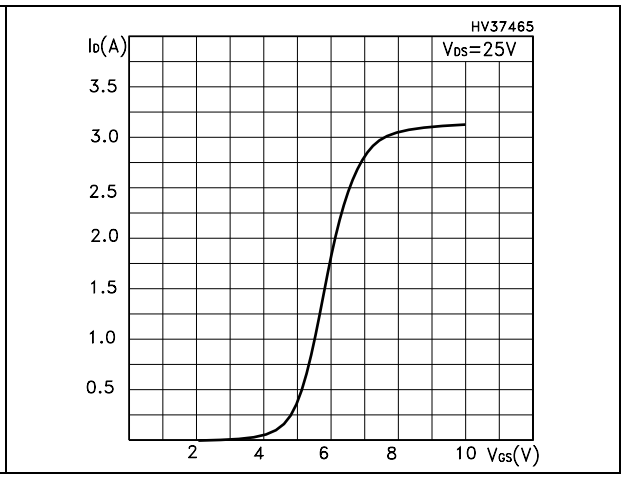


Figure 10. Normalized BV_{DSS} vs. temperature

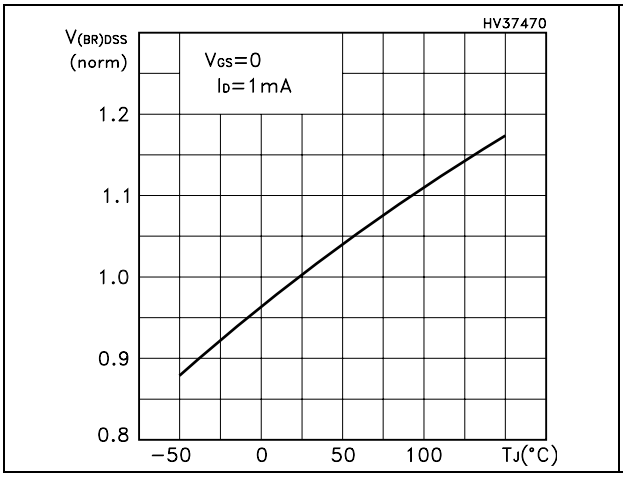


Figure 11. Static drain-source on resistance

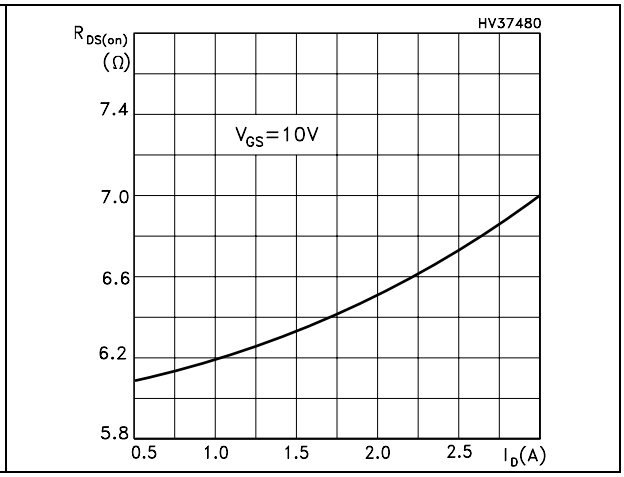


Figure 12. Gate charge vs. gate-source voltage

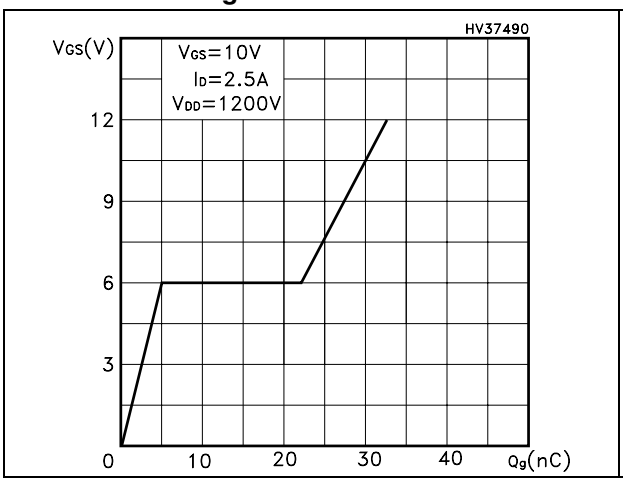


Figure 13. Capacitance variations

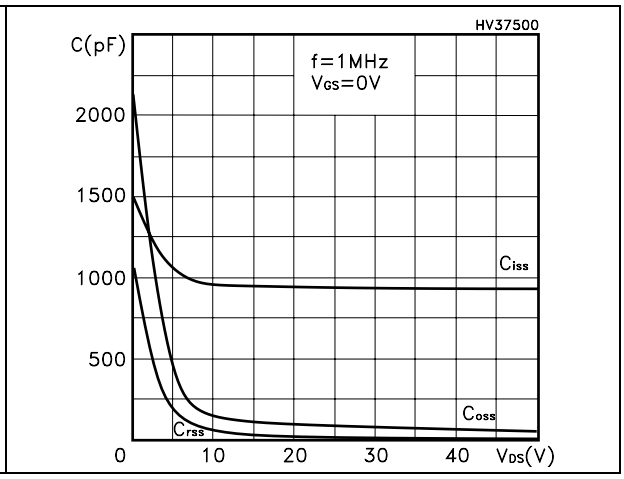


Figure 14. Normalized gate threshold voltage vs. temperature

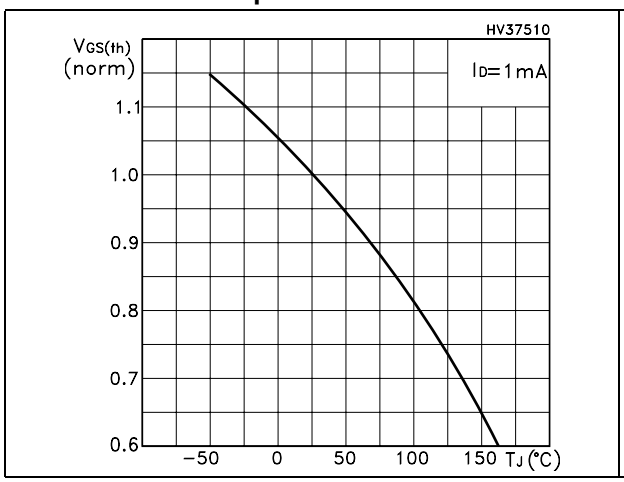


Figure 15. Normalized on resistance vs. temperature

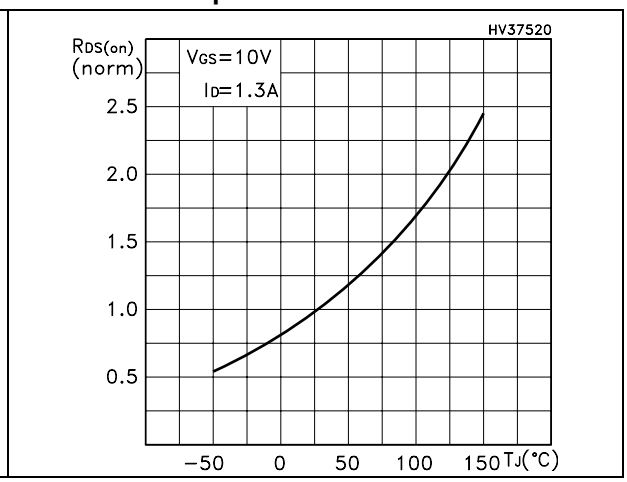


Figure 16. Source-drain diode forward characteristics

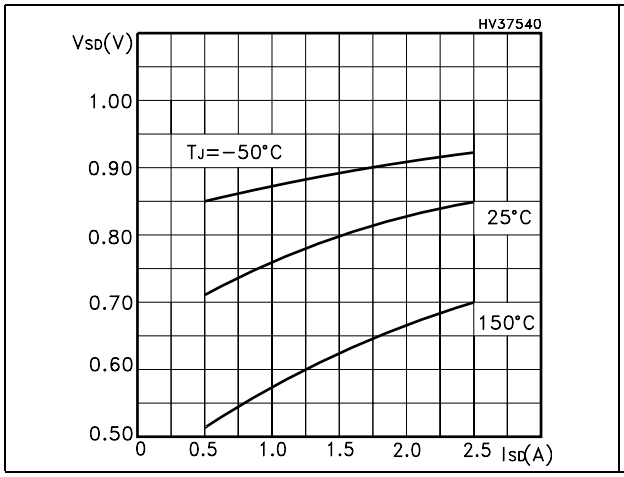
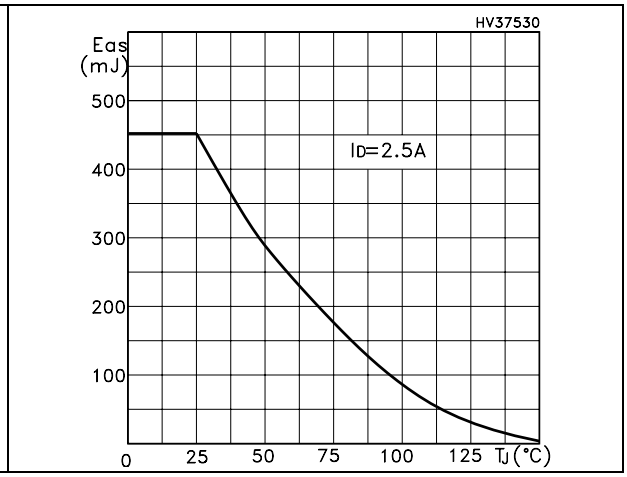


Figure 17. Maximum avalanche energy vs Tj



3 Test circuits

Figure 18. Switching times test circuit for resistive load

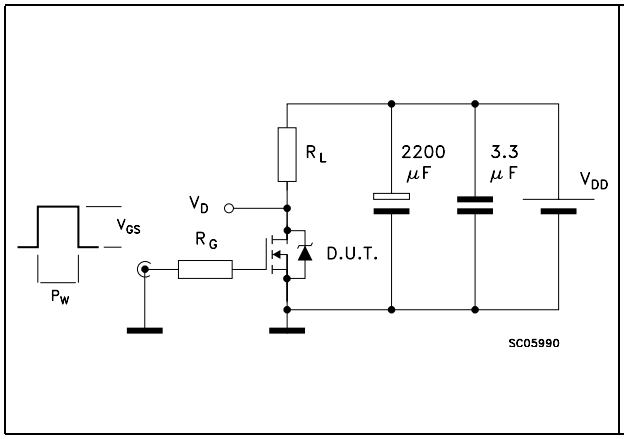


Figure 19. Gate charge test circuit

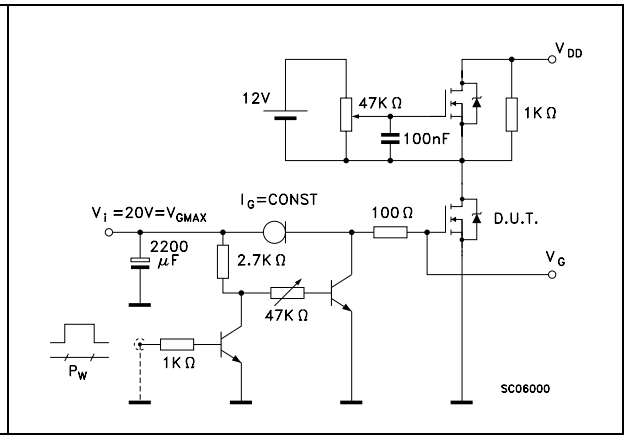


Figure 20. Test circuit for inductive load switching and diode recovery times

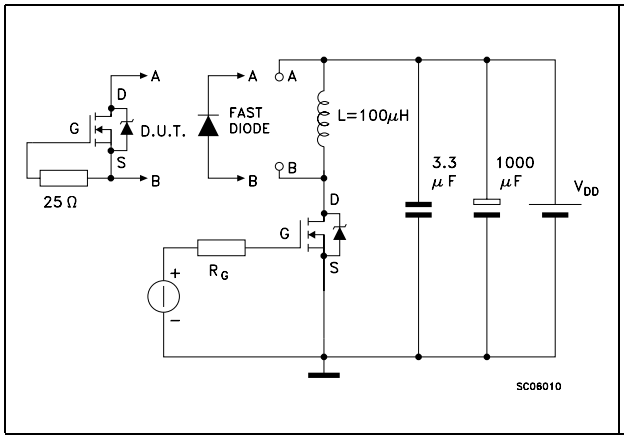


Figure 21. Unclamped Inductive load test circuit

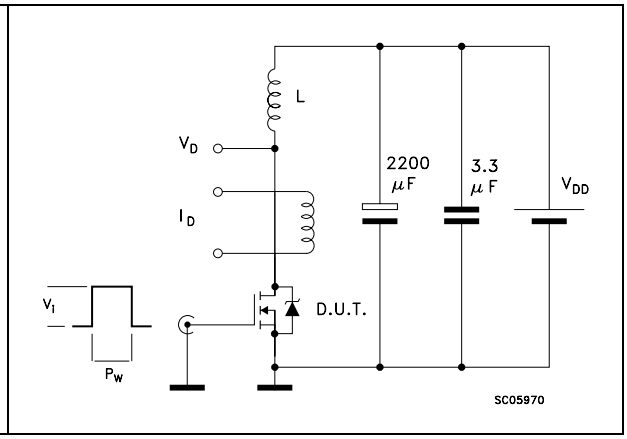


Figure 22. Unclamped inductive waveform

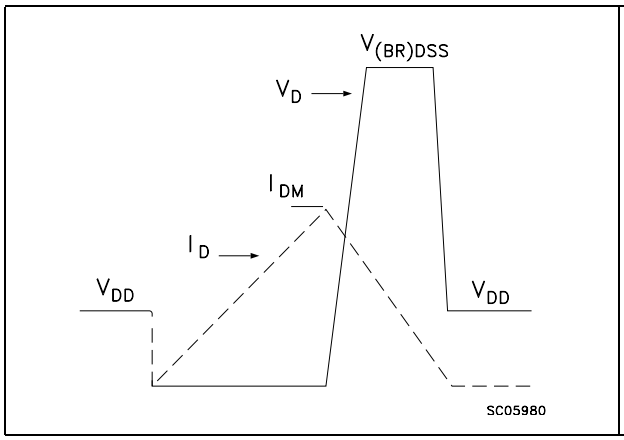
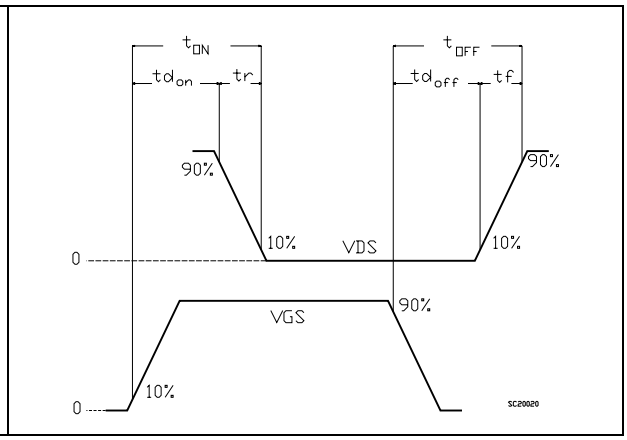


Figure 23. Switching time waveform

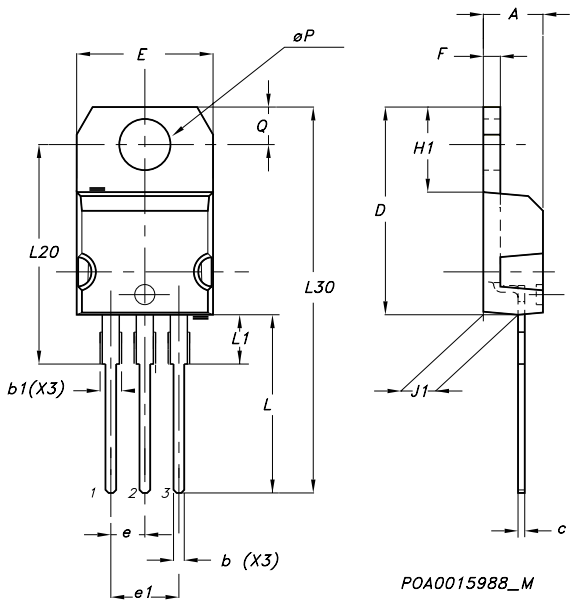


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

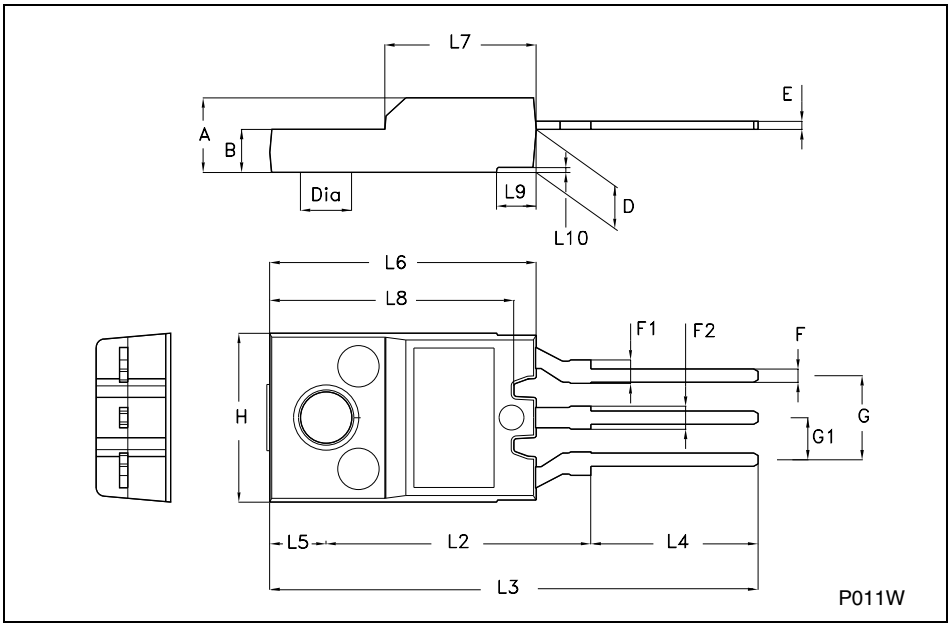
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



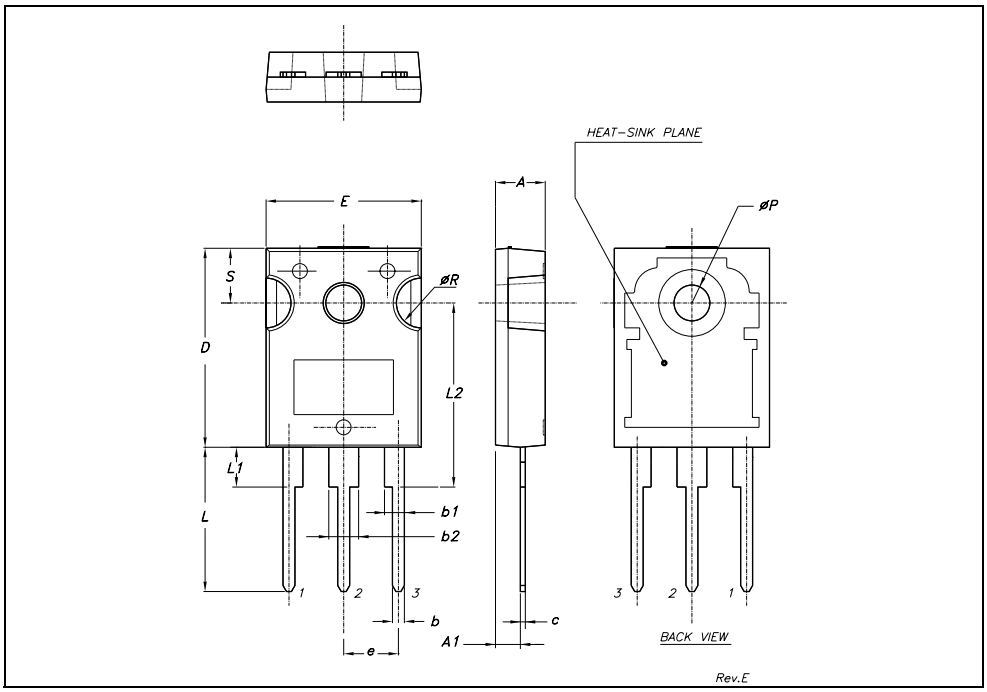
TO-220FH (Fully plastic High voltage) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.3		1.8	0.051		0.070
F2	1.3		1.8	0.051		0.070
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L5		3.4			0.134	
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
L8	14.5		15	0.570		0.590
L9		2.4			0.094	



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 9. Revision history

Date	Revision	Changes
12-Jan-2007	1	First release
17-Apr-2007	2	Added new value on *Table 6.*
14-May-2007	3	The document has been reformatted
27-Jul-2007	4	$R_{DS(on)}$ value changed, updated *Figure 15*