NSD-2101

Piezo Motor Driver ASIC for SQL-RV Series Reduced Voltage SQUIGGLE® RV and UTAF™ Motors

1 General Description

In combination with the SQUIGGLE® RV or UTAF, the NSD-2101 provides the industry's smallest piezo motor drive solution with direct battery drive; no boost circuit required.

The NSD-2101 is a dedicated piezo motor driver ASIC capable of driving a SQL-RV Series Reduced Voltage SQUIGGLE® RV motor or UTAF motor from a single 2.3 to 5.5 VDC supply. The motor can be controlled using a standard I²C interface.

The NSD-2101 uses proprietary control technology to dynamically adjust motor drive frequency to maintain optimal motor performance and minimal power consumption over wide temperature ranges and operating conditions. A built in oscillator eliminates the need for an external master clock.

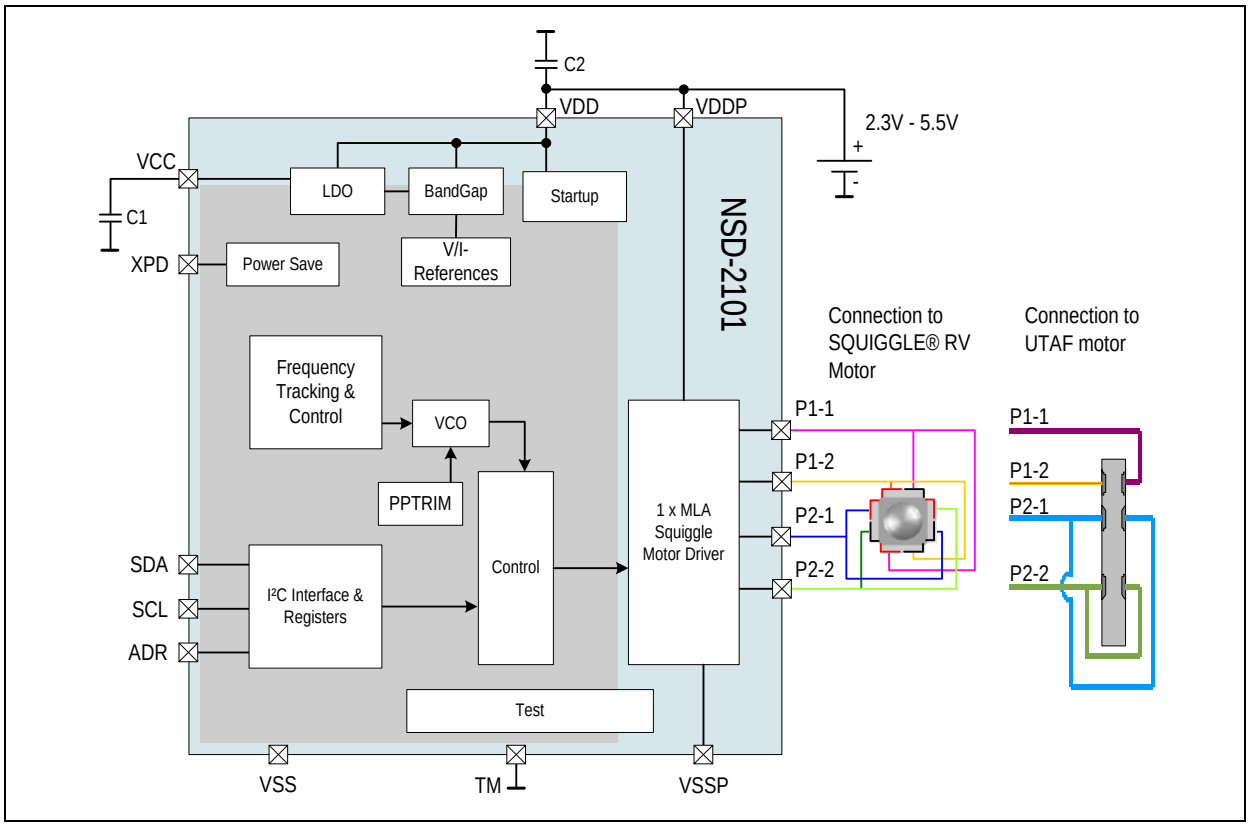
2 Key Features

- Industry's smallest piezo motor drive solution with direct battery drive
  - Wide input supply voltage: 2.3 to 5.5 VDC
  - 1.8 x 1.8 mm 4 x 4 ball grid array or 4 x 4 mm 16-pin QFN (minimum order quantities for QFN apply)
- Low power consumption:
  - Proprietary design optimizes power usage
  - Hard power-down mode for lowest power consumption
  - Idle mode via software for reduced power while preserving frequency calibration
- Proprietary frequency tracking controls maximizes motor performance over a range of operating and environmental conditions
- Built-in oscillator; no external clock or oscillator required
- I²C interface for direct serial interface to microprocessor
- On-chip registers for storing driver instructions

3 Applications

The NSD-2101 is ideal for SQL-RV-1.8 SQUIGGLE® RV piezoelectric motor driver and UTAF piezoelectric motor driver.

Figure 1. NSD-2101 Functional Block Diagram



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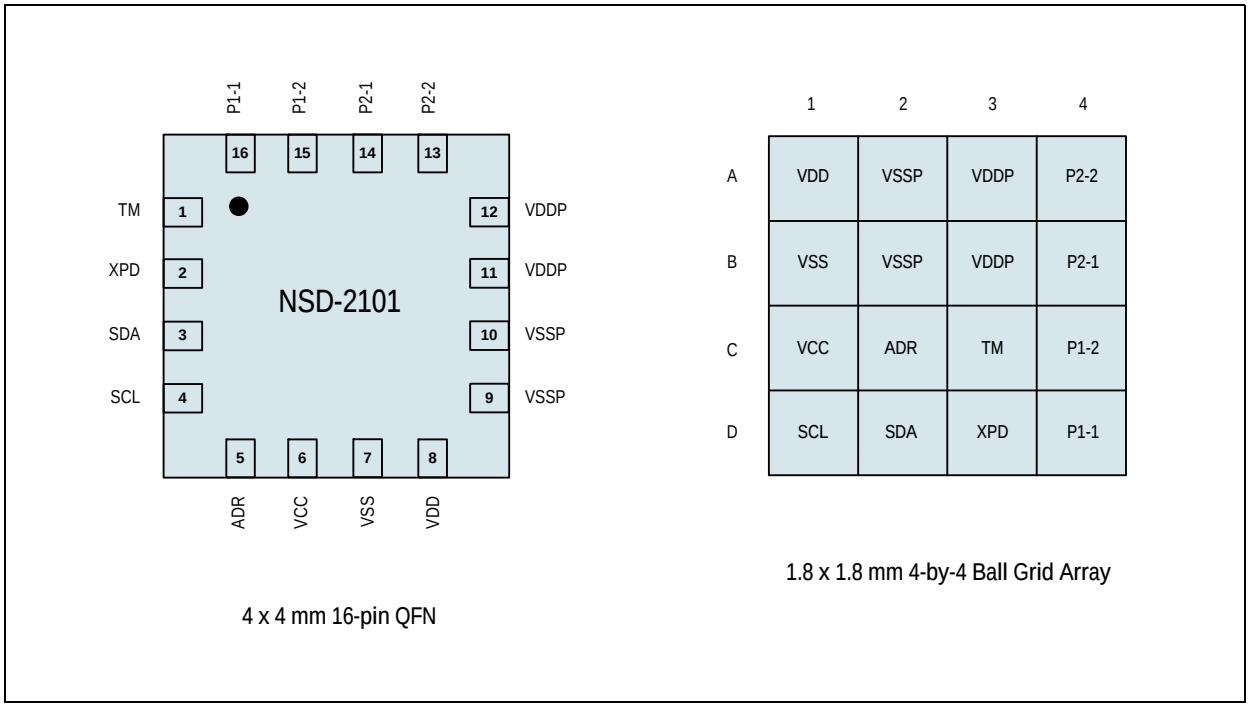
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Character	Description
TM	1	Digital input	Input	Test mode selection input; connected to VSS
XPD	2	Analog I/O		Shut down input, low active
SDA	3	Digital input / Digital output open drain	Input / Output	I²C data IO
SCL	4		Input	I²C clock
ADR	5	Digital input	Input	Address input for I²C
VCC	6	Supply pad	Power	Internal LV Power Supply
VSS	7		GND	Signal Ground Analog
VDD	8		Power	Power Supply
VSSP	9		GND	Power Ground Drivers
VSSP	10			
VDDP	11		Power	Power Supply Driver
VDDP	12			Power Supply Driver
P2-2	13	Analog I/O	Output	Half Bridge Phase2 inverted
P2-1	14			Half Bridge Phase2
P1-2	15			Half Bridge Phase1 inverted
P1-1	16			Half Bridge Phase1

Note: SDA (Data IO) and SCL (Data clock) constitute an I²C interface. Both have open drain outputs.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{VDD}	Voltage at supply pin	-0.3		7	V	
V_{VDDP}	Voltage at supply pin for drivers	-0.3		7	V	
V_{VCC}	Voltage at low voltage supply pin	-0.3		5.0	V	Internal LV supply (VCC)
V_{VSSP}	Voltage at VSSP	-0.3		0.3	V	GND reference for drivers
V_{VSS}	Voltage at VSS	0		0	V	GND reference potential
V_{LV}	Voltage at ADR, SDA, SCL, XPD, TM	-0.3		7	V	
I_{scr}	Input current (latchup immunity)	-100		100	mA	Norm: JESD78
ESD	Electrostatic discharge	±1			kV	Norm: MIL 883 E method 3015. Human body model: R=1.5kΩ, C=100pF, measured and qualified only in QFN16 package.
P_{tot}	Total power dissipation			1	W	
R_{thja}	Thermal resistance QFN16 4x4mm	29.7	33	36.3	K/W	Multi-Layer JEDEC board
T_{strg}	Storage temperature	-40		150	ºC	
Tbody	Package body temperature			260	ºC	Norm: IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn).
	Humidity non-condensing	5		85	%	

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDD}	Voltage at VDD	Supply voltage (VDD/VDDP rise time is between 10µs and 10ms. Above 5.0V only half bridge mode should be used)	2.3		5.5	V
V_{VDDP}	Voltage at VDDP	Driver supply (VDD/VDDP rise time is between 10µs and 10ms. Above 5.0V only half bridge mode should be used)	2.3		5.5	V
V_{VCC}	Voltage at VCC	Internal LV supply	1.9		3.0	V
V_{VSSP}	Voltage at VSSP	GND reference for drivers	-0.1		0.1	V
V_{VSS}	Voltage at VSS	GND reference	0		0	V
V_{LV}	Voltage at SDA,SCL, XPD, TM		-0.3		5.5	V
T_{junc}	Junction temperature		-30		125	ºC
P_{tot}	Total power dissipation	Total power dissipation needs to be less than 1W to keep junction temperature in specified range			1	W
I_{Pd}	Power-down current consumption	XPD=LOW, temp=27ºC; No activity on I²C			5	µA
I_{Sb}	Stand-by current consumption	XPD=HIGH, pulse generation is stopped			3.5	mA
I_{Nom}	Operating current consumption	Without output switching current			10	mA
I_{Idle}	Idle mode current consumption	XPD=HIGH, temp=27ºC, VCO powered down, no digital activity; mode set by I²C, frequency trimming preserved			1.0	mA

6.1 DC/AC Characteristics for Digital Inputs and Outputs

Table 4. CMOS Input: XPD, ADR, CLK

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		1.2		VDD	V
V_{IL}	Low level input voltage		VSS		0.3	V
I_{LEAK}	Input leakage current		-1		+1	µA
C_{IN}	Capacitive Load				15	pF

Table 5. CMOS I²C Interface: SDA, SCL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		1.2		VDD	V
V_{IL}	Low level input voltage		VSS		0.3	V
I_{LEAK}	Input leakage current		-1		+1	µA
V_{OH}	High level output voltage	Depending on external pull-up resistor	V_{VDD} -0.5		V_{VDD}	V
V_{OL}	Low level output voltage	At 3mA output current			VSS+0.4	V
C_L	Capacitive load: SDA, SCL				50	pF
R_{PU}	External pull-up resistor: SDA, SCL	As defined by I²C spec	1.2	6.0	7.1	kΩ
SCL	I²C write frequency	Maximum clock frequency to write data			400	kHz

7 Detailed Description

Figure 1 shows the main building blocks of the system:

- Supply input
- LDO and bypass capacitors
- I²C interface
- Registers
- Oscillator
- Frequency tracking
- Full bridge driver

The input voltage is supplied directly to the full bridge driver. With a full bridge drive, each piezo element sees twice the input voltage (2 x VDD). However, the average input voltage to the piezo can be regulated by the ASIC between VDD and 2 x VDD. This average voltage, which can be set via I²C along with the duty cycle (or pulse width) of the drive signal, determines the speed of the motor. The result being at lower speeds, the motor consumes less power.

I²C registers also define the initial switching frequency of the motor, which can be adjusted from 50 kHz to 200 kHz based on the type of motor being driven. Other registers control motor direction and the number of pulses the motor is active (correlating to distance traveled). The XPD input enables a stand-by mode.

7.1 Output Drivers

The output drivers operate rail to rail and are capable of driving capacitive load up to 60nF. The concept is based on two full bridges per motor. The reduced voltage Squiggle motor consists of 2 plates per phase and 2 phases. In power down mode the output drivers are pulled to ground. The same applies when the motor is off.

Table 6. Characteristics for Output Drivers

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{tr}	Rise/fall time from 0.23V to 2.07V and vice versa	C_{LOAD} 50nF, VDD=2.3V[1]	0.08		0.8	µs
f_{tf}						
C_{LOAD}	Load capacitance		10		60	nF
I_{lim}	Current limit for driver outputs[2]		1000		1600	mA
f_{DFR}	Drive frequency range[3]		50		200	kHz
f_{DC}	Switching frequency duty cycle		1		50	%
t_{DT}	Dead time (additional)	VCO clock cycles[4]	2	4	9	
f_{PS}	Phase shift		-160		+90	deg
f_{PSE}	Phase shift error				±3	deg

1. Measured at 10% to 90% of minimum VDD=2.3V. Maximum with 4 clocks dead-time.
2. Current limit is valid for full bridge and half bridge configuration. Due to the dynamic behavior of the output driver the maximum current limit can not be reached under all conditions. Device can only be used for direct motor drive.
3. For this frequency range, frequency tracking is implemented.
4. Error of dead time is maximum +1 VCO clock cycle.

Figure 3. Motor Drive Concept (SQUIGGLE® RV Motor)

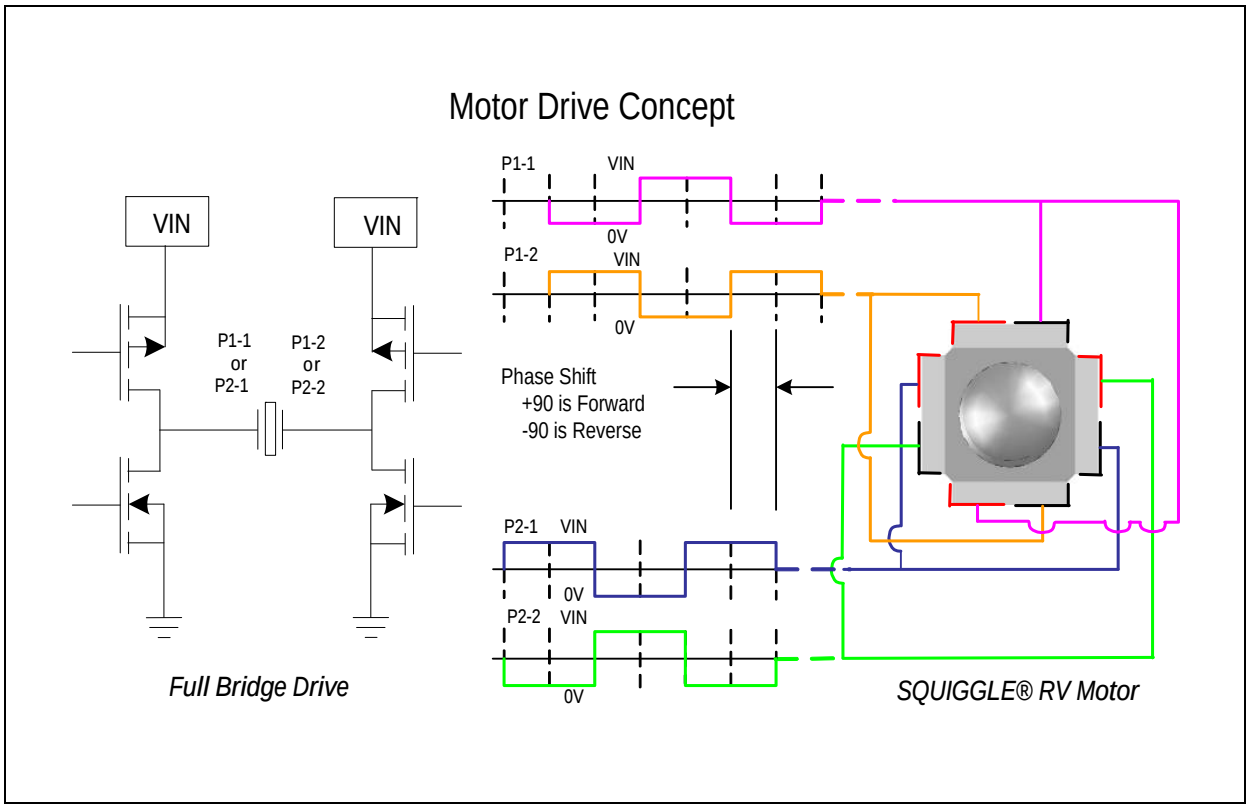
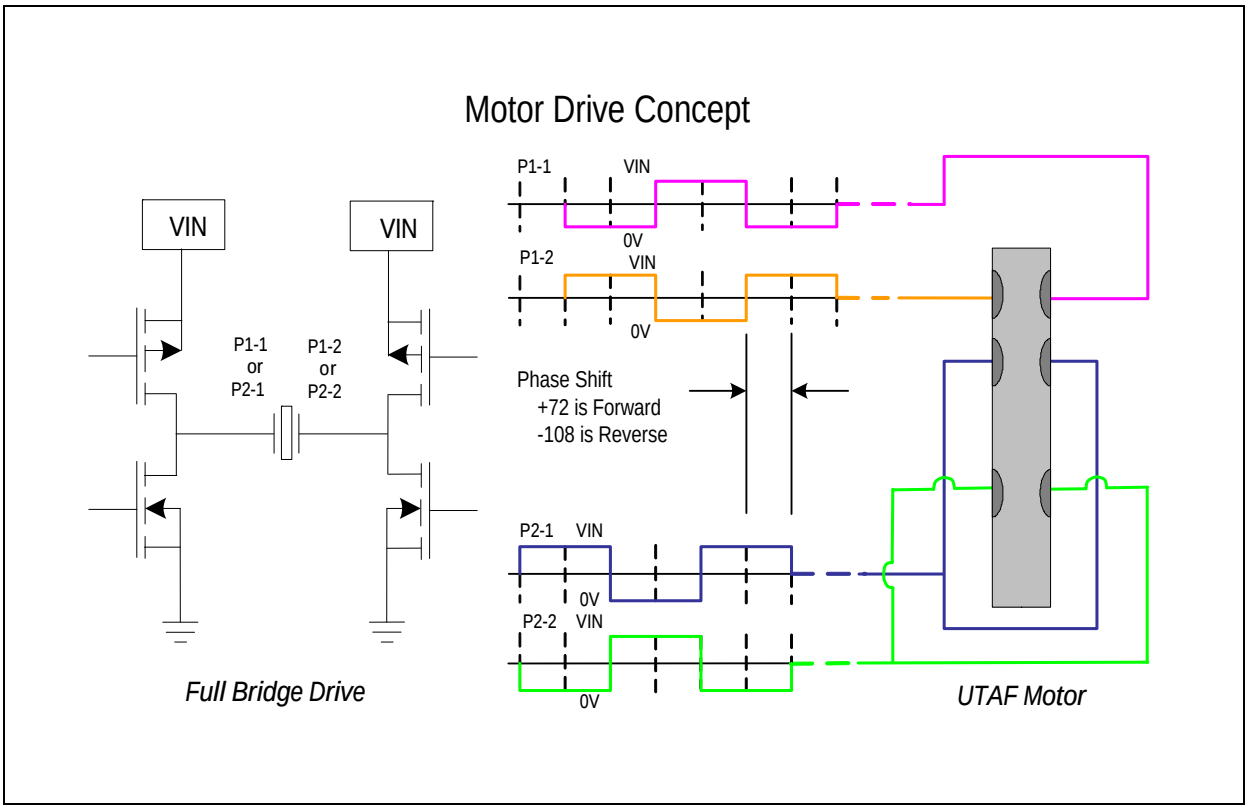
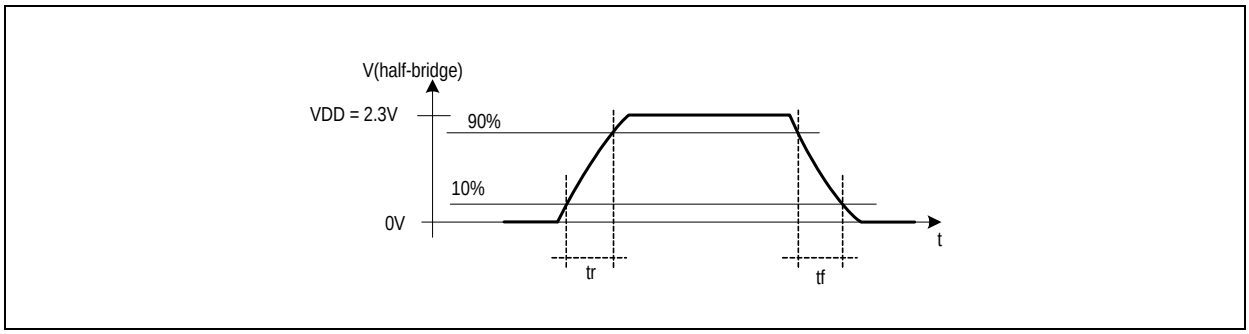


Figure 4. Motor Drive Concept (UTAF Motor)



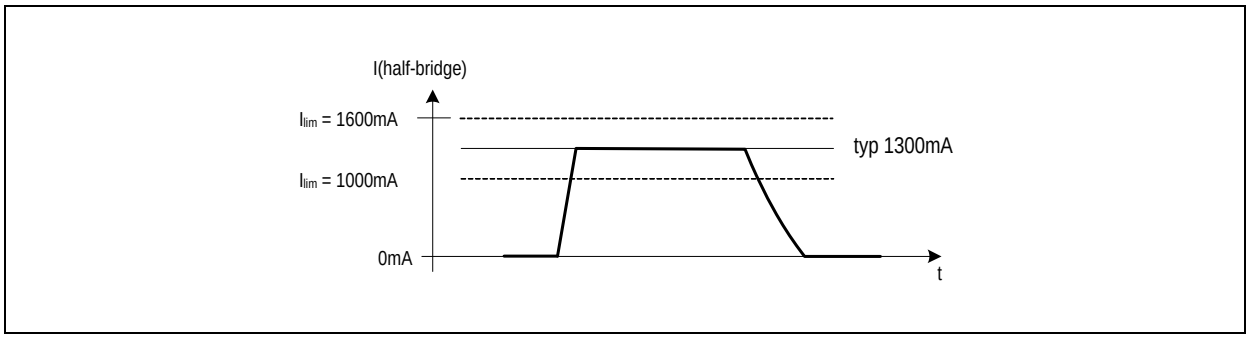
The rise and fall time definition is shown in Figure 5. Time between crossing 10% and 90% threshold of minimum VDD is measured, 10% to 90% for rise time and 90% to 10% for fall time. A full bridge switching cycle will take longer.

Figure 5. Rise / Fall Time Definition



In Figure 6, the effect of current limit in the output drivers is shown. Each half-bridge output can deliver 1000mA.

Figure 6. Output Driver Current Limit



7.2 Power Dissipation Control

Following techniques are implemented to keep the system and on-chip power dissipation low.

- Selectable half bridge mode depending on input supply voltage
- Selective charge control for full bridge mode
- Hybrid Control for full bridge mode

Table 7. Power Dissipation Control

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Selectable half-bridge						
HB_{thr}	Rising Threshold	When half-bridge mode is enabled then the output driver will switch to half-bridge drive depending on input supply voltage. Typical system power dissipation can be reduced down to 25% of standard full-bridge drive. When VDD is higher than 5.0V only half bridge mode should be used to avoid exceeding max total power dissipation of 1W. A typical hysteresis of 100mV is implemented to increase immunity against supply disturbances.	4.3	4.5	4.7	V
HB_{thf}	Falling Threshold		4.2	4.4	4.6	V
Selective charge control for full-bridge						
SCC_{PDS}	Power dissipation saving	By adding an additional state in the full bridge switching scheme the power dissipation can be reduced due to the fact that the effective voltage on the capacitor is reduced.	30		50	%
Hybrid Control for full-bridge						
PS_{PDS}	Power dissipation saving	With this technique the power dissipation can be reduced by switching periodically from full-bridge to half-bridge mode. Power saving in comparison to standard full-bridge drive is mainly depending on duty cycle between half-bridge and full-bridge. Hybrid Control is also used for speed control.			75	%

7.3 Frequency Tracking

Based on the motor type, an initial drive signal period must be written to the NSD-2101. The period is specified in units of 0.04 µsec (based on the nominal internal VCO frequency of 25 MHz). In the case of an SQL-RV-1.8 motor, the period may be 148 (94h) to generate a drive frequency of ~168.9 kHz.

The NSD-2101 is able to then optimize the drive frequency by, on command, sweeping over a range of frequencies, centered at the specified period, and settling on the frequency at which the best motor performance was detected. Alternatively, the NSD-2101 may be commanded to incrementally step the frequency in the direction of increasing motor performance (changing the step direction when the performance drops).

In either case, the NSD-2101 adjusts the frequency by adjusting the VCO trimming, rather than the period count. This affords much higher resolution than is possible by changing the period count.

Whether sweep mode or incremental (see 'Control Register' in Table 8 on page 10), the calibration does not start until a pulse count has been loaded into registers 02h and 03h.

A sweep calibration is typically performed following a power-up. The sweep calibration offers the greatest range of frequencies. Incremental calibration offers the best frequency resolution and can be performed periodically as the motor is being used.

7.4 I²C

The I²C interface is used to control the NSD-2101 and set the value of several registers. These registers will define the direction and duration of the output driver signals, the duty cycle, phase shift and average voltage to the motor.

Start/Stop Condition: A HIGH to LOW transition on the SDA line while SCL is HIGH is the start condition for the bus. A LOW to HIGH transition on the SDA line while SCL is HIGH is the stop condition.

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

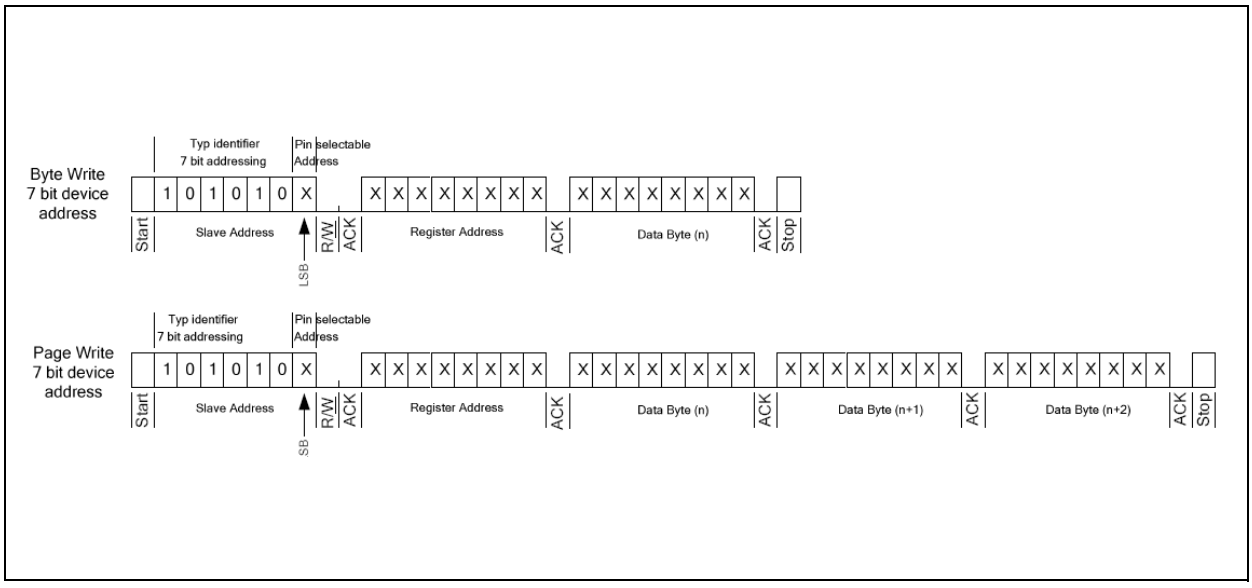
Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The receiver must pull down the SDA line during the acknowledge clock pulse.

The NSD-2101 is a slave device on the bus. There are two different access modes:

- Byte write
- Page write

The device can be addressed using 7-bit addressing. The first 6 bits are fixed. The last bit can be set via package pin.

Figure 7. 7-Bit Device Address



7.5 Register Map

Table 8 lists out the registers which can be addressed over the I²C interface.

Table 8. I²C Registers

Description	Address	Data Byte								Note
		MSB							LSB	
Control Register	00h		PS[1]	PS[0]		CN[1]	CN[0]	P1	P2	
Period count	01h	X	X	X	X	X	X	X	X	
Pulse count (high byte)	02h	P	D	DS[1]	DS[0]		X	X	X	P: Period count MSB; D: Direction bit; DS: Dead time selection bits: '00'=2, '01'=4, '10'=6 and '11'=8 VCO clocks.
Pulse count (low byte)	03h	X	X	X	X	X	X	X	X	
Pulse width	04h	X	X	X	X	X	X	X	X	
Phase shift	05h	X	X	X	X	X	X	X	X	
Period offset	06h	IDL	HB	HYB	DT		X	X	X	CN needs to be 00 to enable Period offset. Period offset is not used when either Incremental or Sweep Frequency Tracking is active. IDL: Sets idle mode; HB: Enable half bridge operation if VDD > HB_{th}; HYB: Enable hybrid speed control; DT: Enable signal for increased dead time; Selection bits(DS[1:0]) are only valid when DT=1; Selection bits should not be changed when the output driver is active.
Hybrid speed	07h	X	X	X	X	X	X	X	X	Hybrid Speed register: 0… half bridge; 128…full bridge operation; linear transition for values in between; Default: 128. Values from 1 to 127 are used for linear speed control.
Reserved register	10h	X	X	X	X	X	X	X	X	Reserved register used for device test only, not accessible during normal operation.

7.6 Control Register

The control register is used to trigger frequency calibration as well as to select and enable the drive phases.

Table 9. Control Register

Control Flag Mask	Abbr	Default	Description
1000 0000		0	Reserved (leave 0)
0100 0000	PS[1]	1	Phase Select for sensing: PS[1] PS[0]: 00=None 01=Phase1 10=Phase2 11= Both Phases
0010 0000	PS[0]	1	
0001 0000		0	Reserved (leave 0)
0000 1000	CN[1]	0	Calibrate Now: CN[1] CN[0]: 00=None 01=Incremental 10=Sweep 11=reserved
0000 0100	CN[0]	0	
0000 0010	P1	1	Enable Phase1
0000 0001	P2	1	Enable Phase2

7.7 Period Counter

The period counter is used to define the switching frequency of the motor. The pulse period is generated by dividing the internal VCO clock frequency by the given period counter value. The MSB in the high byte of the pulse counter (p) is used as the MSB for the period counter.

At 25MHz clock a decimal period counter value of 125 gives an output frequency of 200 kHz. A period counter value of 126 results in a switching frequency of 198.41 kHz. This is equal to a maximum frequency step of 1.59 kHz. The frequency resolution gets better for lower switching frequencies assuming a fixed VCO clock frequency.

Table 10 lists out few examples to define period counter and output switching frequency relationship. The values are given for 25MHz typical VCO clock frequency. The switch frequency is given as:

$$f_D = 25MHz / period\ counter\ value \qquad (EQ\ 1)$$

Table 10. Period Counter Values

Period Counter Value	Typ	Unit
0 0111 1101	200.00	kHz
0 0111 1110	198.41	kHz
0 1001 0001	172.4	kHz
0 1010 0110	150.60	kHz
0 1010 0111	149.70	kHz
1 1111 0011	50.10	kHz
1 1111 0100	50.00	kHz

7.8 Pulse Counter

The pulse counter sets the number of pulses the motor should be active. When a new value is written to the pulse count register an internal counter is started to count generated output pulses. Writing all zeros to the pulse counter stops the motor even if the previous set counter value is not completed, all outputs pulled to ground. The same is valid for power down mode. Bit 6 in the pulse counter (d) is used to set the direction of motor motion.

Table 11. Pulse Counter Values

Pulse Counter Value	Typ	Unit	Conditions
XXXX X000 0000 0000	0	pulses	Motor is off, driver outputs are low
XXXX X100 0000 0000	1024	pulses	
XXXX X111 1111 1111	2047	pulses	Maximum possible number of pulses

7.9 Pulse Width Control

A register is used to define the duty cycle of the driver output signal. The default value for this register set during power up or power down (XPD = LOW) is equal to 00h. In this case the default duty cycle of 50% is generated. The resulting duty cycle and resolution of single steps is depending on the master clock frequency and the switching frequency of the driver output. Table 12 provides an example for 25MHz master clock and 200kHz driver frequency. The value of the duty cycle register should not exceed 50.4% of the period counter value. Pulse Width Modulation is used for speed control when motor is operating in half bridge mode.

Table 12. Pulse Width Register Values

Pulse Width Register	Typ	Unit	Conditions
0000 0000	49.6/50.4	%	default
0000 0001	0.8	%	
0000 1101	10.4	%	
0001 1011	21.6	%	
0011 0101	42.4	%	
0011 1110	49.6	%	
0011 1111	50.4	%	

If operating in half bridge mode, the pulse width can be used to adjust speed. At 50% the motor will operate at its maximum speed. To reduce the speed, the pulse width may be reduced. However, below ~15%, there may not be enough energy in the signal to move the motor.

7.10 Phase Shift

A register is used to define the phase shift between the two phases of the driver output signal. The default value for this register set during power up or power down (XPD = LOW) is equal to 00h. In this case the default phase shift of 90° is generated. The resulting phase shift and resolution of single steps is depending on the master clock frequency and the switching frequency of the driver output. Table 13 provides an example for 25MHz master clock and 200kHz driver frequency. The value of the phase shift register should not exceed 50.4% of the period counter value.

Negative phase shift values are achieved by changing the direction bit: -160deg = 20deg and inverted direction bit.

Table 13. Phase Shift Register Values

Phase Shift Register	Typ	Unit	Conditions
0000 0000	90.5	deg	Default (Normal for both SQL and UTAF)
0000 0001	2.88	deg	
0000 1101	37.44	deg	
0000 1110	40.32	deg	
0001 1111	89.28	deg	
0010 0000	92.16	deg	

7.11 Period Offset

Period Offset register defines the offset which is added to the period counter to shift the switching frequency. It also provides some additional control bits.

This offset is only activated when frequency tracking is stopped. An offset has been provided as some types of motors operate better at slightly below mechanical resonance. Table 14 provides an example for 25MHz master clock and 200kHz nominal driver frequency. Period offset is only supposed to lower drive frequency.

Table 14. Period Offset Register Values

Period Offset Register	Typ	Unit	Conditions
0000 0000	0	%	Default, no change of drive frequency
0000 0001	-0.8	%	
0000 0010	-1.6	%	
0000 0111	-5.6	%	Maximum period offset
1000 0000	0	%	Idle mode enabled
0100 0000	0	%	Half bridge mode enabled
0010 0000	0	%	Hybrid speed control enabled
0001 0000	0	%	Increased dead time enabled

Idle mode reduces power consumption while preserving the most recent frequency calibration. To further reduce power, the XPD pin must be pulled to ground.

7.12 Hybrid Speed Register

The hybrid speed register allows the average voltage as seen by the motor to be set from VDD to 2 x VDD. This provides a power efficient method of reducing the speed of the motor. The value of the register can vary from 0 (half bridge) to 128 (full bridge). The average voltage can be calculated in the following manner.

$$VAVG = VDD + (RegisterValue * VDD / 128) \quad (EQ\ 2)$$

Where: VDD is the supply voltage

Table 15. Hybrid Speed Register Values

Hybrid Speed Register	Typ	Unit	Conditions
0000 0000	0	%	VDD (half bridge)
0010 0000	25	%	VDD + 0.25 * VDD
0110 0000	75	%	VDD + 0.75 * VDD
1000 0000	100	%	VDD + VDD (full bridge)

8 Application Information

The NSD-2101 is designed to drive one SQL-RV-1.8 SQUIGGLE® RV motor or one UTAF motor. Recommended external components are as follows:

Table 16. External Components

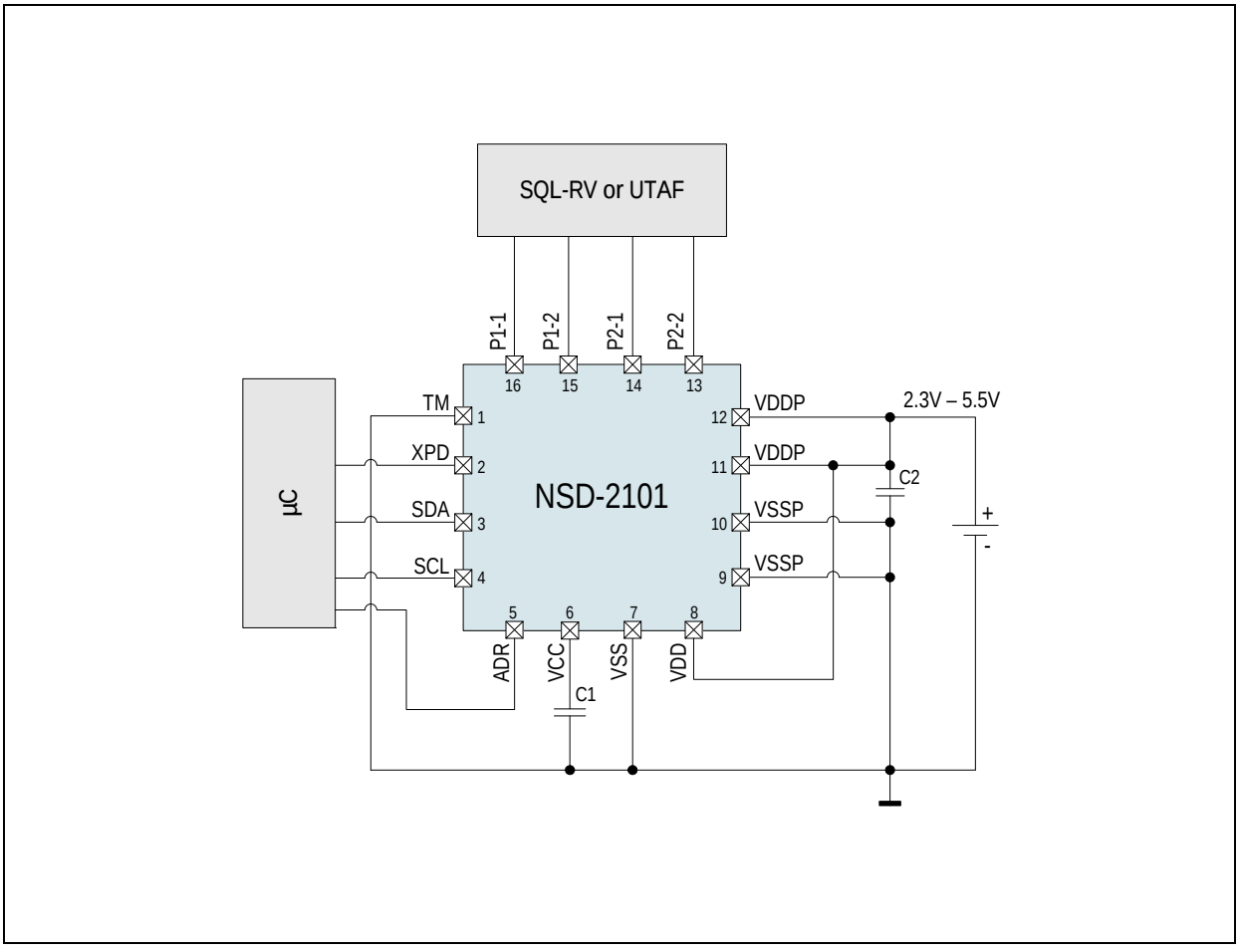
Component	Manufacturer	Part Number	WxLxH [mm]
C1 470nF Cap 4.0V	TAIYO-YUDEN	AMK063BJ474MP-F	(0201)
C2 4.7µF Cap 6.3V	PANASONIC	ECJ-0EB0J475M	For UTAF only (max 35nF) (0402)[1]
C2 10µF Cap 6.3V	PANASONIC	ECJ-1VB0J106M	Full load (0603)[1]

1. A maximum ESR of 100mΩ at motor switching frequency is assumed. The series resistance of the input supply (VDD, VDDP) should be maximum 50mΩ and capable of delivering at least 1W of power. ESR information for C2 is still missing.

New Scale offers a convenient MC-33DB-RV evaluation board which includes the components, along with input and motor connectors, to take full advantage of the NSD-2101 ASIC.

The XPD input can be used to place the ASIC in stand-by mode for minimal current consumption when the motor is not moving. Alternatively, the designer can implement an external switch to power off the ASIC completely when the motor is not moving: the SQUIGGLE® RV motor holds its position with the power off.

Figure 8. NSD-2101



8.1 Integration with SQL-RV-1.8 SQUIGGLE Motor

Communicating with the NSD-2101.

The address of the NSD-2101 is 54h (unless the ADR pin is held high in which case the address would be 55h).

I²C supports 8 data bits and 1 acknowledge bit for a total of 9 bits or clock cycles per byte. When attempting to select a device, the first byte transmitted by the master contains the device address. This address occupies the upper 7 data bits with data bit 0 having a value of zero which indicates a write operation (theNSD-2101 does not support a read operation).

Therefore when addressing the NSD-2101 the actual value sent by the host during the first 8 SCL (clock) cycles would be A8h (or AAh if ADR pin high). If the NSD-2101 is powered and connected properly to the SDA/SCL lines then on the 9th clock pulse, the NSD-2101 will hold the data line low (acknowledge).

The second byte transmitted must be the number of the register to be written. For example, if attempting to send a pulse count, then the register value would be 2.

The third and any subsequent bytes are the values to be written to the specified register and, if more than three bytes are being sent, the following registers in increasing order.

If the following data were sent over the I²C bus:

A80277FF

Then registers 02 and 03 of the NSD-2101 would receive values of 77h and FFh respectively.

Supporting More Than Two NSD-2101s on a Single I²C Bus.

To support more than two NSD-2101 drivers on the same I²C bus, the ADR pin may be used as a chip select. That is, one driver is held low by the host and on all others it is held high. The host then sends commands to the driver with ADR held low. This of course requires that there be a separate chip select line for each NSD-2101.

How Motion is Generated.

Motion is initiated by directing the NSD-2101 to issue pulses to the motor. In the case of the SQL-RV-1.8 motor, to get any motion, the interval between the start of each pulse (i.e. the period) must be within some tolerance (e.g. ±2KHz) of the resonant frequency of the motor (e.g. ~172 kHz).

The closer this period is to the resonant frequency of the motor, the more speed/push force is available. Keep in mind that this is a friction drive which means the amount of motion is dependent on supply voltage, applied frequency vs. actual resonant frequency and the load on the motor.

From an idle state, a minimum of 5 to 10 pulses are required to build up enough orbital motion (of the nut about the screw) to advance the screw. The minimum pulse count varies with load (higher load, more pulses) and whether or not motion is against or with the load (more against, fewer with).

As shown in Figure 3, the drive signal is composed of two waveforms (square waves) and each waveform may be full or half bridge. In the case of the SQL motor, these waveforms are 90 degrees out of phase (in keeping with the geometry of the nut). The phase that leads determines the direction of motion (direction is set by the host using a bit from the pulse count register).

By default the pulse width of each waveform is 50% of the period (i.e. if register 04 is zero; e.g. pulse with would be 2.9 µsec if the period is 5.8 µsec). But you can adjust the pulse width as one means to regulate speed. The shorter the pulse width (below 50% of the period), the less time the piezo has to change shape and thus the amount of engagement between nut and screw is reduced.

The default phase shift between waveforms is 25% of the period (i.e. if register 05 is zero). This can also be adjusted and would be for other motor geometries but in the case of the SQL-RV-1.8; 25% is recommended.

A second means to adjust speed is to set the ratio of full bridge pulses to half bridge pulses (Hybrid Speed Control). This effectively sets the average voltage seen by the motor. If the supply is 3V then in full bridge the motor “sees” 6V. But if the hybrid speed is 33% then, on an average, the motor sees 4V.

Note: Due to dissipation limitations of the driver chip, the maximum supply voltage for full bridge operation is 4.5V (9V to the piezo). Although the driver supports a supply of up to 5.5V, at any level above 4.5V, the output needs to be half bridge. Within that limitation the hybrid speed control is more power efficient than the pulse width control method of the regulating speed since the amount of switching into the capacitive load of the motor is being reduced.

Directing the NSD-2101.

The basic command that is sent to the NSD-2101 is the pulse count (with direction). When a non-zero value is written to registers 02 and 03 by the host microprocessor, the NSD-2101 begins generating pulses on the output pins at the interval defined by the period register (01). For each pulse, the specified pulse count is decremented. Pulse generation continues until the pulse count reaches zero or the host writes a zero to registers 02 and 03. See Register Map (page 10) and Pulse Counter (page 12).

Since the pulse counter is limited to 2047 (11 bits), the maximum duration of motion is the 2047 x period. If the period were 5.8 µsec (172.4 kHz), then the duration would be ~11.8 msec. Therefore to produce continuous motion, the pulse count must be reloaded by the host before the previous pulse count expires (in this case - at least every 11.7 msec - but every 10 msec would provide more margin allowing for variations in motor frequency and overhead in the host processer handling I²C traffic).

Given the nominal 25MHz power-up frequency of the VCO within the NSD-2101, the motor period is specified in units of 40 nsec. Therefore the period value necessary to generate a frequency of 172.4 kHz is 145 (or 91 hexadecimal).

As indicated in the previous section, to generate motion, the pulse period must be very near the interval of the mechanical resonant frequency of the motor. However, for a given motor type, manufacturing tolerances, ambient temperature and mounting have an affect on this resonant frequency. To cancel out these affects, the NSD-2101 supports a frequency tuning (or calibration) feature.

Therefore on power-up, it is recommended that after an appropriate default period count for the given motor type is loaded, a frequency sweep calibration is performed followed by an incremental calibration. See Frequency Tracking (page 9). The sweep needs to be performed only once (for a given power cycle); After that, the incremental calibration will keep the motor in tune.

Note: While performing the frequency calibration, the NSD-2101 is adjusting the trimming of its internal VCO to maximize the performance of the motor (not the period count itself).

Furthermore, it is recommended that frequency calibration be performed in a direction that is against the load (typically forward). The reason is that, depending on the mass being moved (i.e. the inertia), there may be chatter (intermittent contact between the load and the screw) when moving with the load. This chatter can affect the calibration.

Starting a frequency sweep calibration (assuming an SQL-RV-1.8 motor):

Reg	Value (hex)	Comment
00	6B	Enables sweep calibration using both motor phases
01	91	172.4 kHz
02	77	Fwd, DT=11*, Upper 3 bits of pulse count set
03	FF	Lower 8 bits of pulse count set
Actual data stream: A8006B9177FF (the host should wait at least 10 msec after start)		

Starting a frequency incremental calibration:

Reg	Value (hex)	Comment
00	67	Enables inc. calibration using both motor phases
01	91	172.4 kHz
02	77	Fwd, DT=11*, Upper 3 bits of pulse count set
03	FF	Lower 8 bits of pulse count set
Actual data stream: A800679177FF (the host should wait at least 10 msec after start)		

Normal operation:

Reg	Value (hex)	Comment
00	63	Using both motor phases, no calibration enabled.
Actual data stream: A80063		

Moving Fwd (full count):

Reg	Value (hex)	Comment
02	77	Fwd, DT=11*, Upper 3 bits of pulse count set
03	FF	Lower 8 bits of pulse count set
Actual data stream: A80277FF		

Moving Rev (full count):

Reg	Value (hex)	Comment
02	37	Rev, DT=11*, Upper 3 bits of pulse count set
03	FF	Lower 8 bits of pulse count set
Actual data stream: A80237FF		

Stopping the Motor:

Reg	Value (hex)	Comment
02	00	Direction & DT* don't matter. Zero upper count bits
03	00	Zero lower count bits
Actual data stream: A8020000		

Note: *DT (dead time): The time interval between the switching of the low side and the high side of a full bridge waveform. The best power efficiency is achieved when using the maximum dead time (i.e. DT=11). This minimizes the power consumed while having no affect on speed/push force.

8.2 Integration with UTAF Motors

New Scale Technologies works closely with OEM customers to provide assistance in using the UTAF motor with the NSD-2101. Please contact New Scale for assistance.

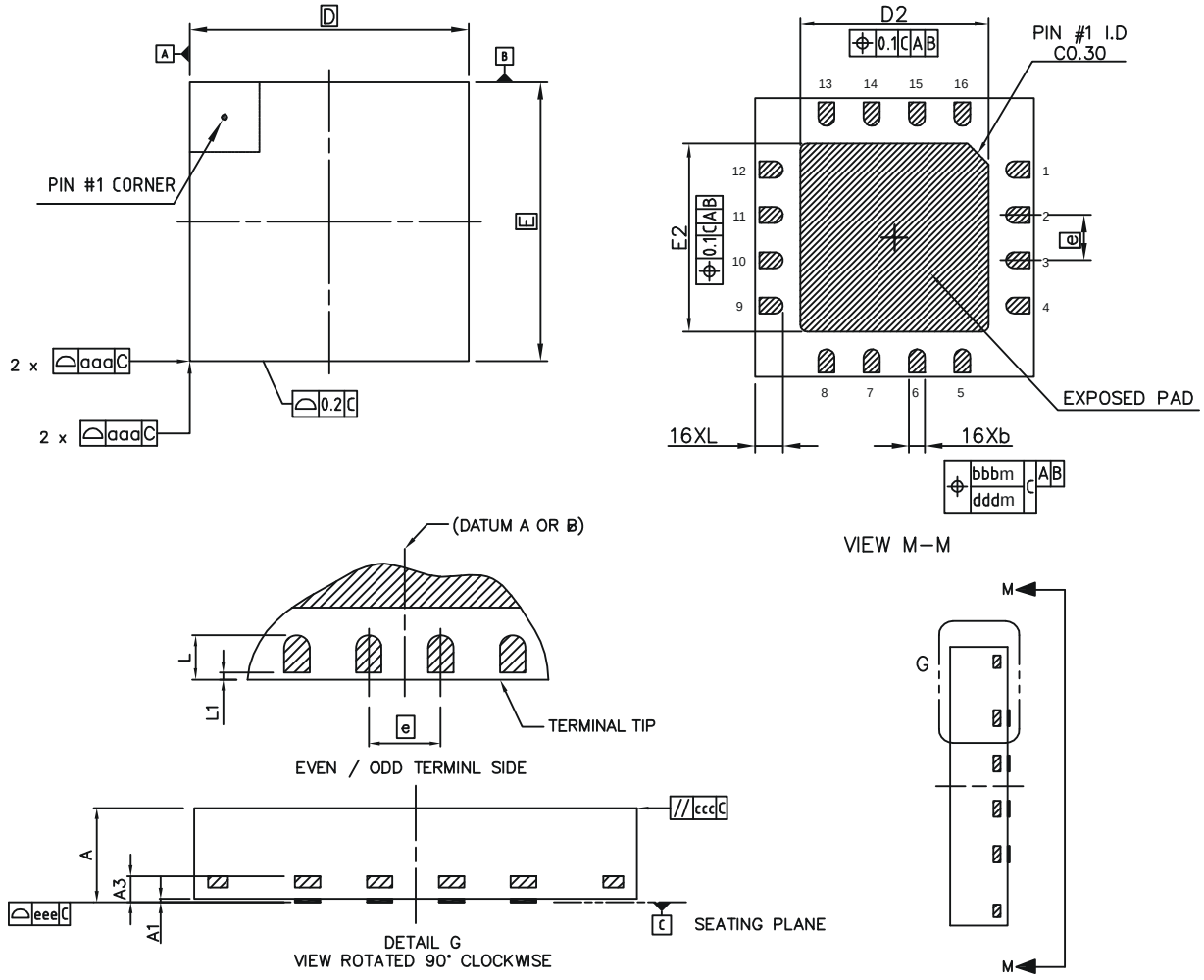
8.3 Integration with Other Motors

The NSD-2101 was designed for use with New Scale Technologies' SQUIGGLE and UTAF motors. Support for other piezo motors may be provided, for a fee, to qualified OEMs. Contact *austriamicrosystems* or New Scale Technologies to discuss your application.

9 Package Drawings and Markings

The devices are available in a 16-pin QFN (4x4mm) package or 16-ball WL-CSP (1.8x1.8mm) package.

Figure 9. 16-pin QFN (4x4mm) Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1			0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D		4.00 BSC	
E		4.00 BSC	
D2	2.50	2.70	2.70
E2	2.50	2.70	2.70

Symbol	Min	Nom	Max
e		0.65 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angles are in degrees.
3. Dimension b applies to metalized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Figure 10. 16-ball WL-CSP (1.8x1.8mm) Package Drawings and Dimensions

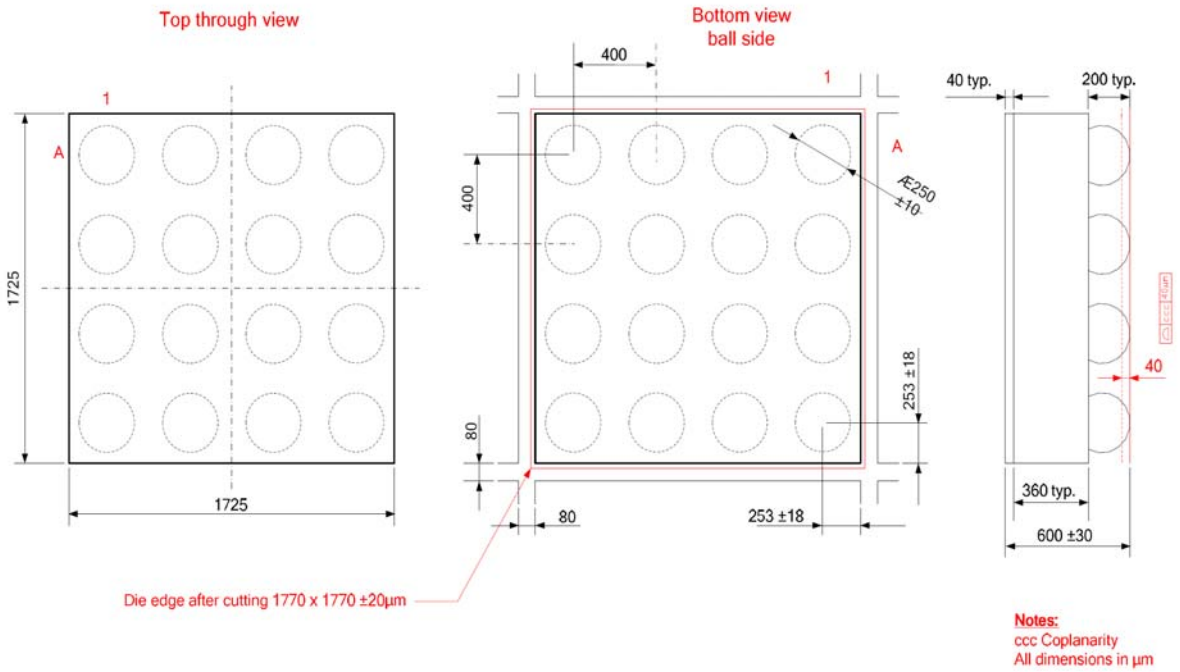
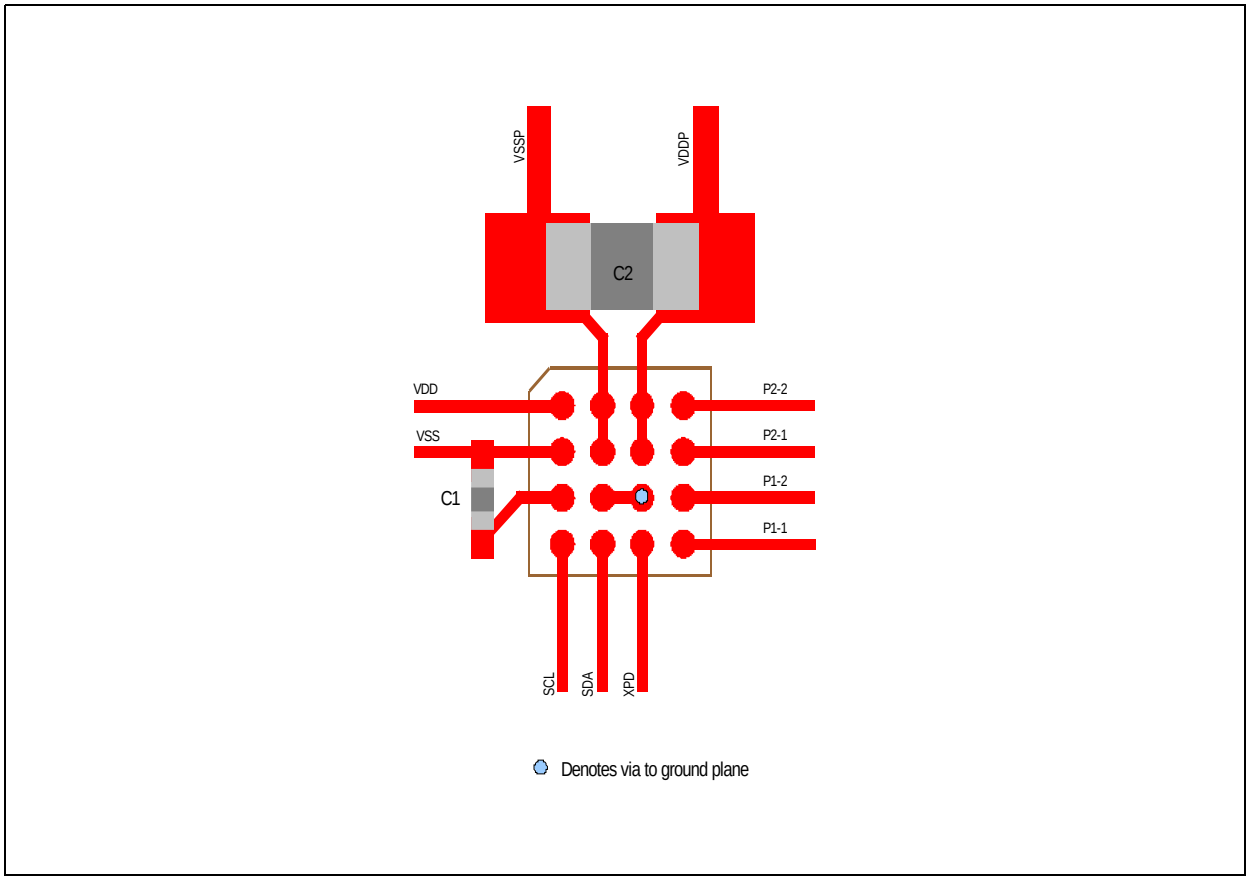


Figure 11. Recommended PCB Layout (Top View)



Revision History

Revision	Date	Owner	Description
0.1	15 Jan, 2010	rweber (NST) / pmo (AMS)	Initial revision
0.2	24 Feb, 2010		Updated Key Features (page 1), Pin Assignments (page 3)
0.3	16 Jun, 2010		Corrected WL-CSP diagram (see Figure 2), added “Top View” to figure title for clarity (see Figure 11)
0.4	26 Aug, 2010		Updated Table 3 with current consumption info, Corrected info in Figure 4 and Table 10, Added Section 8.1, 8.2 and 8.3.
0.5	01 Jul, 2011	rph	Updated Ordering Information (page 21)

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 17.

Table 17. Ordering Information

Ordering Code	Description	Delivery Form	Package
NSD2101-DQFS	Ultrasonic piezo motor driver IC, output for one SQL-RV series reduced voltage SQUIGGLE® RV	Tape & Reel	QFN-16 (4x4mm)
NSD2101-DWLS		Tape & Reel	WL-CSP-16 (1.8x1.8mm)

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is available at http://www.austriamicrosystems.com/Technical-Support

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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