MASTER THESIS

zur Erlangung des akademischen Grades

„Master of Science in Engineering“

im Studiengang MES

Dynamic SystemC-Testbench for automated, constraint-based Verification

Development Stimulator module and Scoreborad module

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Kurzfassung

Content:

* German Abstract

Number of Pages: 1

Abstract

**Schlagwörter:** Schlagwort1, Schlagwort2, Schlagwort3, Schlagwort4, Schlagwort5

Content:

* Abstract

Number of Pages: 1

Acknowledgement

**Keywords:** Keyword1, Keyword2, Keyword3, Keyword4, Keyword5

Content:

* Acknowledgement

Number of Pages: 1

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ANMERKUNG: Dieses Inhaltverzeichnis generiert sich selbst.

# Introduction

Content:

* How Semiconductor components are developed – short history (manually, HDL)
* Verification problem (complex designs, productivity gap)
* History SystemC, SystemVerilog, Intentions, Abstraction Level
* Terms “Direct Testing” “Randomized Testing” “Contraint randomized Testing”

Number of Pages: 2

## Development Environment for SystemC

Content:

* Eclipse C++ IDE
* Visual Studio C++ Express
* SystemC, SCV and TLM library

Number of Pages: 1

## Testbench Design

Content:

* Control-Flow and Data-Flow of a generic Testbench
* Introduction UVM (try to sketch a short history from AVM to OVM to UVM to now)

Number of Pages: 2

## UVM

Content:

* More detailed description of the methodology behind UVM
* Description of the relevant modules for our project

Number of Pages: 5 (incl. Subchapters)

### UVM Sequencer – Stimulus Generator

Content:

* Essentials of UVM Sequence Driver functionality

### UVM Modul 2 – Driver

### UVM Modul 3 – Monitor

### UVM Modul 4 – Scoreboard

# Dynamic SystemC-Testbench

Content:

* Start of main part
* Chapter Structure’s description (What’s in Chapter 2, What’s in Chapters 3,4)

Note: Chapter 2 could be considered as a kind of Requirement Specification for the Modules to develop.

Number of Pages: 8 - 10 (incl. Subchapters)

## Overview over developed general Testbench design

Content:

* Top-Level figure of Testbench
* References to AVM, UVM

## Device under Test – Scalable Fulladder

Content:

* DUT’s structural description (SystemC Class Diagram, Functions, Interfaces, …)

## Control Flow within Testbench

Content:

* Sequence diagrams to Flow of Control
* Involved Signals for Testbench control
* Automatically triggered actions by Module’s sensitivity

## Data Flow within Testbench

Content:

* Data Interface Stimulator-Reference Model, Reference Model-Scoreboard, Stimulator-Driver, Driver-DUT, DUT-Monitor, Monitor-Scoreboard
* Control Flow within Testbench, Dataflow within Testbench, Inputs, Outputs, Fulladder-DUT, Module-Splitting with references to Philipp Maroschek’s part
* Description of the relevant modules for our project

## Input parameters and values for Testbench

Content:

* Definition of Datatype of DUT-Input
* Definition of Testsequences and their number of Testcases to generate

## Generated Outputs by the Testbench

Content:

* Description of the needed information within the scoreboard
* Auxiliary output containers (VCD, Database, …)
* Control Flow within Testbench, Dataflow within Testbench, Inputs, Outputs, Fulladder-DUT, Module-Splitting with references to Philipp Maroschek’s part
* Description of the relevant modules for our project

## Developed Modules

Content:

* Description of the presented modules within this document
* Chapter 3: Stimulator Module, Chapter 4: Scoreboard Module
* Description of Philipp Maroschek’s developed modules, reference to his Master Thesis

# Stimulator for constraint-based randomization

Content:

* Detailed description of Stimulator module
* Class Diagrams, Sequence Diagrams
* Data structures
* Interfaces
* Analysis of produced random values

Number of Pages: 15 - 20 (target value, incl. Subchapters)

# Scoreboard for dynamic Testbench

Content:

* Detailed description of Scoreboard module
* Class Diagrams, Sequence Diagrams
* Data structures
* Interfaces
* Output Textfile syntax

Number of Pages: 15 - 20 (target value, incl. Subchapters)

# Conclusion

Content:

* Findings during Testbench design
* Findings during Module development
* SystemC’s Usability for testbench modeling
* Outlook on further developments to the Testbench

Number of Pages: 2 - 4 ( incl. Subchapters)

Literaturverzeichnis

Abbildungsverzeichnis

Tabellenverzeichnis

Abkürzungsverzeichnis

|  |  |
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| WWW | World Wide Web |
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ANMERKUNG: Sortieren Sie die Liste mit der Funktion „Tabelle sortieren“.

Annex A: Guideline for SystemC Setup on Eclipse IDE

Annex B: Listing of Stimulator files

Annex C: Listing of Scoreboard files