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PCIE-DVR Bridge Architecture

RealTek specification on DVD Recordable Technology

Specification for PCIE-DVR: Root Complex Architecture Specification

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1.1 PCI-Express Root Complex Register

Name	From Addr	To Addr	Size	Description
PCI CFG Register	0x9804_E000	0x9804_E03C	64B	PCI compatible register
PCIe Dev Register	0x9804_E040	0x9804_E0FC	192B	PCI-Express device specific register
PCIe Ext Register	0x9804_E100	0x9804_E9FC	2816B	PCI-Express Extend Configuration
DVR Register	0x9804_EC00	0x9804_EFC-		DVR space register

Table 1: PCI-Express 1.1 Root Complex Register Mapping Table

Name	From Addr	To Addr	Size	Description
PCI CFG Register	0x9803_B000	0x9803_B03C	64B	PCI compatible register
PCIe Dev Register	0x9803_B040	0x9803_B0FC	192B	PCI-Express device specific register
PCIe Ext Register	0x9803_B100	0x9803_B9FC	2816B	PCI-Express Extend Configuration
DVR Register	0x9803_BC00	0x9803_BFC-		DVR space register

Table 2 PCI-Express 2.0 Root Complex Register Mapping Table

The offset of L1SUB_CAP register is wrong in DW MAC data book, please reference table 16.

Register	Offset	Description
L1SUB_CAP_HEADER_REG	0x170	Description: L1 Substates Extended Capability Header. For a description of this standard...
L1SUB_CAPABILITY_REG	0x174	ription: L1 Substates Capability Register. For a description of this standard PCIe...
L1SUB_CONTROL1_REG	0x178	Description: L1 Substates Control 1 Register. For a description of this standard PCIe...
L1SUB_CONTROL2_REG	0x17c	Description: L1 Substates Control 2 Register. For a description of this standard PCIe...

Table 3: Registers for Address Block: PF0_L1SUB_CAP

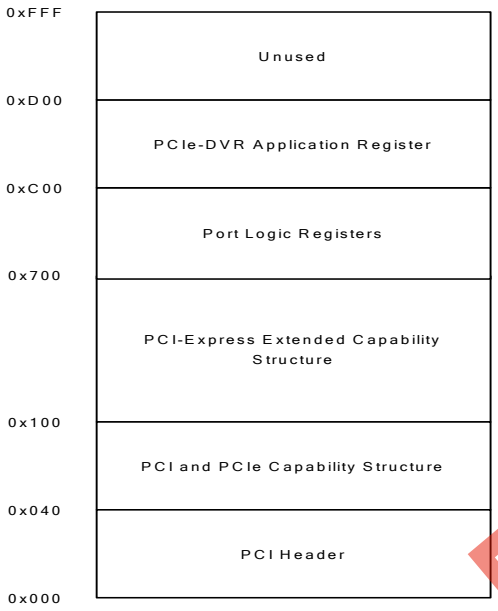

Figure 1: PCI-e register mapping

1.1.1 PCIE 1.1 DVR register

Module::pcie 11	Register::SYS_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC00

Name	Bits	R/W	Default	Comments
Rvd	31..23	-	-	-
clk_reqkeep	22	R/W	‘b0	1: stop request pipe clk from PCIE PHY 0: request pipe clk from PCIE PHY this register is clk_sys domain to avoid dead lock
clk_req_mux	21	R/W	’b0	switch PCIE PHY clk_req_n control from Mac to regif. When set, clk_req_n of PHY control by clk_reqkeep, otherwise by PCIE Mac this register is clk_sys domain to avoid dead lock
tran_en	20	R/W	‘b0	enable pcie translation address
mm_io_type	19	R/W	’b0	PCIE address trans enable in MM mode or IO mode 1 : MM mode 0: IO mode
phy_mdio_oe	18	R/W	‘b0	PCIe MDIO output polarity (FPGA)
phy_mdio_rstN	17	R/W	’b0	PCIe PHY register reset (FPGA)
app_init_rst	16	R/W	’b0	One Pulse trigger
Rvd	15:12	-	-	-
dis_ck_gate	11	R/W	‘b0	Disable clock gating

dis_rw_flow	10	R/W	‘b0	Disable dbus W/R flow control
loopback_en	9	R/W	‘b0	Enable loopback
dir_req_info_en	8	R/W	’b0	Enable to use field 1801_EC18
Rvd	7..6	-	-	-
indir_cfg_en	5	R/W	’b0	Enable cfg command using indirect
dir_cfg_en	4	R/W	’b0	Enable cfg command using direct
rcv_addr0_en	3	R/W	’b0	Receiver address translation enable
rcv_addr1_en	2	R/W	’b0	Receiver address translation enable
app_ltssm_en	1	R/W	’b0	Application ready enable to initial raining
rcv_trans_en	0	R/W	’b0	Receiver translation mechanism enable

Module::pcie 11	Register::INT_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC04

Name	Bits	R/W	Default	Comments
Rvd	31..14	-	-	-
link_up_intp_en	13	R/W	‘b0	-
pcie_legacy_msi_en	12	R/W	‘b0	-
pme_msi_intp_en	11	R/W	‘b0	-
aer_rc_err_msi_intp_en	10	R/W	‘b0	-
cfg_sys_err_rc_intp_en	9	R/W	‘b0	-
pm_to_ack_intp_en	8	R/W	‘b0	-
vendor_msg_intp_en	7	R/W	‘b0	-
rtgt_error_intp_en	6	R/W	‘b0	-
rtgt_timeout_intp_en	5	R/W	‘b0	-
rcpl_error_intp_en	4	R/W	‘b0	-
rcpl_timeout_intp_en	3	R/W	‘b0	-
dir_error_intp_en	2	R/W	‘b0	-
indir_cfg_intp_en	1	R/W	‘b0	-
indir_mio_intp_en	0	R/W	‘b0	-

Module::pcie 11	Register::GNR_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9804_EC08

Name	Bits	R/W	Default	Comments
Rvd	31..16	-	-	-
link_up_int	15	R	‘b0	-
pcie_legacy_msi_int	14	R	‘b0	-
pm_to_ack_int	13	R	‘b0	-
cfg_sys_err_rc_int	12	R	‘b0	-
pcie_legacy_int	11	R	‘b0	Disable through cfg_reg
cfg_radm_vendor_msg_int	10	R	‘b0	-
cfg_pme_msi	9	R	‘b0	-
cfg_pme_int	8	R	‘b0	-
cfg_aer_rc_err_msi	7	R	‘b0	-
cfg_aer_rc_err_int	6	R	‘b0	-
intp_rtgt	5	R	‘b0	Slave receiver interrupt
intp_rcpl	4	R	‘b0	Master receiver interrupt
intp_dir_cfg	3	R	‘b0	Direct CFG interrupt status
intp_dir_mio	2	R	‘b0	Direct MIO interrupt status
intp_cfg	1	R	‘b0	Indirect CFG interrupt status
intp_mio	0	R	‘b0	Indirect MIO interrupt status

Module::pcie 11	Register::PCIE_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9804_EC0C

Name	Bits	R/W	Default	Comments
Rvd	31..4	-	-	-
intp_intd	3	R	‘b0	Interrupt D status register
intp_intc	2	R	‘b0	Interrupt C status register
intp_intb	1	R	‘b0	Interrupt B status register
intp_inta	0	R	‘b0	Interrupt A status register

Module::pcie 11	Register::DBI_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC10

Name	Bits	R/W	Default	Comments
Rvd	31..10	-	-	-
dbi_io_access	9	R/W	‘b0	DBI access is an I/O access
dbi_rom_access	8	R/W	‘b0	DBI access ROM expansion
dbi_bar_num	7..5	R/W	‘b0	BAR number of current DBI
dbi_func_num	4..2	R/W	‘b0	Function number of current DBI
dbi_cs2_access	1	R/W	‘b0	1’b1: read/write CDM mask register
dbi_cmd_access	0	R/W	‘b0	1’b1: ELBI bus, 1’b0: CMD

Module::pcie 11	Register:: INDIR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC14

Name	Bits	R/W	Default	Comments
Rvd	31..14	-	-	-
req_info_align	13	R/W	‘b0	Indirect auto alignament enable
req_info_attr	12..11	R/W	‘b0	-
req_info_ep	10	R/W	‘b0	-
req_info_tc	9..7	R/W	‘b0	-
req_info_type	6..2	R/W	‘b0	-
req_info_fmt	1..0	R/W	‘b0	-

Module::pcie 11	Register:: DIR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC18

Name	Bits	R/W	Default	Comments
Rvd	31..14	-	-	-
req_info_align	13	R/W	‘b0	direct auto alignament enable
req_info_attr	12..11	R/W	‘b0	-
req_info_ep	10	R/W	‘b0	-
req_info_tc	9..7	R/W	‘b0	-
req_info_type	6..2	R/W	‘b0	-
req_info_fmt	1..0	R/W	‘b0	-

Module::pcie 11	Register::MDIO_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC1C

Name	Bits	R/W	Default	Comments
data	31..16	R/W	‘h0	Write data or read data.
phy_addr	15..13	R/W	‘d0	MDIO PHY addressing value.
phy_reg_addr	12..8	R/W	‘d0	MDIO Register addressing value
mdio_busy	7	R/W	‘d0	-

mdio_st	6..5	R/W	‘d0	MDIO host controller state Monitor
mdio_rdy	4	R/W	‘d0	MDIO Pre-amble signal Monitor
mclk_rate	3..2	R/W	‘d0	MDIO clock rate selection: 2’b00: clk_sys/32 2’b01: clk_sys/16 2’b10: clk_sys/8 2’b11: clk_sys/4
mdio_srst	1	R/W	‘d0	Assert 1’b1 to do soft reset
mdio_rdwr	0	R/W	‘d0	1’b0: read , 1’b1: write

Module::pcie 11	Register::PCIE_BASE0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC20
Name	Bits	R/W	Default	Comments	
rtrans_base_addr	31..0	R/W	‘b0	-	

Module::pcie 11	Register::PCIE_BASE1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC24
Name	Bits	R/W	Default	Comments	
rtrans_base_addr	31..0	R/W	‘b0	-	

Module::pcie 11	Register::PCIE_MASK0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC28
Name	Bits	R/W	Default	Comments	
rtrans_mask	31..0	R/W	‘d0	Read only, max 256MB for BA	

Module::pcie 11	Register::PCIE_MASK1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC2C
Name	Bits	R/W	Default	Comments	
rtrans_mask	31..0	R/W	‘d0	Read only, max 256MB for BA	

Module::pcie 11	Register::PCIE_TRAN0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC30
Name	Bits	R/W	Default	Comments	
rtrans_addr_in	31..0	R/W	‘b0	This address replace the address of inbound request header for 31 to 0 bit	

Module::pcie 11	Register::PCIE_TRAN1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC34
Name	Bits	R/W	Default	Comments	
rtrans_addr_in	31..0	R/W	‘b0	This address replace the address of inbound request header for 31 to 0 bit	

Module::pcie 11	Register::CFG_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC38
Name	Bits	R/W	Default	Comments	

Rvd	31..1	-	-	-
go_ct	0	R/W	‘b0	Start DMA transfer, clear after done

Module::pcie 11	Register::CFG_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC3C

Name	Bits	R/W	Default	Comments
Rvd	31..24	R/W	-	-
bus_num	23..16	R/W	‘d0	-
dev_num	15..11	R/W	‘d0	-
fun_num	10..8	R/W	‘d0	-
byte_cnt	7..4	R/W	‘d0	Store byte enable bits
Rvd	3	-	-	-
error_en	2	R/W	‘b0	Enable error timeout timer
byte_en	1	R/W	‘b0	Byte enables default signal “0”: 1111, enable all “1”: Byte_cnt_7to4_0c
wrrd_en	0	R/W	‘b0	“0”: read op, “1”: write op

Module::pcie 11	Register::CFG_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC40

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
error_st	1	R/W	‘b0	Write 1 to clear
done_st	0	R/W	‘b0	Write 1 to clear

Module::pcie 11	Register::CFG_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC44

Name	Bits	R/W	Default	Comments
space_addr	31..0	R/W	‘d0-	PCI CFG format, spec: 3.2.2.3.2

Module::pcie 11	Register::CFG_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC48

Name	Bits	R/W	Default	Comments
space_wdata	31..0	R/W	‘d0	PCI CFG data to be write

Module::pcie 11	Register::CFG_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC4C

Name	Bits	R/W	Default	Comments
space_rdata	31..0	R/W	‘d0	PCI CFG data read back

Module::pcie 11	Register::MIO_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC50

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-
go_ct	0	R/W	‘b0	Start DMA transfer, clear after done

Module::pcie 11	Register::MIO_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC54

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
error_st	1	R/W	'b0	Write 1 to clear
done_st	0	R/W	'b0	Write 1 to clear

Module::pcie 11	Register::MIO_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC58

Name	Bits	R/W	Default	Comments
timeout_cnt_value	31..8	R/W	'd0	Timeout counter expired value
byte_cnt	7.4	R/W	'd0	Store byte enable bits
Rvd	3	-	-	-
error_en	2	R/W	'b0	Enable error timeout counter
byte_en	1	R/W	'b0	Byte enable default signal "0": 1111, enable all "1": byte_cnt_11to8_20
wrrd_en	0	R/W	'b0	"0": read, "1" write

Module::pcie 11	Register::MIO_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC5C

Name	Bits	R/W	Default	Comments
pcie_addr	31..0	R/W	'd0	PCI M and IO address

Module::pcie 11	Register::MIO_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC60

Name	Bits	R/W	Default	Comments
pcie_wdata	31..0	R/W	'd0	PCI MM and IO data to be write

Module::pcie 11	Register::MIO_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC64

Name	Bits	R/W	Default	Comments
pcie_rdata	31..0	R/W	'd0	PCI MM and IO data read back

Module::pcie 11	Register::PHY_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC68

Name	Bits	R/W	Default	Comments
Rvd	31..5	-	-	-
RX50_LINK	4	R/W	'b1	PHY 50ohm power save 0 = saved, by can't link training 1 = off
POW_PCIEX	3	R/W	'b0	Power rstN for pcie phy analog 0 = reset on 1 = reset off
REG_PLLDVR	2..0	R/W	'b0	Enable PLL to give device 100MHz clk. 000 = off, received clock (device) 001 = on, drive clock (host)

Module::pcie 11	Register::PWR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC6C

Name	Bits	R/W	Default	Comments
Rvd	31..7	-	-	-
app_pmxmt_turnoff	6	R/W	'b0	-

app_clk_req_n	5	R/W	‘b0	-
app_clk_pm_en	4	R/W	‘b0	-
sys_aux_pwr_det	3	R/W	‘b0	-
app_ready_enter_123	2	R/W	‘b0	-
app_req_exit_11	1	R/W	‘b0	-
app_req_enter_11	0	R/W	‘b0	-

Module::pcie 11	Register::PCIE_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC70
Name	Bits	R/W	Default	Comments	
Rvd	31..13	-	-	-	
dbg_sel1	12..7	R/W	‘b0	Select debug signal sets to be probed via cp_dbg_out1	
dbg_sel0	6..1	R/W	‘b0	Select debug signal sets to be probed via cp_dbg_out0	
dbg_en	0	R/W	‘b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both cp_dbg_out0 and cp_dbg_out1 are static 16’h0.	

Module::pcie 11	Register::DIR_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC74
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
cfg_rerror_st	1	R/W	‘b0	Write 1 to clear	
mio_rerror_st	0	R/W	‘b0	Write 1 to clear	

Module::pcie 11	Register::DIR_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_EC78
Name	Bits	R/W	Default	Comments	
timeout_cnt_value	31..8	R/W	’d0	-	
Rvd	7..1	-	-	-	
timeout_en	0	R/W	‘b0	Rack to sb2 when read error	

Module::pcie 11	Register::RCPL_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC7C
Name	Bits	R/W	Default	Comments	
Rvd	31..8	-	-	-	
rcpl_status	7..5	R/W	‘d0	Complition status	
rcpl_error_st	4	R/W	‘d0	Write 1 to clear	
tlp_abort_st	3	R/W	‘d0	Write 1 to clear	
dllp_abort_st	2	R/W	‘d0	Write 1 to clear	
ecrc_error_st	1	R/W	‘d0	Write 1 to clear	
rcpl_timeout_st	0	R/W	‘d0	Write 1 to clear	

Module::pcie 11	Register::RCPL_ADR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC80
Name	Bits	R/W	Default	Comments	
nor_error_addr	31..0	R/W	‘d0	-	

Module::pcie 11	Register::RCPL_TOUT0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC84
Name	Bits	R/W	Default	Comments	
to_error_addr	31..0	R/W	‘d0	-	

Module::pcie 11	Register::RCPL_TOUT1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC88
Name	Bits	R/W	Default	Comments	
timeout_num	31:29	R/W	‘d0	-	
timeout_tc	28:26	R/W	‘d0	-	
timeout_attr	25:24	R/W	‘d0	-	
timeout_len	23:12	R/W	‘d0	-	
Rvd	11:8	R/W	‘d0	-	
timeout_tag	7..0	R/W	‘d0	-	

Module::pcie 11	Register::RTGT_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC8C
Name	Bits	R/W	Default	Comments	
Rvd	31..5	-	-	-	
rcpl_compl_st	4	R/W	‘d0	Write 1 to clear	
tlp_abort_st	3	R/W	‘d0	Write 1 to clear	
dllp_abort_st	2	R/W	‘d0	Write 1 to clear	
ecrc_error_st	1	R/W	‘d0	Write 1 to clear	
rcpl_timeout_st	0	R/W	‘d0	Write 1 to clear	

Module::pcie 11	Register::RTGT_ADR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC90
Name	Bits	R/W	Default	Comments	
nor_error_addr	31..0	R/W	‘d0	-	

Module::pcie 11	Register::RTGT_TOUT0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC94
Name	Bits	R/W	Default	Comments	
to_error_addr	31..0	R/W	‘d0	-	

Module::pcie 11	Register::RTGT_TOUT1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC98
Name	Bits	R/W	Default	Comments	
timeout_num	31:29	R/W	‘d0	-	
timeout_tc	28:26	R/W	‘d0	-	
timeout_attr	25:24	R/W	‘d0	-	
timeout_len	23:12	R/W	‘d0	-	
Rvd	11:8	R/W	‘d0	-	
timeout_tag	7..0	R/W	‘d0	-	

Module::pcie 11	Register::AERRO_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_EC9C
Name	Bits	R/W	Default	Comments	

Rvd	31..1	-	-	-
cfg_sys_err_rc	0	R/W	‘b0	Write 1 to clear

Module::pcie 11	Register::AEMSI_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECA0
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-	-	
cfg_aer_int_msg_num	5..1	R/W	‘b0	-	
cfg_aer_rc_err_msi	0	R/W	‘b0	Write 1 to clear	

Module::pcie 11	Register::PME_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECA4
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
radm_pm_to_ack	0	R/W	‘b0	Write 1 to clear	

Module::pcie 11	Register::PMMSI_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECA8
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-	-	
cfg_cap_int_msg_num	5..1	R/W	‘b0	-	
cfg_pme_msi	0	R/W	‘b0	Write 1 to clear	

Module::pcie 11	Register::VEN_MSG0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECAC
Name	Bits	R/W	Default	Comments	
radm_msg_req_id	31..16	R/W	‘b0	-	
Rvd	15..1	-	-	-	
radm_vendor_msg	0	R/W	‘b0	Write 1 to clear	

Module::pcie 11	Register::VEN_MSG1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECB0
Name	Bits	R/W	Default	Comments	
radm_msg_payload	31..0	R/W	‘b0	-	

Module::pcie 11	Register::MAC_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9804_ECB4
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
clk_rdy	16	R	‘b0	set when PCIE PHY pipe clk is stable	
rdlh_link_up	15	R	‘b0		
pm_xtlh_block_tlp	14	R	‘b0		
cfg_bus_master_en	13	R	‘b0		
cfg_pm_no_soft_rst	12	R	‘b0	-	
xmlh_link_up	11	R	‘b0	-	
link_req_rst_not	10	R	‘b0	-	
xmlh_ltssm_state	9..4	R	‘b0	-	

pm_curnt_state	3..1	R	‘b0	-
clk_req_n	0	R	‘b0	-

Module::pcie 11	Register::UNLOCK_MSG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECB8
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
unlock_msg_trigger	0	R/W	’b0	Write 1 to trigger pulse and back to 0	

Module::pcie 11	Register::SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECBC
Name	Bits	R/W	Default	Comments	
reg1	31..16	R/W	‘hffff	Dummy register with value 1	
reg0	15..0	R/W	‘d0	Dummy register with value 0	

Module::pcie 11	Register::LOOP_DATA	Set::4	ATTR::nor_up	Type::SR	ADDR::0x9804_ECC0
Name	Bits	R/W	Default	Comments	
rw_data	31..0	R/W	‘d0	-	

Module::pcie 11	Register::MSI_TRAN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECD 0
Name	Bits	R/W	Default	Comments	
msi_check_addr	31..2	R/W	‘d0	-	
Rvd	1..0	-	-	-	

Module::pcie 11	Register::MSI_DATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECD 4
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
msi_data_st	16	R/W	‘b0	Write 1 to clear	
msi_data	15..0	R/W	‘d0	-	

Module::pcie 11	Register::TMP_REG	Set::4	ATTR::ctrl	Type::SR	ADDR::0x9804_ECD8
Name	Bits	R/W	Default	Comments	
test_reg	31..0	R/W	‘d0	Dummy test register	

Module::pcie 11	Register::LINK_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECE8
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-		
link_up_st	0	R/W	‘b0	Hot-plug link up status	

Module::pcie 11	Register::bist_ctrl	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECEC
Name	Bits	R/W	Default	Comments	
bist4_rm	31..28	R/W	‘h0	control group 4 rm value (all set are clk_sys domain)	
bist4_rme	27	R/W	‘b0	control group 4 rme	
bist3_rm	26..23	R/W	‘h0	control group 3 rm value	
bist3_rme	22	R/W	‘b0	control group 3 rme	
bist2_rm	21..18	R/W	‘h0	control group 2 rm value	

bist2_rme	17	R/W	‘b0	control group 2 rme
bist1_rm	16..13	R/W	’h0	control group 1 rm value
bist1_rme	12	R/W	‘b0	control group 1 rme
bist4_drf_test_resume	11	R/W	‘b0	control group4 sram test resume
drf_bist4_mode_en	10	R/W	‘b0	enable group4 sram drf bist mode
bist4_mode_en	9	R/W	‘b0	enable group4 sram bist mode
bist3_drf_test_resume	8	R/W	‘b0	control group3 sram test resume
drf_bist3_mode_en	7	R/W	‘b0	enable group3 sram drf bist mode
bist3_mode_en	6	R/W	‘b0	enable group3 sram bist mode
bist2_drf_test_resume	5	R/W	‘b0	control group2 sram test resume
drf_bist2_mode_en	4	R/W	‘b0	enable group2 sram drf bist mode
bist2_mode_en	3	R/W	‘b0	enable group2 sram bist mode
bist1_drf_test_resume	2	R/W	‘b0	control group1 sram test resume
drf_bist1_mode_en	1	R/W	‘b0	enable group1 sram drf bist mode
bist1_mode_en	0	R/W	‘b0	enable group1 sram bist mode

Module::pcie 11	Register::bist_status	Set::1	ATTR::nor	Type::SR	ADDR::0x9804_ECF0

Name	Bits	R/W	Default	Comments
Rvd	31..24	-	-	
bist4_drf_start_pause	23	R	‘b0	group 4 status
drf_bist4_done	22	R	‘b0	group 4 status
bist4_done	21	R	‘b0	group 4 status
bist3_drf_start_pause	20	R	‘b0	group 3 status
drf_bist3_done	19	R	‘b0	group 3 status
bist3_done	18	R	‘b0	group 3 status
drf_bist3_fail_1	17	R	‘b0	group 3 fail status
bist3_fail_1	16	R	‘b0	group 3 fail status
drf_bist3_fail_0	15	R	‘b0	group 3 fail status
bist3_fail_0	14	R	‘b0	group 3 fail status
bist2_drf_start_pause	13	R	‘b0	group 2 status
drf_bist2_done	12	R	‘b0	group 2 status
bist2_done	11	R	‘b0	group 2 status
drf_bist2_fail_1	10	R	‘b0	group 2 fail status
bist2_fail_1	9	R	‘b0	group 2 fail status
drf_bist2_fail_0	8	R	‘b0	group 2 fail status
bist2_fail_0	7	R	‘b0	group 2 fail status
bist1_drf_start_pause	6	R	‘b0	group 1 status
drf_bist1_done	5	R	‘b0	group 1 status
bist1_done	4	R	‘b0	group 1 status
drf_bist4_fail_0	3	R	‘b0	group 1 fail status
bist4_fail_0	2	R	‘b0	group 1 fail status
drf_bist1_fail_0	1	R	‘b0	group 1 fail status
bist1_fail_0	0	R	‘b0	group 1 fail status

Module::pcie 11	Register::sram_pwrdn	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECF4

Name	Bits	R/W	Default	Comments
Rvd	31..21	-	-	
iso_pa2pcie	20	R/W	‘b0	phy iso power control 1 : turn on isolation cell 0 : turn off isolation cell
pa33pc_en	19	R/W	‘b1	3.3 V phy hv power control 1 : 3.3V power enable

				0 : 3.3V power disable
pa12pc_en	18	R/W	‘b1	1.2V phy lv power control 1 : 1.2V power enable 0 : 1.2V power disable
mac_phy_snooz	17	R/W	‘b0	control pcie phy L1 fuction
mac_phy_off	16	R/W	‘b0	control pcie phy L1 fuction
Rvd	15..6	-	-	
sram_ls5	5	R/W	‘b0	Disable sram light sleep function
sram_ls4	4	R/W	‘b0	Disable sram light sleep function
sram_ls3	3	R/W	‘b0	control sram light sleep
sram_ls2	2	R/W	‘b0	control sram light sleep
sram_ls1	1	R/W	‘b0	control sram light sleep
sram_ls0	0	R/W	‘b0	control sram light sleep

Module::pcie 11	Register::VEN_MSG2	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9804_ECF8
Name	Bits	R/W	Default	Comments	
radm_msg_payload_hbyte	31..0	R/W	‘b0	-	

Module::pcie 11	Register::pci_base	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ECFC
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The base address for compare SB2 access PCIE R-bus address used.	

Module::pcie 11	Register::pci_mask	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ED00
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The mask bit for mask SB2 access PCIE R-bus address used.	

Module::pcie 11	Register::pci_trans	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9804_ED04
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The translate address for SB2 access PCIE R-bus address used.	

Module::pcie 11	Register::pci_ltr	Set::1	ATTR:: nor	Type::SR	ADDR::0x9804_ED08
Name	bits	Read/Write	Reset State	Comments	
app_ltr_latency	31..0	R	‘b0	Latency Tolerance Reporting(LTR) message information	

1.1.2 PCIE 2.0 DVR register

Module::pcie20	Register::SYS_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC00
Name	Bits	R/W	Default	Comments	
Rvd	31..23	-	-	-	
clk_reqkeep	22	R/W	‘b0	1: stop request pipe clk from PCIE PHY 0: request pipe clk from PCIE PHY this register is clk_sys domain to avoid dead lock	
clk_req_mux	21	R/W	’b0	switch PCIE PHY clk_req_n control from Mac to regif. When set, clk_req_n of PHY control by clk_reqkeep, otherwise by PCIE Mac this register is clk_sys domain to avoid dead lock	
tran_en	20	R/W	‘b0	enable pcie translation address	
mm_io_type	19	R/W	’b0	PCIE address trans enable in MM mode or IO mode 1 : MM mode 0: IO mode	
phy_mdio_oe	18	R/W	‘b0	PCIe MDIO output polarity (FPGA)	
phy_mdio_rstN	17	R/W	’b0	PCIe PHY register reset (FPGA)	
app_init_rst	16	R/W	’b0	One Pulse trigger	
Rvd	15:12	-	-	-	
dis_ck_gate	11	R/W	‘b0	Disable clock gating	
dis_rw_flow	10	R/W	‘b0	Disable dbus W/R flow control	
loopback_en	9	R/W	‘b0	Enable loopback	
dir_req_info_en	8	R/W	’b0	Enable to use field 1801_EC18	
Rvd	7..6	-	-	-	
indir_cfg_en	5	R/W	’b0	Enable cfg command using indirect	
dir_cfg_en	4	R/W	’b0	Enable cfg command using direct	
rcv_addr0_en	3	R/W	’b0	Receiver address translation enable	
rcv_addr1_en	2	R/W	’b0	Receiver address translation enable	
app_ltssm_en	1	R/W	’b0	Application ready enable to initial raining	
rcv_trans_en	0	R/W	’b0	Receiver translation mechanism enable	

Module::pcie20	Register::INT_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC04
Name	Bits	R/W	Default	Comments	
Rvd	31..14	-	-	-	
link_up_intp_en	13	R/W	‘b0	-	
pcie_legacy_msi_en	12	R/W	‘b0	-	
pme_msi_intp_en	11	R/W	‘b0	-	

aer_rc_err_msi_intp_en	10	R/W	‘b0	-
cfg_sys_err_rc_intp_en	9	R/W	‘b0	-
pm_to_ack_intp_en	8	R/W	‘b0	-
vendor_msg_intp_en	7	R/W	‘b0	-
rtgt_error_intp_en	6	R/W	‘b0	-
rtgt_timeout_intp_en	5	R/W	‘b0	-
rcpl_error_intp_en	4	R/W	‘b0	-
rcpl_timeout_intp_en	3	R/W	‘b0	-
dir_error_intp_en	2	R/W	‘b0	-
indir_cfg_intp_en	1	R/W	‘b0	-
indir_mio_intp_en	0	R/W	‘b0	-

Module::pcie20	Register::GNR_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_BC08
Name	Bits	R/W	Default	Comments	
Rvd	31..16	-	-	-	
link_up_int	15	R	‘b0	-	
pcie_legacy_msi_int	14	R	‘b0	-	
pm_to_ack_int	13	R	‘b0	-	
cfg_sys_err_rc_int	12	R	‘b0	-	
pcie_legacy_int	11	R	‘b0	Disable through cfg_reg	
cfg_radm_vendor_msg_int	10	R	‘b0	-	
cfg_pme_msi	9	R	‘b0	-	
cfg_pme_int	8	R	‘b0	-	
cfg_aer_rc_err_msi	7	R	‘b0	-	
cfg_aer_rc_err_int	6	R	‘b0	-	
intp_rtgt	5	R	‘b0	Slave receiver interrupt	
intp_rcpl	4	R	‘b0	Master receiver interrupt	
intp_dir_cfg	3	R	‘b0	Direct CFG interrupt status	
intp_dir_mio	2	R	‘b0	Direct MIO interrupt status	
intp_cfg	1	R	‘b0	Indirect CFG interrupt status	
intp_mio	0	R	‘b0	Indirect MIO interrupt status	

Module::pcie20	Register::PCIE_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_BC0C
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-	-	-	
intp_intd	3	R	‘b0	Interrupt D status register	
intp_intc	2	R	‘b0	Interrupt C status register	
intp_intb	1	R	‘b0	Interrupt B status register	
intp_inta	0	R	‘b0	Interrupt A status register	

Module::pcie20	Register::DBI_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC10
Name	Bits	R/W	Default	Comments	
Rvd	31..10	-	-	-	
dbi_io_access	9	R/W	‘b0	DBI access is an I/O access	
dbi_rom_access	8	R/W	‘b0	DBI access ROM expansion	
dbi_bar_num	7..5	R/W	‘b0	BAR number of current DBI	
dbi_func_num	4..2	R/W	‘b0	Function number of current DBI	
dbi_cs2_access	1	R/W	‘b0	1’b1: read/write CDM mask register	
dbi_cmd_access	0	R/W	‘b0	1’b1: ELBI bus, 1’b0: CMD	

Module::pcie20	Register:: INDIR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC14
Name	Bits	R/W	Default	Comments	
Rvd	31..14	-	-	-	
req_info_align	13	R/W	‘b0	Indirect auto alignament enable	
req_info_attr	12..11	R/W	‘b0	-	
req_info_ep	10	R/W	‘b0	-	
req_info_tc	9..7	R/W	‘b0	-	
req_info_type	6..2	R/W	‘b0	-	
req_info_fmt	1..0	R/W	‘b0	-	

Module::pcie20	Register:: DIR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC18
Name	Bits	R/W	Default	Comments	
Rvd	31..14	-	-	-	
req_info_align	13	R/W	‘b0	direct auto alignament enable	
req_info_attr	12..11	R/W	‘b0	-	
req_info_ep	10	R/W	‘b0	-	
req_info_tc	9..7	R/W	‘b0	-	
req_info_type	6..2	R/W	‘b0	-	
req_info_fmt	1..0	R/W	‘b0	-	

Module::pcie20	Register::MDIO_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC1C
Name	Bits	R/W	Default	Comments	
data	31..16	R/W	‘h0	Write data or read data.	
phy_addr	15..13	R/W	‘d0	MDIO PHY addressing value.	
phy_reg_addr	12..8	R/W	‘d0	MDIO Register addressing value	
mdio_busy	7	R/W	‘d0	-	
mdio_st	6..5	R/W	‘d0	MDIO host controller state Monitor	
mdio_rdy	4	R/W	‘d0	MDIO Pre-amble signal Monitor	
mclk_rate	3..2	R/W	‘d0	MDIO clock rate selection: 2’b00: clk_sys/32 2’b01: clk_sys/16 2’b10: clk_sys/8 2’b11: clk_sys/4	
mdio_srst	1	R/W	‘d0	Assert 1’b1 to do soft reset	
mdio_rdwr	0	R/W	‘d0	1’b0: read , 1’b1: write	

Module::pcie20	Register::PCIE_BASE0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC20
Name	Bits	R/W	Default	Comments	
rtrans_base_addr	31..0	R/W	‘b0	-	

Module::pcie20	Register::PCIE_BASE1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC24
Name	Bits	R/W	Default	Comments	
rtrans_base_addr	31..0	R/W	‘b0	-	

Module::pcie20	Register::PCIE_MASK0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC28
Name	Bits	R/W	Default	Comments	
rtrans_mask	31..0	R/W	‘d0	Read only, max 256MB for BA	

Module::pcie20	Register::PCIE_MASK1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC2C
Name	Bits	R/W	Default	Comments	
rtrans_mask	31..0	R/W	'd0	Read only, max 256MB for BA	

Module::pcie20	Register::PCIE_TRAN0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC30
Name	Bits	R/W	Default	Comments	
rtrans_addr_in	31..0	R/W	'b0	This address replace the address of inbound request header for 31 to 0 bit	

Module::pcie20	Register::PCIE_TRAN1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC34
Name	Bits	R/W	Default	Comments	
rtrans_addr_in	31..0	R/W	'b0	This address replace the address of inbound request header for 31 to 0 bit	

Module::pcie20	Register::CFG_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC38
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
go_ct	0	R/W	'b0	Start DMA transfer, clear after done	

Module::pcie20	Register::CFG_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC3C
Name	Bits	R/W	Default	Comments	
Rvd	31..24	R/W	-	-	
bus_num	23..16	R/W	'd0	-	
dev_num	15..11	R/W	'd0	-	
fun_num	10..8	R/W	'd0	-	
byte_cnt	7..4	R/W	'd0	Store byte enable bits	
Rvd	3	-	-	-	
error_en	2	R/W	'b0	Enable error timeout timer	
byte_en	1	R/W	'b0	Byte enables default signal "0": 1111, enable all "1": Byte_cnt_7to4_0c	
wrrd_en	0	R/W	'b0	"0": read op, "1": write op	

Module::pcie20	Register::CFG_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC40
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
error_st	1	R/W	'b0	Write 1 to clear	
done_st	0	R/W	'b0	Write 1 to clear	

Module::pcie20	Register::CFG_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC44
Name	Bits	R/W	Default	Comments	
space_addr	31..0	R/W	'd0-	PCI CFG format, spec: 3.2.2.3.2	

Module::pcie20	Register::CFG_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC48

Name	Bits	R/W	Default	Comments
space_wdata	31..0	R/W	‘d0	PCI CFG data to be write

Module::pcie20	Register::CFG_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC4C
Name	Bits	R/W	Default	Comments	
space_rdata	31..0	R/W	‘d0	PCI CFG data read back	

Module::pcie20	Register::MIO_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC50
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
go_ct	0	R/W	‘b0	Start DMA transfer, clear after done	

Module::pcie20	Register::MIO_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC54
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
error_st	1	R/W	‘b0	Write 1 to clear	
done_st	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::MIO_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC58
Name	Bits	R/W	Default	Comments	
timeout_cnt_value	31..8	R/W	‘d0	Timeout counter expired value	
byte_cnt	7.4	R/W	‘d0	Store byte enable bits	
Rvd	3	-	-	-	
error_en	2	R/W	‘b0	Enable error timeout counter	
byte_en	1	R/W	‘b0	Byte enable default signal “0”: 1111, enable all “1”: byte_cnt_11to8_20	
wrrd_en	0	R/W	‘b0	“0”: read, “1” write	

Module::pcie20	Register::MIO_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC5C
Name	Bits	R/W	Default	Comments	
pcie_addr	31..0	R/W	‘d0	PCI M and IO address	

Module::pcie20	Register::MIO_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC60
Name	Bits	R/W	Default	Comments	
pcie_wdata	31..0	R/W	‘d0	PCI MM and IO data to be write	

Module::pcie20	Register::MIO_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC64
Name	Bits	R/W	Default	Comments	
pcie_rdata	31..0	R/W	‘d0	PCI MM and IO data read back	

Module::pcie20	Register::PHY_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC68
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-	-	
ISOLATE	5	R/W	‘b0	CPHY_ISOLATE this register is clk_sys domain to avoid dead lock	
RX50_LINK	4	R/W	‘b1	PHY 50ohm power save	

				0 = saved, by can't link training 1 = off
POW_PCIEX	3	R/W	'b0	Power rstN for pcie phy analog 0 = reset on 1 = reset off
REG_PLLDVR	2..0	R/W	'b0	Enable PLL to give device 100MHz clk. 000 = off, received clock (device) 001 = on, drive clock (host)

Module::pcie20	Register::PWR_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC6C
Name	Bits	R/W	Default	Comments	
Rvd	31..7	-	-	-	
app_pmxmt_turnoff	6	R/W	'b0	-	
app_clk_req_n	5	R/W	'b0	-	
app_clk_pm_en	4	R/W	'b0	-	
sys_aux_pwr_det	3	R/W	'b0	-	
app_ready_enter_123	2	R/W	'b0	-	
app_req_exit_11	1	R/W	'b0	-	
app_req_enter_11	0	R/W	'b0	-	

Module::pcie20	Register::PCIE_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC70
Name	Bits	R/W	Default	Comments	
Rvd	31..13	-	-	-	
dbg_sel1	12..7	R/W	'b0	Select debug signal sets to be probed via cp_dbg_out1	
dbg_sel0	6..1	R/W	'b0	Select debug signal sets to be probed via cp_dbg_out0	
dbg_en	0	R/W	'b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both cp_dbg_out0 and cp_dbg_out1 are static 16'h0.	

Module::pcie20	Register::DIR_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC74
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
cfg_rerror_st	1	R/W	'b0	Write 1 to clear	
mio_rerror_st	0	R/W	'b0	Write 1 to clear	

Module::pcie20	Register::DIR_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BC78
Name	Bits	R/W	Default	Comments	
timeout_cnt_value	31..8	R/W	'd0	-	
Rvd	7..1	-	-	-	
timeout_en	0	R/W	'b0	Rack to sb2 when read error	

Module::pcie20	Register::RCPL_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC7C
Name	Bits	R/W	Default	Comments	
Rvd	31..8	-	-	-	
rcpl_status	7..5	R/W	'd0	Complition status	
rcpl_error_st	4	R/W	'd0	Write 1 to clear	

tlp_abort_st	3	R/W	‘d0	Write 1 to clear
dllp_abort_st	2	R/W	‘d0	Write 1 to clear
ecrc_error_st	1	R/W	‘d0	Write 1 to clear
rcpl_timeout_st	0	R/W	‘d0	Write 1 to clear

Module::pcie20	Register::RCPL_ADR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC80
Name	Bits	R/W	Default	Comments	
nor_error_addr	31..0	R/W	‘d0	-	

Module::pcie20	Register::RCPL_TOUT0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC84
Name	Bits	R/W	Default	Comments	
to_error_addr	31..0	R/W	‘d0	-	

Module::pcie20	Register::RCPL_TOUT1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC88
Name	Bits	R/W	Default	Comments	
timeout_num	31:29	R/W	‘d0	-	
timeout_tc	28:26	R/W	‘d0	-	
timeout_attr	25:24	R/W	‘d0	-	
timeout_len	23:12	R/W	‘d0	-	
Rvd	11:8	R/W	‘d0	-	
timeout_tag	7..0	R/W	‘d0	-	

Module::pcie20	Register::RTGT_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC8C
Name	Bits	R/W	Default	Comments	
Rvd	31..5	-	-	-	
rcpl_compl_st	4	R/W	‘d0	Write 1 to clear	
tlp_abort_st	3	R/W	‘d0	Write 1 to clear	
dllp_abort_st	2	R/W	‘d0	Write 1 to clear	
ecrc_error_st	1	R/W	‘d0	Write 1 to clear	
rcpl_timeout_st	0	R/W	‘d0	Write 1 to clear	

Module::pcie20	Register::RTGT_ADR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC90
Name	Bits	R/W	Default	Comments	
nor_error_addr	31..0	R/W	‘d0	-	

Module::pcie20	Register::RTGT_TOUT0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC94
Name	Bits	R/W	Default	Comments	
to_error_addr	31..0	R/W	‘d0	-	

Module::pcie20	Register::RTGT_TOUT1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC98
Name	Bits	R/W	Default	Comments	
timeout_num	31:29	R/W	‘d0	-	
timeout_tc	28:26	R/W	‘d0	-	
timeout_attr	25:24	R/W	‘d0	-	
timeout_len	23:12	R/W	‘d0	-	
Rvd	11:8	R/W	‘d0	-	

timeout_tag	7..0	R/W	‘d0	-

Module::pcie20	Register::AERRO_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BC9C
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
cfg_sys_err_rc	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::AEMSI_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCA0
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-	-	
cfg_aer_int_msg_num	5..1	R/W	‘b0	-	
cfg_aer_rc_err_msi	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::PME_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCA4
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
radm_pm_to_ack	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::PMMSI_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCA8
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-	-	
cfg_cap_int_msg_num	5..1	R/W	‘b0	-	
cfg_pme_msi	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::VEN_MSG0	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCAC
Name	Bits	R/W	Default	Comments	
radm_msg_req_id	31..16	R/W	‘b0	-	
Rvd	15..1	-	-	-	
radm_vendor_msg	0	R/W	‘b0	Write 1 to clear	

Module::pcie20	Register::VEN_MSG1	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCB0
Name	Bits	R/W	Default	Comments	
radm_msg_payload	31..0	R/W	‘b0	-	

Module::pcie20	Register::MAC_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_BCB4
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
clk_rdy	16	R	‘b0	set when PCIE PHY pipe clk is stable	
rdlh_link_up	15	R	‘b0		
pm_xtlh_block_tlp	14	R	‘b0		
cfg_bus_master_en	13	R	‘b0		

cfg_pm_no_soft_rst	12	R	‘b0	-
xmlh_link_up	11	R	‘b0	-
link_req_rst_not	10	R	‘b0	-
xmlh_ltssm_state	9..4	R	‘b0	-
pm_curnt_state	3..1	R	‘b0	-
clk_req_n	0	R	‘b0	-

Module::pcie20	Register::UNLOCK_MSG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCB8
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
unlock_msg_trigger	0	R/W	’b0	Write 1 to trigger pulse and back to 0	

Module::pcie20	Register::SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCBC
Name	Bits	R/W	Default	Comments	
reg1	31..16	R/W	‘hffff	Dummy register with value 1	
reg0	15..0	R/W	‘d0	Dummy register with value 0	

Module::pcie20	Register::LOOP_DATA	Set::4	ATTR::nor_up	Type::SR	ADDR::0x9803_BCC0
Name	Bits	R/W	Default	Comments	
rw_data	31..0	R/W	‘d0	-	

Module::pcie20	Register::MSI_TRAN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCD0
Name	Bits	R/W	Default	Comments	
msi_check_addr	31..2	R/W	‘d0	-	
Rvd	1..0	-	-	-	

Module::pcie20	Register::MSI_DATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCD4
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
msi_data_st	16	R/W	‘b0	Write 1 to clear	
msi_data	15..0	R/W	‘d0	-	

Module::pcie20	Register::TMP_REG	Set::4	ATTR::ctrl	Type::SR	ADDR::0x9803_BCD8
Name	Bits	R/W	Default	Comments	
test_reg	31..0	R/W	‘d0	Dummy test register	

Module::pcie20	Register::LINK_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9803_BCE8
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-		
link_up_st	0	R/W	‘b0	Hot-plug link up status	

Module::pcie20	Register::bist_ctrl	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCEC
Name	Bits	R/W	Default	Comments	
bist4_rm	31..28	R/W	‘h0	control group 4 rm value (all set are clk_sys domain)	
bist4_rme	27	R/W	‘b0	control group 4 rme	
bist3_rm	26..23	R/W	‘h0	control group 3 rm value	
bist3_rme	22	R/W	‘b0	control group 3 rme	
bist2_rm	21..18	R/W	‘h0	control group 2 rm value	

bist2_rme	17	R/W	‘b0	control group 2 rme
bist1_rm	16..13	R/W	’h0	control group 1 rm value
bist1_rme	12	R/W	‘b0	control group 1 rme
bist4_drf_test_resume	11	R/W	‘b0	control group4 sram test resume
drf_bist4_mode_en	10	R/W	‘b0	enable group4 sram drf bist mode
bist4_mode_en	9	R/W	‘b0	enable group4 sram bist mode
bist3_drf_test_resume	8	R/W	‘b0	control group3 sram test resume
drf_bist3_mode_en	7	R/W	‘b0	enable group3 sram drf bist mode
bist3_mode_en	6	R/W	‘b0	enable group3 sram bist mode
bist2_drf_test_resume	5	R/W	‘b0	control group2 sram test resume
drf_bist2_mode_en	4	R/W	‘b0	enable group2 sram drf bist mode
bist2_mode_en	3	R/W	‘b0	enable group2 sram bist mode
bist1_drf_test_resume	2	R/W	‘b0	control group1 sram test resume
drf_bist1_mode_en	1	R/W	‘b0	enable group1 sram drf bist mode
bist1_mode_en	0	R/W	‘b0	enable group1 sram bist mode

Module::pcie20	Register::bist_status	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_BCF0
Name	Bits	R/W	Default	Comments	
Rvd	31..24	-	-		
bist4_drf_start_pause	23	R	‘b0	group 4 status	
drf_bist4_done	22	R	‘b0	group 4 status	
bist4_done	21	R	‘b0	group 4 status	
bist3_drf_start_pause	20	R	‘b0	group 3 status	
drf_bist3_done	19	R	‘b0	group 3 status	
bist3_done	18	R	‘b0	group 3 status	
drf_bist3_fail_1	17	R	‘b0	group 3 fail status	
bist3_fail_1	16	R	‘b0	group 3 fail status	
drf_bist3_fail_0	15	R	‘b0	group 3 fail status	
bist3_fail_0	14	R	‘b0	group 3 fail status	
bist2_drf_start_pause	13	R	‘b0	group 2 status	
drf_bist2_done	12	R	‘b0	group 2 status	
bist2_done	11	R	‘b0	group 2 status	
drf_bist2_fail_1	10	R	‘b0	group 2 fail status	
bist2_fail_1	9	R	‘b0	group 2 fail status	
drf_bist2_fail_0	8	R	‘b0	group 2 fail status	
bist2_fail_0	7	R	‘b0	group 2 fail status	
bist1_drf_start_pause	6	R	‘b0	group 1 status	
drf_bist1_done	5	R	‘b0	group 1 status	
bist1_done	4	R	‘b0	group 1 status	
drf_bist4_fail_0	3	R	‘b0	group 1 fail status	
bist4_fail_0	2	R	‘b0	group 1 fail status	
drf_bist1_fail_0	1	R	‘b0	group 1 fail status	
bist1_fail_0	0	R	‘b0	group 1 fail status	

Module::pcie20	Register::sram_pwrdn	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCF4
Name	Bits	R/W	Default	Comments	
Rvd	31..21	-	-		
iso_pa2pcie	20	R/W	‘b0	phy iso power control 1 : turn on isolation cell 0 : turn off isolation cell	
pa33pc_en	19	R/W	‘b1	3.3 V phy hv power control 1 : 3.3V power enable 0 : 3.3V power disable	
pa12pc_en	18	R/W	‘b1	1.2V phy lv power control	

				1 : 1.2V power enable 0 : 1.2V power disable
mac_phy_snooz	17	R/W	‘b0	control pcie phy L1 fuction
mac_phy_off	16	R/W	‘b0	control pcie phy L1 fuction
Rvd	15..6	-	-	
sram_ls5	5	R/W	‘b0	Disable sram light sleep function
sram_ls4	4	R/W	‘b0	Disable sram light sleep function
sram_ls3	3	R/W	‘b0	control sram light sleep
sram_ls2	2	R/W	‘b0	control sram light sleep
sram_ls1	1	R/W	‘b0	control sram light sleep
sram_ls0	0	R/W	‘b0	control sram light sleep

Module::pcie20	Register::VEN_MSG2	Set::1	ATTR::nor_up	Type: :SR	ADDR::0x9803_BCF8
Name	Bits	R/W	Default	Comments	
radm_msg_payload_hbyte	31..0	R/W	‘b0	-	

Module::pcie20	Register::pci_base	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BCFC
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The base address for compare SB2 access PCIE R-bus address used.	

Module::pcie20	Register::pci_mask	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BD00
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The mask bit for mask SB2 access PCIE R-bus address used.	

Module::pcie20	Register::pci_trans	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_BD04
Name	**bits**	**Read/Write**	**Reset State**	**Comments**	
addr	31..0	R/W	‘b0	The translate address for SB2 access PCIE R-bus address used.	

Module::pcie20	Register::pci_ltr	Set::1	ATTR:: nor	Type::SR	ADDR::0x9803_BD08
Name	bits	Read/Write	Reset State	Comments	
app_ltr_latency	31..0	R	‘b0	Latency Tolerance Reporting(LTR) message information	

1.2 PCIE (type 1) Configuration Space Description

31 16	15 0	
Device ID	Vendor ID	00h
Status	Command	04h
Class Code	Revision ID	08h
BIST / Header Type	Latency Timer / Cacheline Size	0Ch
Base Address Register #1		10h
Base Address Register #2		14h
Secondary Latency Timer / Subordinate Bus Number	Secondary Bus Number / Primary Bus Number	18h

Secondary Status	I/O Limit	I/O Base	1Ch
Memory Limit	Memory Base		20h
Prefetchable Memory Limit	Prefetchable Memory Base		24h
Prefetchable Base Upper 32 Bits			28h
Prefetchable Limit 32 Upper Bits			2Ch
I/O Limit Upper 32 Bits	I/O Base Upper 32 Bits		30h
Reserved		Capabilities Pointer	34h
Expansion ROM Base Address			38h
Bridge Control	Interrupt Pin	Interrupt Line	3Ch

Table 4: PCI Configuration Space Table

Address	Name	Description	Value	R/W
00h-01h	Vendor ID	Manufacture of the Device		Read-only
02h-03h	Device ID	Particular Device ID		Read-only
08h	Revision ID	Vendor defined extension on the Device ID	0x0	Read-only
09h-0Bh	Class Code	Identify the generic function of the device		Read-only
0Eh	Header Type	Identify the layout of second part of predefine header	0x0	Read-only
0Fh	BIST	Used for control and status of BIST		Read-only

-The command register (04h): The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit#	Name	Description	Implemented
0	I/O Space	"0": Disable the device response to I/O commands "1": Device responds to I/O spaces accessed State after Reset# is "0".	Yes
1	Memory Space	"0": Disable the device response to memory access "1": Device responds to Memory accessed State after Reset# is "0"	Yes
2	Bus Master	"0": Disable the device from generating PCI accesses "1": Device behaves as Master State after Reset# is "0"	Yes
3	Special Cycle	"0": Ignore all special cycle operations "1": allow the device to monitor special cycles State after Reset# is "0"	No
4	Memory Write and Invalidate Enable	"0": Memory write is used "1": Device can generate MWIV command State after Reset# is "0" and used for master device	Yes
5	VGA Palette Snoop	"0": Palette snooping is disable "1": Palette snooping is enable State after Reset# is "0"	No
6	Parity Error Response	"0": Palette "1": After Reset# is "0"	Yes
7	Reserved	Hardwire to "0"	No
8	SERR# Enable	"0": disable SERR# driver "1": enable SERR# driver After Reset# is "0"	Yes
9	Fast Back-to-Back	"0": master can't do fast back-to-back	Yes

	Enable	"1": master support fast back-to-back After Reset# is "0"	
10	Interrupt Disable	"0": "1": After Reset# is "0"	Yes
11-15	Reserved	This bit is reserved	No

-The status register (06h): The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit#	Name	Description	Implemented	R/W
0-2	Reserved	This bit is reserved	No	Reserved
3	Interrupt Status		Yes	Read-only
4	Capabilities List	Device implements the new capabilities linked list at offset 34h. "0": implemented, "1" no implemented	Yes	Read-only
5	66 MHz capable	Indicate if the device is capable of running at 66MHz. "0": no capable, "1": yes, capable	No	Read-only
6	Reserved	This bit is reserved	No	Read-only
7	Fast Back-to-Back Capable	If the target accept back-to-back transaction from not the sane agent. "0": no support, "1": yes, support	No	Read-only
8	Master Data Parity Error	The master implements this bit. It is set when 3 conditions are met. 1) The bus agent asserted PERR# 2) The agent setting the bit acted as the bus master for the operation in which the error occurred. 3) The parity Error Response bit is set	Yes	Read/Write
9-10	DEVSEL Timing	Encode the timing of DEVSEL. "00": fast, by default "10": medium "10": slow	Yes	Read-only
11	Signal Target Abort	Signal is enable when the target terminate with signal abort "0": no target-abort, "1": yes, target-abort	Yes	Read/Write
12	Received Slave Abort	This bit must set by the master devise whenever it terminates a transaction with target-abort. "0": no terminate by target, "1": terminate by target	Yes	Read/Write
13	Received Master Abort	Set the bit when the transaction is terminated with master abort. "0": no master-abort, "1": yes, master-abort	Yes	Read/Write
14	Signaled System Error	Set the bit when the device assert SERR# "0": no SERR# assert, "1": yes, SERR# assert	Yes	Read/Write
15	Detected Parity Error	Set the bit when detects a parity error "0": no parity error, "1": parity error	Yes	Read/Write

Address	Name	Description	Value	R/W

0Ch	Cacheline Size	The register use to specify the system cacheline size. Use for memory read line and multiple. Unit: Dwords. Max:64 bytes, because of Dbus	0000_1111	Read/Write
0Dh	Latency Timer	Unit: PCI clock. Number set according PCI local bus spec section 3.5.4.1, Byte transfer: 128 Bytes	38clocks	Read/Write
3Ch	Interrupt Line	Communicate interrupt line routing		Read/Write
3Dh	Interrupt Pin	Tell which interrupt pin the device uses. 05h through FFh are reserved.	1	Read/Write
3Eh	Min_Gnt	Specify how long a burst period the device need		Read-only
3Fh	Max_Lat	Specify how often the device need to gain access to the PCI bus		Read/Write

2 PCIE Design SPEC

2.1 PCIE1.1

- **SRAM list**

SRAM name	Process	Type	Size
PCIE_SFDKV1024X34X1M4F140	TSMC28	Single port	1024x34 bits
PCIE_TF1CKKV64X104X1M2F140	TSMC28	Two port 1Clk	64x104 bits
PCIE_TF1CKKV256X38X1M2F140	TSMC28	Two port 1Clk	256 x 38 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TF1CKKV256X10X1M4F140	TSMC28	Two port 1Clk	256 x 10 bits

- **Clock and timing spec**

Limits	System clock frequency (clk_sys)	pipe clk
Upper bound	syn: 257 MHz / real: 243 MHz	syn: 138.8 MHz / real: 125 MHz
Lower bound	No constraint	No constraint

- **Reset spec**

Reset signal	Description
crt_pcie_rstn	Asynchronous reset.
crt_pcie_phy_rstn	Asynchronous reset.
crt_pcie_phy_mdio_rstn	Asynchronous reset.
crt_pcie_stitch_rstn	Asynchronous reset.
crt_pcie_nonstitch_rstn	Asynchronous reset.
crt_pcie_power_rstn	Asynchronous reset.
crt_pcie_core_rstn	Asynchronous reset.

- **Module area**

Type	Size
Logic area	47524.693736 um^2
SRAM area	28994.539672 um^2

- **ATPG coverage**

ATPG type	Coverage
Test coverage	98.45 %
Fault coverage	97.95 %

- **Power info:SSG0P9VN40C**

Type	Power
Leakage power	1.4151 mW
Switching power	113.8672 mW

- **Clock gated rate**

Type	Rate
Clock gated rate	83.68%

2.2 PCIE2.0

- **SRAM list**

SRAM name	Process	Type	Size
PCIE_SFDKV1024X34X1M4F140	TSMC28	Single port	1024x34 bits
PCIE_TF1CKKV64X104X1M2F140	TSMC28	Two port 1Clk	64x104 bits
PCIE_TF1CKKV256X38X1M2F140	TSMC28	Two port 1Clk	256 x 38 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TFDG2KV72X64X1M1F330	TSMC28	Two port	72 x 64 bits
PCIE_TF1CKKV256X10X1M4F140	TSMC28	Two port 1Clk	256 x 10 bits

- **Clock and timing spec**

Limits	System clock frequency (clk_sys)	pipe clk
Upper bound	syn: 257 MHz / real: 243 MHz	syn: 138.8 MHz / real: 125 MHz
Lower bound	No constraint	No constraint

- **Reset spec**

Reset signal	Description
crt_pcie_rstn	Asynchronous reset.
crt_pcie_phy_rstn	Asynchronous reset.
crt_pcie_phy_mdio_rstn	Asynchronous reset.
crt_pcie_stitch_rstn	Asynchronous reset.
crt_pcie_nonstitch_rstn	Asynchronous reset.
crt_pcie_power_rstn	Asynchronous reset.
crt_pcie_core_rstn	Asynchronous reset.

- **Module area**

Type	Size
Logic area	49786.015755 um^2
SRAM area	28994.539672 um^2

- **ATPG coverage**

ATPG type	Coverage
Test coverage	98.35 %
Fault coverage	97.83 %

- **Power info:SSG0P9VN40C**

Type	Power
Leakage power	1.4704 mW
Switching power	114.3564 mW

- **Clock gated rate**

Type	Rate
Clock gated rate	82.23%