RealcomTec
Real Communications, Inc.
A Subsidiary of Realtek Group

Standard for RealTek DVD Recordable

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Kylin USB3.0

RealTek specification on DVD Recordable Technology

Specification for Kylin: USB3.0 Specification

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1.1 REGISTER:: WRAP_CTR_reg 0x9801_3200

Module::usb	Register::WRAP_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3200
Name	Bits	R/W	Default	Comments	
Rvd	31..7	-	-	-	
rxdetect_value	6	R/W	‘b0		
rxdetect_sel	5	R/W	‘b0		
resume_cycle_sel	4	R/W	‘b0		
sram_debug_sel	3	R/W	‘b0	Select sram 1: host 0: device	
sram_debug_mode	2	R/W	‘b0	Enable sram debug mode	
dbus_multi_req_disable	1	R/W	’b0	Disable multiple request for Dbus 0: enable multiple request 1: disable multiple request	
dev_mode	0	R/W	’b0	Enable peek on AHB burst length 0: host (2) 1: host/dev	

1.2 REGISTER:: GNT_INT_reg 0x9801_3204

Module::usb	Register::GNR_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3204
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
device_int	1	R	‘b0	USB3 Device MAC interrupt	
host_int	0	R	‘b0	USB3 Host MAC interrupt	

1.3 REGISTER:: USB2_PHY_UTMI 0x9801_3208

Module::usb	Register::USB2_PHY_UTMI	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3208
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
reset_utmi_p0	0	R/W	‘b0	UTMI reset to PHY1 (sync and automatically return to low)	

1.4 REGISTER:: USB3_PHY_PIPE 0x9801_320c

Module::usb	Register::USB3_PHY_PIPE	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_320c
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
reset_pipe3_p0	0	R/W	‘b0	PIPE3 reset to PHY1 (sync and automatically return to low)	

1.5 REGISTER:: MDIO_CTR_reg 0x9801_3210

Module::usb	Register::MDIO_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3210

Name	Bits	R/W	Default	Comments
data	31..16	R/W	'h0	Write data or read data.
phy_addr	15..13	R/W	'd0	MDIO PHY addressing value.
phy_reg_addr	12..8	R/W	'd0	MDIO Register addressing value
mdio_busy	7	R/W	'd0	-
mdio_st	6..5	R/W	'd0	MDIO host controller state Monitor
mdio_rdy	4	R/W	'd0	MDIO Pre-amble signal Monitor
mclk_rate	3..2	R/W	'd0	MDIO clock rate selection: 2'b00: clk_sys/32 2'b01: clk_sys/16 2'b10: clk_sys/8 2'b11: clk_sys/4
mdio_srst	1	R/W	'd0	Assert 1'b1 to do soft reset
mdio_rdwr	0	R/W	'd0	1'b0: read , 1'b1: write

1.6 REGISTER:: VSTATUS_port0_reg 0x9801_3214

Module::usb	Register::VSTATUS0_OUT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3214

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
p0_vstatus_out	7..0	R/W	'h00	Vstatus output for port1 (It's used to configure PHY's control register)

The process of configuring PHY control register:

1. write VSTATUS_reg (0x9801_3214), (data output to PHY)
2. write GUSB2PHY Accn (0x1802_8280)
   [25]: vload
   [23]: vBusy
   [11:8]: vcontrol
   [7:0]: vstatus_in (data input from PHY)

Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'b0	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. **Note:** This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. **Note:** These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) ■ UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ■ ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) ■ UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ■ ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.7 REGISTER:: SLP_BACK_EN_port0_reg 0x9801_3218

Module::usb	Register::SLP_BACK0_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3218
Name	Bits	R/W	Default	Comments	

Rvd	31..4	-	-	-
simulation_mode_p0	3	R/W	‘b0	Reduce counter for entering HS
force_hs_mode_p0	2	R/W	‘b0	Force HOST IP enter high speed mode 0: disable 1: enable
test_rst_p0	1	R/W	‘b0	Self loop back reset
test_en_p0	0	R/W	‘b0	Self loop back enable

1.8 REGISTER:: SLP_BACK_CTR_port0_reg 0x9801_321c

Module::usb	Register::SLP_BACK0_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_321c
Name	Bits	R/W	Default	Comments	
Rvd	31..12	-	-	-	
test_speed_p0	11..10	R/W	‘h0	When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2’b01: force PHY in HS 2’b10: force PHY in FS/LS 2’b00/2’b11: normal mode	
test_seed_p0	9..2	R/W	‘h0	Self_loop_back Random generator seed	
test_psl_p0	1..0	R/W	‘h0	Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter	

1.9 REGISTER::SLP_BACK_ST_port0_reg 0x9801_3220

Module::usb	Register::SLP_BACK0_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3220
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
test_fail_p0	1	R	‘b0	Self loop back fail	
test_done_p0	0	R	‘b0	Self loop back done	

Slef_loop_back procedure:

(1) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	F0	DBNC_E	DISCON_E	EN_ERR_UN	LATE_DL	INTG	SOP_KK	SLB_INNER	SLB_EN	

			N	NABLE	DERRUN	LEN					
			1	1	1	1	1	1	0: digital & analog 1: digital only	1	

(2) set test_psl, test_seed and test_speed
(3) set test_rst=1 & test_en=0 (reset)
(4) set test_rst=0 & test_en=0 (reset)
(5) set test_rst=0 & test_en=1 (enable)
(6) polling test_done
(7) check test_fail

Force MAC to enter High-Speed procedure:
(1) In simulation mode: force_hs_mode=1 & simulation_mode=1
(2) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
(3) In normal mode: force_hs_mode=0 & simulation_mode=0

1.10 REGISTER:: PHY2_SLB0_EN_reg 0x9801_3224

Module::usb	Register::PHY2_SLB_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3224
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
p0_usb2phy_slb_hs	1	R/W	'b0	Usbphy port0 self loop back hs mode	
p0_usb2phy_force_slb	0	R/W	'b0	Usbphy port0 self loop back start	

1.11 REGISTER:: PHY2_SLB0_ST_reg 0x9801_3228

Module::usb	Register::PHY2_SLB_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3228
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
p0_usb2phy_slb_fail	1	R	'b0	Usbphy port0 self loop back done	
p0_usb2phy_slb_done	0	R	'b0	Usbphy port0 self loop back fail	

1.12 REGISTER:: USB2_SPD_CTR 0x9801_322C

Module::usb	Register::USB2_SPD_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_322c
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
p0_suspend_r	0	R/W	'b0	-	

1.13 REGISTER:: USB3_ SLB_EN_reg 0x9801_3230

Module::usb	Register:: PHY3_SLB_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3230
Name	Bits	R/W	Default	Comments	
Rvd	31..3	-	-	-	
p0_pipe_bist_sel	2..1	R/W	‘b0	Self loop back select: 00:counter 01:tseq 10:ts1 11:ts2	
p0_pipe_bist_en	0	R/W	‘b0	Self loop back enable	

1.14 REGISTER:: PHY3_ SLB_CT_reg 0x9801_3234

Module::usb	Register::PHY3_SLB_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3234
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	-	
p0_usb3phy_slb_go	0	R/W	‘b0	Usb3phy port0 self loop back start transfer	

1.15 REGISTER:: PHY3_ SLB_ST_reg 0x9801_3238

Module::usb	Register::PHY3_SLB_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3238
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
p0_usb3phy_slb_fail	1	R	‘b0	Usb3phy port0 self loop back done	
p0_usb3phy_slb_done	0	R	‘b0	Usb3phy port0 self loop back enable	

1.16 REGISTER:: USB_DBG_reg 0x9801_3240

Module::usb	Register::USB_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3240
Name	Bits	R/W	Default	Comments	
Rvd	31..13	-	-	-	
dbg_sel1	12..7	R/W	‘b0	Select debug signal sets to be probed via usb_dbg_out1	
dbg_sel0	6..1	R/W	‘b0	Select debug signal sets to be probed via usb_dbg_out0	
dbg_en	0	R/W	‘b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both usb_dbg_out0 and usb_dbg_out1 are static 16’h0.	

1.17 REGISTER:: USB_STCH_reg 0x9801_3244

Module::usb	Register::USB_SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3244
Name	Bits	R/W	Default	Comments	
reg1	31..16	R/W	'hffff	Dummy register with value 1	
reg0	15..0	R/W	'd0	Dummy register with value 0	

1.18 REGISTER:: USB_TMP_SP_reg _0 0x9801_3248

Module::usb	Register::USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3248
Name	Bits	R/W	Default	Comments	
test_sp_reg_0	31..12	R/W	'd0	Dummy test register	
int_inact_status	11	R/W	'd0	ltssm change to ss inactive state	
int_ss_dis_status	10	R/W	'd0	ltssm change to ss disabled state	
int_hreset_status	9	R/W	'd0	ltssm change to hot reset state	
int_recov_status	8	R/W	'd0	ltssm change to recovery state	
int_rx_det_status	7	R/W	'd0	ltssm change to rx detect state	
int_poll_status	6	R/W	'd0	ltssm change to polling state	
int_u3_status	5	R/W	'd0	ltssm change to u3 state	
int_u2_status	4	R/W	'd0	ltssm change to u2 state	
int_u1_status	3	R/W	'd0	ltssm change to u1 state	
int_u0_status	2	R/W	'd0	ltssm change to u0 state	
int_loopbk_status	1	R/W	'd0	ltssm change to loopback state	
int_comp_status	0	R/W	'd0	ltssm change to compliance state	

1.19 REGISTER:: USB_TMP_SP_reg_1 0x9801_324C

Module::usb	Register::USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3248
Name	Bits	R/W	Default	Comments	
test_sp_reg_1	31..0	R/W	'd0	Dummy test register	

1.20 REGISTER:: USB_TMP_reg 0x9801_3250

Module::usb	Register::USB_TMP	Set::3	ATTR::ctrl	Type::SR	ADDR::0x9801_3250
Name	Bits	R/W	Default	Comments	
test_reg	31..0	R/W	'd0	Dummy test register	

1.21 REGISTER:: USB_TMP_reg_3 0x9801_325C

Module::usb	Register::USB_TMP	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3250
Name	Bits	R/W	Default	Comments	
test_reg_3	31..13	R/W	'd0	Dummy test register	
int_inact_en	12	R/W	'd0	ltssm change to ss inactive state interrupt enable	
int_ss_dis_en	11	R/W	'd0	ltssm change to ss disable state interrupt enable	
int_hreset_en	10	R/W	'd0	ltssm change to hot reset state interrupt enable	
int_recov_en	9	R/W	'd0	ltssm change to recovery state interrupt enable	
int_rx_det_en	8	R/W	'd0	ltssm change to rx detect state interrupt enable	
int_poll_en	7	R/W	'd0	ltssm change to polling state interrupt enable	
int_u3_en	6	R/W	'd0	ltssm change to u3 state interrupt enable	
int_u2_en	5	R/W	'd0	ltssm change to u2 state interrupt enable	
int_u1_en	4	R/W	'd0	ltssm change to u1 state interrupt enable	
int_u0_en	3	R/W	'd0	ltssm change to u0 state interrupt enable	
int_loopbk_en	2	R/W	'd0	ltssm change to loopback state interrupt enable	
int_comp_en	1	R/W	'd0	ltssm change to compliance state interrupt enable	
Rvd	0	-	-	-	

1.22 REGISTER:: USB_HMAC_CTR0_reg 0x9801_3260

Module::usb	Register::HMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3260
Name	Bits	R/W	Default	Comments	
Rvd	31	-	-	-	
host_ utmiotg_vbusvalid	30	R/W	'b1	-	
host_fladj_30mhz	29..24	R/W	'd32	-	
host_ppc_present	23	R/W	'b0	-	
host_msi_enable	22	R/W	'b0		
host_pm_pw_state_req	21..20	R/W	'b0		
hub_port_over_current	19..16	R/W	'b0		
Rvd	15..14	-	-	-	
hub_port_perm_attach	13..12	R/W	'b0		
Rvd	11..10	-	-		
host_u2_port_disable	9	R/W	'b0		
host_u3_port_disable	8	R/W	'b0		
host_num_u2_port	7..4	R/W	'd1		
host_num_u3_port	3..0	R/W	'd1		

1.23 REGISTER:: MAC3_HST_ST_reg 0x9801_3264

Module::usb	Register::MAC3_HST_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3264
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-	-	-	
host_current_power_state	3..2	R	‘b0	Current xHC power state	
host_hub_vbus_ctrl	1..0	R	‘b0	Vbus active indication	

1.24 REGISTER::DMAC_CTR0_reg 0x9801_3268

Module::usb	Register::DMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3268
Name	Bits	R/W	Default	Comments	
Rvd	31..27	-	-	-	
xhc_bme	26	R/W	‘b1		
dev_vbus_value	25	R/W	‘b0		
dev_utmiotg_vbusvalid	24	R/W	‘b0		
dev_pm_pw_state_req	23..22	R/W	‘b0		
dev_fladj_30mhz	21..16	R/W	‘d32		
dev_usb_outep_pkt_buff	15..0	R/W	‘hffff		

1.25 REGISTER:: MAC3_DEV_ST_reg 0x9801_326C

Module::usb	Register::MAC3_DEV_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_326c
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
dev_current_power_state	1..0	R	‘b0	Current xHC power state	

1.26 REGISTER:: USB2_PHY_reg 0x9801_3270

Module::usb	Register::USB2_PHY	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3270
Name	Bits	R/W	Default	Comments	
Rvd	31..12	-	-	-	
p0_by_pass_on_0	11	R/W	‘b0	isolation A→D	
p0_DmPulldown	10	R/W	‘b0	Device = 1’b0	
p0_DpPulldown	9	R/W	‘b0	Device = 1’b0	
p0_IDPULLUP	8	R/W	‘b0	Device = 1’b0	
Rvd	7..3	-	-	-	
p0_DmPulldown_sel	2	R/W	‘b0	p0_dmpulldown =~dev_mode ? 1’b1: p0_DmPulldown_sel ? p0_DmPulldown : 1’b0	
p0_DpPulldown_sel	1	R/W	‘b0	p0_dppulldown =~dev_mode ? 1’b1: p0_DpPulldown_sel ? p0_DpPulldown : 1’b0	
p0_IDPULLUP_sel	0	R/W	‘b0	p0_dmpulldown =~dev_mode ? 1’b1: p0_IDPULLUP_sel ? p0_IDPULLUP : 1’b0	

1.27 REGISTER:: USB_RAM_CTR_reg 0x9801_3274

Module::usb	Register::RAM_CTR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3274
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
done_st	16	R/W	'b0	Write 1 to clear	
Rvd	15..1	-	-	-	
go_ct	0	R/W	'b0	Start DMA transfer, clear after done	

1.28 REGISTER:: USB_RAM_ADDR_reg 0x9801_3278

Module::usb	Register::RAM_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3278
Name	Bits	R/W	Default	Comments	
sram_addr	31..0	R/W	'd0	SRAM address, 4-byte align. Bit[0]= use for write/read bit 0: read 1: write	

1.29 REGISTER:: USB_RAM_WDATA_reg 0x9801_327C

Module::usb	Register::RAM_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_327C
Name	Bits	R/W	Default	Comments	
ram_wdata	31..0	R/W	'd0	RAM write data to be write	

1.30 REGISTER:: USB3_RAM_RDATA_reg 0x9801_3280

Module::usb	Register::RAM_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3280
Name	Bits	R/W	Default	Comments	
ram_rdata	31..0	R/W	'd0	USB read data to be read back	

1.31 REGISTER:: USB3_PHY0_ST_reg 0x9801_3284

Module::usb	Register::PHY0_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3284
Name	Bits	R/W	Default	Comments	
Rvd	31..19	-	-	-	
p0_count_num	18..0	R	'b0	USB3 PHY count number value	

1.32 REGISTER:: USB3_OVR_CT_reg 0x9801_3288

Module::usb	Register::USB3_OVR_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3288
Name	Bits	R/W	Default	Comments	
Rvd	31..2	R/W	-	-	
phy3_lperiod	9..7	R/W	'd1	Connect to PHY3	
phy3_hperiod	6..4	R/W	'd3	Connect to PHY3	

phy3_last	3..2	R/W	‘d2	Connect to PHY3
host_ovr_current_value	1	R/W	‘b0	
host_ovr_current_sel	0	R/W	‘b0	

Host MAC register

1.33 REGISTER:: SOFT_Reset 0x9801_3300

Module::usb	Register::SOFT_RESET	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3300
Name	Bits	R/W	Default	Comments	
Rvd	31..3	-	-	-	
rstn_usb2_phy1	2	R/W	‘b0	USB2 PHY1 reset for USB2 IP	
rstn_usb2_phy0	1	R/W	‘b0	USB2 PHY0 reset for USB2 IP	
rstn_usb2	0	R/W	‘b0	USB2 IP system reset	

1.34 REGISTER:: GBL_USB_CT 0x9801_3304

Module::usb	Register::GBL_USB_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3304
Name	Bits	R/W	Default	Comments	
usb_mac_ctrl	31..0	R/W	‘d0	Register use for usb_mac_ctrl	

1.35 REGISTER:: GBL_USB_ARB 0x9801_3308

Module::usb	Register::GBL_USB_ARB	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3308
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-			
dbus_robin_enable	3	R/W	‘b0		
cmd_full_number	2..1	R/W	‘d3		
dbus_arb_priority	0	R/W	‘b0		

1.36 REGISTER:: UNUSED 0x9801_330C

1.37 REGISTER:: USB3_OTG_STS 0x9801_3310

Module::**usb**	Register::USB3_OTG_STS	Set::**1**	ATTR::nor e	Type::**SR**	ADDR::**0x9801_3310**
Name	**Bits**	**R/W**	**Default**	**Comments**	
Rvd	31..1	-	-	-	
otg_interrupt	0	R	‘b0	OTG interrupt from USB3 MAC	

1.38 REGISTER:: USB_BC_STS 0x9801_3314

Module::**usb**	Register::USB_BC_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3314**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..2	-	-	-
chirp_on	1	R	‘b0	battery charging chirp signal from USB3 MAC
bc_interrupt	0	R	‘b0	battery charging interrupt from USB3 MAC

1.39 REGISTER:: USB3_BIST1_CTRL 0x9801_3318

Module::**usb**	Register::USB3_BIST1_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_3318**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..28	-	-	-
usb3_bist1_ls[2:0]	27..25	R/W	3’h0	IP SRAM 0~2 LS value
usb3_bist1_rm_3	24..21	R/W	4’h0	SRAM3 RM value
usb3_bist1_rme_3	20	R/W	‘b0	SRAM3 RM enable
usb3_bist1_rm_2	19..16	R/W	4’h0	SRAM2 RM value
usb3_bist1_rme_2	15	R/W	‘b0	SRAM2 RM enable
usb3_bist1_rm_1	14..11	R/W	4’h0	SRAM1 RM value
usb3_bist1_rme_1	10	R/W	‘b0	SRAM1 RM enable
usb3_bist1_rm_0	9..6	R/W	4’h0	SRAM0 RM value
usb3_bist1_rme_0	5	R/W	‘b0	SRAM0 RM enable
usb3_drf_1_test_resume	4	W/R	‘b0	USB3 DRF BIST1 trigger resume signal
usb3_drf_bist1_en	3	W/R	‘b0	USB3 DRF BIST1 enable
usb3_bist1_en	2	W/R	‘b0	USB3 BIST1 enable
Rvd	1	-	-	-
usb3_bist1_test_mode	0	W/R	‘b0	USB3 BIST1 test mode enable

1.40 REGISTER:: USB3_BIST2_CTRL 0x9801_331c

Module::**usb**	Register::USB3_BIST2_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_331c**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..17	-	-	-
usb3_bist2_ls[1:0]	16..15	R/W	2’h0	Pp SRAM LS value
usb3_bist2_rm_1	14..11	R/W	4’h0	SRAM5 RM value
usb3_bist2_rme_1	10	R/W	‘b0	SRAM5 RM enable
usb3_bist2_rm_0	9..6	R/W	4’h0	SRAM4 RM value
usb3_bist2_rme_0	5	R/W	‘b0	SRAM4 RM enable
usb3_drf_2_test_resume	4	W/R	‘b0	USB3 DRF BIST2 trigger resume signal
usb3_drf_bist2_en	3	W/R	‘b0	USB3 DRF BIST2 enable
usb3_bist2_en	2	W/R	‘b0	USB3 BIST2 enable
Rvd	1	-	-	-
usb3_bist2_test_mode	0	W/R	‘b0	USB3 BIST2 test mode enable

1.41 REGISTER:: USB3_BIST1_STS 0x9801_3320

Module::**usb**	Register::USB3_BIST1_STS		Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3320**
Name	**Bits**	**R/W**	**Default**	**Comments**		
Rvd	31..11	-	-	-		
usb3_drf_bist1_fail_3	10	R	'b0	USB3 DRF1 SRAM3 fail signal		
usb3_bist1_fail_3	9	R	'b0	USB3 BIST1 SRAM3 fail signal		
usb3_drf_bist1_fail_2	8	R	'b0	USB3 DRF1 SRAM2 fail signal		
usb3_bist1_fail_2	7	R	'b0	USB3 BIST1 SRAM2 fail signal		
usb3_drf_bist1_fail_1	6	R	'b0	USB3 DRF1 SRAM1 fail signal		
usb3_bist1_fail_1	5	R	'b0	USB3 BIST1 SRAM1 fail signal		
usb3_drf_bist1_fail_0	4	R	'b0	USB3 DRF1 SRAM0 fail signal		
usb3_bist1_fail_0	3	R	'b0	USB3 BIST1 SRAM0 fail signal		
usb3_drf_1_start_pause	2	R	'b0	USB3 DRF1 start pause signal		
usb3_drf_bist1_done	1	R	'b0	USB3 DRF1 done		
usb3_bist1_done	0	R	'b0	USB3 BIST1 done		

1.42 REGISTER:: USB3_BIST2_STS 0x9801_3324

Module::**usb**	Register::USB3_BIST2_STS		Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3324**
Name	**Bits**	**R/W**	**Default**	**Comments**		
Rvd	31..7	-	-	-		
usb3_drf_bist2_fail_1	6	R	'b0	USB3 DRF2 SRAM5 fail signal		
usb3_bist2_fail_1	5	R	'b0	USB3 BIST2 SRAM5 fail signal		
usb3_drf_bist2_fail_0	4	R	'b0	USB3 DRF2 SRAM4 fail signal		
usb3_bist2_fail_0	3	R	'b0	USB3 BIST2 SRAM4 fail signal		
usb3_drf_2_start_pause	2	R	'b0	USB3 DRF2 start pause signal		
usb3_drf_bist2_done	1	R	'b0	USB3 DRF2 done		
usb3_bist2_done	0	R	'b0	USB3 BIST2 done		

1.43 REGISTER:: USB3_APHY_REG 0x9801_3328

Module::usb	Register::USB3_APHY_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3328
Name	Bits	R/W	Default	Comments	
Rvd	31..5	-	-	-	
usb3_clk_mode_sel	4..3	R/W	'b00	"11" : Diff. 100MHz in, else CKIN_XTAL in. IN RL6227 .CKREF comes from CKIN_XTAL, tie "00".	
usb3_ckbuf_en	2	R/W	'b0	CKREF Buffer Enable tie 0	
usb3_mbias_en	1	R/W	'b1	Bias Circuit Enable. 1: Bias Circuit enable 0: Bias Circuit disable	
usb3_bg_en	0	R/W	'b0	Bandgap Enable. IN RL6227,no BG inside the USB3.0 block, tie 0	

1.44 REGISTER:: USB3_BC_STS2_REG 0x9801_332C

Module::usb	Register::USB3_BC_STS2_REG	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_332c

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
hst_prtbl_det_0_usb3	7	R	‘b0	
hst_comp_out_0_usb3	6	R	‘b0	Debug signal
hst_sh_out_0_usb3	5	R	‘b0	Debug signal
hst_v0p07_out_0_usb3	4	R	‘b0	DP>0.35V, output=low, DP<0.35V, output=high
hst_v0p41_out_0_usb3	3	R	‘b0	DM>THD, output=low, DM<THD, output=high
hst_v0p46_out_0_usb3	2	R	‘b1	don't care. Output=high.
dev_chg_det_0_usb3	1	R	‘b0	Detector result
dev_dcp_det_0_usb3	0	R	‘b0	Detector result

1.45 REGISTER:: USB3_BC_CTL_REG 0x9801_3330

Module::usb	Register::USB3_BC_CTL_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3330

Name	Bits	R/W	Default	Comments
Rvd	31..15	-	-	-
LF_PD_R_en	14	R/W	‘b1	
hst_pow_charge_0_usb3	13	R/W	‘b0	Enable charge, high enable
hst_vdm_src_en_0_usb3	12	R/W	‘b0	Enable VDM_SRC output, high enable
hst_idp_sink_en_0_usb3	11	R/W	‘b0	Enable DP current sink, high enable
hst_app_div_en_0_usb3	10	R/W	‘b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	‘b0	Select Apple charge current 2.1A/1A 0: DP=2.0V, DM=2.7V 1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_usb3	8	R/W	‘b0	Enable comparator for detect Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	‘b0	Enable NOTE mode, high enable, DP=1.25V
hst_dcp_en_0_usb3	6	R/W	‘b0	Enable DCP mode, high enable, short DP and DM.
dev_pow_charge_0_usb3	5	R/W	‘b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb3	4	R/W	‘b0	0: select CHG_DET detect 1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	‘b0	Enable DP output voltage, high enable
dev_vdm_src_en_0_usb3	2	R/W	‘b0	Enable DM output voltage, high enable
dev_idp_sink_en_0_usb3	1	R/W	‘b0	Enable DP current sink, high enable
dev_idm_sink_en_0_usb3	0	R/W	‘b0	Enable DM current sink, high enable

1.46 REGISTER:: USB3_DUMMY_0_REG 0x9801_3334

Module::usb	Register::USB3_DUMMY_0_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3334

Name	Bits	R/W	Default	Comments
dummy_0	31..0	R/W	32’h0	Dummy register,default:0

1.47 REGISTER:: USB3_DUMMY_1_REG 0x9801_3338

Module::usb	Register::USB3_DUMMY_1_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3338

Name	Bits	R/W	Default	Comments
dummy_1	31..0	R/W	32'hFFFF_FFFF	Dummy register,default:1

1.48 REGISTER:: USB3_LTSSM_STS 0x9801_333C

Module::usb	Register::USB3_LTSSM_STS	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_333c

Name	Bits	R/W	Default	Comments
Rvd	31..4	-	-	-
Ltdb_sub_state	3..0	R	'b0	Ltssm sub-state from USB3 IP

1.49 REGISTER:: USB_PHY_CTRL 0x9801_3340

Module::usb	Register::USB_PHY_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3340

Name	Bits	R/W	Default	Comments
Rvd	31..6	-	-	-
usb_ldo_en	5..2	R/W	'b0	U2phy0~U2phy3 ldo enable
usb3_isolate_mac2phy	1..0	R/W	'b0	isolate UPHY A→D

1.50 REGISTER:: USB_PWR_CTRL 0x9801_3344

Module::usb	Register::USB_PWR_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3344

Name	Bits	R/W	Default	Comments
u3_det_time_val	31..16	R/W	'hfa	u3_det_time_val
u2_det_time_val	15..9	R/W	'h3	u2_det_time_val
u3_ip_clk_en	8..7	R/W	'h3	u3_ip_clk_en
u3_ip_rstn	6..5	R/W	'h3	u3_ip_rstn
mac_phy_pll_en	4..3	R/W	'h3	mac_phy_pll_en
u2_det_debounce_en	2	R/W	'b0	u2_det_debounce_en
recv_det_start_hst	1	R/W	'b0	recv_det_start_hst
recv_det_start_drd	0	R/W	'b0	recv_det_start_drd

1.51 REGISTER:: USB_PWR_STS 0x9801_3348

Module::usb	Register::USB_PWR_STS	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3348

Name	Bits	R/W	Default	Comments
usb_pwr_ctrl_en	31	R/W	'h0	usb_pwr_ctrl_en
sw_reset_pwr_fsm	30..29	R/W	'h0	sw_reset_pwr_fsm
rxterm_dly_en	28	R/W	'b1	rxterm_dly_en
Rvd	27..10	-	-	-
recv_det_int_en_hst	9	R/W	'b0	recv_det_int_en_hst
recv_det_int_en_drd	8	R/W	'b0	recv_det_int_en_drd
Rvd	7..2	-	-	-
recv_det_int_sts_hst	1	R/W	'b0	recv_det_int_sts_hst
recv_det_int_sts_drd	0	R/W	'b0	recv_det_int_sts_drd

1.52 REGISTER:: USB_TYPEC_CTRL_CC1_0 0x9801_334C

Module::usb	Register::USB_TYPEC_CTRL_CC1_0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_334C

Name	Bits	R/W	Default	Comments
Rvd	31..30	-	-	-
EN_SWITCH	29	R/W	‘h0	En switch
Txout_sel	28	R/W	‘h0	Txout_sel
Rxin_sel	27	R/W	‘h0	Rxin_sel
Reg_cc1_rp4pk_code	26..22	R/W	‘h0	Reg_cc1_rp4pk_code
Reg_cc1_rp36k_code	21..17	R/W	‘h0	Reg_cc1_rp36k_code
Reg_cc1_rp12k_code	16..12	R/W	‘h0	Reg_cc1_rp12k_code
Reg_cc1_rd_code	11..7	R/W	‘h0	Reg_cc1_rd_code
Reg_cc1_mode	6..5	R/W	‘h0	Reg_cc1_mode
En_cc1_rp4p7k	4	R/W	‘h0	En_cc1_rp4p7k
En_cc1_rp36k	3	R/W	‘h0	En_cc1_rp36k
En_cc1_rp12k	2	R/W	‘h0	En_cc1_rp12k
En_cc1_rd	1	R/W	‘h0	En_cc1_rd
En_cc1_det	0	R/W	‘h0	En_cc1_det

1.53 REGISTER:: USB_TYPEC_CTRL_CC1_1 0x9801_3350

Module::usb	Register::USB_TYPEC_CTRL_CC1_1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3350

Name	Bits	R/W	Default	Comments
Rvd	31..29	-	-	-
Reg_cc1_ vref_2p6v	28..26	R/W	‘h0	Reg_cc1_ vref_2p6v
Reg_cc1_ vref_1p23v	25.22	R/W	‘h0	Reg_cc1_ vref_1p23v
Reg_cc1_ vref_0p8v	21..18	R/W	‘h0	Reg_cc1_ vref_0p8v
Reg_cc1_ vref_0p66v	17..14	R/W	‘h0	Reg_cc1_ vref_0p66v
Reg_cc1_ vref_0p4v	13.11	R/W	‘h0	Reg_cc1_ vref_0p4v
Reg_cc1_vref_0p2v	10..8	R/W	‘h0	Reg_cc1_vref_0p2v
Reg_cc1_ vref1_1p6v	7..4	R/W	‘h0	Reg_cc1_ vref1_1p6v
Reg_cc1_vref0_1p6v	3..0	R/W	‘h0	Reg_cc1_vref0_1p6v

1.54 REGISTER:: USB_TYPEC_CTRL_CC2_0 0x9801_3354

Module::usb	Register::USB_TYPEC_CTRL_CC2_0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3354

Name	Bits	R/W	Default	Comments
Rvd	31..27	-	-	-
Reg_CC2_rp4pk_code	26..22	R/W	‘h0	Reg_CC2_rp4pk_code
Reg_CC2_rp36k_code	21..17	R/W	‘h0	Reg_CC2_rp36k_code
Reg_CC2_rp12k_code	16..12	R/W	‘h0	Reg_CC2_rp12k_code
Reg_CC2_rd_code	11..7	R/W	‘h0	Reg_CC2_rd_code
Reg_CC2_mode	6..5	R/W	‘h0	Reg_CC2_mode
En_CC2_rp4p7k	4	R/W	‘h0	En_CC2_rp4p7k
En_CC2_rp36k	3	R/W	‘h0	En_CC2_rp36k
En_CC2_rp12k	2	R/W	‘h0	En_CC2_rp12k
En_CC2_rd	1	R/W	‘h0	En_CC2_rd

En_CC2_det	0	R/W	'h0	En_CC2_det

1.55 REGISTER:: USB_TYPEC_CTRL_CC2_1 0x9801_3358

Module::usb	Register::USB_TYPEC_CTRL_CC2_1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3358

Name	Bits	R/W	Default	Comments
Rvd	31..29	-	-	-
Reg_CC2_ vref_2p6v	28..26	R/W	'h0	Reg_CC2_ vref_2p6v
Reg_CC2_ vref_1p23v	25.22	R/W	'h0	Reg_CC2_ vref_1p23v
Reg_CC2_ vref_0p8v	21..18	R/W	'h0	Reg_CC2_ vref_0p8v
Reg_CC2_ vref_0p66v	17..14	R/W	'h0	Reg_CC2_ vref_0p66v
Reg_CC2_ vref_0p4v	13.11	R/W	'h0	Reg_CC2_ vref_0p4v
Reg_CC2_vref_0p2v	10..8	R/W	'h0	Reg_CC2_vref_0p2v
Reg_CC2_ vref1_1p6v	7..4	R/W	'h0	Reg_CC2_ vref1_1p6v
Reg_CC2_vref0_1p6v	3..0	R/W	'h0	Reg_CC2_vref0_1p6v

1.56 REGISTER:: USB_TYPEC_STS 0x9801_335C

Module::usb	Register::USB_TYPEC_STS	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_335C

Name	Bits	R/W	Default	Comments
Rvd	31..6	-	-	-
cc2_det	5..3	RO	'h7	CC2_det
cc1_det	2..0	RO	'h7	CC1_det

1.57 REGISTER:: USB_TYPEC_CTRL 0x9801_3360

Module::usb	Register::USB_TYPEC_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3360

Name	Bits	R/W	Default	Comments
Rvd	31..12	-	-	-
cc2_det_int_en	11	R/W	'h0	cc2 det interrupt en
cc1_det_int_en	10	R/W	'h0	cc1 det interrupt en
cc2_det_int	9	R/W	'h0	cc2 det interrupt sts
cc1_det_int	8	R/W	'h0	cc1 det interrupt sts
cc_detect_time_value	7..1	R/W	'h3	debounce time scale
cc_det_debounce_en	0	R/W	'h1	cc detect debounce en

1.58 REGISTER:: USB_DBUS_PWR_CTRL 0x9801_3364

Module::usb	Register::USB_DBUS_PWR_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3364

Name	Bits	R/W	Default	Comments
Rvd	31..12	-	-	-
clk_en_gap	11..10	R/W	'h0	00:50ns 01:300ns 10:500ns 11:1us

sram_ls_gap	9..8	R/W	'h0	00:200ns 01:300ns 10:100ns 11:500ns
Rvd	7..2	-	-	-
dbus_pwr_ctrl_sw_rst	1	R/W	'h0	dbus power ctrl software reset to idle
dbus_pwr_ctrl_en	0	R/W	'h0	dbus power ctrl enable

1.59 REGISTER:: USB3_HOST_WRAP_CTR_reg 0x9801_3C00

Module::usb	Register:: USB3_HOST_WRAP_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C00

Name	Bits	R/W	Default	Comments
Rvd	31..7	-	-	-
rxdetect_value	6	R/W	'b0	
rxdetect_sel	5	R/W	'b0	
resume_cycle_sel	4	R/W	'b0	
sram_debug_sel	3	R/W	'b0	Select sram 1: host 0: device
sram_debug_mode	2	R/W	'b0	Enable sram debug mode
dbus_multi_req_disable	1	R/W	'b0	Disable multiple request for Dbus 0: enable multiple request 1: disable multiple request
dev_mode	0	R/W	'b0	Enable peek on AHB burst length 0: host (2) 1: host/dev

1.60 REGISTER:: USB3_HOST_GNT_INT_reg 0x9801_3C04

Module::usb	Register::USB3_HOST_GNR_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C04

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
device_int	1	R	'b0	USB3 Device MAC interrupt
host_int	0	R	'b0	USB3 Host MAC interrupt

1.61 REGISTER:: USB3_HOST_USB2_PHY_UTMI 0x9801_3C08

Module::usb	Register:: USB3_HOST_USB2_PHY_UTMI	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C08

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-

reset_utmi_p0	0	R/W	'b0	UTMI reset to PHY0 (sync and automatically return to low)

1.62 REGISTER:: USB3_HOST_VSTATUS_port0_reg 0x9801_3C14

Module::usb	Register:: USB3_HOST_VSTATUS0_OUT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C14

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
p0_vstatus_out	7..0	R/W	'h00	Vstatus output for port0 (It's used to configure PHY's control register)

The process of configuring PHY control register:

3. write VSTATUS_reg (0x9801_3C14), (data output to PHY)
4. write GUSB2PHYAccn (p0:0x9803_1280)
   [25]: vload
   [23]: vBusy
   [11:8]: vcontrol
   [7:0]: vstatus_in (data input from PHY)

Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'b0	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. **Note:** This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. **Note:** These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) ■ UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ■ ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) ■ UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ■ ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.63 REGISTER:: USB3_HOST_SLP_BACK_EN_port0_reg 0x9801_3C18

Module::usb	Register::USB3_HOST_SL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C18

	P_BACK0_EN				
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-	-	-	
simulation_mode_p0	3	R/W	‘b0	Port0 Reduce counter for entering HS	
force_hs_mode_p0	2	R/W	‘b0	Port0 Force HOST IP enter high speed mode 0: disable 1: enable	
test_rst_p0	1	R/W	‘b0	Port0 Self loop back reset	
test_en_p0	0	R/W	‘b0	Port0 Self loop back enable	

1.64 REGISTER:: USB3_HOST_SLP_BACK_CTR_port0_reg 0x9801_3C1c

Module::usb	Register:: USB3_HOST_SLP_BACK0_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C1c
Name	Bits	R/W	Default	Comments	
Rvd	31..12	-	-	-	
test_speed_p0	11..10	R/W	‘h0	When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2’b01: force PHY in HS 2’b10: force PHY in FS/LS 2’b00/2’b11: normal mode	
test_seed_p0	9..2	R/W	‘h0	Self_loop_back Random generator seed	
test_psl_p0	1..0	R/W	‘h0	Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter	

1.65 REGISTER:: USB3_HOST_SLP_BACK_ST_port0_reg 0x9801_3C20

Module::usb	Register:: USB3_HOST_SLP_BACK0_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C20
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	

test_fail_p0	1	R	'b0	Port0 Self loop back fail
test_done_p0	0	R	'b0	Port0 Self loop back done

Slef_loop_back procedure:

(8) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	F0	DBNC_EN	DISCON_ENABLE	EN_ERR_UNDERRUN	LATE_DL LEN	INTG	SOP_KK	SLB_INNER	SLB_EN	
			1	1	1	1	1	1	0: digital & analog 1: digital only	1	

(9) set test_psl, test_seed and test_speed
(10) set test_rst=1 & test_en=0 (reset)
(11) set test_rst=0 & test_en=0 (reset)
(12) set test_rst=0 & test_en=1 (enable)
(13) polling test_done
(14) check test_fail

Force MAC to enter High-Speed procedure:

(4) In simulation mode: force_hs_mode=1 & simulation_mode=1
(5) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
(6) In normal mode: force_hs_mode=0 & simulation_mode=0

1.66 REGISTER:: USB3_HOST_PHY2_SLB0_EN_reg 0x9801_3C24

Module::usb	Register:: USB3_HOST_PHY2_SLB_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C24

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_usb2phy_slb_hs	1	R/W	'b0	Usbphy port0 self loop back hs mode
p0_usb2phy_force_slb	0	R/W	'b0	Usbphy port0 self loop back start

1.67 REGISTER:: USB3_HOST_PHY2_SLB0_ST_reg 0x9801_3C28

Module::usb	Register:: USB3_HOST_PHY2_SLB_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C28

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_usb2phy_slb_fail	1	R	‘b0	Usbphy port0 self loop back done
p0_usb2phy_slb_done	0	R	‘b0	Usbphy port0 self loop back fail

1.68 REGISTER:: USB3_HOST_USB2_SPD_CTR 0x9801_3C2C

Module::usb	Register:: USB3_HOST_USB2_SPD_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C2c

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_suspend_r	0	R/W	’b0	-

1.69 REGISTER:: USB3_HOST_USB_DBG_reg 0x9801_3C40

Module::usb	Register:: USB3_HOST_USB_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C40

Name	Bits	R/W	Default	Comments
Rvd	31..13	-	-	-
dbg_sel1	12..7	R/W	‘b0	Select debug signal sets to be probed via usb_dbg_out1
dbg_sel0	6..1	R/W	‘b0	Select debug signal sets to be probed via usb_dbg_out0
dbg_en	0	R/W	‘b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both usb_dbg_out0 and usb_dbg_out1 are static 16’h0.

1.70 REGISTER:: USB3_HOST_USB_STCH_reg 0x9801_3C44

Module::usb	Register:: USB3_HOST_USB_SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C44

Name	Bits	R/W	Default	Comments
reg1	31..16	R/W	‘hffff	Dummy register with value 1
reg0	15..0	R/W	‘d0	Dummy register with value 0

1.71 REGISTER:: USB3_HOST_USB_TMP_SP_reg _0 0x9801_3C48

Module::usb	Register:: USB3_HOST_USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C48
Name	Bits	R/W	Default	Comments	
test_sp_reg_0	31..0	R/W	‘d0	Dummy test register	

1.72 REGISTER:: USB3_HOST_USB_TMP_SP_reg_1 0x9801_3C4C

Module::usb	Register:: USB3_HOST_USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C48
Name	Bits	R/W	Default	Comments	
test_sp_reg_1	31..0	R/W	‘d0	Dummy test register	

1.73 REGISTER:: USB3_HOST_USB_TMP_reg _2 0x9801_3C50

Module::usb	Register:: USB3_HOST_USB_TMP	Set::3	ATTR::ctrl	Type::SR	ADDR::0x9801_3850
Name	Bits	R/W	Default	Comments	
test_reg_2	31..0	R/W	‘d0	Dummy test register	

1.74 REGISTER:: USB3_HOST_USB_TMP_reg_3 0x9801_3C5C

Module::usb	Register:: USB3_HOST_USB_TMP	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C5C
Name	Bits	R/W	Default	Comments	
test_reg_3	31..0	R/W	‘d0	Dummy test register	

1.75 REGISTER:: USB3_HOST_USB_HMAC_CTR0_reg 0x9801_3C60

Module::usb	Register:: USB3_HOST_HMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C60
Name	Bits	R/W	Default	Comments	
Rvd	31..30	-	-	-	
host_fladj_30mhz	29..24	R/W	‘d32	-	
host_ppc_present	23	R/W	‘b0	-	
host_msi_enable	22	R/W	‘b0		
host_pm_pw_state_req	21..20	R/W	‘b0		
hub_port_over_current	19..16	R/W	‘b0		

hub_port_perm_attach	15..12	R/W	‘b0	
host_u2_port_disable	11..9	R/W	‘b0	
host_u3_port_disable	8	R/W	‘b0	
host_num_u2_port	7..4	R/W	‘d1	
host_num_u3_port	3..0	R/W	‘d0	

1.76 REGISTER:: USB3_HOST_MAC3_HST_ST_reg 0x9801_3C64

Module::usb	Register:: USB3_HOST_MAC3_HST_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C64

Name	Bits	R/W	Default	Comments
Rvd	31..6	-	-	-
host_current_power_state	5..4	R	‘b0	Current xHC power state
host_hub_vbus_ctrl	3..0	R	‘b0	Vbus active indication

1.77 REGISTER:: USB3_HOST_DMAC_CTR0_reg 0x9801_3C68

Module::usb	Register:: USB3_HOST_DMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C68

Name	Bits	R/W	Default	Comments
Rvd	31..27	-	-	-
host_xhc_bme	26	R/W	‘b1	
Rvd	25..3	-	-	-
host_utmiotg_vbusvalid	2..0	R/W	‘h7	

1.78 REGISTER:: USB3_HOST_MAC3_DEV_ST_reg 0x9801_3C6C

Module::usb	Register:: USB3_HOST_MAC3_DEV_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C6c

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
dev_current_power_state	1..0	R	‘b0	Current xHC power state

1.79 REGISTER:: USB3_HOST_USB2_PHY_reg 0x9801_3C70

Module::usb	Register:: USB3_HOST_USB2_PHY	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C70

Name	Bits	R/W	Default	Comments

Rvd	31..13	-	-	-
phy_pll_en	12	R/W	‘b1	1:phy pll always on(for CR 480MHz)
p0_by_pass_on_1	11	R/W	‘b0	Isolation A→D
p0_DmPulldown	10	R/W	‘b0	Device = 1’b0
p0_DpPulldown	9	R/W	‘b0	Device = 1’b0
p0_IDPULLUP	8	R/W	‘b0	Device = 1’b0
Rvd	7..3	-	-	-
p0_DmPulldown_sel	2	R/W	‘b0	p0_DmPulldown_sel ? p0_DmPulldown : 1’b0
p0_DpPulldown_sel	1	R/W	‘b0	p0_DpPulldown_sel ? p0_DpPulldown : 1’b0
p0_IDPULLUP_sel	0	R/W	‘b0	p0_IDPULLUP_sel ? p0_IDPULLUP : 1’b0

1.80 REGISTER:: USB3_HOST_USB_RAM_CTR_reg 0x9801_3C74

Module::usb	Register:: USB3_HOST_RAM_CTR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3C74

Name	Bits	R/W	Default	Comments
Rvd	31..17	-	-	-
done_st	16	R/W	‘b0	Write 1 to clear
Rvd	15..1	-	-	-
go_ct	0	R/W	‘b0	Start DMA transfer, clear after done

1.81 REGISTER:: USB3_HOST_USB_RAM_ADDR_reg 0x9801_3C78

Module::usb	Register:: USB3_HOST_RAM_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C78

Name	Bits	R/W	Default	Comments
sram_addr	31..0	R/W	‘d0	SRAM address, 4-byte align. Bit[0]= use for write/read bit 0: read 1: write

1.82 REGISTER:: USB3_HOST_USB_RAM_WDATA_reg 0x9801_3C87C

Module::usb	Register:: USB3_HOST_RAM_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C87C

Name	Bits	R/W	Default	Comments
ram_wdata	31..0	R/W	‘d0	RAM write data to be write

1.83 REGISTER:: USB3_HOST_RAM_RDATA_reg 0x9801_3C80

Module::usb	Register:: USB3_HOST_RAM_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3C80

Name	Bits	R/W	Default	Comments
ram_rdata	31..0	R/W	'd0	USB read data to be read back

1.84 REGISTER:: USB3_HOST_PHY0_ST_reg 0x9801_3C84

Module::usb	Register:: USB3_HOST_PHY0_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C84

Name	Bits	R/W	Default	Comments
Rvd	31..19	-	-	-
p0_count_num	18..0	R	'b0	USB3 PHY count number value

1.85 REGISTER:: USB3_HOST_OVR_CT_reg 0x9801_3C88

Module::usb	Register::USB3_HOST_OVR_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C88

Name	Bits	R/W	Default	Comments
Rvd	31..2	R/W	-	-
phy3_lperiod	9..7	R/W	'd1	Connect to PHY3
phy3_hperiod	6..4	R/W	'd3	Connect to PHY3
phy3_last	3..2	R/W	'd2	Connect to PHY3
host_ovr_current_value	1	R/W	'b0	
host_ovr_current_sel	0	R/W	'b0	

1.86 REGISTER:: USB3_HOST_SOFT_Reset 0x9801_3D00

Module::usb	Register:: USB3_HOST_SOFT_RESET	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D00

Name	Bits	R/W	Default	Comments
Rvd	31..3	-	-	-
rstn_usb2_phy1	2	R/W	'b0	USB2 PHY1 reset for USB2 IP
rstn_usb2_phy0	1	R/W	'b0	USB2 PHY0 reset for USB2 IP
rstn_usb2	0	R/W	'b0	USB2 IP system reset

1.87 REGISTER:: USB3_HOST_GBL_USB_CT 0x9801_3D04

Module::usb	Register::	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D04

	USB3_HOST_GBL_USB_CT				
Name	Bits	R/W	Default	Comments	
usb_mac_ctrl	31..0	R/W	‘d0	Register use for usb_mac_ctrl	

1.88 REGISTER:: USB3_HOST_GBL_USB_ARB 0x9801_3D08

Module::usb	Register:: USB3_HOST_GBL_USB_ARB	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D08
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-			
dbus_robin_enable	3	R/W	‘b0		
cmd_full_number	2..1	R/W	‘d3		
dbus_arb_priority	0	R/W	‘b0		

1.89 REGISTER:: UNUSED 0x9801_3D0C

1.90 REGISTER:: USB3_HOST_OTG_STS 0x9801_3D10

Module::**usb**	Register::USB3_HOST_OTG_STS	Set::**1**	ATTR::none	Type::**SR**	ADDR::**0x9801_3D10**
Name	**Bits**	**R/W**	**Default**	**Comments**	
Rvd	31..1	-	-	-	
otg_interrupt	0	R	‘b0	OTG interrupt from USB3 MAC	

1.91 REGISTER:: USB3_HOST_USB_BC_STS 0x9801_3D14

Module::**usb**	Register:: USB3_HOST_USB_BC_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3D14**
Name	**Bits**	**R/W**	**Default**	**Comments**	
Rvd	31..2	-	-	-	
chirp_on	1	R	‘b0	battery charging chirp signal from USB3 MAC	
bc_interrupt	0	R	‘b0	battery charging interrupt from USB3 MAC	

1.92 REGISTER:: USB3_HOST_BIST1_CTRL 0x9801_3D18 (IP sram)

Module::**usb**	Register::USB3_HOST_BIST1_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_3D18**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..28	-	-	-
usb3_bist1_ls[2:0]	27..25	R/W	3'h0	SRAM0~2 LS value
usb3_bist1_rm_3	24..21	R/W	4'h0	SRAM3 RM value
usb3_bist1_rme_3	20	R/W	'b0	SRAM3 RM enable
usb3_bist1_rm_2	19..16	R/W	4'h0	SRAM2 RM value
usb3_bist1_rme_2	15	R/W	'b0	SRAM2 RM enable
usb3_bist1_rm_1	14..11	R/W	4'h0	SRAM1 RM value
usb3_bist1_rme_1	10	R/W	'b0	SRAM1 RM enable
usb3_bist1_rm_0	9..6	R/W	4'h0	SRAM0 RM value
usb3_bist1_rme_0	5	R/W	'b0	SRAM0 RM enable
usb3_drf_1_test_resume	4	W/R	'b0	USB3 DRF BIST1 trigger resume signal
usb3_drf_bist1_en	3	W/R	'b0	USB3 DRF BIST1 enable
usb3_bist1_en	2	W/R	'b0	USB3 BIST1 enable
Rvd	1	-	-	-
usb3_bist1_test_mode	0	W/R	'b0	USB3 BIST1 test mode enable

1.93 REGISTER:: USB3_HOST_BIST2_CTRL 0x9801_3D1c (PPsram)

Module::**usb**	Register::USB3_HOST_BIST2_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_3D1c**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..17	-	-	-
usb3_bist2_ls[1:0]	16..15	R/W	2'h0	SRAM4~5 LS value
usb3_bist2_rm_1	14..11	R/W	4'h0	SRAM5 RM value
usb3_bist2_rme_1	10	R/W	'b0	SRAM5 RM enable
usb3_bist2_rm_0	9..6	R/W	4'h0	SRAM4 RM value
usb3_bist2_rme_0	5	R/W	'b0	SRAM4 RM enable
usb3_drf_2_test_resume	4	W/R	'b0	USB3 DRF BIST2 trigger resume signal
usb3_drf_bist2_en	3	W/R	'b0	USB3 DRF BIST2 enable
usb3_bist2_en	2	W/R	'b0	USB3 BIST2 enable
Rvd	1	-	-	-
usb3_bist2_test_mode	0	W/R	'b0	USB3 BIST2 test mode enable

1.94 REGISTER:: USB3_HOST_BIST1_STS 0x9801_3D20

Module::**usb**	Register::USB3_HOST_BIST1_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3D20**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..11	-	-	-
usb3_drf_bist1_fail_3	10	R	'b0	USB3 DRF1 SRAM3 fail signal
usb3_bist1_fail_3	9	R	'b0	USB3 BIST1 SRAM3 fail signal

usb3_drf_bist1_fail_2	8	R	‘b0	USB3 DRF1 SRAM2 fail signal
usb3_bist1_fail_2	7	R	‘b0	USB3 BIST1 SRAM2 fail signal
usb3_drf_bist1_fail_1	6	R	‘b0	USB3 DRF1 SRAM1 fail signal
usb3_bist1_fail_1	5	R	‘b0	USB3 BIST1 SRAM1 fail signal
usb3_drf_bist1_fail_0	4	R	‘b0	USB3 DRF1 SRAM0 fail signal
usb3_bist1_fail_0	3	R	‘b0	USB3 BIST1 SRAM0 fail signal
usb3_drf_1_start_pause	2	R	‘b0	USB3 DRF1 start pause signal
usb3_drf_bist1_done	1	R	‘b0	USB3 DRF1 done
usb3_bist1_done	0	R	‘b0	USB3 BIST1 done

1.95 REGISTER:: USB3_HOST_BIST2_STS 0x9801_3D24

Module::**usb**	Register::USB3_HOST_BIST2_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::0x**9801_3D24**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..7	-	-	-
usb3_drf_bist2_fail_1	6	R	‘b0	USB3 DRF2 SRAM5 fail signal
usb3_bist2_fail_1	5	R	‘b0	USB3 BIST2 SRAM5 fail signal
usb3_drf_bist2_fail_0	4	R	‘b0	USB3 DRF2 SRAM4 fail signal
usb3_bist2_fail_0	3	R	‘b0	USB3 BIST2 SRAM4 fail signal
usb3_drf_2_start_pause	2	R	‘b0	USB3 DRF2 start pause signal
usb3_drf_bist2_done	1	R	‘b0	USB3 DRF2 done
usb3_bist2_done	0	R	‘b0	USB3 BIST2 done

1.96 USB3_HOST_BC_STS2_REG 0x9801_3D2C

Module::usb	Register::USB3_HOST_BC_STS2_REG	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3D2C

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
hst_prtbl_det_0_usb3	7	R	‘b0	
hst_comp_out_0_usb3	6	R	‘b0	Debug signal
hst_sh_out_0_usb3	5	R	‘b0	Debug signal
hst_v0p07_out_0_usb3	4	R	‘b0	DP>0.35V, output=low, DP<0.35V, output=high
hst_v0p41_out_0_usb3	3	R	‘b0	DM>THD, output=low, DM<THD, output=high
hst_v0p46_out_0_usb3	2	R	‘b1	don't care. Output=high.
dev_chg_det_0_usb3	1	R	‘b0	Detector result
dev_dcp_det_0_usb3	0	R	‘b0	Detector result

1.97 REGISTER:: USB3_HOST_BC_CTL_REG 0x9801_3D30

Module::usb	Register::USB3_HOST_BC_CTL_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D30

Name	Bits	R/W	Default	Comments
Rvd	31..15	-	-	-
lf_pd_r_en_0_usb3	14	R/W	‘b1	
hst_pow_charge_0_usb3	13	R/W	‘b0	Enable charge, high enable
hst_vdm_src_en_0_usb3	12	R/W	‘b0	Enable VDM_SRC output, high

				enable
hst_idp_sink_en_0_usb3	11	R/W	‘b0	Enable DP current sink, high enable
hst_app_div_en_0_usb3	10	R/W	‘b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	‘b0	Select Apple charge current 2.1A/1A 0: DP=2.0V, DM=2.7V 1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_usb3	8	R/W	‘b0	Enable comparator for detect Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	‘b0	Enable NOTE mode, high enable, DP=1.25V
hst_dcp_en_0_usb3	6	R/W	‘b0	Enable DCP mode, high enable, short DP and DM.
dev_pow_charge_0_usb3	5	R/W	‘b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb3	4	R/W	‘b0	0: select CHG_DET detect 1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	‘b0	Enable DP output voltage, high enable
dev_vdm_src_en_0_usb3	2	R/W	‘b0	Enable DM output voltage, high enable
dev_idp_sink_en_0_usb3	1	R/W	‘b0	Enable DP current sink, high enable
dev_idm_sink_en_0_usb3	0	R/W	‘b0	Enable DM current sink, high enable

1.98 REGISTER:: USB3_HOST_DUMMY_0_REG 0x9801_3D34

Module::usb	Register::USB3_HOST_DUMMY_0_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D34
Name	Bits	R/W	Default	Comments	
dummy_0	31..0	R/W	32’h0	Dummy register,default:0	

1.99 REGISTER:: USB3_HOST_DUMMY_1_REG 0x9801_3D38

Module::usb	Register::USB3_HOST_DUMMY_1_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D38
Name	Bits	R/W	Default	Comments	
dummy_1	31..0	R/W	32’hFFFF_FFFF	Dummy register,default:1	

1.100 REGISTER:: USB3_HOST_USB_DBUS_PWR_CTRL 0x9801_3D60

Module::usb	Register:: USB3_HOST_USB_DBUS_PWR_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D60
Name	Bits	R/W	Default	Comments	
Rvd	31..12	-	-	-	
clk_en_gap	11..10	R/W	‘h0	00:50ns 01:300ns	

				10:500ns 11:1us
sram_ls_gap	9..8	R/W	‘h0	00:200ns 01:300ns 10:100ns 11:500ns
Rvd	7..2	-	-	-
dbus_pwr_ctrl_sw_rst	1	R/W	‘h0	dbus power ctrl software reset to idle
dbus_pwr_ctrl_en	0	R/W	‘h0	dbus power ctrl enable

1.101 REGISTER:: USB3_U3_HOST_WRAP_CTR_reg 0x9801_3E00

Module::usb	Register:: USB3_U3_HOST_WRAP_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E00

Name	Bits	R/W	Default	Comments
Rvd	31..7	-	-	-
rxdetect_value	6	R/W	‘b0	
rxdetect_sel	5	R/W	‘b0	
resume_cycle_sel	4	R/W	‘b0	
sram_debug_sel	3	R/W	‘b0	Select sram 1: host 0: device
sram_debug_mode	2	R/W	‘b0	Enable sram debug mode
dbus_multi_req_disable	1	R/W	’b0	Disable multiple request for Dbus 0: enable multiple request 1: disable multiple request
dev_mode	0	R/W	’b0	Enable peek on AHB burst length 0: host (2) 1: host/dev

1.102 REGISTER:: USB3_U3_HOST_GNT_INT_reg 0x9801_3E04

Module::usb	Register::USB3_U3_HOST_GNR_INT	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E04

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
device_int	1	R	‘b0	USB3 Device MAC interrupt
host_int	0	R	‘b0	USB3 Host MAC interrupt

1.103 REGISTER:: USB3_U3_HOST_USB2_PHY_UTMI 0x9801_3E08

Module::usb	Register:: USB3_U3_HOST_USB2_PHY_UTMI	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E08

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-
reset_utmi_p0	0	R/W	‘b0	UTMI reset to PHY0 (sync and automatically return to low)

1.104 REGISTER:: USB3_U3_HOST_PHY_PIPE 0x9801_3E0c

Module::usb	Register::USB3_U3_HOST_PHY_PIPE	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E0c

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-
reset_pipe3_p0	0	R/W	‘b0	PIPE3 reset to PHY1 (sync and automatically return to low)

1.105 REGISTER:: USB3_U3_HOST_MDIO_CTR_reg 0x9801_3E10

Module::usb	Register:: USB3_U3_HOST_MDIO_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E10

Name	Bits	R/W	Default	Comments
data	31..16	R/W	‘h0	Write data or read data.
phy_addr	15..13	R/W	‘d0	MDIO PHY addressing value.
phy_reg_addr	12..8	R/W	‘d0	MDIO Register addressing value
mdio_busy	7	R/W	‘d0	-
mdio_st	6..5	R/W	‘d0	MDIO host controller state Monitor
mdio_rdy	4	R/W	‘d0	MDIO Pre-amble signal Monitor
mclk_rate	3..2	R/W	‘d0	MDIO clock rate selection: 2’b00: clk_sys/32 2’b01: clk_sys/16 2’b10: clk_sys/8 2’b11: clk_sys/4
mdio_srst	1	R/W	‘d0	Assert 1’b1 to do soft reset
mdio_rdwr	0	R/W	‘d0	1’b0: read , 1’b1: write

1.106 REGISTER:: USB3_U3_HOST_VSTATUS_port0_reg 0x9801_3E14

Module::usb	Register:: USB3_U3_HOST_VSTATUS0_OUT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E14

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
p0_vstatus_out	7..0	R/W	’h00	Vstatus output for port0 (It’s used to configure PHY’s control register)

The process of configuring PHY control register:

5. write VSTATUS_reg (0x9801_3E14), (data output to PHY)
6. write GUSB2PHYAccn (p0:0x981F_8280)
   [25]: vload
   [23]: vBusy
   [11:8]: vcontrol
   [7:0]: vstatus_in (data input from PHY)

Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'b0	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. **Note:** This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. **Note:** These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) ■ UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ■ ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) ■ UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ■ ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:
Vcontrol[3]: low/high address, 0: low, 1: high
Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.107 REGISTER:: USB3_U3_HOST_SLP_BACK_EN_port0_reg 0x9801_3E18

Module::usb	Register::USB3_U3_HOST_SLP_BACK0_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E18

Name	Bits	R/W	Default	Comments
Rvd	31..4	-	-	-
simulation_mode_p0	3	R/W	'b0	Port0 Reduce counter for entering HS
force_hs_mode_p0	2	R/W	'b0	Port0 Force HOST IP enter high speed mode 0: disable 1: enable
test_rst_p0	1	R/W	'b0	Port0 Self loop back reset
test_en_p0	0	R/W	'b0	Port0 Self loop back enable

1.108 REGISTER:: USB3_U3_HOST_SLP_BACK_CTR_port0_reg 0x9801_3E1c

Module::usb	Register:: USB3_U3_HOST_SLP_BACK0_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E1c

Name	Bits	R/W	Default	Comments
Rvd	31..12	-	-	-
test_speed_p0	11..10	R/W	'h0	When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2'b01: force PHY in HS 2'b10: force PHY in FS/LS 2'b00/2'b11: normal mode
test_seed_p0	9..2	R/W	'h0	Self_loop_back Random generator seed
test_psl_p0	1..0	R/W	'h0	Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter

1.109 REGISTER:: USB3_U3_HOST_SLP_BACK_ST_port0_reg 0x9801_3E20

Module::usb	Register:: USB3_U3_HOST_SLP_BACK0_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E20

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
test_fail_p0	1	R	'b0	Port0 Self loop back fail
test_done_p0	0	R	'b0	Port0 Self loop back done

Slef_loop_back procedure:

(15) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	F0	DBNC_EN	DISCON_ENABLE	EN_ERR_UNDERRUN	LATE_DL LEN	INTG	SOP_KK	SLB_INNER	SLB_EN	
			1	1	1	1	1	1	0: digital & analog 1: digital only	1	

(16) set test_psl, test_seed and test_speed
(17) set test_rst=1 & test_en=0 (reset)
(18) set test_rst=0 & test_en=0 (reset)
(19) set test_rst=0 & test_en=1 (enable)
(20) polling test_done
(21) check test_fail

Force MAC to enter High-Speed procedure:

(7) In simulation mode: force_hs_mode=1 & simulation_mode=1
(8) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
(9) In normal mode: force_hs_mode=0 & simulation_mode=0

1.110 REGISTER:: USB3_U3_HOST_PHY2_SLB0_EN_reg 0x9801_3E24

Module::usb	Register:: USB3_U3_HOST_PHY2_SLB_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E24

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_usb2phy_slb_hs	1	R/W	'b0	Usbphy port0 self loop back hs mode

p0_usb2phy_force_slb	0	R/W	‘b0	Usbphy port0 self loop back start

1.111 REGISTER:: USB3_U3_HOST_PHY2_SLB0_ST_reg 0x9801_3E28

Module::usb	Register:: USB3_U3_HOST_PHY2_SLB_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E28

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_usb2phy_slb_fail	1	R	‘b0	Usbphy port0 self loop back done
p0_usb2phy_slb_done	0	R	‘b0	Usbphy port0 self loop back fail

1.112 REGISTER:: USB3_U3_HOST_USB2_SPD_CTR 0x9801_3E2C

Module::usb	Register:: USB3_U3_HOST_USB2_SPD_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E2c

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_suspend_r	0	R/W	’b0	-

1.113 REGISTER:: USB3_U3_HOST_ SLB_EN_reg 0x9801_3E30

Module::usb	Register:: USB3_U3_HOST_PHY3_SLB_EN	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E30

Name	Bits	R/W	Default	Comments
Rvd	31..3	-	-	-
p0_pipe_bist_sel	2..1	R/W	‘b0	Self loop back select: 00:counter 01:tseq 10:ts1 11:ts2
p0_pipe_bist_en	0	R/W	‘b0	Self loop back enable

1.114 REGISTER:: USB3_U3_HOST_PHY3_ SLB_CT_reg 0x9801_3E34

Module::usb	Register:: USB3_U3_HOST_PHY3_SLB_CT	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E34

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-

p0_usb3phy_slb_go	0	R/W	'b0	Usb3phy port0 self loop back start transfer

1.115 REGISTER:: USB3_U3_HOST_PHY3_ SLB_ST_reg 0x9801_3E38

Module::usb	Register:: USB3_U3_HOST_PHY3_SLB_ST	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E38

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
p0_usb3phy_slb_fail	1	R	'b0	Usb3phy port0 self loop back done
p0_usb3phy_slb_done	0	R	'b0	Usb3phy port0 self loop back mode

1.116 REGISTER:: USB3_U3_HOST_USB_DBG_reg 0x9801_3E40

Module::usb	Register:: USB3_U3_HOST_USB_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E40

Name	Bits	R/W	Default	Comments
Rvd	31..13	-	-	-
dbg_sel1	12..7	R/W	'b0	Select debug signal sets to be probed via usb_dbg_out1
dbg_sel0	6..1	R/W	'b0	Select debug signal sets to be probed via usb_dbg_out0
dbg_en	0	R/W	'b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both usb_dbg_out0 and usb_dbg_out1 are static 16'h0.

1.117 REGISTER:: USB3_U3_HOST_USB_STCH_reg 0x9801_3E44

Module::usb	Register:: USB3_U3_HOST_USB_SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E44

Name	Bits	R/W	Default	Comments
reg1	31..16	R/W	'hffff	Dummy register with value 1
reg0	15..0	R/W	'd0	Dummy register with value 0

1.118 REGISTER:: USB3_U3_HOST_USB_TMP_SP_reg _0 0x9801_3E48

Module::usb	Register:: USB3_U3_HOST_USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E48

Name	Bits	R/W	Default	Comments
test_sp_reg_0	31..12	R/W	'd0	Dummy test register
int_inact_status	11	R/W	'd0	ltssm change to ss inactive state
int_ss_dis_status	10	R/W	'd0	ltssm change to ss disabled state
int_hreset_status	9	R/W	'd0	ltssm change to hot reset state
int_recov_status	8	R/W	'd0	ltssm change to recovery state
int_rx_det_status	7	R/W	'd0	ltssm change to rx detect state
int_poll_status	6	R/W	'd0	ltssm change to polling state
int_u3_status	5	R/W	'd0	ltssm change to u3 state
int_u2_status	4	R/W	'd0	ltssm change to u2 state
int_u1_status	3	R/W	'd0	ltssm change to u1 state
int_u0_status	2	R/W	'd0	ltssm change to u0 state
int_loopbk_status	1	R/W	'd0	ltssm change to loopback state
int_comp_status	0	R/W	'd0	ltssm change to compliance state

1.119 REGISTER:: USB3_U3_HOST_USB_TMP_SP_reg_1 0x9801_3E4C

Module::usb	Register:: USB3_U3_HOST_USB_TMP_SP	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E48

Name	Bits	R/W	Default	Comments
test_sp_reg_1	31..0	R/W	'd0	Dummy test register

1.120 REGISTER:: USB3_U3_HOST_USB_TMP_reg _2 0x9801_3E50

Module::usb	Register:: USB3_U3_HOST_USB_TMP	Set::3	ATTR::ctrl	Type::SR	ADDR::0x9801_3850

Name	Bits	R/W	Default	Comments
test_reg_2	31..0	R/W	'd0	Dummy test register

1.121 REGISTER:: USB3_U3_HOST_USB_TMP_reg_3 0x9801_3E5C

Module::usb	Register:: USB3_U3_HOST_USB_TMP	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E5C

Name	Bits	R/W	Default	Comments
test_reg_3	31..13	R/W	'd0	Dummy test register
int_inact_en	12	R/W	'd0	ltssm change to ss inactive state interrupt enable

int_ss_dis_en	11	R/W	‘d0	ltssm change to ss disable state interrupt enable
int_hreset_en	10	R/W	‘d0	ltssm change to hot reset state interrupt enable
int_recov_en	9	R/W	‘d0	ltssm change to recovery state interrupt enable
int_rx_det_en	8	R/W	‘d0	ltssm change to rx detect state interrupt enable
int_poll_en	7	R/W	‘d0	ltssm change to polling state interrupt enable
int_u3_en	6	R/W	‘d0	ltssm change to u3 state interrupt enable
int_u2_en	5	R/W	‘d0	ltssm change to u2 state interrupt enable
int_u1_en	4	R/W	‘d0	ltssm change to u1 state interrupt enable
int_u0_en	3	R/W	‘d0	ltssm change to u0 state interrupt enable
int_loopbk_en	2	R/W	‘d0	ltssm change to loopback state interrupt enable
int_comp_en	1	R/W	‘d0	ltssm change to compliance state interrupt enable
Rvd	0	-	-	-

1.122 REGISTER:: USB3_U3_HOST_USB_HMAC_CTR0_reg 0x9801_3E60

Module::usb	Register:: USB3_U3_HOST_HMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E60

Name	Bits	R/W	Default	Comments
Rvd	31..30	-	-	-
host_fladj_30mhz	29..24	R/W	‘d32	-
host_ppc_present	23	R/W	‘b0	-
host_msi_enable	22	R/W	‘b0	
host_pm_pw_state_req	21..20	R/W	‘b0	
hub_port_over_current	19..16	R/W	‘b0	
hub_port_perm_attach	15..12	R/W	‘b0	
host_u2_port_disable	11..9	R/W	‘b0	
host_u3_port_disable	8	R/W	‘b0	
host_num_u2_port	7..4	R/W	‘d1	
host_num_u3_port	3..0	R/W	‘d1	

1.123 REGISTER:: USB3_U3_HOST_MAC3_HST_ST_reg 0x9801_3E64

Module::usb	Register:: USB3_U3_HOST_MAC3_HST_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E64

Name	Bits	R/W	Default	Comments

Rvd	31..6	-	-	-
host_current_power_state	5..4	R	‘b0	Current xHC power state
host_hub_vbus_ctrl	3..0	R	‘b0	Vbus active indication

1.124 REGISTER:: USB3_U3_HOST_DMAC_CTR0_reg 0x9801_3E68

Module::usb	Register:: USB3_U3_HOST_DMAC_CTR0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E68

Name	Bits	R/W	Default	Comments
Rvd	31..27	-	-	-
host_xhc_bme	26	R/W	‘b1	
Rvd	25..3	-	-	-
host_utmiotg_vbusvalid	2..0	R/W	‘h7	

1.125 REGISTER:: USB3_U3_HOST_MAC3_DEV_ST_reg 0x9801_3E6C

Module::usb	Register:: USB3_U3_HOST_MAC3_DEV_ST	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E6c

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
dev_current_power_state	1..0	R	‘b0	Current xHC power state

1.126 REGISTER:: USB3_U3_HOST_USB2_PHY_reg 0x9801_3E70

Module::usb	Register:: USB3_U3_HOST_USB2_PHY	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E70

Name	Bits	R/W	Default	Comments
Rvd	31..13	-	-	-
phy_pll_en	12	R/W	‘b1	1:phy pll always on(for CR 480MHz)
p0_by_pass_on_1	11	R/W	‘b0	Isolation A→D
p0_DmPulldown	10	R/W	‘b0	Device = 1’b0
p0_DpPulldown	9	R/W	‘b0	Device = 1’b0
p0_IDPULLUP	8	R/W	‘b0	Device = 1’b0
Rvd	7..3	-	-	-
p0_DmPulldown_sel	2	R/W	‘b0	p0_DmPulldown_sel ? p0_DmPulldown : 1’b0
p0_DpPulldown_sel	1	R/W	‘b0	p0_DpPulldown_sel ? p0_DpPulldown : 1’b0
p0_IDPULLUP_sel	0	R/W	‘b0	p0_IDPULLUP_sel ? p0_IDPULLUP : 1’b0

1.127 REGISTER:: USB3_U3_HOST_USB_RAM_CTR_reg 0x9801_3E74

Module::usb	Register:: USB3_U3_HOST_RAM_CTR	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E874

Name	Bits	R/W	Default	Comments
Rvd	31..17	-	-	-
done_st	16	R/W	'b0	Write 1 to clear
Rvd	15..1	-	-	-
go_ct	0	R/W	'b0	Start DMA transfer, clear after done

1.128 REGISTER:: USB3_U3_HOST_USB_RAM_ADDR_reg 0x9801_3E78

Module::usb	Register:: USB3_U3_HOST_RAM_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E78

Name	Bits	R/W	Default	Comments
sram_addr	31..0	R/W	'd0	SRAM address, 4-byte align. Bit[0]= use for write/read bit 0: read 1: write

1.129 REGISTER:: USB3_U3_HOST_USB_RAM_WDATA_reg 0x9801_3E87C

Module::usb	Register:: USB3_U3_HOST_RAM_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E87C

Name	Bits	R/W	Default	Comments
ram_wdata	31..0	R/W	'd0	RAM write data to be write

1.130 REGISTER:: USB3_U3_HOST_RAM_RDATA_reg 0x9801_3E80

Module::usb	Register:: USB3_U3_HOST_RAM_RDATA	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E80

Name	Bits	R/W	Default	Comments
ram_rdata	31..0	R/W	'd0	USB read data to be read back

1.131 REGISTER:: USB3_U3_HOST_PHY0_ST_reg 0x9801_3E84

Module::usb	Register::	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E84

	USB3_U3_HOST_PHY0_ST				
Name	Bits	R/W	Default	Comments	
Rvd	31..19	-	-	-	
p0_count_num	18..0	R	'b0	USB3 PHY count number value	

1.132 REGISTER:: USB3_U3_HOST_OVR_CT_reg 0x9801_3E88

Module::usb	Register::USB3_U3_HOST_OVR_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E88
Name	Bits	R/W	Default	Comments	
Rvd	31..2	R/W	-	-	
phy3_lperiod	9..7	R/W	'd1	Connect to PHY3	
phy3_hperiod	6..4	R/W	'd3	Connect to PHY3	
phy3_last	3..2	R/W	'd2	Connect to PHY3	
host_ovr_current_value	1	R/W	'b0		
host_ovr_current_sel	0	R/W	'b0		

1.133 REGISTER:: USB3_U3_HOST_SOFT_Reset 0x9801_3F00

Module::usb	Register:: USB3_U3_HOST_SOFT_RESET	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F00
Name	Bits	R/W	Default	Comments	
Rvd	31..3	-	-	-	
rstn_usb2_phy1	2	R/W	'b0	USB2 PHY1 reset for USB2 IP	
rstn_usb2_phy0	1	R/W	'b0	USB2 PHY0 reset for USB2 IP	
rstn_usb2	0	R/W	'b0	USB2 IP system reset	

1.134 REGISTER:: USB3_U3_HOST_GBL_USB_CT 0x9801_3F04

Module::usb	Register:: USB3_U3_HOST_GBL_USB_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F04
Name	Bits	R/W	Default	Comments	
usb_mac_ctrl	31..0	R/W	'd0	Register use for usb_mac_ctrl	

1.135 REGISTER:: USB3_U3_HOST_GBL_USB_ARB 0x9801_3F08

Module::usb	Register:: USB3_U3_HOST_GBL_USB_ARB	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F08

Name	Bits	R/W	Default	Comments
Rvd	31..4	-		
dbus_robin_enable	3	R/W	‘b0	
cmd_full_number	2..1	R/W	‘d3	
dbus_arb_priority	0	R/W	‘b0	

1.136 REGISTER:: UNUSED 0x9801_3F0C

1.137 REGISTER:: USB3_U3_HOST_OTG_STS 0x9801_3F10

Module::**usb**	Register::USB3_U3_HOST_OTG_STS	Set::**1**	ATTR::none	Type::**SR**	ADDR::**0x9801_3F10**

Name	Bits	R/W	Default	Comments
Rvd	31..1	-	-	-
otg_interrupt	0	R	‘b0	OTG interrupt from USB3 MAC

1.138 REGISTER:: USB3_U3_HOST_USB_BC_STS 0x9801_3F14

Module::**usb**	Register:: USB3_U3_HOST_USB_BC_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3F14**

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
chirp_on	1	R	‘b0	battery charging chirp signal from USB3 MAC
bc_interrupt	0	R	‘b0	battery charging interrupt from USB3 MAC

1.139 REGISTER:: USB3_U3_HOST_BIST1_CTRL 0x9801_3F18 (IP sram)

Module::**usb**	Register::USB3_U3_HOST_BIST1_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_3F18**

Name	Bits	R/W	Default	Comments
Rvd	31..28	-	-	-
usb3_bist1_ls[2:0]	27..25	R/W	3’h0	SRAM0~2 LS value
usb3_bist1_rm_3	24..21	R/W	4’h0	SRAM3 RM value
usb3_bist1_rme_3	20	R/W	‘b0	SRAM3 RM enable
usb3_bist1_rm_2	19..16	R/W	4’h0	SRAM2 RM value
usb3_bist1_rme_2	15	R/W	‘b0	SRAM2 RM enable
usb3_bist1_rm_1	14..11	R/W	4’h0	SRAM1 RM value
usb3_bist1_rme_1	10	R/W	‘b0	SRAM1 RM enable
usb3_bist1_rm_0	9..6	R/W	4’h0	SRAM0 RM value
usb3_bist1_rme_0	5	R/W	‘b0	SRAM0 RM enable

usb3_drf_1_test_resume	4	W/R	'b0	USB3 DRF BIST1 trigger resume signal
usb3_drf_bist1_en	3	W/R	'b0	USB3 DRF BIST1 enable
usb3_bist1_en	2	W/R	'b0	USB3 BIST1 enable
Rvd	1	-	-	-
usb3_bist1_test_mode	0	W/R	'b0	USB3 BIST1 test mode enable

1.140 REGISTER:: USB3_U3_HOST_BIST2_CTRL 0x9801_3F1c (PPsram)

Module::**usb**	Register::USB3_U3_HOST_BIST2_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9801_3F1c**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..17	-	-	-
usb3_bist2_ls[1:0]	16..15	R/W	2'h0	SRAM4~5 LS value
usb3_bist2_rm_1	14..11	R/W	4'h0	SRAM5 RM value
usb3_bist2_rme_1	10	R/W	'b0	SRAM5 RM enable
usb3_bist2_rm_0	9..6	R/W	4'h0	SRAM4 RM value
usb3_bist2_rme_0	5	R/W	'b0	SRAM4 RM enable
usb3_drf_2_test_resume	4	W/R	'b0	USB3 DRF BIST2 trigger resume signal
usb3_drf_bist2_en	3	W/R	'b0	USB3 DRF BIST2 enable
usb3_bist2_en	2	W/R	'b0	USB3 BIST2 enable
Rvd	1	-	-	-
usb3_bist2_test_mode	0	W/R	'b0	USB3 BIST2 test mode enable

1.141 REGISTER:: USB3_U3_HOST_BIST1_STS 0x9801_3F20

Module::**usb**	Register::USB3_U3_HOST_BIST1_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3F20**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..11	-	-	-
usb3_drf_bist1_fail_3	10	R	'b0	USB3 DRF1 SRAM3 fail signal
usb3_bist1_fail_3	9	R	'b0	USB3 BIST1 SRAM3 fail signal
usb3_drf_bist1_fail_2	8	R	'b0	USB3 DRF1 SRAM2 fail signal
usb3_bist1_fail_2	7	R	'b0	USB3 BIST1 SRAM2 fail signal
usb3_drf_bist1_fail_1	6	R	'b0	USB3 DRF1 SRAM1 fail signal
usb3_bist1_fail_1	5	R	'b0	USB3 BIST1 SRAM1 fail signal
usb3_drf_bist1_fail_0	4	R	'b0	USB3 DRF1 SRAM0 fail signal
usb3_bist1_fail_0	3	R	'b0	USB3 BIST1 SRAM0 fail signal
usb3_drf_1_start_pause	2	R	'b0	USB3 DRF1 start pause signal
usb3_drf_bist1_done	1	R	'b0	USB3 DRF1 done
usb3_bist1_done	0	R	'b0	USB3 BIST1 done

1.142 REGISTER:: USB3_U3_HOST_BIST2_STS 0x9801_3F24

Module::**usb**	Register::USB3_U3_HOS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9801_3F24**

T_BIST2_STS				
Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..7	-	-	-
usb3_drf_bist2_fail_1	6	R	‘b0	USB3 DRF2 SRAM5 fail signal
usb3_bist2_fail_1	5	R	‘b0	USB3 BIST2 SRAM5 fail signal
usb3_drf_bist2_fail_0	4	R	‘b0	USB3 DRF2 SRAM4 fail signal
usb3_bist2_fail_0	3	R	‘b0	USB3 BIST2 SRAM4 fail signal
usb3_drf_2_start_pause	2	R	‘b0	USB3 DRF2 start pause signal
usb3_drf_bist2_done	1	R	‘b0	USB3 DRF2 done
usb3_bist2_done	0	R	‘b0	USB3 BIST2 done

1.143 REGISTER:: USB3_U3_HOST_APHY_REG 0x9801_3F28

Module::usb	Register::USB3_U3_HOST_APHY_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F28

Name	Bits	R/W	Default	Comments
Rvd	31..5	-	-	-
usb3_clk_mode_sel	4..3	R/W	‘b00	“11” : Diff. 100MHz in, else CKIN_XTAL in. IN RL6227 ,CKREF comes from CKIN_XTAL, tie “00”.
usb3_ckbuf_en	2	R/W	‘b0	CKREF Buffer Enable tie 0
usb3_mbias_en	1	R/W	‘b1	Bias Circuit Enable. 1: Bias Circuit enable 0: Bias Circuit disable
usb3_bg_en	0	R/W	‘b0	Bandgap Enable. IN RL6227,no BG inside the USB3.0 block, tie 0

1.144 REGISTER:: USB3_U3_HOST_BC_STS2_REG 0x9801_3F2C

Module::usb	Register::USB3_U3_HOST_BC_STS2_REG	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3F2C

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
hst_prtbl_det_0_usb3	7	R	‘b0	
hst_comp_out_0_usb3	6	R	‘b0	Debug signal
hst_sh_out_0_usb3	5	R	‘b0	Debug signal
hst_v0p07_out_0_usb3	4	R	‘b0	DP>0.35V, output=low, DP<0.35V, output=high
hst_v0p41_out_0_usb3	3	R	‘b0	DM>THD, output=low, DM<THD, output=high
hst_v0p46_out_0_usb3	2	R	‘b1	don't care. Output=high.
dev_chg_det_0_usb3	1	R	‘b0	Detector result
dev_dcp_det_0_usb3	0	R	‘b0	Detector result

1.145 REGISTER:: USB3_U3_HOST_BC_CTL_REG 0x9801_3F30

Module::usb	Register::USB3_U3_HOST_BC_CTL_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F30

Name	Bits	R/W	Default	Comments
Rvd	31..15	-	-	-
lf_pd_r_en_0_usb3	14	R/W	‘b1	

hst_pow_charge_0_usb3	13	R/W	‘b0	Enable charge, high enable
hst_vdm_src_en_0_usb3	12	R/W	‘b0	Enable VDM_SRC output, high enable
hst_idp_sink_en_0_usb3	11	R/W	‘b0	Enable DP current sink, high enable
hst_app_div_en_0_usb3	10	R/W	‘b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	‘b0	Select Apple charge current 2.1A/1A 0: DP=2.0V, DM=2.7V 1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_usb3	8	R/W	‘b0	Enable comparator for detect Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	‘b0	Enable NOTE mode, high enable, DP=1.25V
hst_dcp_en_0_usb3	6	R/W	‘b0	Enable DCP mode, high enable, short DP and DM.
dev_pow_charge_0_usb3	5	R/W	‘b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb3	4	R/W	‘b0	0: select CHG_DET detect 1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	‘b0	Enable DP output voltage, high enable
dev_vdm_src_en_0_usb3	2	R/W	‘b0	Enable DM output voltage, high enable
dev_idp_sink_en_0_usb3	1	R/W	‘b0	Enable DP current sink, high enable
dev_idm_sink_en_0_usb3	0	R/W	‘b0	Enable DM current sink, high enable

1.146 REGISTER:: USB3_U3_HOST_DUMMY_0_REG 0x9801_3F34

Module::usb	Register::USB3_U3_HOST_DUMMY_0_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F34
Name	Bits	R/W	Default	Comments	
dummy_0	31..0	R/W	32’h0	Dummy register,default:0	

1.147 REGISTER:: USB3_U3_HOST_DUMMY_1_REG 0x9801_3F38

Module::usb	Register::USB3_U3_HOST_DUMMY_1_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F38
Name	Bits	R/W	Default	Comments	
dummy_1	31..0	R/W	32’hFFFF_FFFF	Dummy register,default:1	

1.148 REGISTER:: USB3_U3_HOST_LTSSM_STS 0x9801_3F3C

Module::usb	Register::USB3_U3_HOST_LTSSM_STS	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3F3C
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-	-	-	
Ltdb_sub_state	3..0	R	‘b0	Ltssm sub-state from USB3 IP	

1.149 REGISTER:: USB3_U3_HOST_USB_DBUS_PWR_CTRL 0x9801_3F60

Module::usb	Register:: USB3_U3_HOST_USB_DBUS_PWR_CTRL	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F60

Name	Bits	R/W	Default	Comments
Rvd	31..12	-	-	-
clk_en_gap	11..10	R/W	'h0	00:50ns 01:300ns 10:500ns 11:1us
sram_ls_gap	9..8	R/W	'h0	00:200ns 01:300ns 10:100ns 11:500ns
Rvd	7..2	-	-	-
dbus_pwr_ctrl_sw_rst	1	R/W	'h0	dbus power ctrl software reset to idle
dbus_pwr_ctrl_en	0	R/W	'h0	dbus power ctrl enable