Standard for RealTek DVD Recordable

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DVD-R2 Serial-ATA

RealTek specification on DVD Recordable Technology

Kylin Serial-ATA Controller Architecture Specification

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Registers Description

1.1 SATA Registers

1. SATA MAC (IP) from 0x9803_F000 ~ 0x9803_F1FF (only support 2 phy port)
2. SATA Wrapper from 0x9803_FF00 ~ 0x9803_FFFF

1.1.1 SATA Wrapper Register

Module::sata	Register::SATA_MAC_IN	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF00
Name	Bits	R/W	Default	Comments	
Rvd	31..5	-	-	-	
Mbist_sata_st	4	R	‘b0	SATA Memory BIST status	
cp_pod1	3	R	‘b0	SATA MAC port 1 cold presence	
cp_pod0	2	R	‘b0	SATA MAC port 0 cold presence	
pme_req	1	R	’b0	SATA IP power management request (for PCIE board)	
sata_mac_int	0	R	’b0	SATA HOST MAC IP interrupt	

Module::sata	Register::SATA_FORCE_RST	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF10
Name	Bits	R/W	Default	Comments	
Rvd	31..3	-	-	-	
sata_phy_rst_force	2	R/W	‘b0	SATA PHY reset force mode	
sata_phy_rstn	1..0	R/W	‘b0	SATA PHY force reset_n (this bit valid only when sata_phy_rst_force =1)	

Module::sata	Register::SATA_SAVE	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF14
Name	Bits	R/W	Default	Comments	
Rvd	31..2	-	-	-	
sata_ls_en	1	R/W	‘b1		
sata_clk_gate_en	0	R/W	‘b1		

Module::sata	Register::SATA_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF20
Name	Bits	R/W	Default	Comments	
Rvd	31..18	-	-	-	
rx_error_CDR_sel	17..16	R/W	‘d0	rx error select for APHY 2’b00 : only data window error occur but exclude bist 2’b01 : error but exclude bist 2’b10 : error occur 2’b11 : MAC original error	
rx_error_sel	15..14	R/W	‘d1	rx error select 2’b00 : only data window error occur but exclude bist 2’b01 : error but exclude bist 2’b10 : error occur 2’b11 : MAC original error	
clk_mode_sel_1	13..12	R/W	‘b0		
clk_mode_sel_0	11..10	R/W	‘b0		
ckbuf_en1	9	R/W	‘b1		

ckbuf_en0	8	R/W	‘b1	
mp_switch1	7	R/W	‘b0	Port 1 Mechanical switch register (TO IP)
mp_switch0	6	R/W	‘b0	Port 0 Mechanical switch register (TO IP)
cp_det1	5	R/W	‘b0	Port 1 Cold presence detect register (TO IP)
cp_det0	4	R/W	‘b0	Port 0 Cold presence detect register (TO IP)
phy_rx_err_1	3	R/W	‘b0	SATA port 1RX decode and disparity error 0: rx without error 1: rx error
phy_rx_err_0	2	R/W	‘b0	SATA port 1RX decode and disparity error 0: rx without error 1: rx error
phy_iprx_en_1	1	R/W	‘b0	SATA PHY 1 8b/10b decode/encode 0 : disable (MAC do it) 1 : enable (PHY do it)
phy_iprx_en_0	0	R/W	‘b0	SATA PHY 0 8b/10b decode/encode 0 : disable (MAC do it) 1 : enable (PHY do it)

Module::sata	Register::SATA_PHY_MON	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF24
Name	Bits	R/W	Default	Comments	
Rvd	31..4	-	-	-	
phy_rdy_1	3	R	‘b0	Port 1 PHY ready	
phy_rdy_0	2	R	‘b0	Port 0 PHY ready	
phy_calibrated_1	1	R	‘b0	Port 1 PHY Assert high when PHY-analog module had complete fine tune clock Assert low when “phy_spdsel” had command to change operation speed and return to high when speed change had complete	
phy_calibrated_0	0	R	‘b0	Port 0 PHY Assert high when PHY-analog module had complete fine tune clock Assert low when “phy_spdsel” had command to change operation speed and return to high when speed change had complete	

Module::sata	Register::SATA_wrapper_dma_ctrl	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF30
Name	Bits	R/W	Default	Comments	
Rvd	31..18	-	-	-	
rdata_in_order	17	R/W	’d1	In the 2dc-sys, MAC not support outstanding, We can set rdata_in_order=1 or outstd_rcmd=1.	

wcmd_bufable_sel	16	R/W	'd0	we add an option "wlast_opt" to assert bvalid when wlast is asserted
Rvd	15..12	-	-	-
outstd_wcmd	11..8	R/W	'd4	Maxinum outstanding for write commands.
Rvd	7..5	-	-	-
outstd_rcmd	4..0	R/W	'd4	Maxinum outstanding for read commands.

Module::sata	Register::SATA_wrapper_dc_ctrl	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF34

Name	Bits	R/W	Default	Comments
Rvd	31..28	-	-	-
dbus2_remote_cmd_num	27..24	R/W	'd2	
Rvd	23..20	-	-	
dbus_remote_cmd_num	19..16	R/W	'd2	
Rvd	15..14	-	-	
dbus2_remote_wdata_num	13..8	R/W	'd32	
Rvd	7..6	-	-	
dbus_remote_wdata_num	5..0	R/W	'd32	

Module::sata	Register::SATA_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF40

Name	Bits	R/W	Default	Comments
Rvd	31..13	-	-	-
dbg_sel1	12..7	R/W	'b0	**Select debug signal sets to be probed via usb_dbg_out1**
dbg_sel0	6..1	R/W	'b0	Select debug signal sets to be probed via usb_dbg_out0
dbg_en	0	R/W	'b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both usb_dbg_out0 and usb_dbg_out1 are static 16'h0.

Module::sata	Register::WRAP_CTR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF50

Name	Bits	R/W	Default	Comments
Rvd	31..2	-	-	-
sram_debug_sel	1	R/W	'b0	Select sram 1: host 0: device
sram_debug_mode	0	R/W	'b0	Enable sram debug mode

Module::sata	Register::MDIO_CTR	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF60

Name	Bits	R/W	Default	Comments
data	31..16	R/W	'h0	Write data or read data.
phy_addr	15..14	R/W	'd0	MDIO PHY addressing value. Bit 2'b00: SATA1.0 2'b01: SATA2.0 2'b10: SATA3.0 2'b11: SGMII
phy_reg_addr	13..8	R/W	'd0	MDIO Register addressing value Others : not support yet

mdio_busy	7	R	‘d0	MDIO host busy Monitor ※If we write MDIO register, we have to read MDIO bit[7]=0 first.
mdio_st	6..5	R	‘d0	MDIO host controller state Monitor
mdio_rdy	4	R	‘d0	MDIO Pre-amble signal Monitor
mclk_rate	3..2	R/W	‘d0	MDIO clock rate selection: 2’b00: clk_sys/64 2’b01: clk_sys/32 2’b10: clk_sys/16 2’b11: clk_sys/8
mdio_srst	1	R/W	‘d0	Assert 1’b1 to do soft reset
mdio_rdwr	0	R/W	‘d0	1’b0: read , 1’b1: write

Module::sata	Register::MDIO_CTR1	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF64
Name	Bits	R/W	Default	Comments	
Rvd	31..1	-	-	Write data or read data.	
phy_sel	0	R/W	‘d0	0: PHY0 1: PHY1 ※If we want to write this bit, we have to read MDIO bit[7]=0 first.	

Module::sata	Register::SPD	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF68
Name	Bits	R/W	Default	Comments	
Rvd	31..8	-	-	Write data or read data.	
p1_spd_mode_st	7..6	R	‘d0	Phy1 current spd_mode	
p0_spd_mode_st	5..4	R	‘d0	Phy0 current spd_mode	
p1_spd_mode	3..2	R/W	‘d2	Phy1 max speed 2’b00: GEN1 2’b01: GEN2 2’b10: GEN3	
p0_spd_mode	1..0	R/W	‘d2	Phy0 max speed 2’b00: GEN1 2’b01: GEN2 2’b10: GEN3	

Module::sata	Register::RAM_CTR	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF70
Name	Bits	R/W	Default	Comments	
Rvd	31..17	-	-	-	
done_st	16	R/W	‘b0	Access MAC reg will set to 1	
Rvd	15..1	-	-	-	
go_ct	0	R/W	‘b0	Start DMA transfer, clear after done (Write 1 to clear)	

Module::sata	Register::RAM_ADDR	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF74
Name	Bits	R/W	Default	Comments	
sram_addr	31..0	R/W	‘d0	SRAM address, 4-byte align. Bit[0]= use for write/read bit 0: read 1: write	

Module::sata	Register::RAM_WDATA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FF78
Name	Bits	R/W	Default	Comments	

ram_wdata	31..0	R/W	‘d0	RAM write data to be write

Module::sata	Register::RAM_RDATA	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF7C
Name	Bits	R/W	Default	Comments	
ram_rdata	31..0	R/W	‘d0	SATA read data to be read back	

Module::sata	Register::SATA_MAC_p0_dbg0	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF80
Name	Bits	R/W	Default	Comments	
p0_csr_diagnr	31..0	R	‘d0	Port 0 CSR diagnr 0	

Module::sata	Register::SATA_MAC_p0_dbg1	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF84
Name	Bits	R/W	Default	Comments	
p0_csr_diagnr1	31..0	R	‘d0	Port 0 CSR diagnr 1	

Module::sata	Register::SATA_MAC_p0_dbg2	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF88
Name	Bits	R/W	Default	Comments	
p0_csr_is	31..0	R	‘d0	Port 0 CSR interrupt status	

Module::sata	Register::SATA_MAC_p0_dbg3	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF8C
Name	Bits	R/W	Default	Comments	
p0_csr_cmd	31..0	R	‘d0	Port 0 CSR command status	

Module::sata	Register::SATA_MAC_p1_dbg0	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF90
Name	Bits	R/W	Default	Comments	
p1_csr_diagnr	31..0	R	‘d0	Port 1 CSR diagnr 0	

Module::sata	Register::SATA_MAC_p1_dbg1	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF94
Name	Bits	R/W	Default	Comments	
p1_csr_diagnr1	31..0	R	‘d0	Port 1 CSR diagnr 1	

Module::sata	Register::SATA_MAC_p1_dbg2	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF98
Name	Bits	R/W	Default	Comments	
p1_csr_is	31..0	R	‘d0	Port 1 CSR interrupt status	

Module::sata	Register::SATA_MAC_p1_dbg3	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FF9c
Name	Bits	R/W	Default	Comments	
p1_csr_cmd	31..0	R	‘d0	Port 1 CSR command status	

Module::sata	Register::SATA_MAC_p0_dbg4	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FFA0
Name	Bits	R/W	Default	Comments	
Rvd	31..6	-	-		
p0_rx_error	5	R	‘d0	Port 0 rx error status	

p0_link_state	4..0	R	‘d0	Port 0 link state machine

Module::sata	Register::SATA_MAC_p1_dbg4	Set::1	ATTR::nor	Type::SR	ADDR::0x9803_FFA4

Name	Bits	R/W	Default	Comments
Rvd	31..6	-	-	
p1_rx_error	5	R	‘d0	Port 1 rx error status
p1_link_state	4..0	R	‘d0	Port 1 link state machine

Module::**sata**	Register::SATA_BIST1_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9803_FFB0**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..17	-	-	-
sata_bist1_ls[1:0]	16..15	R/W	’h0	Wrapper SRAM 0~1 LS value
sata_bist1_rm_1	14..11	R/W	’h0	SRAM1 RM value
sata_bist1_rme_1	10	R/W	‘b0	SRAM1 RM enable
sata_bist1_rm_0	9..6	R/W	’h0	SRAM0 RM value
sata_bist1_rme_0	5	R/W	‘b0	SRAM0 RM enable
sata_drf_1_test_resume	4	R/W	‘b0	SATA DRF BIST1 trigger resume signal
sata_drf_bist1_en	3	R/W	‘b0	SATA DRF BIST1 enable
sata_bist1_en	2	R/W	‘b0	SATA BIST1 enable
sata_bist1_rstn	1	R/W	‘b0	SATA BIST1 reset_n
sata_bist1_test_mode	0	R/W	‘b0	SATA BIST1 test mode enable

Module::**sata**	Register::SATA_BIST2_CTRL	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9803_FFB4**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..11	-	-	-
sata_bist2_ls[5:0]	10..5	R/W	’h0	IP SRAM 0~5 LS value
sata_drf_2_test_resume	4	R/W	‘b0	SATA DRF BIST2 trigger resume signal
sata_drf_bist2_en	3	R/W	‘b0	SATA DRF BIST2 enable
sata_bist2_en	2	R/W	‘b0	SATA BIST2 enable
sata_bist2_rstn	1	R/W	‘b0	SATA BIST2 reset_n
sata_bist2_test_mode	0	R/W	‘b0	SATA BIST2 test mode enable

Module::**sata**	Register::SATA_BIST2_CTRL1	Set::**1**	ATTR::ctrl	Type::**SR**	ADDR::**0x9803_FFB8**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..30	-	-	-
sata_bist2_rm_5	29..26	R/W	’h0	SRAM5 RM value
sata_bist2_rme_5	25	R/W	‘b0	SRAM5 RM enable
sata_bist2_rm_4	24.21	R/W	’h0	SRAM4 RM value
sata_bist2_rme_4	20	R/W	‘b0	SRAM4 RM enable
sata_bist2_rm_3	19..16	R/W	’h0	SRAM3 RM value
sata_bist2_rme_3	15	R/W	‘b0	SRAM3 RM enable
sata_bist2_rm_2	14..11	R/W	’h0	SRAM2 RM value
sata_bist2_rme_2	10	R/W	‘b0	SRAM2 RM enable
sata_bist2_rm_1	9..6	R/W	’h0	SRAM1 RM value
sata_bist2_rme_1	5	R/W	‘b0	SRAM1 RM enable
sata_bist2_rm_0	4..1	R/W	’h0	SRAM0 RM value
sata_bist2_rme_0	0	R/W	‘b0	SRAM0 RM enable

Module::sata	Register::SATA_BIST1_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9803_FFC0**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..7	-	-	-
sata_drf_bist1_fail_1	6	R	‘b0	SATA DRF1 SRAM1 fail signal
sata_bist1_fail_1	5	R	‘b0	SATA BIST1 SRAM1 fail signal
sata_drf_bist1_fail_0	4	R	‘b0	SATA DRF1 SRAM0 fail signal
sata_bist1_fail_0	3	R	‘b0	SATA BIST1 SRAM0 fail signal
sata_drf_1_start_pause	2	R	‘b0	SATA DRF1 start pause signal
sata_drf_bist1_done	1	R	‘b0	SATA DRF1 done
sata_bist1_done	0	R	‘b0	SATA BIST1 done

Module::**sata**	Register::SATA_BIST2_STS	Set::**1**	ATTR::nor	Type::**SR**	ADDR::**0x9803_FFC4**

Name	**Bits**	**R/W**	**Default**	**Comments**
Rvd	31..15	-	-	-
sata_drf_bist2_fail_5	14	R	‘b0	SATA DRF2 SRAM5 fail signal
sata_bist2_fail_5	13	R	‘b0	SATA BIST2 SRAM5 fail signal
sata_drf_bist2_fail_4	12	R	‘b0	SATA DRF2 SRAM4 fail signal
sata_bist2_fail_4	11	R	‘b0	SATA BIST2 SRAM4 fail signal
sata_drf_bist2_fail_3	10	R	‘b0	SATA DRF2 SRAM3 fail signal
sata_bist2_fail_3	9	R	‘b0	SATA BIST2 SRAM3 fail signal
sata_drf_bist2_fail_2	8	R	‘b0	SATA DRF2 SRAM2 fail signal
sata_bist2_fail_2	7	R	‘b0	SATA BIST2 SRAM2 fail signal
sata_drf_bist2_fail_1	6	R	‘b0	SATA DRF2 SRAM1 fail signal
sata_bist2_fail_1	5	R	‘b0	SATA BIST2 SRAM1 fail signal
sata_drf_bist2_fail_0	4	R	‘b0	SATA DRF2 SRAM0 fail signal
sata_bist2_fail_0	3	R	‘b0	SATA BIST2 SRAM0 fail signal
sata_drf_2_start_pause	2	R	‘b0	SATA DRF2 start pause signal
sata_drf_bist2_done	1	R	‘b0	SATA DRF2 done
sata_bist2_done	0	R	‘b0	SATA BIST2 done

Module::sata	Register::SATA_DUMMY_0_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FFC8

Name	Bits	R/W	Default	Comments
dummy_0	31..0	R/W	’h0000_0000	Dummy register,default:0

Module::sata	Register::SATA_DUMMY_1_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9803_FFCC

Name	Bits	R/W	Default	Comments
dummy_1	31..0	R/W	’hffffffff	Dummy register,default:1

1.1.2 SATA MAC IP Register (0x1803_F000~0x1803_F1FF)

[Note] SATA MAC IP register detail please go to see Appendix B.

Offset Address	Register Name and Description
0x00	CAP (HBA Capabilities Register) Type: RO Reset: See detailed description
0x04	GHC (Global HBA Control Register) Type: See detailed description Reset: 0x8000_0000
0x08	IS (Interrupt Status Register) Type: RW1C Reset: 0x0000_0000
0x0C	PI (Ports Implemented Register) Type: RO Reset: HwInit
0x10	VS (AHCI Version Register) Type: RO Reset: 0x0001_0100
0x14	CCC_CTL (Command Completion Coalescing Control) Type: RW Reset: See detailed description
0x18	CCC_PORTS (Command Completion Coalescing Ports) Type: RW Reset: 0x0000_0000
0x1C - 0x23	Reserved. Reset: 0
0x24	CAP2 (HBA Capabilities Extended Register) Type: RO Reset: 0x0000_0004
0x28 - 0x9F	Reserved. Reset: 0
0xA0	BISTAFR (BIST Activate FIS Register) Type: RO Reset: 0x0000_0000

Appendix D : SATA PHY register table

1.1. Register definition

Offset	Access	Tag	Description
0x00	R/W	ANA00	Analog Control Register
0x01	R/W	ANA01	Analog Control Register
0x02	R/W	ANA02	Analog Control Register
0x03	R/W	ANA03	Analog Control Register
0x04	R/W	ANA04	Analog Control Register
0x05	R/W	ANA05	Analog Control Register
0x06	R/W	ANA06	Analog Control Register
0x07	R/W	ANA07	Analog Control Register
0x08	R/W	ANA08	Analog Control Register
0x09	R/W	ANA09	Analog Control Register
0x0a	R/W	ANA0A	Analog Control Register
0x0b	R/W	ANA0B	Analog Control Register
0x0c	R/W	ANA0C	Analog Control Register
0x0d	R/W	ANA0D	Analog Control Register
0x0e	R/W	ANA0E	Analog Control Register
0x0f	R/W	ANA0F	Analog Control Register
0x10	R/W	DMR	Debug mode Register
0x11	R/W	BACR	Basic Control Register
0x12	R/W	IER	Interrupt Enable Register
0x13	R/W	BCSR	BIST Control/Status Register
0x14	R/W	BPR	Bist mode Pattern Register
0x15	R/W	BPNR2	BIST mode repeat number register 2
0x16	R/W	BFNR	BIST mode FTS ordered sets number register
0x17	R/W	BRNR2	BIST mode receive packet number register
0x18	R/W	BENR	BIST mode error number register

1.2. Register table

ANA00 (Address:0x00)

Bit	Name	R/W	Default	Description
0.15	REG_CDR_ACC2_MANUAL	R/W	1'B0	0: automatic mode 1: fore integral ki to generated wave
0.14:5	REG_CDR_ACC2_PERIOD	R/W	10'B1000000000	The period of the generated wave (integral ki)

0.4	REG_CDR_BYPASS_SDM_int	R/W	1'B0	0: automatic mode 1: fix the value of ST by manual
0.3	REG_CDR_RESET_SEL	R/W	1'b1	CDR reset selector "0": CLKREQB (Normal) "1": AFEN (Save power)
0.2			1'B0	
0.1	REG_CKREF_DBG_EN	R/W	1'B0	Debug test out enable 0: disable, 1: Enable
0.0	REG_CMU_BYPASS_PI	R/W	1'b0	When no fractional divider or SSC,bypass Phase Intepolator for CMU loop 0: including PI inside the loop 1: bypass PI inside the loop

ANA01 (Address:0x01)

Bit	Name	R/W	Default	Description
1.15:9	REG_EQ_DEFAULT[6:0]	R/W	7'b1110000	Initial value for Equalizer, Bit[1:0] are useless This register use binary code format, and will transform to Gray code format automatically to control Equalizer "00000" means min. AC gain, whereas "11111" means max. AC gain. Each code indicates 0.5dB AC Gain. Actual AC gain for "00000" depends on the value of REG_RX_EQ_DCGAIN[1:0]. The higher the DCGAIN, The lower the actual AC gain corresponding to "00000". We set initial value as max. to quarantee the eye-diagram can be enlarged in the beginning for a very lossy channel, and then leads to a proper value due to adaptation of Equalizer
1.8:6	REG_CDR_KI	R/W	3'b100	CDR KI selection
1.5:0	REG_CDR_KP[5:0]	R/W	6'b001000	

ANA02 (Address:0x02)

Bit	Name	R/W	Default	Description
2.15	REG_CDR_PI_M_MODE	R/W	1'B0	0: automatic mode 1: fix the value of ST by manual

2.14	REG_RST_SEL	R/W	1'b1	CDR_DEC output RCVBIT reset sel "1" : reset by reset_n "0" : no reset
2.13	REG_CDR_SQU_TRI	R/W	1'B1	Choose the generated wave of integral ki 0: generate the square wave 1: generate the triangle wave Note: only work when REG_CDR_ACC2_MANUAL = 1
2.12:10	REG_CDR_TESTOUT_SEL[2:0]	R/W	3'B000	CDR DEC test out enable
2.9	REG_CDR_TEST_EN	R/W	1'B0	CDR DEC test out enable
2.8	REG_CMU_CP_NEW_EN	R/W	1'B 0	CMU CP new mode selection 0: old mode 1: new mode
2.7	REG_CMU_FREQSEL	R/W	1'B0	CMU clock source selection 0: single end (NR in) 1: diff buffer in(analog buffer)
2.6	REG_CMU_LDO_MODESEL	R/W	1'B1	CMU LDO mode selsetion 0: PFD+ L2H => 3.3V 1: PFD+ L2H => Vldo
2.5			1'B0	
2.4	REG_RX_ACGAIN_SEL	R/W	1'b0	RX EQ ac gain code select: "1": new stage around '0': old stage by stage
2.3	REG_CMU_25MOUT_EN	R/W	1'B0	CMU 25MHz clock output enable
2.2	REG_CMU_CCO_BKVCO	R/W	1'B1	CMU CCO big kvco ebable
2.1	REG_CMU_CKREF_SEL	R/W	1'B1	CMU reference clock pre-divider selection 0: DIV4 1: bypass
2.0	REG_CMU_EN_CENTER_IN	R/W	1'b0	Enable center SSC "1" : Enable "0" : Disable no used for PCIe

ANA03 (Address:0x03)

Bit	Name	R/W	Default	Description
3.15:8	REG_TIMER_MAXHOLD[7:0]	R/W	8'b00100111	MAX HOLD timer setting, Each step : 512nsec, Default : 20usec (EQ stable time) => 39 steps => 00100111
3.7	REG_MAXHOLD_EN	R/W	1'b0	Enable signal for MAXHOLD function "1" : Enable "0" : Disable

3.6	REG_OOBS_DEBEN	R/W	1'b1	Debounce Enable "0" : Bypass OOBS Debounce "1" : Enable OOBS Debounce
3.5:1	REG_OOBS_SEN_VAL<4:0>	R/W	5'b11000	Set sensitivity reference voltage [4:0] Reference Voltage Vrp = 792.5 + 64*v<4> + 32*v<3> + 16*v<2> + 8*v<1> + 4*v<0> Vrn = 792.5 + 64*v<4>' + 32*v<3>' + 16*v<2>' + 8*v<1>' + 4*v<0>' (v<n>' = 1 – v<n>) Vth = SEN_VAL<4:0> - SEN_VAL<4:0>'
3.0	REG_CPHY_POR	R/W	1'b1	CPHY power-on selection 0: power-on = MAINPWR 1: power-on = MAINPWR & POW_CPHY

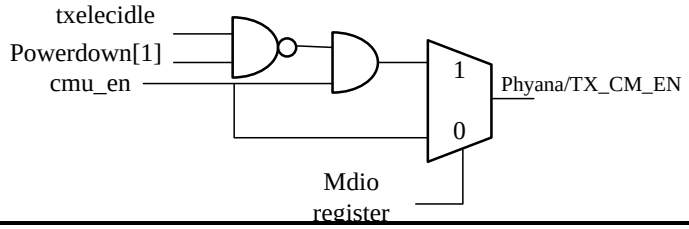
ANA04 (Address:0x04)

Bit	Name	R/W	Default	Description
4.15:14	REG_CMU_LDO_VREF [1:0]	R/W	2'b01	CMU LDO voltage selection 11: 2.2v 10: 2.1v 01: 2.0v 00: 1.9v
4.13	REG_CMU_EN_SSC	R/W	1'b1	Enable SSC function "1" : Enable "0" : Disable
4.12	REG_CMUEN_TOGGLE	R/W	1'b1	This REG and with CMU Enable « 1 » : OUT = CMU_EN « 0 » : OUT = 0
4.11:0	REG_CMU_FCODE_IN<11:0> (RLE0403 only)	R/W	12'b001011110101	Fractional code of loop divider (Controlled by CLK_MODE_SEL[1:0]) 12'd0 for SATA, no used for PCIe

ANA05 (Address:0x05)

Bit	Name	R/W	Default	Description
5.15:13		R/W	3'b001	
5.12	REG_EN_SATA	R/W	1'b1	TX SATA mode enable
5.11	REG_CMU_FCODE_IN<12> (RLE0403 only)	R/W	1'b1	Fractional code of loop divider bit[12]

5.10:3	REG_CMU_NCODE_IN<7:0> (RLE0403 only)	R/W	8'b01011010	Integer code of loop divider,real divider code is (Controlled by CLK_MODE_SEL[1:0]) 1.100MHz MODE: CK_REF_IN =100M, CMU_SEL_PREDIV=1' b1(PFD trength =50MHz), CMU_BYPASS_PI=1'b1 VCO frequency=50*2*(CMU_N_CODE[8:0] +2)=2.5GHz -> CMU_NCODE[7:0] = (Fvco / 2 / Fref-2) = 23 2.25MHz MODE: CK_REF_IN =25M, CMU_SEL_PREDIV=1' b0(PFD trength =25MHz), CMU_BYPASS_PI=1'b1 VCO frequency=25*2*(CMU_N_CODE[8:0] +2)=2.5GHz -> CMU_NCODE[7:0] = (Fvco / 2 / Fref -2) = 48 3.SSC MODE CK_REF_IN =12M, CMU_SEL_PREDIV=1'b0(PFD trength =24MHz), CMU_BYPASS_PI=1'b0, VCO frequency =12M*2*(CMU_N_CODE[7:0]+2 + CMU_F_CODE[12:0] / 8192)=2.5GHz ->若無 offset, CMU_NCODE[7:0] =102, CMU_FCODE[12:0] =1365 (Fvco=2.499996G) (N=Fvco / 2 / Fref -2, F = 4096*(Fvco / 2 / Fref – N -2)) ->若 offset=-5000ppm, CMU_N_CODE[7:0] =101, CMU_F_CODE[12:0] =5290 若正在展頻，且展頻三角波的 Fcode 爲 F_SSC，則此時 VCO 頻率爲： VCO frequency = Fref*2*(CMU_NCODE[7:0] + 2 + (CMU_F_CODE[12:0] + F_SSC)/ 8192) 此頻率即在 0~-5000ppm 中選擇(2.5G ~ 2.5G*0.995)
5.2:1	REG_CMU_PI_ISEL	R/W	2'B01	CMU PI current selection, 11: max, 00: min

5.0	REG_TX_CM_EN_sel	R/W	1'B0	1'b0：tx_cm_en = cmu_en 1'b1：when txelecidle = 1 and powerdown[1] = 1 ,tx_cm_en=0.Else, tx_cm_en = cmu_en 

ANA06 (Address:0x06)

Bit	Name	R/W	Default	Description
6.15:5	REG_CDR_INT_INIT	R/W	11'B0000 0000000	The initial vale of generated wave in integral ki.
6.4:0	REG_CMU_CP_ISEL[4:0]	R/W	5'B00011	CMU CP current select Icp=1.25u + 1.25u*<0> + 2.5u*<1> + 5u*<2> + 10u*<3> + 20u*<4>

ANA07 (Address:0x07)

Bit	Name	R/W	Default	Description
7.15:13	REG_LFPS_LPERIOD<2:0>	R/W	001b	The LFPS detect down limit = (LFPS_LPERIOD + 1) * 4ns R/W
7.12:10	REG_LFPS_HPERIOD<2:0>	R/W	011b	The LFPS detect up limit = (LFPS_HPERIOD + 10) * 4ns R/W
7.9:8	REG_LFPS_LAST<1:0>	R/W	10	The LFPS signal extended time = (LFPS_LAST + 1) * 4ns R/W
7.7:6	REG_CMU_PREDIV[1:0]	R/W	2'B00	CMU reference clock pre-divider selection 00: bypass 01: DIV2 10: DIV4 11: DIV8
7. 5			1'B0	
7.4	REG_CMU_SSC_ORDER	R/W	1'b0	SSC order selector "0" : 1 "1" : 2
7.3	REG_CMU_SSC_MODE	R/W	1'b0	SSC mode selector "0": ramp "1": square
7.2:0	REG_CMU_WEIGHT_SEL<2:0>	R/W	3'b000	STEP_IN<6:0> weighting selector

ANA08 (Address:0x08)

Bit	Name	R/W	Default	Description

8.15:4	REG_CMU_TBASE_IN<11:0>	R/W	12'B0011_0101_1001	SSC profile step number 12'd3031 for -0.5% down SSC for 100MHz no used for PCIe 1). 100MHz In 展頻三角波頻率 = 100M/CMU_TBASE_IN[11:0] 設 CMU_TBASE_IN[11:0] =12'd3031，展頻三角波頻率 = 32.992KHz 2). 25MHz In 展頻三角波頻率 = 25M/CMU_TBASE_IN[11:0] 設 CMU_TBASE_IN[11:0] =12'd759，展頻三角波頻率 = 32.9381KHz 3).24MHz In 展頻三角波頻率 = 24M/CMU_TBASE_IN[11:0] 設 CMU_TBASE_IN[11:0] =12'd729，展頻三角波頻率 = 32.9218KHz 注:CMU_TBASE_IN 最好不要是 2 的倍數，防止 Sigma-Delta pattern 太明顯。
8.3		R/W	1'b0	Reserved
8.2	REG_FORCE_RCVDET	R/W	1'b0	Control signal to select the detected result of receiver detection "1" : Always return "1" on the RXDET signal. "0" : Detected result comes from receiver detection.
8.1:0	REG_IBRXSEL<1:0>	R/W	2'b01	Tuning range of current sources for RX [1:0] Range 00 -12.5% 01 Normal 10 +12.5% 11 +25.0%

ANA09 (Address:0x09)

Bit	Name	R/W	Default	Description
9.15:14	REG_IBTXSEL<1:0>	R/W	2'b01	Tuning range of current sources for TX [1:0] Range 00 -12.5% 01 Normal 10 +12.5% 11 +25.0%

9.13:12	REG_OOBS_CALI<1:0>	R/W	2'b01	Set the unit current of CALIBER in OOBS blocks [1:0] Unit Current 00 50uA/4 01 50uA/5 10 50uA/5 11 50uA/6
9.11	REG_OOBS_CALSEL	R/W	1'b0	Selection of clock frequency for OOBS sensitivity calibration "1" : 25MHz "0" : 12.5MHz
9.10		R/W	1'b0	Reaerved
9.9	REG_OOBS_FORCECAL	R/W	1'b1	Control signal for forcing calibration of signal detector."1" -> "0" -> "1" will do one time of calibration.
9.8	REG_OOBS_FREQSEL	R/W	1'b0	Frequency selection for OOBS clock when this clock comes from CMU "1" : 125MHz "0" : 250MHz
9.7	REG_OOBS_NSQDLY	R/W	1'b0	Control signal of de-bouncing time for signal detector. "1" : two symbols of time. "0" : three symbols of time
9.6	REG_OOBS_RXIDLE_MANUAL	R/W	1'b0	RXIDLE selection 0: rxidle = #NSQ 1: rxidle = #NSQ & #LFPS_DET
9.5			1'B0	
9.4	REG_OOBS_SEL	R/W	1'b1	Select OOBS' operating mode "1" : Manual mode, controlled by REG_OOBS_SEN_VAL[4:0] "0" : Auto-calibration
9.3:0	REG_OOBS_SEN<3:0>	R/W	4'b1100	Set sensitivity reference voltage [3:0] Reference Voltage 0000 80mV 1000 90mV 1100 100mV 1110 110mV 1111 120mV

ANA0A (Address:0x0a)

Bit	Name	R/W	Default	Description
10.15	REG_RX_OFFSET_SEL	R/W	1'b1	Selection of enable signal for offset calibration "1" : pow_offset_k = #OOBS_CALEN .AND. PRSTB "0" : pow_offset_k = #OOBS_CALEN .AND. RXEN

10.14:12	REG_CMU_SR[2:0]	R/W	3'B011	CMU Rs selection Rs = 3 * REG<2:0>+3
10.11	REG_RX_EN_SELF	R/W	1'b0	Selection between normal operation and manual mode. Should be co-operated with FORCERUN. "1" : Manual mode "0" : Normal mode
10.10	REG_CMU_SC	R/W	1'B1	CMU Cp selection 0: small Cp 1: big Cp
10.9	REG_RX_EQ_SLICER_EN	R/W	1'b1	control register of slicer in eq filter. "1" : enable slicer, eqin = [-1,1] "0" : disable slicer, eqin = [-20,20]
10.8:7	REG_RX_EQ_GAIN<1:0>	R/W	2'b00	equalizer filter gain control. [1:0] EQ Gain 00 0.5 01 1 10 2 11 4
10.6	REG_RX_EQ_EN	R/W	1'B0	Hold equalizer output or not "0" : hold equalizer output (after RXEN+10us delay) "1" : equalizer normal operation Refer to REG_REV3[0]
10.5	REG_RX_EQ_SELREG	R/W	1'b0	equalizer output select "1" : use REG_FILTER_OUT[6:0] as output. "0" : use EQ's filtered output Refer to REG_REV0[15:9]
10.4:3		R/W	2'b00	
10.2	REG_RX_FORCERUN	R/W	1'b0	Enable bit of PLL and RX in self-testing mode. "1" : Enable "0" : Disable
10.1	~~CLK_MODE_SEL~~	R/W	1'B0	~~REFCLK input select: 11: REFCLK from SOC system XTal~~ ~~Others : REFCLK from USB3 APAD~~
10.0	~~REG_EQED_SEL~~	R/W	1'b0	1:use HB's new algorithm 0:old algorithm

ANA0B (Address:0x0b)

Bit	Name	R/W	Default	Description
11.15:14	REG_OOBS_CM[1:0]	R/W	2'B10	OOBS common mode voltage (USB3 RX input high-pass filter bias voltage) 00: 0.72V, 01: 0.78V, 10: 0.82V, 11: 0.87V
11.13:12	REG_OOBS_DM	R/W	2'B10	OOBS diff. mode voltage (sensitivities voltage) 00: 10mV, 01: 20m V, 10: 30m V, 11: 40m V

11.11:10	REG_OOBS_TYPE_SEL	R/W	2'B10	Reserve
11. 9			1'B0	
11.8:5	REG_RX_OFFSET_ADJR<3:0>	R/W	4'b1000	offset code when OFFSET_AUTO_K = 0.
11.4			1'B0	
11.3:2	REG_RX_OFFSET_RANGE<1:0>	R/W	2'b01	DC offset calibration tuning range select: [1:0] Ibp – Ibn 00 -40u ~ + 35u 01 -80u ~ + 70u 10 -80u ~ + 70u 11 -160u ~ + 140u
11.1	REG_RX_PIENSEL	R/W	1'b0	Select PIEN as "1": RXEN "0": AFEN
11.0	REG_RX_PS_AFE	R/W	1'b1	Enable signal for AFE's power down mode "1" : Power-down AFE when RX is in IDLE state "0" : AFE is always ON

ANA0C (Address:0x0c)

Bit	Name	R/W	Default	Description
12.15	REG_RX_PSAVE_SEL	R/W	1'b1	Close RX clock or not when RXIDLE "0": CLKREQB (Normal) "1": AFEN (Save power)
12.14	REG_RX_SEL_RXIDLE	R/W	1'b1	Select NSQ_DLY and NSQ_CDR_D signal for receiver "1" : Signal = VOUT_CDR_D .OR. (U3_ISO1 .NOR. PDOWN) "0" : Signal = VOUT_CDR_D
12.13:12	REG_LFPS_DBG[1:0]	R/W	2'b00	Reserve
12.11:10	REG_LFPS_IHF_SEL[1:0]	R/W	2'b00	Reserve
12.9:8	REG_LFPS_ILF_SEL[1:0]	R/W	2'b00	Reserve
12.7:6	REG_LFPS_VRBHF_SEL[1:0]	R/W	2'b00	Reserve
12.5:4	REG_LFPS_VRBLF_SEL[1:0]	R/W	2'b00	Reserve

12.3:2	REG_RXDSEL<1:0>	R/W	2'b00	Threshold value of Rx detection function [1:0] Cap 00 0.03 nF 01 1.9 nF 10 7.5 nF 11 30 nF Above value is only for reference. Actual value is not guaranteed and will change by process.
12.1			1'B0	
12.0			1'B0	

ANA0D (Address:0x0d)

Bit	Name	R/W	Default	Description
13.15	REG_RX_ENKOFFSET	R/W	1'B1	Enable RX offset calibration (RX offset bias circuit control)
13.14	REG_RX_LPFEN_MANUAL	R/W	1'B1	Gating CDR digital LPF when REG_RX_RESET_MANUAL = 1, REG_LPFEN_MANUAL =0, CDR digital LPF always = 0
13.13	REG_RX_OFFSET_AUTOK	R/W	1'B1	Use RX offset auto calibration result 1: use auto K value 0: force offset value = REG_RX_OFFSET_ADJR<3:0> (0 x0B(8:5))
13.12:11			2'B01	
13.10	REG_RX_RESET_MANUAL	R/W	1'B1	CDR digital LPF enable = RXEN and REG_RESET_MANUAL MUX out
13.9	REG_RX_SEL_IBN	R/W	1'B1	RA_AMP current type selection 0: constant Gm bias 1 : conventional
13.8:7	REG_RX_SPDSEL[1:0]	R/W	2'B10	CPHY speed selection 11: reserved 10: 5G/6G 01: 2.5G/3G 00: 1.25G/1.5G
13.6	REG_RX_TEST_EN	R/W	1'B0	RX_TOP debug signal test out enable
13.5:2	REG_RX_Z0_RX[3:0]	R/W	4'B0111	RX termination res value selection 0000: 59ohm ~ 0111: 45ohm ~ 1111: 36ohm @TT
13.1			1'B0	
13.0	REG_TX_EN_TEST	R/W	1'b0	Control signal for enabling testing outputs. "1" : enable "0" : disable and all testing outputd are LOW

ANA0E (Address:0x0e)

Bit	Name	R/W	Default	Description
14.15	REG_TX_EN_VCM_RES	R/W	1'b0	Select signal for TX output VCM "1" : VDDTX*(12/24) "0" : VDDTX*(13/24)
14.14			1'B0	
14.13:12	REG_TX_SEL_VCM<1:0>	R/W	2'b10	Rx detector vref select signal [1:0] Vref(V) 00 VDDTX*(15/24) 01 VDDTX*(16/24) 10 VDDTX*(17/24) 11 VDDTX*(18/24)
14.11:8	REG_TX_LFPS[3:0]	R/W	3'B0000	Selection of TX LFPS's delay time Delay time get larger if LFPS[1:0] is larger LFPS[3:2] is output floating.
14.7	REG_TXCKRD_DUTY_SEL	R/W	1'B0	TXCKRD Duty Cycle SEL [0] Duty Cycle 0 40% 1 60%
14.6	REG_TX_BEAEN	R/W	1'B0	Force TX to transmit Beacon. "1" : Enable "0" : Disable
14.5	REG_TX_EN_SEL	R/W	1'B0	1: Enable Rx detector 0: Disable Rx detector
14.4	REG_TX_MODE	R/W	1'B0	1: opab mode 0: cmfb mode
14.3	TX_CM_ON_PCIE	R/W	1'B0	
14.2	TX_CM_EN_USB	R/W	1'B0	
14.1:0			2'B00	

ANA0F (Address:0x0f)

Bit	Name	R/W	Default	Description
15.15:12	REG_CDR_KP1[2:0]	R/W	3'b000	
15.11:10	REG_CDR_KP2[2:0]	R/W	3'b000	
15.9:3		R/W		
15.2:0	REG_BG_SEL[2:0]	R/W	3'b000	Bandgap voltage selection

ANA10 (Address:0x10)

Bit	Name	R/W	Default	Description
		R/W	00	
16.13	reg_dphy_top_cfg 0[13] (reg_rst_delay)	R/W	1	0 : reset w/o synchronization, 1 : reset w/i synchronization
16.12	reg_dphy_top_cfg 0[12] (reg_deglitch)	R/W	1	0 : w/o clock deglitch, 1 : w/I clock deglitch
16.11	reg_dphy_top_cfg 0[11] (reg_cfg_rstn)	R/W	1	0 : soft reset, 1 : normal
16.10	reg_dphy_top_cfg 0[10] (reg_clk_sel)	R/W	0	0 : normal mode, 1 : loopback mode
16.9:8	reg_dphy_top_cfg 0[9:8] (reg_spdcg_dly)	R/W	01	speed change delay for synchronization circuit
16.7	reg_dphy_top_cfg 0[7] (reg_lane_swap_sel)	R/W	0	0 : SATA @ lane 0, 1 : SATA @ lane 1 , don't use in RL6421
16.6:0		R/W	0000000	

ANA11 (Address:0x11)

Bit	Name	R/W	Default	Description
17.15:2		R/W	0000000 0000000	
17.1	REG_USB_PCIE_SEL	R/W	1'b1	
17.0		R/W	0	

ANA12(Address:0x12)

Bit	Name	R/W	Default	Description
18.15:10		R/W	000000	
18.9:0	reg_dphy_top_cfg 1[9:0] (reg_start_delay)	R/W	0001100 100	delay ber_notify after calib_ok

ANA13 (Address:0x13)

Bit	Name	R/W	Default	Description

19.15:4	Reg_sata_cfg0[15:4]	R/W	0000000 00000	
19.3	reg_sata_cfg0[3] (reg_beacon_en)	R/W	0	(PCIE only)
19.2	reg_sata_cfg0[2] (reg_det_en)	R/W	0	(PCIE only)
19.1	reg_sata_cfg0[1] (reg_detect)	R/W	0	(PCIE only)
19.0	reg_sata_cfg0[0] (reg_bist_sel)	R/W	0	(0 : normal mode, 1 : bist enable)

ANA14 (Address:0x14)

Bit	Name	R/W	Default	Description
20.15:13	Reg_sata_cfg1[15:13]	R/W	000	
20.12	reg_sata_cfg1[12] (reg_spd_sel)	R/W	1	0 : spd_sel from MAC, 1 : spd_sel from reg
20.11:10	reg_sata_cfg1[11:10] (reg_debug)	R/W	00	debug selection
20.9	reg_sata_cfg1[9] (reg_comdet_dis)	R/W	0	0 : normal mode, 1 : disable comma detection
20.8	reg_sata_cfg1[8] (reg_clk_sel)	R/W	0	don't use in RL6421
20.7:5	**reg_sata_cfg1[7:5] (reg_comsel)**	R/W	011	000: 3 com det 001: 4 com det 010: 6 com det 011: 8 com det 100: 10 com det 101: 12 com det 110: 14 com det 111: 16 com det
20.4	reg_sata_cfg1[4] (reg_lpk)	R/W	0	0 : normal mode of comma detect, 1 : debug mode of comma detect
20.3	reg_sata_cfg1[3] (reg_bit20_sel)	R/W	1	1 : 20-bit mode
20.2		R/W	0	
20.1:0	reg_sata_cfg1[1:0] (reg_spd_sel)	R/W	00	speed sel of reg

ANA15 (Address:0x15)

Bit	Name	R/W	Default	Description

21.15:12	reg_sata_cfg2[15:12] (reg_oobs_rstb_sel)	R/W	0001	bit3 : force to disable oobs, bit2 : disable oobs @ slumber, bit1 : disable oobs @ partial, bit0 : disable oobs @ devslp
21.11:8	reg_sata_cfg2[11:8] (reg_ckwr_en_sel)	R/W	0111	bit3 : force to disable clkwr_en, bit2 : disable @ slumber, bit1 : disable @ partial, bit0 : disable @ devslp
21.7:4	reg_sata_cfg2[7:4] (reg_cm_om_sel)	R/W	0001	bit3 : force to disable tx_cm_on, bit2 : disable @ slumber, bit1 : disable @ partial, bit0 : disable @ devslp
21.3:0	reg_sata_cfg2[3:0] (reg_pow_sata)	R/W	0111	don't use in RL6421

ANA16 (Address:0x16)

Bit	Name	R/W	Default	Description
22.15:12	reg_sata_cfg3[15:12] (reg_cmu_en_sel)	R/W	0111	bit3 : force to disable cmu_en, bit2 : disable @ slumber, bit1 : disable @ partial, bit0 : disable @ devslp
22.11:8	reg_sata_cfg3[11:8] (reg_pdown_sel)	R/W	0111	bit3 : force to enable pdown, bit2 : enable @ slumber, bit1 : enable @ partial, bit0 : enable @ devslp
22.7:4	reg_sata_cfg3[7:4] (reg_rx_en_sel)	R/W	0111	bit3 : force to disable rx_en, bit2 : disable @ slumber, bit1 : disable @ partial, bit0 : disable @ devslp
22.3:0	reg_sata_cfg3[3:0] (reg_rx50_link_sel)	R/W	0000	bit3 : force to disable rx50_link, bit2 : disable @ slumber, bit1 : disable @ partial, bit0 : disable @ devslp

ANA17 (Address:0x17)

Bit	Name	R/W	Default	Description
23.15:9	Reg_sata_cfg4[15:9]	R/W	0000000	
23.8	**reg_sata_cfg4[8] (reg_fld_rst_biterr_sel)**	R/W	0	1: disable fld_rst_function 0:enable fld_rst function
23.7:3	**reg_sata_cfg4[7:3] (reg_enable_cnt)**	R/W	00100	After enable_cnt start to bit error check Time unit : clk_wr/160
23.2:1	**reg_sata_cfg4[2:1] (reg_deglitch_sel)**	R/W	10	00:no deglitch 01: use bit error & pm_ack to deglitch rxidle 10: use bit error to deglitch rxidle 11: use pm_ack to deglitch rxidle
23.0	**reg_sata_cfg4[0] (reg_biterr_en)**	R/W	1	1: Bit error check enable 0:disable bit error check

ANA18 (Address:0x18)

Bit	Name	R/W	Default	Description
24.15:12	Reg_sata_cfg5[15:12]	R/W	0000	
24.11:8	**reg_sata_cfg5[11:8] (reg_counter_num)**	R/W	1000	Reset bit error counter every reg_counter_num
24.7:4	**reg_sata_cfg5[7:4] (reg_err_bit_num)**	R/W	1000	When bit error number = reg_err_bit_num reset fld_rst
24.3:0	**reg_sata_cfg5[3:0] (reg_delay_cnt)**	R/W	1000	Rxidle deglitch state after reg_delay_cnt return to 00

ANA19(reserved register: 0x19)

Bit	1.1.2.1.1.1.1 Name	R/W	Default	Description
25.15:9	REG_FILTER_OUT<6:0>	R/W	7'b1110000	Adpative EQ 的初始值 Refer to ANA0A
25.8:3	REG_TX_RESERVED[5:0]	R/W	6'B000000	Its reserved, no connect.
25.2	REG_RX_DLYNSQ_SEL	R/W	1'b1	Selection of NSQ's delay time "1" : Clock for delay counter is 250MHz/4 "0" : Clock for delay counter is 250MHz/2
25.1			1'b0	
25.0		R/W	1'B0	

ANA1A(reserved register: 0x1a)

Bit	1.1.2.1.1.1.2 Name	R/W	Default	Description
15:14			2'b00	
26.13:4	REG_LFPS_CNT[9:0]	R/W	10'b0100100110	[13:4] cmu_en=0, LFPS counter= REG_RESERVED[13:9] delay=(counter+2.5)*20ns cmu_en=1, lFPS counter = REG_RESERVED[8:4] delay=(counter+2.5)*32ns
3:0		R/W	4'b0000	

ANA1B(reserved register: 0x1b)

Bit	1.1.2.1.1.1.3 Name	R/W	Default	Description
27.15:0	REG_RX_RESERVED[15:0]	R/W	16'B1111111100000000	Bit<0> for REG_CDR_CLK_INV Bit<1> for REG_CDR_ST_MODE

ANA1C (Address:0x1c)

Bit	Name	R/W	Default	Description

28.15	Inverse_d2analog	R/W	0	
28.14	Prbs_en	R/W	0	
28.13:12	Prbs_sel[1:0]	R/W	00	
28.11	Prbs_reverse	R/W	0	
28.10	Mdio_pattern_en	R/W	0	
28.9:0	Mdio_pattern[19:10]	R/W	0000000000	

ANA1D (Address:0x1d)

Bit	Name	R/W	Default	Description
29.15:6	Mdio_pattern[9:0]	R/W	0000000000	
29.5	Inverse_rxdata	R/W	0	
29.4:1	Reg_inbuf_num[3:0]	R/W	0000	
29.0	Loopback_en	R/W	0	

ANA1E (Address:0x1e)

Bit	Name	R/W	Default	Description
30.15	Reg_fofost_clr	R/W	0	
30.14:12	Debug_sel[2:0]	R/W	000	
30.11	prbs_clear	R/W	0	
30.10	prbs_sync	R		
30.9	prbs_fail	R		
30.8:0				

ANA1F (Address:0x1f)

Bit	Name	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		

ANA20 (Page1, 0x20)

Bit	1.1.2.1.1.1.4 name	R/W	Default	Description
0.15	RX_EQ_training	R/W	1'b1	1'B1:gate_usb3_rx_eq_trainging

	_SEL			1’B0:usb3_rx_eq_trainging
0.14	REG_CDR_SEL	R/W	1’b1	Selection of RX’s Reset mechanism “1” : RX Receiver is reset by PRSTB, and current mirror for RX is controlled by PRSTB .OR. CMU_EN “0” : RX Receiver is reset by RXEN .AND. CKUSABLE, and current mirror for RX is controlled by CMU_EN
0.13			1’B0	
0.12	REG_RXDET_DELAY	R/W	1’b1	0：Original 1：Delay rxdetect
0.11:10	REG_RXDET_DELAY	R/W	2’b01	00：25us 01：50us 10：100us 11：200us
0.9		R/W	1’B0	
0.8	REG_TX_CLK_STOP_EN	R/W	1’b0	enable clock gating during electrical idle for power saving, high active
0..7:4	REG_TXDRV_DAC_BC[3:0]	R/W	4’B1010	Beacon LFPS Amplitude control, LFPS Amplitude is sum of REG_TXDRV_DAC_BC[3:0]+REG_TXDRV_DAC_POST0_BC[3:0]+REG_TXDRV_DAC_POST1_BC[3:0]. Default Vpp=1V
0.3:0	REG_TXDRV_DAC_DAT	R/W	4’B1010	Normal operation Amplitude control, Amplitude is sum of REG_TXDRV_DAC[3:0]+REG_TXDRV_DAC_POST0[3:0]+REG_TXDRV_POST1[3:0]. Default Vpp=1V

ANA21 (Page1, 0x21)

Bit	1.1.2.1.1.1.5 a m e	R/W	Default	Description
1.15:12	REG_TXDRV_DAC_POST0[3:0]	R/W	4’B1000	Normal operation Amplitude control
1.11:8	REG_TXDRV_DAC_POST0_BC[3:0]	R/W	4’B1000	Beacon LFPS Amplitude control
1.7:4	REG_TXDRV_DAC_POST1[3:0]	R/W	4’B1010	Normal operation Amplitude control
1.3:0	REG_TXDRV_D	R/W	4’B1010	Beacon LFPS Amplitude control

	AC_POST1_BC[3:0]			

ANA22 (Page1, 0x22)

Bit	1.1.2.1.1.1.6 Name	R/W	Default	Description
2.15:6	REG_TX_DEEMP_EN[9:0]	R/W	10'B0000000001	Deemphasis enable, bits [4:0] is available. Default 3.5dB 5'b00001, bits[9:5] are no connect.
2.5:4	REG_TX_IDLE_DLY_SEL[1:0]	R/W	2'B01	Idle signal delay control, [00]=1T, [01]=2T, [10]=3T
2.3:2			2'B00	
2.1	REG_RX_BERCHK_SEL	R/W	1'b1	Selection of BER checker function "1" : BER checker is turned on if CALIB_OK = 1 and received data is not LFPS patterns "0" : BER checker is turned on by BER_NOTIFY signal
2.0	REG_LFPS_DEBEN	R/W	1'b1	Selection of debouncing function in LFPS detector "1" : Enable "0" : Disable

ANA23 (Page1, 0x23)

Bit	1.1.2.1.1.1.7 Name	R/W	Default	Description
3.15:12	REG_TX_TERM	R/W	4'B1010	TX terminal resistance setting. Default 50ohm 4'B0000= 1078ohm 4'B 0001= 360ohm 4'B 0010= 216ohm 4'B 0011= 154ohm 4'B 0100= 120ohm 4'B 0101= 98ohm 4'B 0110= 83ohm 4'B 0111= 72ohm 4'B 1000= 63ohm 4'B 1001= 57ohm 4'B 1010= 51.3ohm (Default) 4'B 1011= 46.9ohm 4'B 1100= 43.1ohm 4'B 1101= 40ohm 4'B 1110= 37.2ohm

				4’B 1111=34.8ohm
3.11	REG_TX_TERM_OFF_SEL	R/W	1’B1	TX terminal resistance will set to 1k during LFPS signal for power saving. Low active.
3. 10:8	REG_TX_VCM_CTRL	R/W	3’B011	Commom mode Voltage setting, default 500mV 3’B000=1/4*Vin 3’B001=1/3*Vin 3’B010=5/12*Vin 3’B011=1/2*Vin (Dfault) 3’B100=7/12*Vin 3’B101=2/3*Vin 3’B110=3/4*Vin 3’B111=5/6*Vin
3. 7:5	REG_TX_VREF_CTRL	R/W	3’B011	**CMFB** reference voltage, default 250mV 3’B000=100mv 3’B001=150mv 3’B010=200mv 3’B011=250mv (Dfault) 3’B100=300mv 3’B101=350mv 3’B110=400mv 3’B111=450mv **OPAB** reference voltage, default 500mV 3’B000=650mv 3’B001=600mv 3’B010=550mv 3’B011=500mv (Dfault) 3’B100=450mv 3’B101=400mv 3’B110=350mv 3’B111=300mv
3. 4		R/W	1’B0	
3. 3:0	REG_RX_PI_IBSEL[3:0]	R/W	4’B0110	RX CDR PI bias current selection

ANA24 (Page1, 0x24)

Bit	1.1.2.1.1.1.8 a m e	R/W	Default	Description
		R/W		
4..14	Pow_sel	R/W	1	1: from POW_SATA 0: tie 1
		R/W		
		R/W		

ANA25 (Page1, 0x25)

Bit	1.1.2.1.1.1.9 a m e	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		

ANA26 (Page1, 0x26)

Bit	1.1.2.1.1.1.1(a m e	R/W	Default	Description
6.15:14		R/W		
6.13:12	REG_TX_PDOWN_DLY_SEL[1:0]	R/W	2'B00	
6.11	REG_TX_SER_STOP_EN	R/W	1'B0	
6.10:9	REG_RX_EQ_IBSEL[1:0]	R/W	2'b10	
6.8:7	REG_TESTOUT_SEL	R/W	2'b00	Test out selection. "1" : select DEBUG_OUT_L; "0" : select DEBUG_OUT_H.
6.6	REG_CDR_CLK_INV	R/W	1'b0	
6.5	REG_CDR_DYNKP_EN	R/W	1'b0	
6.4	REG_CDR_DLPF_EN	R/W	1'b0	Enable signal of CDR's digital LPF "1" : Enable "0" : Disable digital LPF, but data synchronization and adaptive EQ should be active
6.3	REG_CDR_ST_DSEL	R/W	1'b1	
6.2	REG_CDR_ST_MODE	R/W	1'b0	
6.1:0	REG_RX_EQ_	R/W	2'b10	equalizer filter gain control.

	DCGAIN<1:0>			[1:0] EQ DC Gain 00 -2.2dB 01 5.2dB 10 12.5dB 11 19.9dB

ANA27 (Page1, 0x27)

Bit	1.1.2.1.1.1.11 ame	R/W	Default	Description
7.15		R/W	1‘b0	
7.14		R/W	1‘b0	
7.13	Rxidle_select	R/W	1‘b0	Select rxidle_sel= (~calib_ok) “0” rxidle_sel= (~calib_ok) “1” rxidle_sel= rxidle_sel_pre
7.12:0	REG_CMU_STEP_IN<12:0>	R/W	’13’B0100 0_10010001	SSC profile per-step delta code, (Controlled by CLK_MODE_SEL[1:0]) CMU_STEP_IN[6:0] = 展頻深度 * (CMU_N_CODE[7:0] + 2 + (CMU_F_CODE[12:0] / 8192)) * 2 ^19 / (CMU_TBASE_IN[11:0] / 2) 對於 SATA mode 來說， 若展頻深度-0.5%， CMU_TBASE_IN[11:0] =12’d1517 @Fin 100M, Fpfd 50M, Fssc 33K， CMU_NCODE_IN[7:0] = 23， CMU_FCODE_IN[7:0] = 0 則 CMU_STEP_IN[5:0] = 5。

ANA28 (Page1, 0x28)

Bit	1.1.2.1.1.1.12 ame	R/W	Default	Description
8.15:11	REG_EQ_UPPER_LIMIT[4:0]	R/W	5’b11111	eq ac gain auto mode maximum limit
8.10:6	REG_EQOUT_OFFSET[4:0]	R/W	5’b00000	eq ac gain offset add
8.5		R/W	1‘b0	
8.:4:0	REG_TIMER_EQ	R/W	5‘b00010	

ANA29 (Page1, 0x29)

Bit	1.1.2.1.1.1.13 Name	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		

ANA2A (Page1, 0x2a)

Bit	1.1.2.1.1.1.14 Name	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		

ANA2B (Page1, 0x2b)

Bit	1.1.2.1.1.1.15 Name	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		

ANA2C (Page1, 0x2C)

Bit	1.1.2.1.1.1.16 Name	R/W	Default	Description
12.15:0	REG_CDR_ST_M_VALUE[31:16]	R/W	16'B1111111111111111	The value of ST in manual mode

ANA2D (Page1, 0x2D)

Bit	1.1.2.1.1.1.17 Name	R/W	Default	Description
13.15:0	REG_CDR_ST_	R/W	16'B111	The value of ST in manual mode

	M_VALUE[15:0]		1111111111111	

ANA2E (Page1, 0x2E)

Bit	1.1.2.1.1.1.18 Name	R/W	Default	Description
14.15:11	REG_CDR_TIMER_BER[4:0]	R/W	5'B00000	The timer count of BER_NOTIFY
14.10:6	REG_CDR_TIMER_EQ[4:0]	R/W	5'B00000	The timer count of EQ
14. 5:1	REG_CDR_TIMER_LPF[4:0]	R/W	5'B00000	The timer count of LPF
14. 0		R/W		

ANA2F (Page1, 0x2f)

Bit	1.1.2.1.1.1.19 Name	R/W	Default	Description
		R/W		
		R/W		
		R/W		
		R/W		