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RTD1296DB-VA1-CG
RTD1296DC-VA1-CG
RTD1296PB-VA1-CG

4K UHD MULTIMEDIA SOC WITH AP ROUTER ENGINE AND HIGH-SPEED INTERFACES; 10/100/1000M ETHERNET, HDMI, USB3.0, SATA, PCIE, SDIO, AND DTV

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTD1296 controller ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2016/03/28	First release.
1.1	2016/04/13	Revised Table 3 Recommended Operating Conditions, page 35 (CPU_DVS, GPU_DVS, MEM_VDD). Revised section 32 Ordering Information, page 84.
1.2	2016/04/29	Revised Table 1 Pin Descriptions, page 8 (Pins R9, T19, U19, V19, AA9, AA11, AB9, AB11, AB12, AC5, AC8, AD6, AD7, AE5, AF1, AF2, AF5, AG1, AH1). Revised Table 3 Recommended Operating Conditions, page 35 (CPU_DVS, GPU_DVS, MEM_DVS).
1.3	2016/06/02	Removed Mobile High-Definition Link (MHL) data. Corrected minor typing errors. Revised section 8.8 Power-On Sequence, page 39. Revised section 32 Ordering Information, page 84.
1.4	2016/06/30	Corrected minor typing errors. Revised section 8.7 Thermal Considerations, page 38. Added Table 10 Power-On Reset Trigger Level, page 40. Added section 14.11 DC Fan Control, page 56. Revised section 32 Ordering Information, page 84.
1.5	2016/08/11	Corrected minor typing errors. Revised pin V1 (RST_OUT) description. Revised Table 8 Thermal Parameters for the RTD1296, page 38. Added Table 9 Power-On Sequence Duration, page 39.
1.6	2017/01/26	Revised Table 1 Pin Descriptions, page 8 (Pins T1, T2, AA28, AC1, AC2, AD4). Revised Table 3 Recommended Operating Conditions, page 35 (CPU_DVS, GPU_DVS). Revised section 9.1 DDR3/DDR4 Controller Unit, page 41 (Added 'Supports Scrambling').

Table of Contents

1. GENERAL DESCRIPTION 1

2. FEATURES 2

3. SYSTEM APPLICATIONS DIAGRAM 4

4. BLOCK DIAGRAM 5

5. PIN ASSIGNMENTS 6

5.1. PACKAGE IDENTIFICATION 6
5.2. PIN ASSIGNMENTS (BOTTOM VIEW) 7

6. PIN DESCRIPTIONS 8

7. LICENSES 34

8. SYSTEM GLOBAL RESOURCES 35

8.1. ABSOLUTE MAXIMUM RATINGS 35
8.2. RECOMMENDED OPERATING CONDITIONS 35
8.3. POWER MANAGEMENT 36
8.4. POWER RIPPLE 37
8.5. CRYSTAL REQUIREMENTS 37
8.6. RESET, CLOCK, AND PLL 38
8.7. THERMAL CONSIDERATIONS 38
8.8. POWER-ON SEQUENCE 39

9. DDR CONTROLLER UNIT 41

9.1. DDR3/DDR4 CONTROLLER UNIT 41
9.1.1. Features 41
9.1.2. DCU Block External Pin Description 41
9.2. LPDDR2/LPDDR3 CONTROLLER UNIT 43
9.2.1. Features 43
9.2.2. LPDDR2/LPDDR3 Block External Pin Description 43
9.3. DCU BLOCK PIN MUX TABLE 44

10. FLASH CONTROLLER 46

10.1. FEATURES 46
10.2. SERIAL FLASH BLOCK EXTERNAL PIN DESCRIPTION 46
10.3. NAND FLASH BLOCK EXTERNAL PIN DESCRIPTION 47
10.4. BOOT DEVICE SELECTION 47

11. EMMC CONTROLLER 48

11.1. FEATURES 48
11.2. EMMC BLOCK EXTERNAL PIN DESCRIPTION 48
11.3. NAND/EMMC PIN MUX DESCRIPTION 48

12. GENERAL SPI INTERFACE 49

12.1. FEATURES 49
12.2. GENERAL SPI EXTERNAL SIGNAL DESCRIPTION 49

13. HIGH-SPEED UART 50

13.1. FEATURES 50
13.2. HIGH-SPEED UART MODULE EXTERNAL PIN DESCRIPTION 50

14. PERIPHERALS 51

14.1. GENERAL PURPOSE I/O 51
14.2. UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER 51
14.2.1. Features 51
14.2.2. UART Block External Pin Description 51
14.3. I2C SERIAL INTERFACE 52
14.3.1. Features 52
14.3.2. I2C Block External Pin Description 52
14.4. INFRARED RECEIVER CONTROLLER 53
14.4.1. Features 53
14.4.2. IR RX Block External Pin Description 53
14.5. INFRARED TRANSMITTER CONTROLLER 53
14.5.1. Features 53
14.5.2. IR TX Block External Pin Description 53
14.6. TIMER CONTROL 54
14.6.1. Features 54
14.7. REAL TIME CLOCK 54
14.7.1. Features 54
14.7.2. RTC Block External Pin Description 54
14.8. LSADC (LOW SPEED ADC) 55
14.9. PWM (PULSE WIDTH MODULATION) 55
14.10. SMART CARD INTERFACE 55
14.10.1. Features 55
14.10.2. Smart Card Controller External Pin Description 55
14.11. DC FAN CONTROL 56
14.11.1. Features 56
14.11.2. DC Fan Control External Pin Description 56
14.11.3. Typical 4-Wire Fan Interface 56

15. TV ENCODER 57

15.1. FEATURES 57
15.2. TV ENCODER ANALOG OUTPUT INTERFACE 57

16. HDMI TRANSMITTER 58

16.1. FEATURES 58
16.2. HDMI BLOCK EXTERNAL PIN DESCRIPTION 59

17. HDMI RECEIVER 60

17.1. FEATURES 60
17.2. HDMI RECEIVER BLOCK EXTERNAL PIN DESCRIPTION 60

18. AUDIO-IN INTERFACE 61

18.1. FEATURES 61
18.2. AUDIO EXTERNAL SIGNAL DESCRIPTIONS 62

19. AUDIO-OUT INTERFACE 63

19.1. FEATURES 63
19.2. AUDIO EXTERNAL SIGNAL DESCRIPTIONS 64

20. SATA CONTROLLER 65
20.1. FEATURES 65
20.2. SATA BLOCK EXTERNAL PIN DESCRIPTION 66
20.3. TYPICAL SATA APPLICATION 66
21. PCI EXPRESS 1.1 67
21.1. FEATURES 67
21.2. PCI EXPRESS BLOCK EXTERNAL PIN DESCRIPTION 67
21.3. TYPICAL PCI EXPRESS 1.1 APPLICATION 67
22. PCI EXPRESS 2.0 68
22.1. FEATURES 68
22.2. PCI EXPRESS 2.0 BLOCK EXTERNAL PIN DESCRIPTION 68
22.3. TYPICAL PCI EXPRESS 2.0 APPLICATION 68
23. GIGABIT ETHERNET CONTROLLER 69
23.1. FEATURES 69
23.2. ETHERNET 10/100/1000M BLOCK EXTERNAL PIN DESCRIPTION 69
23.3. TYPICAL GIGABIT ETHERNET APPLICATION 70
24. HW NAT 70
24.1. FEATURES 70
24.2. NAT BLOCK EXTERNAL PIN DESCRIPTION 71
24.3. TYPICAL GIGABIT ETHERNET APPLICATION 73
25. USB 2.0/USB 3.0 HOST/DEVICE CONTROLLER 75
25.1. FEATURES 75
25.2. USB BLOCK EXTERNAL PIN DESCRIPTION 76
26. TRANSPORT MODULE 77
26.1. FEATURES 77
26.2. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 77
27. CARD READER CONTROLLER 78
27.1. FEATURES 78
27.2. CARD READER BLOCK EXTERNAL PIN DESCRIPTION 78
28. LVDS (FLAT PANEL DISPLAY LINK) 79
28.1. FEATURES 79
28.2. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 79
29. DISPLAYPORT 80
29.1. FEATURES 80
29.2. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 80
30. SOLDERING REFLOW PROFILE 81
31. MECHANICAL DIMENSIONS 82
31.1. MECHANICAL DIMENSIONS NOTES 83
32. ORDERING INFORMATION 84

List of Tables

TABLE 1. PIN DESCRIPTIONS 8
TABLE 2. POWER SUPPLY SPECIFICATION 35
TABLE 3. RECOMMENDED OPERATING CONDITIONS 35
TABLE 4. DC CHARACTERISTICS 36
TABLE 5. POWER RIPPLE 37
TABLE 6. CRYSTAL REQUIREMENTS FOR THE RTD1296 37
TABLE 7. SYSTEM GLOBAL RESOURCES EXTERNAL PIN DESCRIPTION 38
TABLE 8. THERMAL PARAMETERS FOR THE RTD1296 38
TABLE 9. POWER-ON SEQUENCE DURATION 39
TABLE 10. POWER-ON RESET TRIGGER LEVEL 40
TABLE 11. DCU BLOCK EXTERNAL PIN DESCRIPTION 41
TABLE 12. LPDDR2/LPDDR3 BLOCK EXTERNAL PIN DESCRIPTION 43
TABLE 13. DCU BLOCK EXTERNAL PIN MUX TABLE 44
TABLE 14. SERIAL FLASH BLOCK EXTERNAL PIN DESCRIPTION 46
TABLE 15. NAND FLASH BLOCK EXTERNAL PIN DESCRIPTION 47
TABLE 16. BOOT DEVICE SELECTION 47
TABLE 17. EMMCREADER BLOCK EXTERNAL PIN DESCRIPTION 48
TABLE 18. NAND/EMMC PIN MUX DESCRIPTION 48
TABLE 19. GENERAL SPI EXTERNAL SIGNAL DESCRIPTION 49
TABLE 20. HIGH-SPEED UART MODULE EXTERNAL PIN DESCRIPTION 50
TABLE 21. UART BLOCK EXTERNAL PIN DESCRIPTION 51
TABLE 22. I2C BLOCK EXTERNAL PIN DESCRIPTION 52
TABLE 23. IR RX BLOCK EXTERNAL PIN DESCRIPTION 53
TABLE 24. IR TX BLOCK EXTERNAL PIN DESCRIPTION 53
TABLE 25. RTC BLOCK EXTERNAL PIN DESCRIPTION 54
TABLE 26. LSADC INTERFACE 55
TABLE 27. SMART CARD CONTROLLER EXTERNAL PIN DESCRIPTION 55
TABLE 28. DC FAN CONTROL EXTERNAL PIN DESCRIPTION 56
TABLE 29. TV ENCODER ANALOG OUTPUT INTERFACE 57
TABLE 30. HDMI BLOCK EXTERNAL PIN DESCRIPTION 59
TABLE 31. HDMI RECEIVER BLOCK EXTERNAL PIN DESCRIPTION 60
TABLE 32. AUDIO IN BLOCK PIN DESCRIPTION 62
TABLE 33. AUDIO OUT BLOCK PIN DESCRIPTION 64
TABLE 34. SATA BLOCK EXTERNAL PIN DESCRIPTION 66
TABLE 35. PCI EXPRESS BLOCK EXTERNAL PIN DESCRIPTION 67
TABLE 36. PCI EXPRESS 2.0 BLOCK EXTERNAL PIN DESCRIPTION 68
TABLE 37. ETHERNET 10/100/1000M BLOCK EXTERNAL PIN DESCRIPTION 69
TABLE 38. NAT BLOCK EXTERNAL PIN DESCRIPTION 71
TABLE 39. USB BLOCK EXTERNAL PIN DESCRIPTION 76
TABLE 40. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 77
TABLE 41. CARD READER BLOCK EXTERNAL PIN DESCRIPTION 78
TABLE 42. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 79
TABLE 43. TRANSPORT MODULE EXTERNAL PIN DESCRIPTION 80
TABLE 44. CLASSIFICATION REFLOW PROFILE 81
TABLE 45. ORDERING INFORMATION 84

List of Figures

FIGURE 1. SYSTEMS APPLICATION DIAGRAM 4
FIGURE 2. BLOCK DIAGRAM 5
FIGURE 3. PACKAGE IDENTIFICATION 6
FIGURE 4. PIN ASSIGNMENTS (BOTTOM VIEW) 7
FIGURE 5. POWER-ON SEQUENCE TIMING DIAGRAM 39
FIGURE 6. TYPICAL 4-WIRE FAN INTERFACE 56
FIGURE 7. I2S AUDIO-IN INTERFACE CONFIGURATION 62
FIGURE 8. I2S AUDIO-OUT INTERFACE CONFIGURATION 64
FIGURE 9. TYPICAL SATA APPLICATION 66
FIGURE 10. TYPICAL PCI EXPRESS 1.1 APPLICATION 67
FIGURE 11. TYPICAL PCI EXPRESS 2.0 APPLICATION 68
FIGURE 12. TYPICAL GIGABIT ETHERNET APPLICATION 70
FIGURE 13. FLEXIBLE INTERFACE OF HW NAT 73
FIGURE 14. LED INDICATOR IN DIRECT MODE 73
FIGURE 15. LED INDICATOR IN SCAN MODE 74
FIGURE 16. SCAN MODE TIMING CHART (EXAMPLE) 74
FIGURE 17. SOLDERING TEMPERATURE PROFILE 81

1. General Description

The RTD1296DB/RTD1296DC/RTD1296PB are cutting-edge High Definition Media Processor SoCs (System-on-Chip) for Consumer Electronics featuring a Trusted Execution Environment with an independent secure operating system, VP9 and H.265 decoding up to Ultra HD, and Full H.264 HD media Decoding and Encoding with multiple formats, Wireless/Wired Networking, HDMI Receiver, DTV, and a comprehensive set of High-Speed peripherals.

The RTD1296 operates as an IPv6 1WAN-2LAN router and equipped with a high-performance quad-core CPU, ARM Cortex-A53, with 1M L2 Cache embedded. The RTD1296 also integrates an efficient ARM T820 Graphic Processing Unit (GPU) to accelerate 2D and 3D graphics processing, which achieves competitive performance as Mali-450 8-core configuration. For acceleration of the OSD and 2D user interface, the built-in Streaming Engine of the RTD1296 provides commonly used drawing functions. The CPU is dedicated to applications, while most of the functions of the RTD1296 utilize separate hardware circuits to provide efficiently optimized systems. The Video DSP of the RTD1296 is dedicated to manipulating, decoding, and encoding of video streams in various formats, e.g. decoding 4K2K H.265, Full HD MPEG1/2/4/H.264/H.264 MVC, AVC/VC-1, VP8, AVS, AVS Plus, HD JPEG, etc. Video decoding and encoding can run simultaneously.

Additionally, video post processing of the RTD1296 is handled by a video processing subsystem that supports 3D de-interlacing, video scaling up to 4K2K and so on. Audio decoding is carried out by an Audio DSP that is capable of decoding a set of audio formats, e.g. DTS HD, Dolby® Digital Plus, TrueHD, and other popular formats. The Audio DSP also performs audio post processing.

The RTD1296 provides a secure environment for a rich operating system, bringing UHD and HDR content to big screens. A secure video path and secure storage are fundamentally essential to secure systems. With the deployment of ARM TrustZone and the implementation of a proprietary security mechanism, the RTD1296 protects video and highly confidential information from leaks. An independent secure operating system runs on the RTD1296. In addition, the RTD1296 hardware offers a cryptography engine, true random number generator, and sufficient One-Time Programmable ROM (OTP) space, which are also substantial elements for a Trusted Execution Environment.

The RTD1296 supports a comprehensive set of peripherals. An HDMI Transmitter and Receiver with PHY are integrated in the RTD1296. The HDMI interface supports HDCP. Other interfaces include USB2.0/USB3.0 Host/Device with PHY integrated, NAND/NOR/eMMC flash controller, Card reader supporting SD/MMC, high-speed UART for Bluetooth, Gigabit Ethernet MAC and PHY, 4-bit SDIO, IrDA Receiver and Transmitter, and dual transport stream interfaces.

The RTD1296 is designed as a cost efficient solution for Ultra High Definition Media Player, Router, OTT Streaming Player, Android TV, DTV Set-top box, or Miracast Wireless Display Adapter.

2. Features

- System and Peripherals
  - ARM Cortex-A53 Quad-Core processor with floating-point unit and NEON SIMD engine embedded, supporting the 64/32-bit ARMv8 architecture
  - 1MB L2 Cache
  - ARM T820 MP3(3-core) GPU – Mali-450 8-core equivalent
  - ARM TrustZone for Trusted Execution Environment (TEE) with independent secure operating system and integrated secure hardware
  - Supports OpenGL ES3.1, OpenCL 1.2 FP, DirectX 11.1, RenderScript Compute, ASTC, ARM Frame Buffer Compression
  - Video DSP with HW acceleration
  - Audio DSP with HW acceleration
  - Supports up to 4GB DDR4/DDR3 SDRAM with two dual-channels of 16-bit data interface (total 64-bit) or up to 2GB LPDDR3/LPDDR2 SDRAM with 64-bit data interface
  - Supports Serial Flash with dual I/O data interface
  - Supports NAND Flash with maximum 72-bit ECC
  - Supports eMMC 5.0
  - Boot-ROM and OTP (One-Time Programmable ROM) for Secure-Boot and Key storage
  - Integrates 10/100/1000 Ethernet MAC and PHY
  - Integrates two USB3.0 Super Speed Dual-Role Device controller and PHY with supports for Type C receptacle
  - Integrates dual USB2.0 High Speed Host/ Device controller and PHY
  - Integrates hardware NAT and IP6 engine for AP router application
  - Supports SDIO 3.0 interface
  - Supports SD3.0 interface
  - Supports RGMII/SGMII
  - Supports SATA III
  - Supports PCI Express1.1/2.0
  - Supports UART/I2C/GPIO/IrDA Rx/EJTAG/RTC
- Video and Picture Decoding Functions
  - H.265 MP@L5.1 Main Tier
  - VP9 Profile 0
  - MPEG1, VCD 1.0/2.0, SVCD
  - Supports HD MPEG2 (up to MP@HL 1080i), ISO/IFO/VOB/TS
  - Supports HD MPEG4 SP/ASP (720p/1080i/1080p), Xvid
  - H.264 BP@L3, MP and HP@L4.2
  - H.264 MVC SHP@L4.1
  - VC-1 SP, MP, AP@L3
  - AVS JZ@L6.2, AVS+ 1080@60P
  - H.263 Profile0/3@L70 1080@60P
  - Sorenson Spark L70
  - Theora 720P
  - VP8 1080@60P
  - HD JPEG with 32K x 32K maximum resolution
  - Full-pixel JPEG decode with high resolution zoom-in

- Video up-scaling from SD to Ultra HD (720p/1080i/1080p/2160p)
- Supports 24/30/36 bits deep color

- Video and Picture Encoding Functions
  - MPEG 4 SP@L5
  - H.264 BP, MP, HP@L4.2
  - H.264 MVC SHP 1080@30P
  - H.263 Profile3@L70 1080@60P
  - HD JPEG in high resolution

- Video and Picture Color Spectrum
  - Deliver metadata using SMPTE ST2086, CEA-861.3 through HDMI 2.0a
  - Support conversion between ITU-R Recommendation BT.2020, BT.709 and other color spaces.
  - Support SMPTE ST 2084 EOTF/OETF

- Audio Interfaces and Functions
  - Built-in Audio Codec with 24-bit resolution
  - Four I2S interface (8 channels) for Audio input/output
  - IEC 60958 (SPDIF) digital audio output
  - 7.1 CH down-mix
  - MPEG I Layer 1, 2, 3 (2-CH) and MPEG II Layer 1, 2 (Multi-Channel)
  - LPCM, ADPCM, ALAC, FLAC, AAC, WAV, AIFF, VSELP, and OGG Vorbis
  - DTS HD, Dolby Digital Plus, TrueHD (Licensee Only)
  - WMA/WMA Pro, Dolby Digital AC3, and DTS (Licensee Only)
  - LPCM/ADPCM/MP3/AAC audio recording
  - DTS Broadcast capable (Licensee Only)
  - Dolby Digital Consumer Encoder capable (Licensee Only)

- Video Interfaces and Functions
  - TV encoder with 12-bit video D/A converters
  - NTSC and PAL TV systems
  - Composite analog video output
  - HDMI v2.0 transmitter/receiver with CEC, support for 3D over HDMI
  - 3D De-interlacer
  - Bitmap OSD
  - Support for CGMS-A, WSS

- Cryptography
  - MD5
  - AES 128/192/256-bit with cipher modes of ECB/CBC/CTR/CTS
  - DES, TDES
  - SHA-1, SHA-256
  - Multi2

- DRM and Link Protection
  - PlayReady, Widevine
  - HDCP2.2, DTCP-IP

- Power Design
  - Support for Dynamic Voltage Frequency Scaling

- True Random Number Generator
- Miscellaneous
  - Thermal Sensor
  - Speed Sensor
  - Voltage sensor

- Package: 19mm x 19mm, TFBGA 636 with 0.65mm ball pitch

3. System Applications Diagram

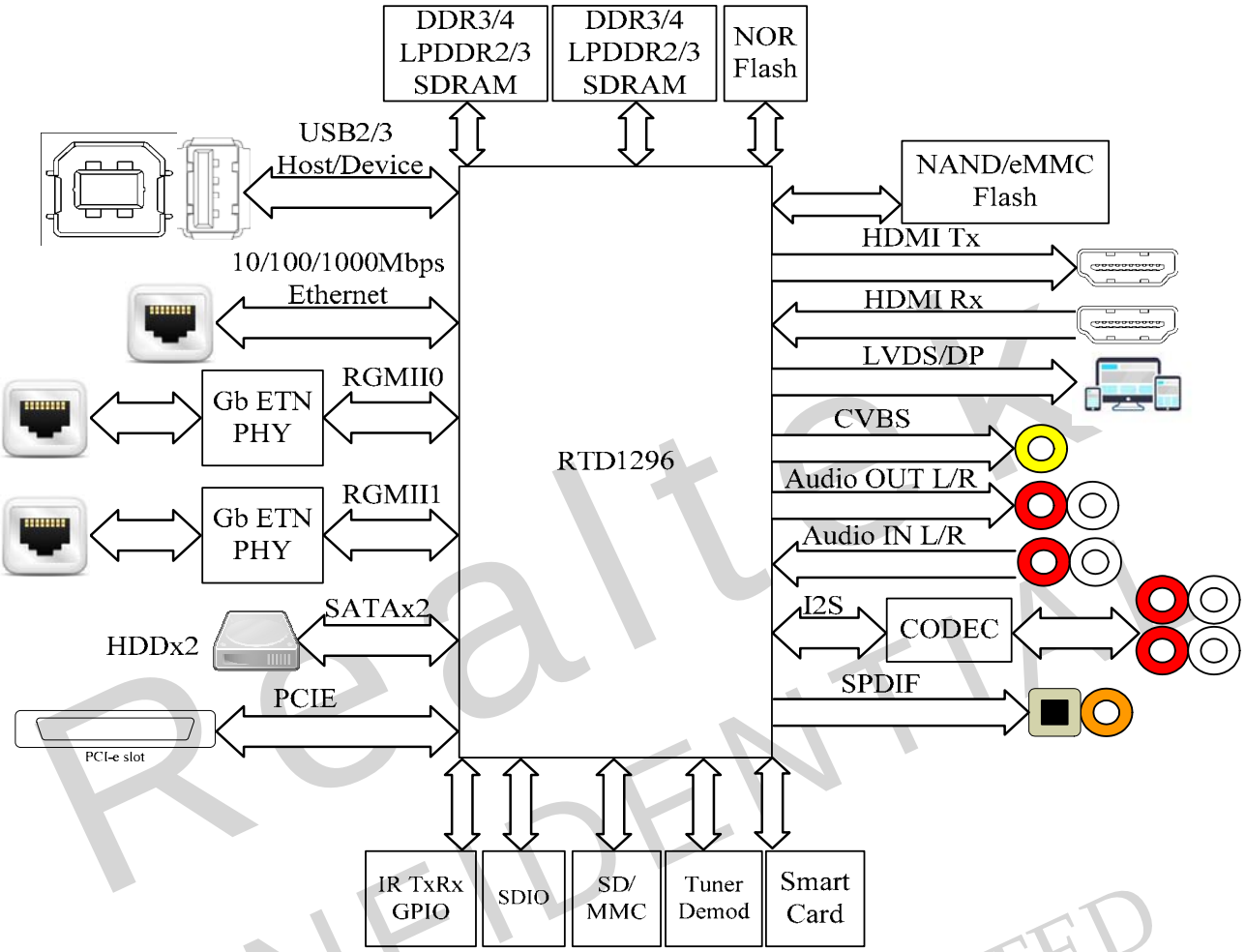

Figure 1. Systems Application Diagram

4. Block Diagram

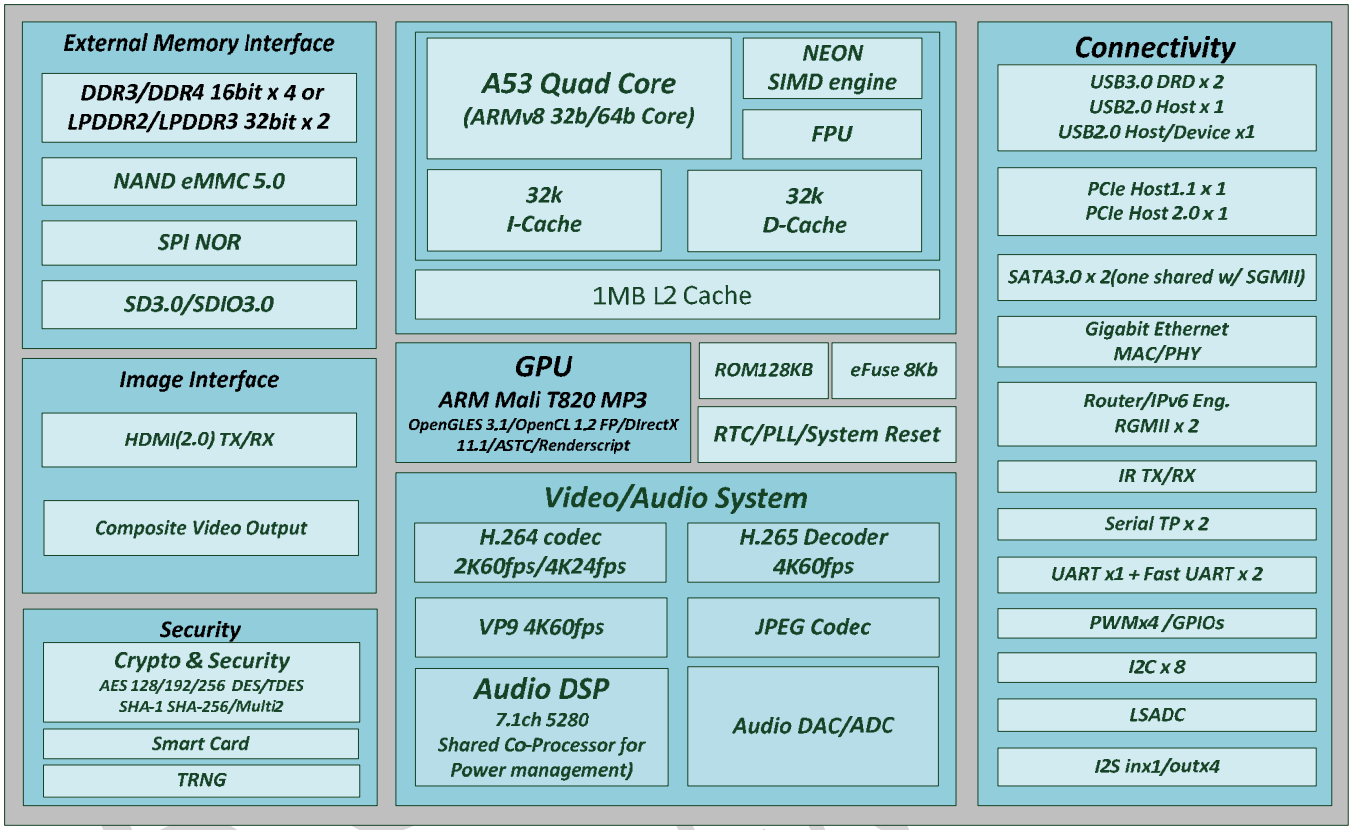

Figure 2. Block Diagram

5. Pin Assignments

5.1. Package Identification

XX in the model number indicates DB, DC, or PB model. Green package is indicated by the 'G' in GXXXX (Figure 3)

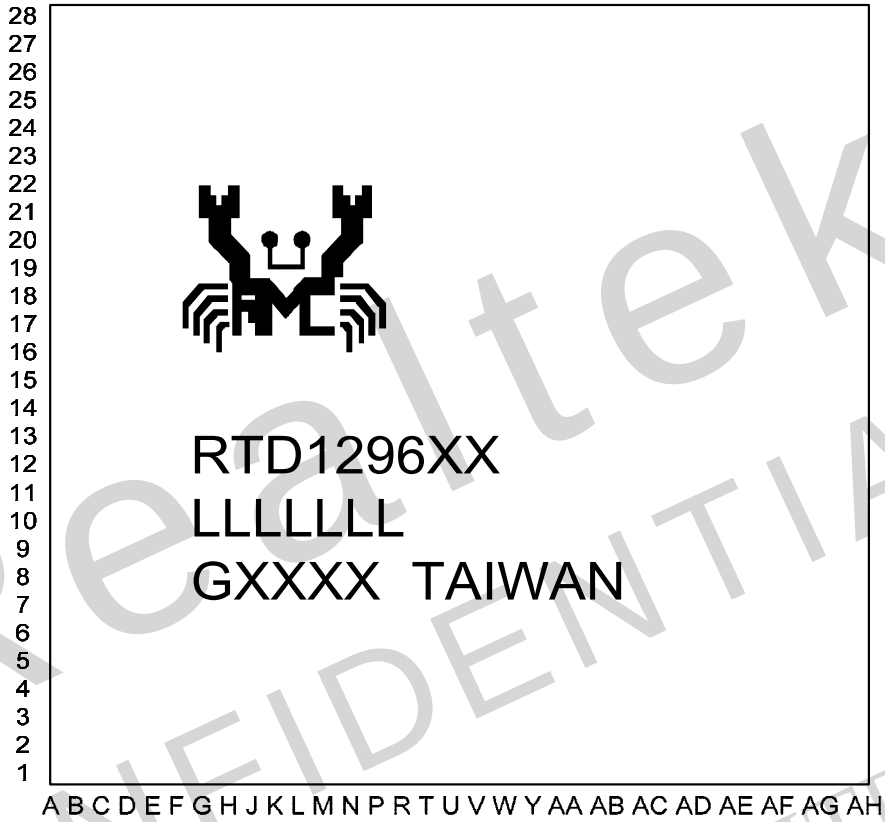

Figure 3. Package Identification

5.2. Pin Assignments (Bottom View)

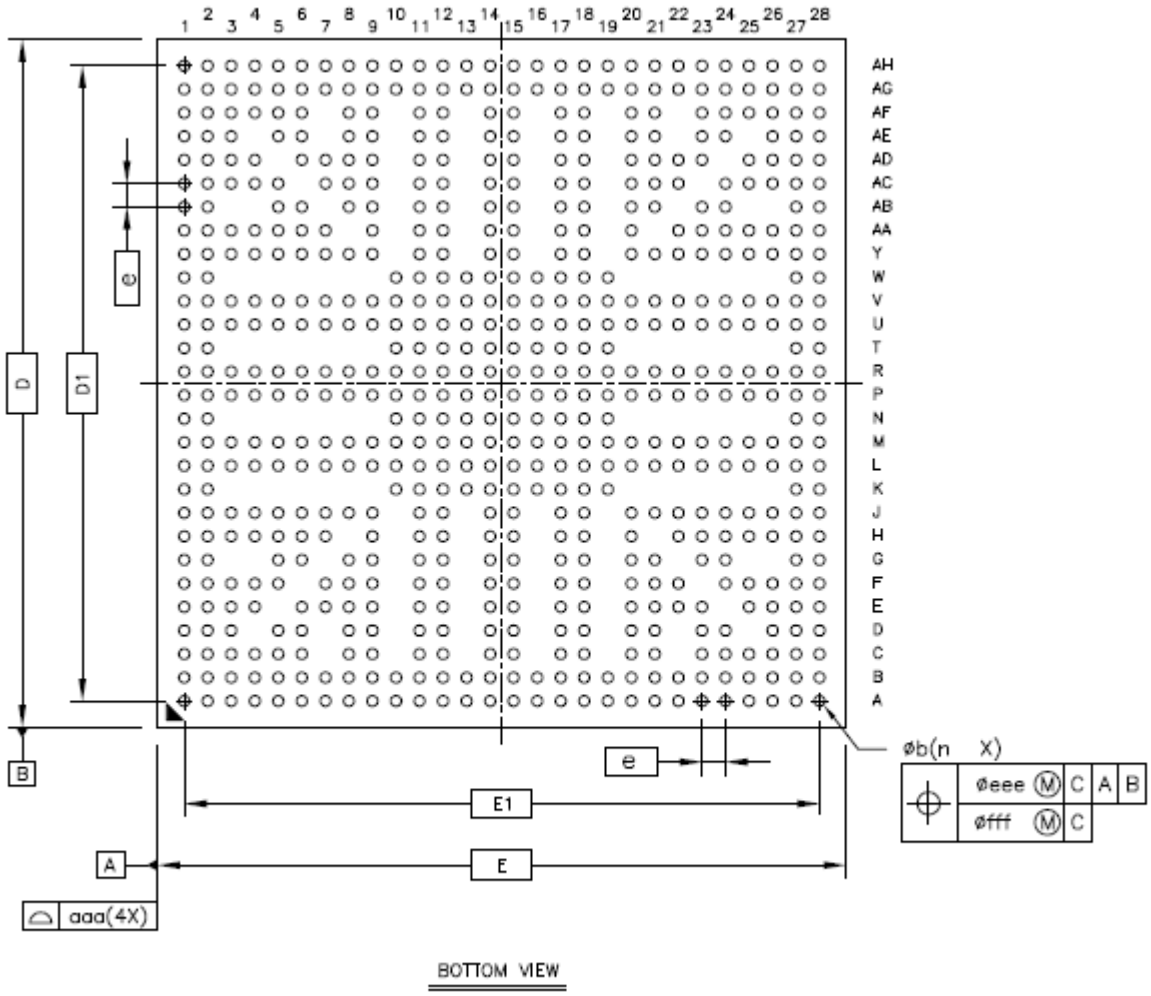

Figure 4. Pin Assignments (Bottom View)

6. Pin Descriptions

DI: Digital Input

DO: Digital Output

DB: Digital Bi-Directional

GND: Ground

AI: Analog Input

AO: Analog Output

AB: Analog Bi-Directional

PWR: Power Supply

Table 1. Pin Descriptions

Pin No.	Pin Name	I/O	Default Value	Description
A1	USB_DP2	AB	-	USB2 D+ signal (USB2 Host/ Device)
A2	USB_DM2	AB	-	USB2 D- signal (USB2 Host/ Device)
A3	USB_DM1	AB	-	USB2 D- signal (USB2 HOST)
A4	TYPEC_D-	AB	-	USB2 D- signal (USB3 TC)
A5	TYPEC_CC1	AB	-	USB3 TC Configuration Channel
A6	RTC_XI	AI	-	32.768kHz Crystal Oscillator Input
A7	XO	AO	-	27MHz Crystal Oscillator Output
A8	XI	AI	-	27MHz Crystal Oscillator Input
A9	Channel1_DDR4_DQ21	DB	-	Channel 1 DDR4 Data Bit21
	Channel1_DDR3_DQ23	DB	-	Channel 1 DDR3 Data Bit 23
	Channel1_LPDDR3_DQ16	DB	-	Channel 1 LPDDR3 Data Bit 16
A10	Channel1_DDR4_DQ17	DB	-	Channel 1 DDR4 Data Bit17
	Channel1_DDR3_DQ17	DB	-	Channel 1 DDR3 Data Bit 17
	Channel1_LPDDR3_DQ20	DB	-	Channel 1 LPDDR3 Data Bit 20
A11	Channel1_DDR3_DQS2#/ DDR4_DQS2_c	DB	-	Channel 1DDR3/4 DQ[23:16] Data Strobe
A12	Channel1_DDR4_DQ18	DB	-	Channel 1 DDR4 Data Bit18
	Channel1_DDR3_DQ16	DB	-	Channel 1 DDR3 Data Bit 16
	Channel1_LPDDR3_DQ1	DB	-	Channel 1 LPDDR3 Data Bit 1
A13	Channel1_DDR4_DQ20	DB	-	Channel 1 DDR4 Data Bit20
	Channel1_DDR3_DQ22	DB	-	Channel 1 DDR3 Data Bit 22
	Channel1_LPDDR3_DQ5	DB	-	Channel 1 LPDDR3 Data Bit 5
A14	Channel1_DDR4_A13	DO	-	Channel 1 DDR4 Address Bit 13
	Channel1_DDR3_A8	DO	-	Channel 1 DDR3 Address Bit 8
	Channel1_LPDDR3_CA0	DO	-	Channel 1 LPDDR3 Command/Address Bit 0
A15	Channel1_DDR4_A9	DO	-	Channel 1 DDR4 Address Bit 9
	Channel1_DDR3_A6	DO	-	Channel 1 DDR3 Address Bit 6
	Channel1_LPDDR3_CA2	DO	-	Channel 1 LPDDR3 Command/Address Bit 2
A16	Channel1_DDR4_A5	DO	-	Channel 1 DDR4 Address Bit 5
	Channel1_DDR3_A11	DO	-	Channel 1 DDR3 Address Bit 11
	Channel1_LPDDR3_CA3	DO	-	Channel 1 LPDDR3 Command/Address Bit 3

Pin No.	Pin Name	I/O	Default Value	Description
A17	Channel1_DDR4_TEN	DO	-	Channel 1 DDR4 Connectivity Enable
	Channel1_DDR3_A1	DO	-	Channel 1 DDR3Address Bit 1
A18	Channel1_DDR4_A3	DO	-	Channel 1 DDR4 Address Bit 3
	Channel1_DDR3_A12	DO	-	Channel 1 DDR3 Address Bit 12
	Channel1_LPDDR3_CA6	DO	-	Channel 1 LPDDR3 Command/Address Bit 6
A19	Channel1_DDR4_A12	DO	-	Channel 1 DDR4 Address Bit 12
	Channel1_DDR3_A10	DO	-	Channel 1 DDR3Address Bit 10
	Channel1_LPDDR3_CA8	DO	-	Channel 1 LPDDR3 Command/Address Bit 8
A20	Channel1_DDR4_CS1	DO	-	Channel 1 DDR4 Chip Select Output 1
	Channel1_DDR3_CS1	DO	-	Channel 1 DDR3 Chip Select Output 1
A21	Channel1_DDR3/4_CKE	DO	-	Channel 1 DDR3/4 Clock Enable Output
	Channel1_LPDDR3_CKE	DO	-	Channel 1 LPDDR3 Clock Enable Output
A22	Channel1_DDR3_CK/DDR4_CK_t	DO	-	Channel 1 DDR3/4 Clock Positive Output
A23	Channel1_DDR4_DQ5	DB	-	Channel 1 DDR4 Data Bit 5
	Channel1_DDR3_DQ7	DB	-	Channel 1 DDR3 Data Bit 7
	Channel1_LPDDR3_DQ8	DB	-	Channel 1 LPDDR3 Data Bit 8
A24	Channel1_DDR4_DQ1	DB	-	Channel 1 DDR4 Data Bit 1
	Channel1_DDR3_DQ1	DB	-	Channel 1 DDR3 Data Bit 1
	Channel1_LPDDR3_DQ12	DB	-	Channel 1 LPDDR3 Data Bit 12
A25	Channel1_DDR3_DQS0#/DDR4_DQS0_c	DB	-	Channel 1DDR3/4 DQ[7:0] Data Strobe
A26	Channel1_DDR4_DQ2	DB	-	Channel 1 DDR4 Data Bit 2
	Channel1_DDR3_DQ0	DB	-	Channel 1 DDR3 Data Bit 0
	Channel1_LPDDR3_DQ25	DB	-	Channel 1 LPDDR3 Data Bit 25
A27	Channel1_DDR4_DQ4	DB	-	Channel 1 DDR4 Data Bit 4
	Channel1_DDR3_DQ6	DB	-	Channel 1 DDR3 Data Bit 6
	Channel1_LPDDR3_DQ29	DB	-	Channel 1 LPDDR3 Data Bit 29
A28	Channel0_DDR4_DQ23	DB	-	Channel 0 DDR4 Data Bit 23
	Channel0_DDR3_DQ21	DB	-	Channel 0 DDR3 Data Bit 21
	Channel0_LPDDR3_DQ17	DB	-	Channel 0 LPDDR3 Data Bit 17
B1	USB_DP3	AB	-	USB2 D+ signal (USB2 Host)
B2	USB_DM3	AB	-	USB2 D- signal (USB2 Host)
B3	USB_DP1	AB	-	USB2 D+ signal (USB2 HOST)
B4	TYPEC_D+	AB	-	USB2 D+ signal (USB3 TC)
B5	TYPEC_CC2	AB	-	USB3 TC Configuration Channel
B6	RTC_XO	AO	-	32.768kHz Crystal Oscillator Output
B7	RTCVDD	PWR	-	RTC Power.
B8	Channel1_DDR4_DQ23	DB	-	Channel 1 DDR4 Data Bit 23
	Channel1_DDR3_DQ21	DB	-	Channel 1 DDR3 Data Bit 21
	Channel1_LPDDR3_DQ17	DB	-	Channel 1 LPDDR3 Data Bit 17

Pin No.	Pin Name	I/O	Default Value	Description
B9	Channel1_DDR4_DQ19	DB	-	Channel 1 DDR4 Data Bit 19
	Channel1_DDR3_DQ19	DB	-	Channel 1 DDR3 Data Bit 19
	Channel1_LPDDR3_DQ21	DB	-	Channel 1 LPDDR3 Data Bit 21
B10	Channel1_DDR3/4_DM2	DO	-	Channel 1DDR3/4 DQ[23:16] Data Mask
	Channel1_LPDDR3_DM2	DO	-	Channel 1 LPDDR3 DQ[23:16] Data Mask
B11	Channel1_DDR3_DQS2/ DDR4_DQS2_t	DB	-	Channel 1DDR3/4 DQ[23:16] Data Strobe
B12	Channel1_DDR4_DQ16	DB	-	Channel 1 DDR4 Data Bit 16
	Channel1_DDR3_DQ18	DB	-	Channel 1 DDR3 Data Bit 18
	Channel1_LPDDR3_DQ0	DB	-	Channel 1 LPDDR3 Data Bit 0
B13	Channel1_DDR4_DQ22	DB	-	Channel 1 DDR4 Data Bit 22
	Channel1_DDR3_DQ20	DB	-	Channel 1 DDR3 Data Bit 20
	Channel1_LPDDR3_DQ4	DB	-	Channel 1 LPDDR3 Data Bit 4
B14	Channel1_DDR4_A7	DO	-	Channel 1 DDR4 Address Bit 7
	Channel1_DDR3_A14	DO	-	Channel 1 DDR3 Address Bit 14
	Channel1_LPDDR3_CA1	DO	-	Channel 1 LPDDR3 Command/Address Bit 1
B15	Channel1_DDR4_ALERT#	DB	-	Channel 1 DDR4 Alert
	Channel1_DDR3_ALERT#	DB	-	Channel 1 DDR3 Alert
B16	Channel1_DDR4_A1	DO	-	Channel 1 DDR4 Address Bit 1
	Channel1_DDR3_A4	DO	-	Channel 1 DDR3 Address Bit 4
	Channel1_LPDDR3_CA4	DO	-	Channel 1 LPDDR3 Command/Address Bit 4
B17	Channel1_DDR4_BA1	DO	-	Channel 1 DDR4 Bank Address 1
	Channel1_DDR3_BA1	DO	-	Channel 1 DDR3 Bank Address 1
	Channel1_LPDDR3_CA5	DO	-	Channel 1 LPDDR3 Command/Address Bit 5
B18	Channel1_DDR4_CAS#/ A15	DO	-	Channel 1 DDR4 Column Address Select Output/ Address Bit 15
	Channel1_DDR3_A15	DO	-	Channel 1 DDR3Address Bit 15
	Channel1_LPDDR3_CA7	DO	-	Channel 1 LPDDR3 Command/Address Bit 7
B19	Channel1_DDR4_RAS#/ A16	DO	-	Channel 1 DDR4 Row Address Select Output /Address Bit 16
	Channel1_DDR3_A16	DO	-	Channel 1 DDR3 Address Bit 16
	Channel1_LPDDR3_CA9	DO	-	Channel1 LPDDR3 Command/Address Bit 9
B20	Channel1_DDR3/4_CS0	DO	-	Channel 1 DDR3/4 Chip Select Output 0
	Channel1_LPDDR3_CS0	DO	-	Channel 1 LPDDR3 Chip Select Output 0
B21	Channel1_DDR3_CK#/ DDR4_CK_c	DO	-	Channel 1 DDR3/4 Clock Output
B22	Channel1_DDR4_DQ7	DB	-	Channel 1 DDR4 Data Bit 7
	Channel1_DDR3_DQ5	DB	-	Channel 1 DDR3 Data Bit 5
	Channel1_LPDDR3_DQ9	DB	-	Channel 1 LPDDR3 Data Bit 9
B23	Channel1_DDR4_DQ3	DB	-	Channel 1 DDR4 Data Bit 3
	Channel1_DDR3_DQ3	DB	-	Channel 1 DDR3 Data Bit 3
	Channel1_LPDDR3_DQ13	DB	-	Channel 1 LPDDR3 Data Bit 13

Pin No.	Pin Name	I/O	Default Value	Description
B24	Channel1_DDR4_DM0	DO	-	Channel 1DDR4 DQ[7:0] Data Mask
	Channel1_DDR3_DM0	DO	-	Channel 1DDR3 DQ[7:0] Data Mask
	Channel1_LPDDR3_DM1	DO	-	Channel 1 LPDDR3 DQ[15:8] Data Mask
B25	Channel1_DDR3_DQS0/ DDR4_DQS0_t	DB	-	Channel 1DDR3/4 DQ[7:0] Data Strobe
B26	Channel1_DDR4_DQ0	DB	-	Channel 1 DDR4 Data Bit0
	Channel1_DDR3_DQ2	DB	-	Channel 1 DDR3 Data Bit 2
	Channel1_LPDDR3_DQ24	DB	-	Channel 1 LPDDR3 Data Bit 24
B27	Channel1_DDR4_DQ6	DB	-	Channel 1 DDR4 Data Bit 6
	Channel1_DDR3_DQ4	DB	-	Channel 1 DDR3 Data Bit 4
	Channel1_LPDDR3_DQ28	DB	-	Channel 1 LPDDR3 Data Bit 28
B28	Channel0_DDR4_DQ21	DB	-	Channel 0 DDR4 Data Bit 21
	Channel0_DDR3_DQ23	DB	-	Channel 0 DDR3 Data Bit 23
	Channel0_LPDDR3_DQ16	DB	-	Channel 0 LPDDR3 Data Bit 16
C1	USB3_HSON	AB	-	USB3 TX D+ signal.
C2	USB3_HSOP	AB	-	USB3 TX D- signal.
C3	GND	GND	-	Digital Ground
C4	GND	GND	-	Digital Ground
C5	TYPEC_RX2-	AI	-	USB3 TC RX D- signal.
C6	TYPEC_TX1+	AO	-	USB3 TC TX D+ signal.
C8	GND	GND	-	Digital Ground
C9	Channel1_DDR4_DQ27	DB	-	Channel 1 DDR4 Data Bit27
	Channel1_DDR3_DQ28	DB	-	Channel 1 DDR3 Data Bit 28
	Channel1_LPDDR3_DQ22	DB	-	Channel 1 LPDDR3 Data Bit 22
C11	GND	GND	-	Digital Ground
C12	Channel1_DDR4_DQ30	DB	-	Channel 1 DDR4 Data Bit 30
	Channel1_DDR3_DQ29	DB	-	Channel 1 DDR3 Data Bit 29
	Channel1_LPDDR3_DQ7	DB	-	Channel 1 LPDDR3 Data Bit 7
C14	GND	GND	-	Digital Ground
C15	Channel1_DDR4_A2	DO	-	Channel 1 DDR4 Address Bit 2
	Channel1_DDR3_A7	DO	-	Channel 1 DDR3 Address Bit 7
C17	GND	GND	-	Digital Ground
C18	Channel1_DDR4_A10	DO	-	Channel 1 DDR4 Address Bit 10
	Channel1_DDR3_BA0	DO	-	Channel 1 DDR3 Bank Address 0
C20	GND	GND	-	Digital Ground
C21	Channel1_DDR4_DQ9	DB	-	Channel 1 DDR4 Data Bit 9
	Channel1_DDR3_DQ10	DB	-	Channel 1 DDR3 Data Bit 10
	Channel1_LPDDR3_DQ10	DB	-	Channel 1 LPDDR3 Data Bit 10
C23	GND	GND	-	Digital Ground
C24	Channel1_DDR4_DQ8	DB	-	Channel 1 DDR4 Data Bit 8
	Channel1_DDR3_DQ15	DB	-	Channel 1 DDR3 Data Bit 15
	Channel1_LPDDR3_DQ27	DB	-	Channel 1 LPDDR3 Data Bit 27

Pin No.	Pin Name	I/O	Default Value	Description
C25	Channel1_DDR4_DQ10	DB	-	Channel 1 DDR4 Data Bit 10
	Channel1_DDR3_DQ9	DB	-	Channel 1 DDR3 Data Bit 9
	Channel1_LPDDR3_DQ26	DB	-	Channel 1 LPDDR3 Data Bit 26
C26	GND	GND	-	Digital Ground
C27	Channel0_DDR4_DQ19	DB	-	Channel 0 DDR4 Data Bit 19
	Channel0_DDR3_DQ19	DB	-	Channel 0 DDR3 Data Bit 19
	Channel0_LPDDR3_DQ21	DB	-	Channel 0 LPDDR3 Data Bit 21
C28	Channel0_DDR4_DQ17	DB	-	Channel 0 DDR4 Data Bit 17
	Channel0_DDR3_DQ17	DB	-	Channel 0 DDR3 Data Bit 17
	Channel0_LPDDR3_DQ20	DB	-	Channel 0 LPDDR3 Data Bit 20
D1	USB3_HSIN	AB	-	USB3 RX D+ signal
D2	USB3_HSIP	AB	-	USB3 RX D- signal
D3	GND	GND	-	Digital Ground
D5	TYPEC_RX2+	AI	-	USB3 TC RX D+ signal.
D6	TYPEC_TX1-	AO	-	USB3 TC TX D- signal.
D8	Channel1_DDR4_DQ29	DB	-	Channel 1 DDR4 Data Bit 29
	Channel1_DDR3_DQ24	DB	-	Channel 1 DDR3 Data Bit 24
	Channel1_LPDDR3_DQ19	DB	-	Channel 1 LPDDR3 Data Bit 19
D9	Channel1_DDR4_DQ31	DB	-	Channel 1 DDR4 Data Bit31
	Channel1_DDR3_DQ30	DB	-	Channel 1 DDR3 Data Bit 30
	Channel1_LPDDR3_DQ23	DB	-	Channel 1 LPDDR3 Data Bit 23
D11	Channel1_DDR4_DM3	DO	-	Channel 1 DDR4 DQ[31:24] Data Mask
	Channel1_DDR3_DM3	DO	-	Channel 1 DDR3 DQ[31:24] Data Mask
	Channel1_LPDDR3_DM0	DO	-	Channel 1 LPDDR3 DQ[7:0] Data Mask
D12	Channel1_DDR4_DQ24	DB	-	Channel 1 DDR4 Data Bit24
	Channel1_DDR3_DQ31	DB	-	Channel 1 DDR3 Data Bit 31
	Channel1_LPDDR3_DQ3	DB	-	Channel 1 LPDDR3 Data Bit 3
D14	Channel1_DDR4_RESET#	DO	-	Channel 1 DDR4 Reset
	Channel1_DDR3_RESET#	DO	-	Channel 1 DDR3 Reset
D15	Channel1_DDR4_A11	DO	-	Channel 1 DDR4 Address Bit 11
	Channel1_DDR3_A9	DO	-	Channel 1 DDR3 Address Bit 9
D17	Channel1_DDR4_A4	DO	-	Channel 1 DDR4 Address Bit 4
	Channel1_DDR3_A3	DO	-	Channel 1 DDR3 Address Bit 3
D18	Channel1_DDR4_BA0	DO	-	Channel 1 DDR4 Bank Address 0
	Channel1_DDR3_BA2	DO	-	Channel 1 DDR3 Bank Address 2
D20	Channel1_DDR3/4_ODT	DO	-	Channel 1 DDR3/4 On-Die Termination
	Channel1_LPDDR3_ODT	DO	-	Channel 1 LPDDR3 On-Die Termination
D21	Channel1_DDR4_DQ13	DB	-	Channel 1 DDR4 Data Bit13
	Channel1_DDR3_DQ8	DB	-	Channel 1 DDR3 Data Bit 8
	Channel1_LPDDR3_DQ11	DB	-	Channel 1 LPDDR3 Data Bit 11
D23	Channel1_DDR3_DQS1/DDR4_DQS1_t	DB	-	Channel 1DDR3/4 DQ[15:8] Data Strobe

Pin No.	Pin Name	I/O	Default Value	Description
D24	Channel1_DDR4_DQ14	DB	-	Channel 1 DDR4 Data Bit 14
	Channel1_DDR3_DQ13	DB	-	Channel 1 DDR3 Data Bit 13
	Channel1_LPDDR3_DQ31	DB	-	Channel 1 LPDDR3 Data Bit 31
D26	Channel0_DDR4_DQ29	DB	-	Channel 0 DDR4 Data Bit29
	Channel0_DDR3_DQ24	DB	-	Channel 0 DDR3 Data Bit 24
	Channel0_LPDDR3_DQ19	DB	-	Channel 0 LPDDR3 Data Bit 19
D27	Channel0_DDR3/4_DM2	DO	-	Channel 0 DDR3/4 DQ[23:16] Data Mask
	Channel0_LPDDR3_DM2	DO	-	Channel 0 LPDDR3 DQ[23:16] Data Mask
D28	Channel0_DDR3_DQS2#/ DDR4_DQS2_c	DB	-	Channel 0 DDR3/4 DQ[23:16] Data Strobe
E1	ETN_MDIN0	AB	-	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB- pair, and is the receive pair in 10Base-T and 100Base-TX.
E2	ETN_MDIP0	AB	-	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+ pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+ pair, and is the receive pair in 10Base-T and 100Base-TX.
E3	ETN_MDIN2	AB	-	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC- pair. In MDI crossover mode, this pair acts as the BI_DD- pair.
E4	ETN_MDIP2	AB	-	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+ pair. In MDI crossover mode, this pair acts as the BI_DD pair.
E6	TYPEC_TX2+	AO	-	USB3 TC TX D+ signal.
E7	TYPEC_RX1-	AI	-	USB3 TC RX D- signal.
E8	Channel1_DDR4_DQ25	DB	-	Channel 1 DDR4 Data Bit25
	Channel1_DDR3_DQ26	DB	-	Channel 1 DDR3 Data Bit 26
	Channel1_LPDDR3_DQ18	DB	-	Channel 1 LPDDR3 Data Bit 18
E9	Channel1_DDR3_DQS3#/ DDR4_DQS3_c	DB	-	Channel 1DDR3/4 DQ[31:24] Data Strobe
E11	Channel1_DDR3/4_DVRI23	PWR	-	Channel 1 DDR3/4 Reference Voltage Input
E12	Channel1_DDR4_DQ26	DB	-	Channel 1 DDR4 Data Bit 26
	Channel1_DDR3_DQ25	DB	-	Channel 1 DDR3 Data Bit 25
	Channel1_LPDDR3_DQ2	DB	-	Channel 1 LPDDR3 Data Bit 2
E14	Channel1_DDR4_PAR	DO	-	Channel 1 DDR4 Command and Address Parity
	Channel1_DDR3_A13	DO	-	Channel 1 DDR3 Address Bit 13
E15	Channel1_DDR4_A8	DO	-	Channel 1 DDR4 Address Bit 8
	Channel1_DDR3_A2	DO	-	Channel 1 DDR3 Address Bit 2
E17	Channel1_DDR4_A6	DO	-	Channel 1 DDR4 Address Bit 6
	Channel1_DDR3_A0	DO	-	Channel 1 DDR3 Address Bit 0
E18	Channel1_DDR4_BG0	DO	-	Channel 1 DDR4 Bank Group 0
	Channel1_DDR3_WE#	DO	-	Channel 1 DDR3 Write Enable Output

Pin No.	Pin Name	I/O	Default Value	Description
E20	Channel1_DDR4_ WE#/A14	DO	-	Channel 1 DDR4 Write Enable Output /Address Bit 14
	Channel1_DDR3_RAS#	DO	-	Channel 1 DDR3 Row Address Select Output
E21	Channel1_DDR4_DQ15	DB	-	Channel 1 DDR4 Data Bit 15
	Channel1_DDR3_DQ14	DB	-	Channel 1 DDR3 Data Bit 14
	Channel1_LPDDR3_DQ15	DB	-	Channel 1 LPDDR3 Data Bit 15
E22	Channel1_DDR3_DQS1#/ DDR4_DQS1_c	DB	-	Channel 1DDR3/4 DQ[15:8] Data Strobe
E23	Channel1_DDR4_DM1	DO	-	Channel 1DDR4 DQ[15:8] Data Mask
	Channel1_DDR3_DM1	DO	-	Channel1DDR3 DQ[15:8] Data Mask
	Channel1_LPDDR3_DM3	DO	-	Channel 1 LPDDR3 DQ[31:24] Data Mask
E25	Channel0_DDR4_DQ31	DB	-	Channel 0 DDR4 Data Bit 31
	Channel0_DDR3_DQ30	DB	-	Channel 0 DDR3 Data Bit 30
	Channel0_LPDDR3_DQ23	DB	-	Channel 0 LPDDR3 Data Bit 23
E26	Channel0_DDR4_DQ27	DB	-	Channel 0 DDR4 Data Bit 27
	Channel0_DDR3_DQ28	DB	-	Channel 0 DDR3 Data Bit 28
	Channel0_LPDDR3_DQ22	DB	-	Channel 0 LPDDR3 Data Bit 22
E27	Channel0_DDR3_DQS2/D DR4_DQS2_t	DB	-	Channel 0 DDR3/4 DQ[23:16] Data Strobe
E28	Channel0_DDR4_DQ18	DB	-	Channel 0 DDR4 Data Bit18
	Channel0_DDR3_DQ16	DB	-	Channel 0 DDR3 Data Bit 16
	Channel0_LPDDR3_DQ1	DB	-	Channel 0 LPDDR3 Data Bit 1
F1	ETN_MDIN1	AB	-	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA- pair, and is the transmit pair in 10Base-T and 100Base-TX.
F2	ETN_MDIP1	AB	-	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
F3	ETN_MDIN3	AB	-	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD- pair. In MDI crossover mode, this pair acts as the BI_DC- pair.
F4	ETN_MDIP3	AB	-	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+ pair. In MDI crossover mode, this pair acts as the BI_DC+ pair.
F5	TYPEC_TX2-	AO	-	USB3 TC TX D+ signal.
F7	TYPEC_RX1+	AI	-	USB3 TC RX D+ signal.
F8	USB2_3V3	PWR	-	USB and Power-on-Reset Power 3.3V
F9	Channel1_DDR3_DQS3/D DR4_DQS3_t	DB	-	Channel 1DDR3/4 DQ[31:24] Data Strobe
F11	USB2_1V	PWR	-	USB Power

Pin No.	Pin Name	I/O	Default Value	Description
F12	Channel1_DDR4_DQ28	DB	-	Channel 1 DDR4 Data Bit28
	Channel1_DDR3_DQ27	DB	-	Channel 1 DDR3 Data Bit 27
	Channel1_LPDDR3_DQ6	DB	-	Channel 1 LPDDR3 Data Bit 6
F14	DDR_VIO2	PWR	-	DDR Power
F15	Channel1_DDR4_A0	DO	-	Channel 1 DDR4 Address Bit 0
	Channel1_DDR3_A5	DO	-	Channel 1 DDR3 Address Bit 5
F17	DDR_VIO2	PWR	-	DDR Power
F18	Channel1_DDR4_ACT#	DO	-	Channel 1 DDR4 Activation Command
	Channel1_DDR3_CAS#	DO	-	Channel 1 DDR3 Column Address Select Output
F20	DDR_VIO2	PWR	-	DDR Power
F21	Channel1_DDR4_DQ11	DB	-	Channel 1 DDR4 Data Bit11
	Channel1_DDR3_DQ12	DB	-	Channel 1 DDR3 Data Bit 12
	Channel1_LPDDR3_DQ14	DB	-	Channel 1 LPDDR3 Data Bit 14
F22	Channel1_DDR4_DQ12	DB	-	Channel 1 DDR4 Data Bit 12
	Channel1_DDR3_DQ11	DB	-	Channel 1 DDR3 Data Bit 11
	Channel1_LPDDR3_DQ30	DB	-	Channel 1 LPDDR3 Data Bit 30
F24	Channel0_DDR3_DQS3#/ DDR4_DQS3_c	DB	-	Channel 0 DDR3/4 DQ[31:24] Data Strobe
F25	Channel0_DDR3_DQS3/D DR4_DQS3_t	DB	-	Channel 0 DDR3/4 DQ[31:24] Data Strobe
F26	GND	GND	-	Digital Ground
F27	Channel0_DDR4_DQ16	DB	-	Channel 0 DDR4 Data Bit16
	Channel0_DDR3_DQ18	DB	-	Channel 0 DDR3 Data Bit 18
	Channel0_LPDDR3_DQ0	DB	-	Channel 0 LPDDR3 Data Bit 0
F28	Channel0_DDR4_DQ20	DB	-	Channel 0 DDR4 Data Bit20
	Channel0_DDR3_DQ22	DB	-	Channel 0 DDR3 Data Bit 22
	Channel0_LPDDR3_DQ5	DB	-	Channel 0 LPDDR3 Data Bit 5
G1	GPIO_35	DB	-	General Purpose IO 35
	RGMII0_RXCTL	DI		RGMII receive control signal
G2	GPIO_34	DB	-	General Purpose IO 34
	RGMII0_RXC	DI		RGMII continuous receive reference clock
G5	GND	GND	-	Digital Ground
G6	GPHY_3V3	PWR	-	Ethernet Power
G8	USB3_1V	PWR	-	USB Power
G9	SATA1_IN	AI	-	SATA RX Channel Negative Input
G11	SATA0_ON	AO	-	SATA TX Channel Negative Output
	HSON	AO	-	SERDES differential output
G12	SATA0_IN	AI	-	SATA RX Channel Negative Input
	HSIN	AI	-	SERDES differential input
G14	GND	GND	-	Digital Ground
G15	GND	GND	-	Digital Ground
G17	GND	GND	-	Digital Ground
G18	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
G20	Channel1_DDR3/4_DVRI01	PWR	-	Channel 1 DDR3/4 Reference Voltage Input
G21	Channel1_DDR3/4_ZQ	PWR	-	Channel 1 DDR3/4 ZQ Calibration
G23	Channel0_DDR4_DQ25	DB	-	Channel 0 DDR4 Data Bit25
	Channel0_DDR3_DQ26	DB	-	Channel 0 DDR3 Data Bit 26
	Channel0_LPDDR3_DQ18	DB	-	Channel 0 LPDDR3 Data Bit 18
G24	Channel0_DDR4_DM3	DO	-	Channel 0DDR4 DQ[31:24] Data Mask
	Channel0_DDR3_DM3	DO	-	Channel 0DDR3 DQ[31:24] Data Mask
	Channel0_LPDDR3_DM0	DO	-	Channel 0 LPDDR3 DQ[7:0] Data Mask
G27	Channel0_DDR4_DQ22	DB	-	Channel 0 DDR4 Data Bit22
	Channel0_DDR3_DQ20	DB	-	Channel 0 DDR3 Data Bit 20
	Channel0_LPDDR3_DQ4	DB	-	Channel 0 LPDDR3 Data Bit 4
G28	Channel0_DDR4_A13	DO	-	Channel 0 DDR4 Address Bit 13
	Channel0_DDR3_A8	DO	-	Channel 0 DDR3 Address Bit 8
	Channel0_LPDDR3_CA0	DO	-	Channel 0 LPDDR3 Command/Address Bit 0
H1	GPIO_37	DB	-	General Purpose IO 37
	RGMII0_RXD1	DI		RGMII Receive Data
H2	GPIO_36	DB	-	General Purpose IO 36
	RGMII0_RXD0	DI		RGMII Receive Data
H3	GPIO_40	DB	-	General Purpose IO 40
	RGMII0_MDIO	DB		GMAC to management data input/output
H4	RGMII0_MDC	DO	-	GMAC to Management data clock.
H5	IGPIO_13	DB	1	Isolation General Purpose IO 13
	UR1_TX	DO		UART 1 Transmit Data Output
H6	GPHY_1V	PWR	-	Ethernet Power
H7	SATA1_ON	AO	-	SATA TX Channel Negative Output
H9	SATA1_IP	AI	-	SATA RX Channel Positive Input
H11	SATA0_OP	AO	-	SATA TX Channel Positive Output
	HSOP	AO	-	SERDES differential output
H12	SATA0_IP	AI	-	SATA RX Channel Positive Input
	HSIP	AI	-	SERDES differential input
H14	SATA0_1V	PWR	-	SATA Power
H15	CORE_1V	PWR	-	Core Power
H17	CORE_1V	PWR	-	Core Power
H18	DDR_3V3	PWR	-	DDR Power
H20	GND	GND	-	Digital Ground
H22	Channel0_DDR3/4_ZQ	PWR	-	Channel 0 DDR3/4 ZQ Calibration
H23	Channel0_DDR4_DQ24	DB	-	Channel 0 DDR4 Data Bit24
	Channel0_DDR3_DQ31	DB	-	Channel 0 DDR3 Data Bit 31
	Channel0_LPDDR3_DQ3	DB	-	Channel 0 LPDDR3 Data Bit 3
H24	Channel0_DDR4_DQ30	DB	-	Channel 0 DDR4 Data Bit30
	Channel0_DDR3_DQ29	DB	-	Channel 0 DDR3 Data Bit 29
	Channel0_LPDDR3_DQ7	DB	-	Channel 0 LPDDR3 Data Bit 7

Pin No.	Pin Name	I/O	Default Value	Description
H25	Channel0_DDR4_DQ28	DB	-	Channel 0 DDR4 Data Bit28
	Channel0_DDR3_DQ27	DB	-	Channel 0 DDR3 Data Bit 27
	Channel0_LPDDR3_DQ6	DB	-	Channel 0 LPDDR3 Data Bit 6
H26	Channel0_DDR4_DQ26	DB	-	Channel 0 DDR4 Data Bit26
	Channel0_DDR3_DQ25	DB	-	Channel 0 DDR3 Data Bit 25
	Channel0_LPDDR3_DQ2	DB	-	Channel 0 LPDDR3 Data Bit 2
H27	Channel0_DDR4_A7	DO	-	Channel 0 DDR4 Address Bit 7
	Channel0_DDR3_A14	DO	-	Channel 0 DDR3 Address Bit 14
	Channel0_LPDDR3_CA1	DO	-	Channel 0 LPDDR3 Command/Address Bit 1
H28	Channel0_DDR4_A9	DO	-	Channel 0 DDR4 Address Bit 9
	Channel0_DDR3_A6	DO	-	Channel 0 DDR3 Address Bit 6
	Channel0_LPDDR3_CA2	DO	-	Channel 0 LPDDR3 Command/Address Bit 2
J1	GPIO_39	DB	-	General Purpose IO 39
	RGMII0_RXD3	DI		RGMII Receive Data
J2	GPIO_38	DB	-	General Purpose IO 38
	RGMII0_RXD2	DI		RGMII Receive Data
J3	GND	GND	-	Digital Ground
J4	IGPIO_12	DB	1	Isolation General Purpose IO 12
	UR1_RX	DI		UART 1 Receive Data Output
J5	IGPIO_14	DB	1	Isolation General Purpose IO 14
	UR1_CTS#	DI		UART 1 Clear to Send Input
J6	GPHY_1V	PWR	-	Ethernet Power
J7	SATA1_OP	AO	-	SATA TX Channel Positive Output
J8	RGMII1_VDD	PWR	-	RGMII Pin Power
J9	UR1_VDD	PWR	-	UR1_TX, UR1_RX, UR1_CTS#, UR1_RTS# Pin Power
J11	GND	GND	-	Digital Ground
J12	TYPEC_1V	PWR	-	USB3 TC Power
J14	GND	GND	-	Digital Ground
J15	PLL_1V	PWR	-	PLL Power
J17	CORE_1V	PWR	-	Core Power
J18	CORE_1V	PWR	-	Core Power
J20	DDR_VIO2	PWR	-	DDR Power
J21	GND	GND	-	Digital Ground
J22	Channel0_DDR3/4_DVRI23	PWR	-	Channel 0 DDR3/4 Reference Voltage Input
J23	DDR_VIO	PWR	-	DDR Power
J24	Channel0_DDR4_RESET#	DO	-	Channel 0 DDR4 Reset
	Channel0_DDR3_RESET#	DO	-	Channel 0 DDR3 Reset
J25	Channel0_DDR4_PAR	DO	-	Channel 0 DDR4 Command and Address Parity
	Channel0_DDR3_A13	DO	-	Channel 0 DDR3 Address Bit 13
J26	GND	GND	-	Digital Ground
J27	Channel0_DDR4_ALERT#	DB	-	Channel 0 DDR4 Alert
	Channel0_DDR3_ALERT#	DB	-	Channel 0 DDR3 Alert

Pin No.	Pin Name	I/O	Default Value	Description
J28	Channel0_DDR4_A5	DO	-	Channel 0 DDR4 Address Bit 5
	Channel0_DDR3_A11	DO	-	Channel 0 DDR3 Address Bit 11
	Channel0_LPDDR3_CA3	DO	-	Channel 0 LPDDR3 Command/Address Bit 3
K1	GPIO_29	DB	-	General Purpose IO 29
	RGMII0_TXCTL	DO		RGMII Transmit control signal
K2	GPIO_28	DB	-	General Purpose IO 28
	RGMII0_TXC	DO		RGMII Transmit control signal
K10	ISO_1V	PWR	-	ISO block Power
K11	ISO_1V	PWR	-	ISO block Power
K12	RGMII0_VDD	PWR	-	RGMII Pin Power
K13	GND	GND	-	Digital Ground
K14	PLL_3V3	PWR	-	PLL Power
K15	GND	GND	-	Digital Ground
K16	GND	GND	-	Digital Ground
K17	GND	GND	-	Digital Ground
K18	CORE_1V	PWR	-	Core Power
K19	CORE_1V	PWR	-	Core Power
K27	Channel0_DDR4_A1	DO	-	Channel 0 DDR4 Address Bit 1
	Channel0_DDR3_A4	DO	-	Channel 0 DDR3 Address Bit 4
	Channel0_LPDDR3_CA4	DO	-	Channel 0 LPDDR3 Command/Address Bit 4
K28	Channel0_DDR4_TEN	DO	-	Channel 0 DDR4 Connectivity Enable
	Channel0_DDR3_A1	DO	-	Channel 0 DDR3Address Bit 1
L1	GPIO_31	DB	-	General Purpose IO 31
	RGMII0_TXD1	DO		RGMII Transmit Data
L2	GPIO_30	DB	-	General Purpose IO 30
	RGMII0_TXD0	DO		RGMII Transmit Data
L3	GND	GND	-	Digital Ground
L4	CBUS_3V3	PWR	-	CBUS Power
L5	IGPIO_15	DB	1	Isolation General Purpose IO 15
	UR1_RTS#	DO		UART 1 Request to Send Output
L6	GPIO_48	DB	-	General Purpose IO 48
	RGMII1_RXC	DI		RGMII continuous receive reference clock
L7	GPIO_51	DB	-	General Purpose IO 51
	RGMII1_RXD1	DI		RGMII Receive Data
L8	GPIO_50	DB	-	General Purpose IO 50
	RGMII1_RXD0	DI		RGMII Receive Data
L9	ISO_3V3	PWR	-	ISO block Power
L10	GND	GND	-	Digital Ground
L11	GND	GND	-	Digital Ground
L12	GND	GND	-	Digital Ground
L13	SATA1_1V	PWR	-	SATA Power
L14	GND	GND	-	Digital Ground
L15	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
L16	GND	GND	-	Digital Ground
L17	GND	GND	-	Digital Ground
L18	CORE_1V	PWR	-	Core Power
L19	CORE_1V	PWR	-	Core Power
L20	CORE_1V	PWR	-	Core Power
L21	CORE_1V	PWR	-	Core Power
L22	GND	GND	-	Digital Ground
L23	Channel0_DDR4_A11	DO	-	Channel 0 DDR4 Address Bit 11
	Channel0_DDR3_A9	DO	-	Channel 0 DDR3 Address Bit 9
L24	Channel0_DDR4_A2	DO	-	Channel 0 DDR4 Address Bit 2
	Channel0_DDR3_A7	DO	-	Channel 0 DDR3 Address Bit 7
L25	Channel0_DDR4_A0	DO	-	Channel 0 DDR4 Address Bit 0
	Channel0_DDR3_A5	DO	-	Channel 0 DDR3 Address Bit 5
L26	Channel0_DDR4_A8	DO	-	Channel 0 DDR4 Address Bit 8
	Channel0_DDR3_A2	DO	-	Channel 0 DDR3 Address Bit 2
L27	Channel0_DDR4_BA1	DO	-	Channel 0 DDR4 Bank Address 1
	Channel0_DDR3_BA1	DO	-	Channel 0 DDR3 Bank Address 1
	Channel0_LPDDR3_CA5	DO	-	Channel 0 LPDDR3 Command/Address Bit 5
L28	Channel0_DDR4_A3	DO	-	Channel 0 DDR4 Address Bit 3
	Channel0_DDR3_A12	DO	-	Channel 0 DDR3Address Bit 12
	Channel0_LPDDR3_CA6	DO	-	Channel 0 LPDDR3 Command/Address Bit 6
M1	GPIO_33	DB	-	General Purpose IO 33
	RGMII0_TXD3	DO		RGMII Transmit Data
M2	GPIO_32	DB	-	General Purpose IO 32
	RGMII0_TXD2	DO		RGMII Transmit Data
M3	GND	GND	-	Digital Ground
M4	CBUS_1V8	PWR	-	CBUS Power
M5	GPIO_49	DB	-	General Purpose IO 49
	RGMII1_RXCTL	DI		RGMII receive control signal
M6	MBIAS_GND	GND	-	Bandgap Ground
M7	GPIO_52	DB	-	General Purpose IO 53
	RGMII1_RXD2	DI		RGMII Receive Data
M8	GPIO_53	DB	-	General Purpose IO 52
	RGMII1_RXD3	DI		RGMII Receive Data
M9	GND	GND	-	Digital Ground
M10	GND	GND	-	Digital Ground
M11	GND	GND	-	Digital Ground
M12	GND	GND	-	Digital Ground
M13	GND	GND	-	Digital Ground
M14	GND	GND	-	Digital Ground
M15	GND	GND	-	Digital Ground
M16	GND	GND	-	Digital Ground
M17	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
M18	GND	GND	-	Digital Ground
M19	GND	GND	-	Digital Ground
M20	CORE_1V	PWR	-	Core Power
M21	CORE_1V	PWR	-	Core Power
M22	GND	GND	-	Digital Ground
M23	DDR_VIO	PWR	-	DDR Power
M24	Channel0_DDR4_A4	DO	-	Channel 0 DDR4 Address Bit 4
	Channel0_DDR3_A3	DO	-	Channel 0 DDR3 Address Bit3
M25	Channel0_DDR4_A6	DO	-	Channel 0 DDR4 Address Bit 6
	Channel0_DDR3_A0	DO	-	Channel 0 DDR3 Address Bit0
M26	GND	GND	-	Digital Ground
M27	Channel0_DDR4_CAS#/A15	DO	-	Channel 0 DDR4 Column Address Select Output/ Address Bit 15
	Channel0_DDR3_A15	DO	-	Channel 0 DDR3Address Bit 15
	Channel0_LPDDR3_CA7	DO	-	Channel 0 LPDDR3 Command/Address Bit 7
M28	Channel0_DDR4_A12	DO	-	Channel 0 DDR4 Address Bit 12
	Channel0_DDR3_A10	DO	-	Channel 0 DDR3Address Bit 10
	Channel0_LPDDR3_CA8	DO	-	Channel 0 LPDDR3 Command/Address Bit 8
N1	IGPIO_27	DB	1	Isolation General Purpose IO 27
	ETN_LED0	DO		Customized Ethernet LED0
	PWM0_1	DO		PWM0 Output. Location1
N2	IGPIO_28	DB	1	Isolation General Purpose IO 28
	ETN_LED1	DO		Customized Ethernet LED1
	PWM1_1	DO		PWM 1 Output. Location1
N10	GND	GND	-	Digital Ground
N11	GND	GND	-	Digital Ground
N12	GND	GND	-	Digital Ground
N13	GND	GND	-	Digital Ground
N14	GND	GND	-	Digital Ground
N15	GND	GND	-	Digital Ground
N16	GND	GND	-	Digital Ground
N17	GND	GND	-	Digital Ground
N18	GND	GND	-	Digital Ground
N19	GND	GND	-	Digital Ground
N27	Channel0_DDR4_RAS#/A16	DO	-	Channel 0 DDR4 Row Address Select Output /Address Bit 16
	Channel0_DDR3_A16	DO	-	Channel 0 DDR3 Address Bit 16
	Channel0_LPDDR3_CA9	DO	-	Channel 0 LPDDR3 Command/Address Bit 9
N28	Channel0_DDR4_CS1	DO	-	Channel 0 DDR4 Chip Select Output 1
	Channel0_DDR3_CS1	DO	-	Channel 0 DDR3 Chip Select Output 1
P1	IGPIO_19	DB	1/ 5V tolerance	Isolation General Purpose IO 19
	I2C1_SDA	DB		I2C Serial Data

Pin No.	Pin Name	I/O	Default Value	Description
P2	HDMITX_HPD	DI	0/ 5V tolerance	HDMI TX Hot Plug Detection
	IGPIO_6	DB		Isolation General Purpose IO 6
P3	GND	GND	-	Digital Ground
P4	HDMITX_CKN	AO	-	HDMI Output Clock Pair-
P5	MBIAS_3V3	PWR	-	Bandgap Power
P6	REXT	PWR	-	Bandgap Voltage of Whole Chip. Connect to GND via a 6.19KΩ, ±1% Resistor
P7	GPIO_43	DB	-	General Purpose IO 43
	RGMII1_TXCTL	DO		RGMII Transmit control signal
P8	GPIO_42	DB	-	General Purpose IO 42
	RGMII1_TXC	DO		RGMII Transmit control signal
P9	GND	GND	-	Digital Ground
P10	GND	GND	-	Digital Ground
P11	GND	GND	-	Digital Ground
P12	GND	GND	-	Digital Ground
P13	GND	GND	-	Digital Ground
P14	GND	GND	-	Digital Ground
P15	GND	GND	-	Digital Ground
P16	GND	GND	-	Digital Ground
P17	GND	GND	-	Digital Ground
P18	GND	GND	-	Digital Ground
P19	GND	GND	-	Digital Ground
P20	GND	GND	-	Digital Ground
P21	CORE_1V	PWR	-	Core Power
P22	GND	GND	-	Digital Ground
P23	Channel0_DDR4_BA0	DO	-	Channel 0 DDR4 Bank Address 0
	Channel0_DDR3_BA2	DO		Channel 0 DDR3 Bank Address 2
P24	Channel0_DDR4_A10	DO	-	Channel 0 DDR4 Address Bit 10
	Channel0_DDR3_BA0	DO		Channel 0 DDR3 Bank Address 0
P25	Channel0_DDR4_ACT#	DO	-	Channel 0 DDR4 Activation Command
	Channel0_DDR3_CAS#	DO		Channel 0 DDR3 Column Address Select Output
P26	Channel0_DDR4_BG0	DO	-	Channel 0 DDR4 Bank Group 0
	Channel0_DDR3_WE#	DO		Channel 0 DDR3 Write Enable Output
P27	Channel0_DDR3/4_CS0	DO	-	Channel 0 DDR3/4 Chip Select Output 0
	Channel0_LPDDR3_CS0	DO		Channel 0 LPDDR3 Chip Select Output 0
P28	Channel0_DDR3/4_CKE	DO	-	Channel 0 DDR3/4 Clock Enable Output
	Channel0_LPDDR3_CKE	DO		Channel 0 LPDDR3 Clock Enable Output
R1	IGPIO_18	DB	1/ 5V tolerance	Isolation General Purpose IO 18
	I2C1_SCL	DB		I2C Serial Clock
R2	HDMITX_CEC	AB	-	HDMI TX Consumer Electronics Control
R3	GND	GND	-	Digital Ground
R4	HDMITX_CKP	AO	-	HDMI TX Clock Pair -
R5	HDMITX_D0N	AO	-	HDMI TX Data Pair 0-/

Pin No.	Pin Name	I/O	Default Value	Description
R6	HDMITX_D0P	AO	-	HDMI TX Data Pair 0+
R7	GPIO_44	DB	-	General Purpose IO 44
	RGMII1_TXD0	DO		RGMII Transmit Data
R8	GPIO_45	DB	-	General Purpose IO 45
	RGMII1_TXD1	DO		RGMII Transmit Data
R9	NC	-	-	-
R10	GND	GND	-	Digital Ground
R11	GND	GND	-	Digital Ground
R12	GND	GND	-	Digital Ground
R13	GND	GND	-	Digital Ground
R14	GND	GND	-	Digital Ground
R15	GND	GND	-	Digital Ground
R16	GND	GND	-	Digital Ground
R17	GND	GND	-	Digital Ground
R18	GND	GND	-	Digital Ground
R19	GPIO_3V3	PWR	-	Digital IO Power
R20	GPIO_3V3	PWR	-	Digital IO Power
R21	GPIO_3V3	PWR	-	Digital IO Power
R22	GND	GND	-	Digital Ground
R23	DDR_VIO	PWR	-	DDR Power
R24	Channel0_DDR3/4_ODT	DO	-	Channel 0 DDR3/4 On-Die Termination
	Channel0_LPDDR3_ODT	DO	-	Channel 0 LPDDR3 On-Die Termination
R25	Channel0_DDR4_WE#/A14	DO	-	Channel 0 DDR4 Write Enable Output /Address Bit 14
	Channel0_DDR3_RAS#	DO	-	Channel 0 DDR3 Row Address Select Output
R26	GND	GND	-	Digital Ground
R27	Channel0_DDR3_CK#/DDR4_CK_c	DO	-	Channel 0 DDR3/4 Clock Output
R28	Channel0_DDR3_CK/DDR4_CK_t	DO	-	Channel 0 DDR3/4 Clock Output
T1	IGPIO_23	DB	1/ 5V tolerance	Isolation General Purpose IO 23
	PWM2_0	DO		PWM 2 output. Location0
	UR2_RX_L1	DI		UART 2 Receive Data Input. Location1
T2	IGPIO_24	DB	1/ 5V tolerance	Isolation General Purpose IO 24
	PWM3_0	DO		PWM 3 Output. Location0
	UR2_ TX_L1	DO		UART 2 Transmit Data Output. Location1
T10	GND	GND	-	Digital Ground
T11	GND	GND	-	Digital Ground
T12	GPU_DVS	PWR	-	GPU DVFS Power
T13	GPU_DVS	PWR	-	GPU DVFS Power
T14	GND	GND	-	Digital Ground
T15	CPU_DVS	PWR	-	CPU DVFS Power
T16	CPU_DVS	PWR	-	CPU DVFS Power
T17	CPU_DVS	PWR	-	CPU DVFS Power

Pin No.	Pin Name	I/O	Default Value	Description
T18	CPU_DVS	PWR	-	CPU DVFS Power
T19	MEM_DVS	PWR	-	L2 Cache DVFS Power
T27	Channel0_DDR4_DQ7	DB	-	Channel 0 DDR4 Data Bit7
	Channel0_DDR3_DQ5	DB	-	Channel 0 DDR3 Data Bit 5
	Channel0_LPDDR3_DQ9	DB	-	Channel 0 LPDDR3 Data Bit 9
T28	Channel0_DDR4_DQ5	DB	-	Channel 0 DDR4 Data Bit5
	Channel0_DDR3_DQ7	DB	-	Channel 0 DDR3 Data Bit 7
	Channel0_LPDDR3_DQ8	DB	-	Channel 0 LPDDR3 Data Bit8
U1	IGPIO_25	DB	1/ 5V tolerance	Isolation General Purpose IO 25
	RTC_32K	DO		Output 32K clock to board for BT wake on module use, when BT in suspend mode. 32K clock for power saving
U2	STBY_0*	DB	1/ 5V tolerance	Power Control in Standby Mode
U3	HDMITX_D1P	AO	-	HDMI TX Data Pair 1+
U4	HDMITX_D1N	AO	-	HDMI TX Data Pair 1-
U5	GND	GND	-	Digital Ground
U6	HDMITX_3V3	PWR	-	HDMI TX Power
U7	GPIO_46	DB	-	General Purpose IO 46
	RGMII1_TXD2	DO		RGMII Transmit Data
U8	HDMIRX_PVDD	PWR	-	HDMI RX Power
U9	GND	GND	-	Digital Ground
U10	GPU_DVS	PWR	-	GPU DVFS Power
U11	GPU_DVS	PWR	-	GPU DVFS Power
U12	GPU_DVS	PWR	-	GPU DVFS Power
U13	GPU_DVS	PWR	-	GPU DVFS Power
U14	GND	GND	-	Digital Ground
U15	CPU_DVS	PWR	-	CPU DVFS Power
U16	CPU_DVS	PWR	-	CPU DVFS Power
U17	CPU_DVS	PWR	-	CPU DVFS Power
U18	CPU_DVS	PWR	-	CPU DVFS Power
U19	MEM_DVS	PWR	-	L2 Cache DVFS Power
U20	LSADC_3V3	PWR	-	LSADC Power
U21	LSADC1	AI	-	Low Speed ADC1
U22	DDRPLL_1V	PWR	-	DDR PLL Power
U23	Channel0_DDR4_DQ13	DB	-	Channel 0 DDR4 Data Bit13
	Channel0_DDR3_DQ8	DB	-	Channel 0 DDR3 Data Bit 8
	Channel0_LPDDR3_DQ11	DB	-	Channel 0 LPDDR3 Data Bit 11
U24	Channel0_DDR4_DQ9	DB	-	Channel 0 DDR4 Data Bit9
	Channel0_DDR3_DQ10	DB	-	Channel 0 DDR3 Data Bit 10
	Channel0_LPDDR3_DQ10	DB	-	Channel 0 LPDDR3 Data Bit 10
U25	Channel0_DDR4_DQ11	DB	-	Channel 0 DDR4 Data Bit11
	Channel0_DDR3_DQ12	DB	-	Channel 0 DDR3 Data Bit 12
	Channel0_LPDDR3_DQ14	DB	-	Channel 0 LPDDR3 Data Bit 14

Pin No.	Pin Name	I/O	Default Value	Description
U26	Channel0_DDR4_DQ15	DB	-	Channel 0 DDR4 Data Bit15
	Channel0_DDR3_DQ14	DB	-	Channel 0 DDR3 Data Bit 14
	Channel0_LPDDR3_DQ15	DB	-	Channel 0 LPDDR3 Data Bit 15
U27	Channel0_DDR4_DQ3	DB	-	Channel 0 DDR4 Data Bit 3
	Channel0_DDR3_DQ3	DB	-	Channel 0 DDR3 Data Bit 3
	Channel0_LPDDR3_DQ13	DB	-	Channel 0 LPDDR3 Data Bit 13
U28	Channel0_DDR4_DQ1	DB	-	Channel 0 DDR4 Data Bit 1
	Channel0_DDR3_DQ1	DB	-	Channel 0 DDR3 Data Bit 1
	Channel0_LPDDR3_DQ12	DB	-	Channel 0 LPDDR3 Data Bit 12
V1	RST_OUT	DB	1	Default Input. When a watchdog reset is triggered, output low to reset on-board PMICs. 0: Reset, 1: Active
V2	IGPIO_16	DB	1	Isolation General Purpose IO 16
	I2C0_SCL	DB		I2C Serial Clock
V3	HDMITX_1V	PWR	-	HDMI TX Power
V4	GND	GND	-	Digital Ground
V5	HDMITX_D2N	AO	-	HDMI TX Data Pair 2-
V6	HDMITX_D2P	AO	-	HDMI TX Data Pair 2+
V7	GPIO_47	DB	-	General Purpose IO 47
	RGMII1_TXD3	DO		RGMII Transmit Data
V8	HDMIRX_1V	PWR	-	HDMI RX Power
V9	HDMIRX_3V3	PWR	-	HDMI RX Power
V10	GPU_DVS	PWR	-	GPU DVFS Power
V11	GPU_DVS	PWR	-	GPU DVFS Power
V12	GPU_DVS	PWR	-	GPU DVFS Power
V13	GPU_DVS	PWR	-	GPU DVFS Power
V14	GND	GND	-	Digital Ground
V15	CPU_DVS	PWR	-	CPU DVFS Power
V16	CPU_DVS	PWR	-	CPU DVFS Power
V17	CPU_DVS	PWR	-	CPU DVFS Power
V18	CPU_DVS	PWR	-	CPU DVFS Power
V19	MEM_DVS	PWR	-	L2 Cache DVFS Power
V20	LSADC_GND	GND	-	Digital Ground
V21	PCIE2_CKP	AO	-	PCI Express Clock+
V22	PCIE2_CKN	AO	-	PCI Express Clock-
V23	DDR_VIO	PWR	-	DDR Power
V24	Channel0_DDR3_DQS1/ DDR4_DQS1_t	DB	-	Channel 0 DDR3/4 DQ[15:8] Data Strobe
V25	Channel0_DDR3_DQS1#/ DDR4_DQS1_c	DB	-	Channel 0 DDR3/4 DQ[15:8] Data Strobe
V26	GND	GND	-	Digital Ground
V27	Channel0_DDR4_DM0	DO	-	Channel 0DDR4 DQ[7:0] Data Mask
	Channel0_DDR3_DM0	DO	-	Channel 0DDR3 DQ[7:0] Data Mask
	Channel0_LPDDR3_DM1	DO	-	Channel 0 LPDDR3 DQ[15:8] Data Mask

Pin No.	Pin Name	I/O	Default Value	Description
V28	Channel0_DDR3_DQS0#/ DDR4_DQS0_c	DB	-	Channel 0 DDR3/4 DQ[7:0] Data Strobe
W1	IGPIO_17	DB	1	Isolation General Purpose IO 17
	I2C0_SDA	DB		I2C Serial Data
W2	IGPIO_29	DB	1	Isolation General Purpose IO 29
	NAT_LED0	DO		LED for NAT
	SC_RST#	DO		Smart Card reset
	PWM2_1	DO		PWM 2 output. location 1
W10	GND	GND	-	Digital Ground
W11	GND	GND	-	Digital Ground
W12	GND	GND	-	Digital Ground
W13	GND	GND	-	Digital Ground
W14	GND	GND	-	Digital Ground
W15	GND	GND	-	Digital Ground
W16	GND	GND	-	Digital Ground
W17	CPU_DVS	PWR	-	CPU DVFS Power
W18	CPU_DVS	PWR	-	CPU DVFS Power
W19	SD_CAP	PWR	-	SD/MMC Pin Power, connect to an external capacitor
W27	Channel0_DDR3_DQS0/ DDR4_DQS0_t	DB	-	Channel 0 DDR3/4 DQ[7:0] Data Strobe
W28	Channel0_DDR4_DQ2	DB	-	Channel 0 DDR4 Data Bit2
	Channel0_DDR3_DQ0	DB	-	Channel 0 DDR3 Data Bit 0
	Channel0_LPDDR3_DQ25	DB	-	Channel 0 LPDDR3 Data Bit 25
Y1	IGPIO_30	DB	1	Isolation General Purpose IO 30
	NAT_LED1	DO		LED for NAT
	SC_CLK	DO		Smart Card clock
	PWM3_1	DB		PWM 3 output. location 1
Y2	IGPIO_31	DB	0	Isolation General Purpose IO 31
	NAT_LED2	DO		LED for NAT
	SC_DATA	DB		Smart Card data in/out
Y3	IGPIO_32	DB	0	Isolation General Purpose IO 32
	NAT_LED3	DO		LED for NAT
	SC_CD	DI		Smart Card card detect
Y4	HDMITX_1V8	PWR	-	HDMI TX 1.8V
Y5	GND	GND	-	Digital Ground
Y6	AO_3V3	PWR	-	Digital IO Power
Y7	VDAC_3V3	PWR	-	Video DAC Power
Y8	DMIC_VDD	PWR	-	Digital MIC Power
Y9	ADAC_3V3	PWR	-	Audio DAC Power
Y11	GND	GND	-	Digital Ground
Y12	GND	GND	-	Digital Ground
Y14	GND	GND	-	Digital Ground
Y15	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
Y17	GND	GND	-	Digital Ground
Y18	GND	GND	-	Digital Ground
Y20	PCIE2_1V	PWR	-	PCI Express Power
Y21	PCIE2_RXN	AI	-	PCI Express RX-
Y22	PCIE2_RXP	AI	-	PCI Express RX+
Y23	Channel0_DDR4_DM1	DO	-	Channel 0DDR4 DQ[15:8] Data Mask
	Channel0_DDR3_DM1	DO	-	Channel 0DDR3 DQ[15:8] Data Mask
	Channel0_LPDDR3_DM3	DO	-	Channel 0 LPDDR3 DQ[31:24] Data Mask
Y24	Channel0_DDR4_DQ8	DB	-	Channel 0 DDR4 Data Bit8
	Channel0_DDR3_DQ15	DB	-	Channel 0 DDR3 Data Bit 15
	Channel0_LPDDR3_DQ27	DB	-	Channel 0 LPDDR3 Data Bit 27
Y25	Channel0_DDR4_DQ10	DB	-	Channel 0 DDR4 Data Bit10
	Channel0_DDR3_DQ9	DB	-	Channel 0 DDR3 Data Bit 9
	Channel0_LPDDR3_DQ26	DB	-	Channel 0 LPDDR3 Data Bit 26
Y26	Channel0_DDR4_DQ14	DB	-	Channel 0 DDR4 Data Bit 14
	Channel0_DDR3_DQ13	DB	-	Channel 0 DDR3 Data Bit 13
	Channel0_LPDDR3_DQ31	DB	-	Channel 0 LPDDR3 Data Bit 31
Y27	Channel0_DDR4_DQ0	DB	-	Channel 0 DDR4 Data Bit0
	Channel0_DDR3_DQ2	DB	-	Channel 0 DDR3 Data Bit 2
	Channel0_LPDDR3_DQ24	DB	-	Channel 0 LPDDR3 Data Bit 24
Y28	Channel0_DDR4_DQ4	DB	-	Channel 0 DDR4 Data Bit4
	Channel0_DDR3_DQ6	DB	-	Channel 0 DDR3 Data Bit 6
	Channel0_LPDDR3_DQ29	DB	-	Channel 0 LPDDR3 Data Bit 29
AA1	UR0_TX	DO	-	UART 0 Transmit Data Output
AA2	UR0_RX	DI	1	UART 0 Receive Data Input
AA3	VRP	PWR	-	Common mode voltage output
AA4	VREF	PWR	-	Common Mode Reference Voltage for Audio DAC
AA5	IR_RX	DI	1	Infrared Input from IR Receiver
AA6	RESET#	DI	1	Chip Reset
AA7	TESTMODE	DI	0	Select Test Mode
AA9	NC	-	-	-
AA11	NC	-	-	-
AA12	BOOTSEL	DI	0	Boot Selection High: Boot from NOR Flash Low: Boot from Internal ROM.
AA14	SCPUPLL_3V3	PWR	-	SCPU PLL Power
AA15	GPIO_17	DB	1	General Purpose IO 17
	USB_12M	DO		USB2 ohci 12M clock output
AA17	GPIO_18	DB	1	General Purpose IO 18
AA18	GPIO_12	DB	1	General Purpose IO 12
	I2C4_SDA	DB		I2C Serial Data
AA20	PCIE1_1V	PWR	-	PCI Express Power
AA22	GND	GND	-	Digital Ground

Pin No.	Pin Name	I/O	Default Value	Description
AA23	LSADC0	AI	-	Low Speed ADC0
AA24	Channel0_DDR3/4_DVRI01	PWR	-	Channel 0 DDR3/4 Reference Voltage Input
AA25	Channel0_DDR4_DQ12	DB	-	Channel 0 DDR4 Data Bit 12
	Channel0_DDR3_DQ11	DB	-	Channel 0 DDR3 Data Bit 11
	Channel0_LPDDR3_DQ30	DB	-	Channel 0 LPDDR3 Data Bit 30
AA26	GND	GND	-	Digital Ground
AA27	Channel0_DDR4_DQ6	DB	-	Channel 0 DDR4 Data Bit6
	Channel0_DDR3_DQ4	DB	-	Channel 0 DDR3 Data Bit 4
	Channel0_LPDDR3_DQ28	DB	-	Channel 0 LPDDR3 Data Bit 28
AA28	OTP_1V8	PWR	-	OTP Power 1.8V
AB1	STBY_1*	DB	1/ 5V tolerance	Power Control in Standby Mode
AB2	IGPIO_9	DB	0	Isolation General Purpose IO 9
	IR_TX	DO		Infrared Output from IR transmitter
AB5	IGPIO_33	DB	1/ 5V tolerance	Isolation General Purpose IO 33
	UR2_CTS_N	DI		UART 2 Clear to Send Input. location1
AB6	IGPIO_34	DB	1/ 5V tolerance	Isolation General Purpose IO 34
	UR2_RTS_N	DO		UART 2 Request to Send Output. location1
AB8	DP_1V	PWR	-	DP Power
AB9	NC	-	-	-
AB11	NC	-	-	-
AB12	IO_VDD	PWR	-	GPIO[11~12] and GPIO[16~20] Pin Power
AB14	TP_3V3	PWR	-	Digital IO Power
AB15	GPIO_16	DB	1	General Purpose IO 16
AB17	GPIO_19	DB	1	General Purpose IO 19
AB18	GPIO_11	DB	1	General Purpose IO 11
	I2C4_SCL	DB		I2C Serial Clock
AB20	PCIE2_TXP	AO	-	PCI Express TX+
AB21	PCIE2_TXN	AO	-	PCI Express TX-
AB23	SDIO_D3	DB	1	SDIO Data3
	GPIO_94	DB		General Purpose IO 94
AB24	SDIO_CMD	DB	1	SDIO Command Line
	GPIO_89	DB		General Purpose IO 89
AB27	NAND_RD#	DO	1	NAND Flash Read Enable
	eMMC_CMD	DB		eMMC Command Line
	EJ_TDI	DI		JTAG Test Data Input
AB28	NAND_RDY	DI	1	NAND Flash Ready
	eMMC_RST#	DI		eMMC reset signal
	EJ_TDO	DO		JTAG Test Data Output
AC1	IGPIO_2	DB	1	Isolation General Purpose IO 2
	UR2_RX_L0	DI		UART 2 receive data input. location0.
	EJ_RST#	DI		JTAG Reset

Pin No.	Pin Name	I/O	Default Value	Description
AC2	IGPIO_3	DO	1	Isolation General Purpose IO 3
	UR2_TX_L0	DB		UART 2 Transmit Data Output. location0
	EJ_TDI	DI		JTAG Test Data Input
AC3	IGPIO_4	DI	1	Isolation General Purpose IO 4
	UR2_CTS#	DB		UART 2 Clear to Send Input. location0
	EJ_TDO	DO		JTAG Test Data Output
AC4	IGPIO_5	DO	1	Isolation General Purpose IO 5
	UR2_RTS#	DB		UART 2 Request to Send Output. location0
	EJ_TMS	DI		JTAG Test Mode Select
AC5	NC	-	-	-
AC7	GND	GND	-	Digital Ground
AC8	NC	-	-	-
AC9	GND	GND	-	Digital Ground
AC11	DP_3V3	PWR	-	DP Power
AC12	DP_1V8	PWR	-	DP Power
AC14	DP_LANE3N	AO	-	DP lane 3 TX negative
AC15	DP_LANE0P	AO	-	DP lane 0 TX positive
AC17	GPIO_20	DB	1	General Purpose IO 20
AC18	USB_ID	DI	1/ 5V tolerance	USB Identification. Denotes the pin on the USB Micro connectors that is used to differentiate a Micro-A plug from a Micro-B plug attached
	GPIO_15	DB		General Purpose IO 15
	TEST_LOOP_DIS	DI		Test loop disable for SCPU ejtag protect
AC20	GND	GND	-	Digital Ground
AC21	PCIE1_RXN	AI	-	PCI Express RX-
AC22	PCIE1_CKN	AO	-	PCI Express Clock-
AC24	SDIO_VDD	PWR	-	SDIO Pin Power
AC25	SDIO_D1	DB	1	SDIO Data1
	GPIO_92	DB		General Purpose IO 92
AC26	SDIO_D2	DB	1	SDIO Data2
	GPIO_93	DB		General Purpose IO 93
AC27	NAND_CE0#	DO	1	NAND Flash Chip Enable 0
	GPIO_78	DB		General Purpose IO 78
AC28	NAND_CE1#	DO	1	NAND Flash Chip Enable 1
	GPIO_79	DB		General Purpose IO 79
AD1	IGPIO_7	DB	0	Isolation General Purpose IO 7
	EJ_TCLK	DI		JTAG Test Mode Clock
	DP_HPD	DI		DP Hot Plug Detection
AD2	IGPIO_21	DB	0/ 5V tolerance	Isolation General Purpose IO 21
	PWM0_0	DO		PWM 0 Output. location0
AD3	IGPIO_22	DB	0/ 5V tolerance	Isolation General Purpose IO 22
	HDMIRX_HPD_CTRL	DO		HDMI RX Hot Plug Control
	PWM1_0	DO		PWM 1 Output. location0

Pin No.	Pin Name	I/O	Default Value	Description
AD4	HDMIRX_5V_DET	DO	5V tolerance	HDMI RX 5V detect
AD6	NC	-	-	-
AD7	NC	-	-	-
AD8	GND	GND	-	Digital Ground
AD9	HDMIRX_D1P	AI	-	HDMI RX Data Pair 1+
AD11	GND	GND	-	Digital Ground
AD12	DP_LANE4P	AO	-	DP lane 4 TX positive
AD14	DP_LANE3P	AO	-	DP lane 3 TX positive
AD15	DP_LANE0N	AO	-	DP lane 0 TX negative
AD17	GPIO_25	DB	1	General Purpose IO 25
	TP1_DATA	DI		Transport Stream 1 data
	I2C3_SDA	DB		I2C Serial Data Signal
AD18	TP1_SYNC	DI	1	Transport Stream 1 sync.
	GPIO_10	DB		General Purpose IO 10
	I2C2_SDA	DB		I2C Serial Data Signal
AD20	GPIO_96	DB	1	General Purpose IO 96
	PCIE2_CLKREQ	DB		PCI Express reference clock request signal
AD21	PCIE1_RXP	AI	-	PCI Express RX+
AD22	PCIE1_CKP	AO	-	PCI Express Clock+
AD23	SD_1V8	PWR	-	SD/MMC Power
AD25	SDIO_CLK	DO	0	SDIO Clock Output
	GPIO_90	DB		General Purpose IO 90
AD26	SDIO_D0	DB	1	SDIO Data0
	GPIO_91	DB		General Purpose IO 91
AD27	NAND_ALE	DO	-	NAND Flash Address Latch Enable
	GPIO_65	DB		General Purpose IO 65
AD28	NAND_CLE	DO	-	NAND Flash Command Latch Enable
	eMMC_CLK	DO		eMMC Clock Output
AE1	NC	-	-	-
AE2	NC	-	-	-
AE3	HDMIRX_CEC	AB	-	HDMI RX Consumer Electronics Control
AE5	NC	-	-	-
AE6	HDMIRX_CKN	AI	-	HDMI RX clock input pair -
AE8	HDMIRX_D0P	AI	-	HDMI RX Data Pair 0+
AE9	HDMIRX_D1N	AI	-	HDMI RX Data Pair 1-
AE11	HDMIRX_D2P	AI	-	HDMI RX Data Pair 2+
AE12	DP_LANE4N	AO	-	DP lane 4 TX negative
AE14	DP_LANE2P	AO	-	DP lane 2 TX positive
AE15	DP_LANE1N	AO	-	DP lane 1 TX negative
AE17	GPIO_26	DB	1	General Purpose IO 26
	TP1_CLK	DI		Transport stream 1 clock
	I2C2_SCL	DB		I2C Serial Clock Output

Pin No.	Pin Name	I/O	Default Value	Description
AE18	TP1_VALID	DI	1	Transport stream 1 data valid
	GPIO_27	DB		Isolation General Purpose IO 27
	I2C3_SCL	DB		I2C Serial Clock Output
AE20	GPIO_95	DB	1	General Purpose IO 95
	PCIE1_CLKREQ	DB		PCI Express reference clock request signal
AE21	PCIE1_TXP	AO	-	PCI Express TX+
AE23	SD_CD	DI	1	SD/MMC Card Detect
	GPIO_84	DB		General Purpose IO 84
AE24	SD_D0	DB	0	SD/MMC Data0
	GPIO_85	DB		General Purpose IO 85
	AJ_RST#	DI		EJTAG test reset input
AE26	NAND_VDD	PWR	-	NAND & eMMC Pin Power
AE27	NAND_D0	DB	1	NAND Flash Data 0
	eMMC_D0	DB		eMMC Data 0
AE28	NAND_WR#	DO	1	NAND Flash Write Enable
	GPIO_67	DB		General Purpose IO 67
AF1	NC	-	-	-
AF2	NC	-	-	-
AF3	ADAC_GND	GND	-	Audio DAC Ground
AF4	GND	GND	-	Digital Ground
AF5	NC	-	-	-
AF6	HDMIRX_CKP	AI	-	HDMI RX clock input pair +
AF8	HDMIRX_D0N	AI	-	HDMI RX Data Pair 0-
AF9	GND	GND	-	Digital Ground
AF11	HDMIRX_D2N	AI	-	HDMI RX Data Pair 2-
AF12	GND	GND	-	Digital Ground
AF14	DP_LANE2N	AO	-	DP lane 2 TX negative
AF15	DP_LANE1P	AO	-	DP lane 1 TX positive
AF17	GND	GND	-	Digital Ground
AF18	SPI_SI	DB	-	Serial Flash Controller Data Input
AF20	GPIO_100	DB	1	General Purpose IO 100
AF21	PCIE1_TXN	AO	-	PCI Express TX-
AF23	SD_WP	DI	1	SD/MMC Write Protect
	GPIO_83	DB		General Purpose IO 83
	AJ_TDI	DI		EJTAG Test Data Input
AF24	SD_D1	DB	0	SD/MMC Data1
	GPIO_86	DB		General Purpose IO 86
AF25	GND	GND	-	Digital Ground
AF26	NAND_D5	DB	1	NAND Flash Data 5
	eMMC_D5	DB		eMMC Data 5
	EJ_RST#	DI		JTAG Reset
AF27	NAND_D2	DB	1	NAND Flash Data 2
	eMMC_D2	DB		eMMC Data 2

Pin No.	Pin Name	I/O	Default Value	Description
AF28	NAND_D1	DB	1	NAND Flash Data 1
	eMMC_D1	DB		eMMC Data 1
AG1	NC	-	-	-
AG2	CVBS	AO	-	Composite output
AG3	AO_L	AO	-	Audio DAC Output Left Channel
AG4	AO_R	AO	-	Audio DAC Output Right Channel
AG5	AIR	AI	-	Audio line input right channel
AG6	MIC1R	AI	-	Analog microphone right channel (differential pad)
AG7	MIC2R	AI	-	Analog microphone right channel (differential pad)
AG8	IGPIO_26	DB	1/ 5V tolerance	Isolation General Purpose IO 26
	I2C6_SDA	DB		I2C Serial Data
AG9	GPIO_56	DB	1	General Purpose IO 56
	DMIC_DATA	DI		Digital MIC data
	AI_LRCK	DB		AI I2S word select output to ADC
AG10	GPIO_58	DB	-	General Purpose IO 58
	AO_BCK	DB		I2S bit clock output to DAC.
AG11	GPIO_60	DB	1	General Purpose IO 60
	AO_D0	DO		I2S serial data output 0
AG12	GPIO_62	DB	1	General Purpose IO 62
	AICK	DO		AI 256x clock output to ADC
	AO_D2	DO		I2S serial data output 2
AG13	GPIO_54	DB	1	General Purpose IO 54
	SPDIF	DO		IEC 60958 (SPDIF) Output
AG14	DP_AUXN	AB	-	A port A pair positive OUTN
AG15	GPIO_14	DB	1	General Purpose IO 14
	I2C5_SDA	DB		I2C Serial Data Signal
	NF_CE3#	DO		NAND Flash chip_enable[3]
AG16	GPIO_22	DB	1	General Purpose IO 22
	AI_BCK	DB		AI I2S bit clock output to ADC
	TP0_CLK	DI		Transport Stream 0 clock
AG17	TP0_SYNC	DI	1	Transport stream 0 sync.
	GPIO_24	DB		General Purpose IO 24
	AI_SDO	DI		AI I2S serial data input from ADC
AG18	SPI_CE#	DO	1	Serial Flash Controller Chip Select Output
AG19	GPIO_97	DB	0	General Purpose IO 97
	P2S_DA	DO		Parallel in Serial output date
AG20	GPIO_99	DB	1	General Purpose IO 99
AG21	GPIO_5	DB	1	General Purpose IO 5
	GSPI_SCK	DO		Serial Interface Controller Clock
	AJ_TDI	DI		EJTAG test data input.
AG22	GPIO_7	DB	1	General Purpose IO 7
	GSPI_MOSI	DO		Serial Interface Controller Data Output
	AJ_TMS	DI		EJTAG test mode select input.

Pin No.	Pin Name	I/O	Default Value	Description
AG23	GPIO_9	DB	1/ 5V tolerance	General Purpose IO 9
	FAN_IN	DI		To detect Dc Fan Sensors
AG24	SD_CMD	DB	0	SD/MMC Command Line
	GPIO_81	DB		General Purpose IO 81
	AJ_TMS	DI		EJTAG test mode select input.
AG25	SD_D2	DB	0	SD/MMC Data2
	GPIO_87	DB		General Purpose IO 87
AG26	NAND_D7	DB	1	NAND Flash Data 7
	eMMC_D7	DB		eMMC Data 7
	EJ_TCLK	DI		JTAG Test Mode Clock
AG27	NAND_DQS	DB	-	Nand flash data strobe for double data rate
	GPIO_77	DB		General Purpose IO 77
AG28	NAND_D3	DB	1	NAND Flash Data 3
	eMMC_D3	DB		eMMC Data 3
AH1	NC	-	-	-
AH2	GND	GND	-	Digital Ground
AH3	ADAC_GND	GND	-	Audio DAC Ground
AH4	AIL	AI	-	Audio line input left channel
AH5	MIC1L	AI	-	Analog microphone left channel (differential pad)
AH6	MIC2L	AI	-	Analog microphone left channel (differential pad)
AH7	MICBIAS	AO	-	MICBIAS output
AH8	IGPIO_20	DB	1/ 5V tolerance	Isolation General Purpose IO 20
	I2C6_SCL	DB		I2C Serial Clock
AH9	GPIO_55	DB	1	General Purpose IO 55
	AI_BCK	DB		AI I2S bit clock output to ADC
	DMIC_CLK	DO		Digital MIC clock output
AH10	GPIO_57	DB	-	General Purpose IO 57
	AO_LRCK	DB		I2S word select output to DAC
AH11	GPIO_59	DB	1	General Purpose IO 59
	AO_CK	DO		256x clock output to DAC.
AH12	GPIO_61	DB	1	General Purpose IO 61
	AO_D1	DO		I2S serial data output 1
AH13	GPIO_63	DB	1	General Purpose IO 63
	AI_SDO	DI		AI I2S serial data input from ADC
	AO_D3	DO		I2S serial data output 3
AH14	DP_AUXP	AB	-	A port A pair negative OUTP
AH15	GPIO_13	DB	1	General Purpose IO 13
	I2C5_SCL	DB		I2C Serial Clock Output
	NF_CE2#	DO		NAND Flash chip_enable[2]
AH16	TP0_DATA	DI	1	Transport Stream 0 data
	GPIO_21	DB		General Purpose IO 21
	AICK	DO		AI 256x clock output to ADC

Pin No.	Pin Name	I/O	Default Value	Description
AH17	TP0_VALID	DI	1	Transport stream 0 data valid
	GPIO_23	DB		General Purpose IO 23
	AI_LRCK	DO		I2S Word Select Clock Output to ADC
AH18	SPI_CK	DO	-	Serial Flash Controller Clock
AH19	SPI_SO	DB	-	Serial Flash Controller Data Output
AH20	GPIO_98	DB	0	General Purpose IO 98
	P2S_CK	DO		Parallel in Serial Clock output
AH21	GPIO_4	DB	1	General Purpose IO 4
	GSPI_MISO	DI		Serial Interface Controller Data Input
	AJ_RST#	DI		EJTAG test reset input.
AH22	GPIO_6	DB	1	General Purpose IO 6
	GSPI_CS	DO		Serial Interface Controller Chip Select Output
	AJ_TDO	DO		EJTAG test data output
AH23	GPIO_8	DB	1	Isolation General Purpose IO 8
	AJ_TCLK	DI		EJTAG test clock input.
AH24	SD_CLK	DO	0	SD/MMC Clock Output
	GPIO_82	DB		General Purpose IO 82
	AJ_TDO	DO		EJTAG test data output
AH25	SD_D3	DB	0	SD/MMC Data3
	GPIO_88	DB		General Purpose IO 88
	AJ_TCLK	DI		EJTAG test clock input
AH26	eMMC_DQS	DI	0	EMMC HS400 Data Strobe (200Mhz)
	GPIO_80	DB		General Purpose IO 80
AH27	NAND_D6	DB	1	NAND Flash Data 6
	eMMC_D6	DB		eMMC Data 6
	EJ_TMS	DI		JTAG Test Mode Select
AH28	NAND_D4	DB	1	NAND Flash Data 4
	eMMC_D4	DB		eMMC Data 4

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8. System Global Resources

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 2. Power Supply Specification

Symbol		Min.	Max.	Unit	Description
CPU_DVS		-0.4	1.15	V	Voltage on power pin for CPU
GPU_DVS		-0.4	1.15	V	Voltage on power pin for GPU
MEM_DVS		-0.4	1.15	V	Voltage on power pin for L2 Cache
1V		-0.4	1.15	V	Supply voltage on power pin for Analog or Digital Logic
ISO_1V		-0.4	1.15	V	Voltage on power pin for Isolated Block Logic
DDR_VIO	For DDR3	-0.4	1.65	V	Voltage on power pin for DDR controller
	For DDR3L		1.485		
	For DDR4		1.32		
1.8V		-0.4	1.98	V	Supply voltage on power pin for Analog or Digital Logic
3.3V		-0.4	3.63	V	Voltage on power pin for I/O Pad, Analog or Digital Logic
RTCVDD		-0.4	3.63	V	Voltage on power pin for RTC Block
DC input		-0.4	Corresponding Supply Voltage +0.4	V	Input voltage on any I/O pin
DC output		-0.4	Corresponding Supply Voltage +0.4	V	Output voltage on any I/O pin
Tstg		-55	150	°C	Storage temperature

8.2. Recommended Operating Conditions

It is important to provide adequate power and ground for high-speed digital and sensitive analog design. To achieve the best quality, the power and ground pins are separated into several groups. The DC voltage listed in Table 3 does not include ripple.

Table 3. Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit	Description
CPU_DVS	0.78	1.0	1.12	V	Voltage on power pin for CPU
GPU_DVS	0.88	1.0	1.12	V	Voltage on power pin for GPU
MEM_DVS	0.88	0.9	1.02	V	Voltage on power pin for L2 Cache
1V	0.95	1.0	1.05	V	Supply voltage on power pin for Analog or Digital Logic
ISO_1V	0.95	1.0	1.05	V	Voltage on power pin for Isolated Block Logic

Symbol		Min.	Typ.	Max.	Unit	Description
DDR_VIO	For DDR3	1.425	1.5	1.575	V	Voltage on power pin for DDR controller
	For DDR3L	1.2825	1.35	1.4175		
	For DDR4	1.14	1.2	1.26		
1.8V		1.71	1.8	1.89	V	Supply voltage on power pin for Analog or Digital Logic
3.3V		3.135	3.3	3.465	V	Voltage on power pin for I/O Pad, Analog or Digital Logic
RTCVDD		1.5	3.3	3.465	V	Voltage on power pin for RTC Block
Tj		0	-	125	°C	Junction Temperature

Table 4. DC Characteristics

Symbol		Min.	Typ.	Max.	Unit	Description
V_{OH}	For DDR_VIO	-	0.9*DDR_VIO	-	V	Minimum high level output voltage
	For 1.8V I/O	1.45**	-	-		
	For 3.3V I/O	2.6**	-	-		
V_{OL}	For DDR_VIO	-	0.1*DDR_VIO	-	V	Maximum low level output voltage
	For 1.8V I/O	-	-	0.45*		
	For 3.3V I/O	-	-	0.39*		
V_{IH}	For DDR_VIO	0.5*DDR_VIO +0.100	-	DDR_VIO	V	Maximum high level input voltage
	For 1.8V I/O	1.27	-	-		
	For 3.3V I/O	2.2	-	-		
V_{IL}	For DDR_VIO	0	-	0.5*DDR_VIO -0.100	V	Maximum low level input voltage
	For 1.8V I/O	-	-	0.58		
	For 3.3V I/O	-	-	0.78		

**Test Condition: IOL=2mA*

***Test Condition: IOH=-2mA*

8.3. Power Management

The RTD1296 provides a Sleep Mode that shuts down all PLLs and logic to save power during idle state. Sleep Mode is entered via a software instruction sequence, and exited by a hardware reset. External wake-up events may be selected to automatically generate a wake-up reset.

For lower power consumption in Sleep Mode, all parts of the RTD1296 can be powered off except for the isolation block. The wake-up function still works in this Sleep Mode.

Some RTD1296 modules can be individually powered down by gating off their clock tree. Those modules can be powered on without resetting the whole chip.

8.4. Power Ripple

Table 5. Power Ripple

Symbol		Max.	Unit	Description
CPU_DVS		70	mV	Voltage on power pin for CPU
GPU_DVS		60	mV	Voltage on power pin for GPU
MEM_DVS		40	mV	Voltage on power pin for L2 Cache
1V		40	mV	Supply voltage on power pin for Analog or Digital Logic
ISO_1V		40	mV	Voltage on power pin for Isolated Block Logic
DDR_VIO	For DDR3	50	mV	Voltage on power pin for DDR controller
	For DDR3L			
	For DDR4			
1.8V		40	mV	Supply voltage on power pin for Analog or Digital Logic
3.3V		40	mV	Voltage on power pin for I/O Pad, Analog or Digital Logic
RTCVDD		60	mV	Voltage on power pin for RTC Block

8.5. Crystal Requirements

Table 6. Crystal Requirements for the RTD1296

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	27	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C	-30	-	30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C	-30	-	30	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle	-	-	-	%
ESR	Equivalent Series Resistance	-	-	40	Ω
Jitter	Broadband Peak-to-Peak Jitter	-	-	-	ps
DL	Drive Level	-	-	-	mW

8.6. Reset, Clock, and PLL

Table 7. System Global Resources External Pin Description

Pin Name	Type	Description
RESET#	DI	Chip Reset, Schmitt Trigger Input
XTLI	AI	System Clock 27MHz
XTLO	AO	System Clock 27MHz
REXT	PWR	Bandgap Voltage of Whole Chip. Connect to GND via a 6.19KΩ, ±1% Resistor

The external RESET# signal is a low active Schmitt trigger input. To take effect, it must be held low for at least 500ns. An external crystal (27MHz) is required for normal function, and the embedded PLL circuit will generate all necessary clock signals for various modules. The crystal accuracy should be under 30ppm to ensure the best quality.

8.7. Thermal Considerations

To maintain a stable operating condition, the system designer should stay within maximum temperature limits.

Table 8. Thermal Parameters for the RTD1296

Thermal Resistance	Value	Comment
Theta JA	16.06 (°C/W)	References: EIA/JESD51-2, EIA/JESD51-8, EIA/JESD51-7
Theta JC	2.05 (°C/W)	
Theta JB	8.03 (°C/W)	

8.8. Power-On Sequence

Generally, the power-on sequence should be as follows:

- Apply RTCVDD.
- Apply CPU_DVS, GPU_DVS, ISO_1V, 1V simultaneously
- Apply DDR_VIO, 3.3V, 1.8V, MEM_DVS in sequence
- Wait for power supplies to stabilize
- Reset operation completes
- System boots up

The RTD1296 integrates a Power-On-Reset (POR) circuit to ensure the chip powers up in a default state. It monitors the status of 3.3V and CPU_DVS. The POR circuit reset will release after 2^{20} crystal clock cycles when both powers (3.3V & 1.8V) are stable. Figure 5 graphically shows the Power-On sequence timing. The detailed duration is listed in Table 9.

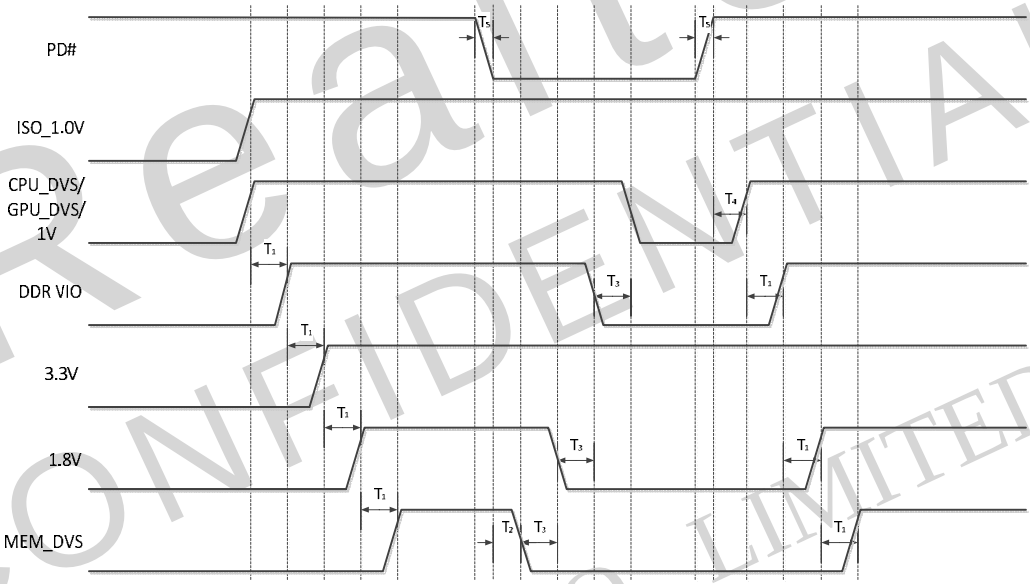


Figure 5. Power-On Sequence Timing Diagram

Table 9. Power-On Sequence Duration

Symbol	Description	Min	Typical	Max	Unit
T1	90% voltage delay between rails	1		10	ms
T2	50% voltage delay after PD# low	1		10	ms
T3	50% voltage delay between rails	1		10	ms
T4	90% voltage delay after PD# high	1		10	ms
T5	PD# rise and fall time	0		1	ms

Table 10. Power-On Reset Trigger Level

Power Rail	Power-On Reset Trigger Level (V)
CPU_DVS	0.5
GPU_DVS	0.5
1V	0.5
ISO_1V	0.5
MEM_DVS	0.5
DDR_VIO	Don't Care
1.8V	Don't Care
3.3V	2.1

Note: The IC will enter power on state if the power rails indicate above values.

9. DDR Controller Unit

9.1. DDR3/DDR4 Controller Unit

The RTD1296 DDR3/4 Controller Unit (DCU) provides memory control signals required for external DDR3 SDRAM access. With two channels of 32-bit-wide DDR3 SDRAM, the DCU can access up to 4GB.

9.1.1. Features

- Supports up to 4GB
- Supports Spread Spectrum Clocking (SSC)
- Supports Scrambling
- 1.35V/1.5V compatible DDR3L/DDR3 I/O
- 1.2V compatible DDR4 I/O

9.1.2. DCU Block External Pin Description

Table 11. DCU Block External Pin Description

Pin Name	Type	Description
Channel0_DDR3_CK/DDR4_CK_t	DO	Channel 0 DDR3/4 Clock Positive Output
Channel0_DDR3_CK#/DDR4_CK_c	DO	Channel 0 DDR3/4 Clock Negative Output
Channel0_DDR3/4_CKE	DO	Channel 0 DDR3/4 Clock Enable Output
Channel0_DDR3/4_ODT	DO	Channel 0 DDR3/4 On-Die Termination
Channel0_DDR3/4_CS#	DO	Channel 0 DDR3/4 Chip Select Output
Channel0_DDR3/4_RAS#	DO	Channel 0 DDR3/4 Row Address Select Output
Channel0_DDR3/4_CAS#	DO	Channel 0 DDR3/4 Column Address Select Output
Channel0_DDR3/4_WE#	DO	Channel 0 DDR3/4 Write Enable Output
Channel0_DDR3/4_RESET#	DO	Channel 0 DDR3/4 Reset
Channel0_DDR3_DQS0/DDR4_DQS0_t	DB	Channel 0 DDR3/4 DQ[7:0] Data Strobe
Channel0_DDR3_DQS0#/DDR4_DQS0_c	DB	Channel 0 DDR3/4 DQ[7:0] Data Strobe
Channel0_DDR3_DQS1/DDR4_DQS1_t	DB	Channel 0 DDR3/4 DQ[15:8] Data Strobe
Channel0_DDR3_DQS1#/DDR4_DQS1_c	DB	Channel 0 DDR3/4 DQ[15:8] Data Strobe
Channel0_DDR3_DQS2/DDR4_DQS2_t	DB	Channel 0 DDR3/4 DQ[23:16] Data Strobe
Channel0_DDR3_DQS2#/DDR4_DQS2_c	DB	Channel 0 DDR3/4 DQ[23:16] Data Strobe
Channel0_DDR3_DQS3/DDR4_DQS3_t	DB	Channel 0 DDR3/4 DQ[31:24] Data Strobe
Channel0_DDR3_DQS3#/DDR4_DQS3_c	DB	Channel 0 DDR3/4 DQ[31:24] Data Strobe
Channel0_DDR3/4_DM0	DO	Channel 0 DDR3/4 DQ[7:0] Data Mask
Channel0_DDR3/4_DM1	DO	Channel 0 DDR3/4 DQ[15:8] Data Mask
Channel0_DDR3/4_DM2	DO	Channel 0 DDR3/4 DQ[23:16] Data Mask
Channel0_DDR3/4_DM3	DO	Channel 0 DDR3/4 DQ[31:24] Data Mask
Channel0_DDR3/4_A[15:0]	DO	Channel 0 DDR3/4 Address[15:0]

Pin Name	Type	Description
Channel0_DDR3_BA[2:0]	DO	Channel 0 DDR3 Bank Address[2:0]
Channel0_DDR4_BA[1:0]	DO	Channel 0 DDR4 Bank Address[1:0]
Channel0_DDR4_BG0	DO	Channel 0 DDR4 Bank Group 0
Channel0_DDR3/4_DQ[31:0]	DB	Channel 0 DDR3/4 Data[31:0]
Channel0_DDR4_ACT#	DO	Channel 0 DDR4 Activation Command
Channel0_DDR4_PAR	DO	Channel 0 DDR4 Command and Address Parity
Channel0_DDR3/4_ALERT#	DB	Channel 0 DDR4 Alert
Channel0_DDR4_TEN	DO	Channel 0 DDR4 Connectivity Enable
Channel1_DDR3_CK/DDR4_CK_t	DO	Channel 1 DDR3/4 Clock Positive Output
Channel1_DDR3_CK#/DDR4_CK_c	DO	Channel 1DDR3/4 Clock Negative Output
Channel1_DDR3/4_CKE	DO	Channel 1DDR3/4 Clock Enable Output
Channel1_DDR3/4_ODT	DO	Channel 1DDR3/4 On-Die Termination
Channel1_DDR3/4_CS#	DO	Channel 1DDR3/4 Chip Select Output
Channel1_DDR3/4_RAS#	DO	Channel 1DDR3/4 Row Address Select Output
Channel1_DDR3/4_CAS#	DO	Channel 1DDR3/4 Column Address Select Output
Channel1_DDR3/4_WE#	DO	Channel 1DDR3/4 Write Enable Output
Channel1_DDR3/4_RESET#	DO	Channel 1DDR3/4 Reset
Channel1_DDR3_DQS0/DDR4_DQS0_t	DB	Channel 1DDR3/4 DQ[7:0] Data Strobe
Channel1_DDR3_DQS0#/DDR4_DQS0_c	DB	Channel 1DDR3/4 DQ[7:0] Data Strobe
Channel1_DDR3_DQS1/DDR4_DQS1_t	DB	Channel 1DDR3/4 DQ[15:8] Data Strobe
Channel1_DDR3_DQS1#/DDR4_DQS1_c	DB	Channel 1DDR3/4 DQ[15:8] Data Strobe
Channel1_DDR3_DQS2/DDR4_DQS2_t	DB	Channel 1DDR3/4 DQ[23:16] Data Strobe
Channel1_DDR3_DQS2#/DDR4_DQS2_c	DB	Channel 1DDR3/4 DQ[23:16] Data Strobe
Channel1_DDR3_DQS3/DDR4_DQS3_t	DB	Channel 1DDR3/4 DQ[31:24] Data Strobe
Channel1_DDR3_DQS3#/DDR4_DQS3_c	DB	Channel 1DDR3/4 DQ[31:24] Data Strobe
Channel1_DDR3/4_DM0	DO	Channel 1DDR3/4 DQ[7:0] Data Mask
Channel1_DDR3/4_DM1	DO	Channel 1DDR3/4 DQ[15:8] Data Mask
Channel1_DDR3/4_DM2	DO	Channel 1DDR3/4 DQ[23:16] Data Mask
Channel1_DDR3/4_DM3	DO	Channel 1DDR3/4 DQ[31:24] Data Mask
Channel1_DDR3/4_A[15:0]	DO	Channel 1DDR3/4 Address[15:0]
Channel1_DDR3_BA[2:0]	DO	Channel 1DDR3 Bank Address[2:0]
Channel1_DDR4_BA[1:0]	DO	Channel 1DDR4 Bank Address[1:0]
Channel1_DDR4_BG0	DO	Channel 1DDR4 Bank Group 0
Channel1_DDR3/4_DQ[31:0]	DB	Channel 1DDR3/4 Data[31:0]
Channel1_DDR4_ACT#	DO	Channel 1DDR4 Activation Command
Channel1_DDR4_PAR	DO	Channel 1DDR4 Command and Address Parity
Channel1_DDR4_ALERT#	DB	Channel 1DDR4 Alert
Channel1_DDR4_TEN	DO	Channel 1DDR4 Connectivity Enable

9.2. LPDDR2/LPDDR3 Controller Unit

The RTD1296 LPDDR2/3 Controller Unit provides low power memory control signals required for external LPDDR2/3 SDRAM access. With two channels 32-bit-wide LPDDR2/3 SDRAM, the DCU can access up to 2GB.

9.2.1. Features

- Supports up to 2GB
- Supports Spread Spectrum Clocking (SSC)
- Supports Scrambling
- 1.2V compatible LPDDR2/LPDDR3 I/O

9.2.2. LPDDR2/LPDDR3 Block External Pin Description

Table 12. LPDDR2/LPDDR3 Block External Pin Description

Pin Name	Type	Description
Channel0_LPDDR2/3_CK_t	DO	Channel 0 LPDDR2/3 Clock Positive Output
Channel0_LPDDR2/3_CK_c	DO	Channel 0 LPDDR2/3 Clock Negative Output
Channel0_LPDDR2/3_CKE	DO	Channel 0 LPDDR2/3 Clock Enable Output
Channel0_LPDDR3_ODT	DO	Channel 0 LPDDR3 On-Die Termination
Channel0_LPDDR2/3_CS#	DO	Channel 0 LPDDR2/3 Chip Select Output
Channel0_LPDDR2/3_DQS0_t	DB	Channel 0 LPDDR2/3 DQ[7:0] Data Strobe
Channel0_LPDDR2/3_DQS0_c	DB	Channel 0 LPDDR2/3 DQ[7:0] Data Strobe
Channel0_LPDDR2/3_DQS1_t	DB	Channel 0 LPDDR2/3 DQ[15:8] Data Strobe
Channel0_LPDDR2/3_DQS1_c	DB	Channel 0 LPDDR2/3 DQ[15:8] Data Strobe
Channel0_LPDDR2/3_DQS2_t	DB	Channel 0 LPDDR2/3 DQ[23:16] Data Strobe
Channel0_LPDDR2/3_DQS2_c	DB	Channel 0 LPDDR2/3 DQ[23:16] Data Strobe
Channel0_LPDDR2/3_DQS3_t	DB	Channel 0 LPDDR2/3 DQ[31:24] Data Strobe
Channel0_LPDDR2/3_DQS3_c	DB	Channel 0 LPDDR2/3 DQ[31:24] Data Strobe
Channel0_LPDDR2/3_DM0	DO	Channel 0 LPDDR2/3 DQ[7:0] Data Mask
Channel0_LPDDR2/3_DM1	DO	Channel 0 LPDDR2/3 DQ[15:8] Data Mask
Channel0_LPDDR2/3_DM2	DO	Channel 0 LPDDR2/3 DQ[23:16] Data Mask
Channel0_LPDDR2/3_DM3	DO	Channel 0 LPDDR2/3 DQ[31:24] Data Mask
Channel0_LPDDR2/3_CA[9:0]	DO	Channel 0 LPDDR2/3 Command/Address[9:0]
Channel0_LPDDR2/3_DQ[31:0]	DB	Channel 0 LPDDR2/3 Data[31:0]
Channel1_LPDDR2/3_CK_t	DO	Channel 1 LPDDR2/3 Clock Positive Output
Channel1_LPDDR2/3_CK_c	DO	Channel 1 LPDDR2/3 Clock Negative Output
Channel1_LPDDR2/3_CKE	DO	Channel 1 LPDDR2/3 Clock Enable Output
Channel1_LPDDR3_ODT	DO	Channel 1 LPDDR3 On-Die Termination
Channel1_LPDDR2/3_CS#	DO	Channel 1 LPDDR2/3 Chip Select Output
Channel1_LPDDR2/3_DQS0_t	DB	Channel 1 LPDDR2/3 DQ[7:0] Data Strobe
Channel1_LPDDR2/3_DQS0_c	DB	Channel 1 LPDDR2/3 DQ[7:0] Data Strobe

Pin Name	Type	Description
Channel1_LPDDR2/3_DQS1_t	DB	Channel 1 LPDDR2/3 DQ[15:8] Data Strobe
Channel1_LPDDR2/3_DQS1_c	DB	Channel 1 LPDDR2/3 DQ[15:8] Data Strobe
Channel1_LPDDR2/3_DQS2_t	DB	Channel 1 LPDDR2/3 DQ[23:16] Data Strobe
Channel1_LPDDR2/3_DQS2_c	DB	Channel 1 LPDDR2/3 DQ[23:16] Data Strobe
Channel1_LPDDR2/3_DQS3_t	DB	Channel 1 LPDDR2/3 DQ[31:24] Data Strobe
Channel1_LPDDR2/3_DQS3_c	DB	Channel 1 LPDDR2/3 DQ[31:24] Data Strobe
Channel1_LPDDR2/3_DM0	DO	Channel 1 LPDDR2/3 DQ[7:0] Data Mask
Channel1_LPDDR2/3_DM1	DO	Channel 1 LPDDR2/3 DQ[15:8] Data Mask
Channel1_LPDDR2/3_DM2	DO	Channel 1 LPDDR2/3 DQ[23:16] Data Mask
Channel1_LPDDR2/3_DM3	DO	Channel 1 LPDDR2/3 DQ[31:24] Data Mask
Channel1_LPDDR2/3_CA[9:0]	DO	Channel 1 LPDDR2/3 Command/Address[9:0]
Channel1_LPDDR2/3_DQ[31:0]	DB	Channel 1 LPDDR2/3 Data[31:0]

9.3. DCU Block Pin Mux Table

Table 13. DCU Block External Pin Mux Table

Ball Number		DDR3	DDR4	LPDDR3
Channel 0	Channel 1	Channel 0/1		
Y26	D24	DQ13	DQ14	DQ31
AA25	F22	DQ11	DQ12	DQ30
Y28	A27	DQ6	DQ4	DQ29
AA27	B27	DQ4	DQ6	DQ28
Y24	C24	DQ15	DQ8	DQ27
Y25	C25	DQ9	DQ10	DQ26
W28	A26	DQ0	DQ2	DQ25
Y27	B26	DQ2	DQ0	DQ24
Y23	E23	DM1	DM1	DM3
V27	B24	DM0	DM0	DM1
U26	E21	DQ14	DQ15	DQ15
U25	F21	DQ12	DQ11	DQ14
U27	B23	DQ3	DQ3	DQ13
U28	A24	DQ1	DQ1	DQ12
U23	D21	DQ8	DQ13	DQ11
U24	C21	DQ10	DQ9	DQ10
T27	B22	DQ5	DQ7	DQ9
T28	A23	DQ7	DQ5	DQ8
P28	A21	CKE	CKE	CKE
R24	D20	ODT	ODT	ODT
P27	B20	CSN_0	CSN_0	CSN
N27	B19	A16	RASN/A16	CA9
R25	E20	RASN	WEN/A14	-
P25	F18	CASN	ACTN	-

Ball Number		DDR3	DDR4	LPDDR3
Channel 0	Channel 1	Channel 0/1		
M28	A19	A10	A12	CA8
M27	B18	A15	CASN/A15	CA7
N28	A20	CSN_1	CSN_1	-
P26	E18	WEN	BG0	-
L28	A18	A12	A3	CA6
L27	B17	BA1	BA1	CA5
P24	C18	BA0	A10	-
P23	D18	BA2	BA0	-
K28	A17	A1	TEN	-
K27	B16	A4	A1	CA4
M24	D17	A3	A4	-
M25	E17	A0	A6	-
J28	A16	A11	A5	CA3
J27	B15	ALT	ALERTN	-
L25	F15	A5	A0	-
L26	E15	A2	A8	-
H28	A15	A6	A9	CA2
H27	B14	A14	A7	CA1
L24	C15	A7	A2	-
L23	D15	A9	A11	-
G28	A14	A8	A13	CA0
J24	D14	RSTN	RSTN	-
J25	E14	A13	PAR	-
H24	C12	DQ29	DQ30	DQ7
H25	F12	DQ27	DQ28	DQ6
F28	A13	DQ22	DQ20	DQ5
G27	B13	DQ20	DQ22	DQ4
H23	D12	DQ31	DQ24	DQ3
H26	E12	DQ25	DQ26	DQ2
E28	A12	DQ16	DQ18	DQ1
F27	B12	DQ18	DQ16	DQ0
G24	D11	DM3	DM3	DM0
D27	B10	DM2	DM2	DM2
E25	D9	DQ30	DQ31	DQ23
E26	C9	DQ28	DQ27	DQ22
C27	B9	DQ19	DQ19	DQ21
C28	A10	DQ17	DQ17	DQ20
D26	D8	DQ24	DQ29	DQ19
G23	E8	DQ26	DQ25	DQ18
A28	B8	DQ21	DQ23	DQ17
B28	A9	DQ23	DQ21	DQ16

10. Flash Controller

The flash controller supports Serial NOR flash memory and 8-bit NAND type flash memory. Each type could be configured as boot device.

10.1. Features

- Serial NOR Flash
  - Supports up to 32MB
  - Supports dual I/O read
  - Complies with MXIC protocol
- NAND Flash
  - Built-in SRAM buffer to improve performance
  - Built-in 6/12/24/40/43/65/72-bit ECC mechanism to enhance data reliability
  - Built-in randomizer to enhance data reliability
  - Supports up to 2 flash chips with interleave accessing
  - Supports ONFI2.2 and toggle DDR1.0

10.2. Serial Flash Block External Pin Description

Table 14. Serial Flash Block External Pin Description

Pin Name	Type	Description
SPI_CE#	DO	Serial Flash Chip Select Output
SPI_CK	DO	Serial Flash Clock
SPI_SI/SIO0	DB	Serial Flash Data Input (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)
SPI_SO/SIO1	DB	Serial Flash Data Output (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)

10.3. NAND Flash Block External Pin Description

Table 15. NAND Flash Block External Pin Description

Pin Name	Type	Description
NAND_CLE	DO	NAND Flash Command Latch Enable
NAND_ALE	DO	NAND Flash Address Latch Enable
NAND_RD#	DO	NAND Flash Read Enable
NAND_WR#	DO	NAND Flash Write Enable
NAND_RDY	DI	NAND Flash Ready
NAND_CE[1:0]#	DO	NAND Flash Chip Enable[1:0]
NAND_D[7:0]	DB	NAND Flash Data[7:0]

10.4. Boot Device Selection

Table 16. Boot Device Selection

Boot Device	Boot from ROM	BOOT_SEL	GPIO57	GPIO58
NOR	No	1	x	x
NOR(ROM)	Yes	0	1	0
eMMC	Yes	0	0	1
USB Device	Yes	0	1	1
NAND	Yes	0	0	0

11. eMMC Controller

The eMMC controller supports eMMC. The data bit width is up to 8 bits. As pins are shared with NAND flash, the system can boot from eMMC, NAND, or serial NOR.

11.1. Features

- Supports eMMC 5.0
- Bus width: 1-bit, 4-bit, 8-bit
- Bus speed: Backwards compatibility with legacy MMC card, High speed SDR, HS200, HS400
- Voltage: 1.8V and 3.3V

11.2. eMMC Block External Pin Description

Table 17. eMMCReader Block External Pin Description

Pin Name	Type	Description
eMMC_RST#	DO	eMMC reset signal
eMMC_CLK	DO	eMMC Clock Output
eMMC_CMD	DB	eMMC Command Line
eMMC_D[7:0]	DB	eMMC Data[7:0]
eMMC_DQS	DI	eMMC data strobe

11.3. NAND/eMMC Pin Mux Description

Table 18. NAND/eMMC Pin Mux Description

NAND Flash Pin	eMMC Pin
NAND_CLE	eMMC_CLK
NAND_DD0	eMMC_DD0
NAND_DD1	eMMC_DD1
NAND_DD2	eMMC_DD2
NAND_DD3	eMMC_DD3
NAND_DD4	eMMC_DD4
NAND_DD5	eMMC_DD5
NAND_DD6	eMMC_DD6
NAND_DD7	eMMC_DD7
NAND_RD#	eMMC_CMD
NAND_RDY	eMMC_RST#

12. General SPI Interface

The low pin-count is the most important benefit of the Serial Peripheral Interface (SPI). The General SPI controller (G-SPI) is used to control devices with an SPI interface, such as SPI flash or A/D converters. In normal mode, SO is serial data output port, SI is serial data input port. In dual lane mode, both SI and SO are serial input/outputs.

12.1. Features

- Frequency: 0.395MHz~50.625MHz
- Single and dual IO modes
- Phase and polarity are changeable
- Endian is configurable
- Command length: 1~32bits
- Address and dummy bit length: 0~32bits
- Read/write data length: 0~128bits
- Flexible timing: Tcs_high (CE falling edge to previous CE rising edge time), Tcs_end (last SCK rising edge to CE rising time), and Tcs_start (CE falling edge to first SCK rising edge time) are configurable

12.2. General SPI External Signal Description

Table 19. General SPI External Signal Description

Pin Name	Type	Description
GSPI_CS	DO	Serial Interface Controller Chip Select Output
GSPI_SCK	DO	Serial Interface Controller Clock
GSPI_MOSI/SIO0	DI	Serial Interface Controller Data Output (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)
GSPI_MISO/SIO1	DO	Serial Interface Controller Data Input (for 1 x I/O) / Serial Data Input & Output (for 2 x I/O Read Mode)

13. High-Speed UART

The RTD1296 provides a high-speed UART for external Bluetooth transceiver connection (data rate is up to 3MHz). With hardware auto flow and DMA control, data transmission is unhindered.

13.1. Features

- 32 bytes for each TX & RX FIFO
- UART1 supports H5
- Programmable data rate up to 3MHz
- Hardware auto flow control CTS/RTS signal with polarity selectable
- Interrupt output signal occurs whenever one of the several prioritized interrupt types is enabled and active
- Receive error
- Receive data available
- Character timeout
- Transmitter holding register empty or below threshold interrupt

13.2. High-Speed UART Module External Pin Description

Table 20. High-Speed UART Module External Pin Description

Pin Name	Type	Description
UR1_RX	DI	UART1 Receive Data Input
UR1_TX	DO	UART1 Transmit Data Output
UR1_CTS#	DI	UART1 Clear to Send Input
UR1_RTS#	DO	UART1 Request to Send Output
UR2_RX	DI	UART2 Receive Data Input
UR2_TX	DO	UART2 Transmit Data Output
UR2_CTS#	DI	UART2 Clear to Send Input
UR2_RTS#	DO	UART2 Request to Send Output

14. Peripherals

14.1. General Purpose I/O

The RTD1296 provides multiple GPIO pins. Each general-purpose pin can be individually configured as an input or output pin via the direction configuration register. The Data output and input register (refer to the RTD1296 AN02 GPIO Pin Mux Description.pdf document) can be used to control signals (high or low) when the GPIO pin is configured as output, and show the status when the GPIO pin is configured as input.

When a GPIO pin is configured as input, it can also be configured as an interrupt generator (set in the interrupt enable and detection polarity register) (refer to the RTD1296 AN02 GPIO Pin Mux Description.pdf document).

14.2. Universal Asynchronous Receiver and Transmitter

The RTD1296 provides two 16C550 compatible UARTs (Universal Asynchronous Receiver and Transmitter).

14.2.1. Features

- UART CH0 with 32-byte FIFO
- Programmable character properties, such as number of data bits per character (5~8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5, or 2)
- Interrupt output signal occurs whenever one of the several prioritized interrupt types are enabled and active
- Receive Error
- Receive Data Available
- Character Timeout
- Transmitter Holding Register Empty at or below threshold

14.2.2. UART Block External Pin Description

Table 21. UART Block External Pin Description

Pin Name	Type	Description
UR0_RX	DI	UART 0 Receive Data Input
UR0_TX	DO	UART 0 Transmit Data Output

14.3. I2C Serial Interface

The RTD1296 can support seven master/slave I2C-bus serial interfaces. A direct Serial Data Line (SDA) and Serial Clock Line (SCL) carry information between bus master and peripheral devices that are connected to the I2C-bus. The SDA and SCL lines are bi-directional.

14.3.1. Features

- Two-wire/Three-wire I2C serial interface
- Supports two speeds: Standard mode (100Kbps) and Fast mode (400Kbps)
- Clock synchronization
- Master or slave I2C operation
- Supports multi-Master operation (bus arbitration)
- 7-bit or 10-bit addressing
- 8-byte transmit and receive buffers
- 5V tolerance for I2C1_SCL, I2C1_SDA and I2C6_SCL, I2C6_SDA

14.3.2. I2C Block External Pin Description

Table 22. I2C Block External Pin Description

Pin Name	Type	Description
I2C0_SCL	DB	I2C Serial Clock Output
I2C0_SDA	DB	I2C Serial Data Signal
I2C1_SCL	DB	I2C Serial Clock Output
I2C1_SDA	DB	I2C Serial Data Signal
I2C2_SCL	DB	I2C Serial Clock Output
I2C2_SDA	DB	I2C Serial Data Signal
I2C3_SCL	DB	I2C Serial Clock Output
I2C3_SDA	DB	I2C Serial Data Signal
I2C4_SCL	DB	I2C Serial Clock Output
I2C4_SDA	DB	I2C Serial Data Signal
I2C5_SCL	DB	I2C Serial Clock Output
I2C5_SDA	DB	I2C Serial Data Signal
I2C6_SCL	DB	I2C Serial Clock Output
I2C6_SDA	DB	I2C Serial Data Signal

14.4. Infrared Receiver Controller

The RTD1296 Infrared Receiver controller is designed for receiving commands from consumer remote controllers. It receives signals from an external IR receiver, translates signal zeros into data zeros, and accumulates data bits that conform to the register setting requirements and buffers.

14.4.1. Features

- IR channel with 2 layers of 32-bit FIFO
- Supports Bi-phase Modulation (e.g., PHILIPS RC-5, RC-6A)
- Supports Pulse Width Modulation (e.g., SONY SIRC)
- Supports Pulse Position Modulation (e.g., NEC, SHARP, PHILIPS RC-MM)
- Address and command length up to 32 bits
- Supports RAW mode for software decode remote signal

14.4.2. IR RX Block External Pin Description

Table 23. IR RX Block External Pin Description

Pin Name	Type	Description
IR_RX	DI	Infrared Input from IR Receiver; 3.3V Tolerant
PWM_30Hz	DO	Output 30Hz square wave for RC-MM beacon signal; 3.3V Tolerant

14.5. Infrared Transmitter Controller

The RTD1296 Infrared Transmitter controller is designed for transmitting commands to a TV IR host.

14.5.1. Features

- IR channel with 2 layers of 32-bit FIFO
- Supports NEC and PHILIPS RC-5 protocol
- Address and command length up to 32 bits

14.5.2. IR TX Block External Pin Description

Table 24. IR TX Block External Pin Description

Pin Name	Type	Description
IR_TX	DO	Infrared Output to IR Transmitter; 3.3V Tolerant

14.6. Timer Control

The RTD1296 provides three 32-bit timers, a 90kHz timer, and a watchdog timer. The 32-bit timer and watchdog timer count at a fixed 27MHz rate. The 90kHz timer counts at 90kHz. The 32-bit timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. Hardware will automatically disable timer interrupts after a time-out in counter mode. Software must enable the timer interrupt and set the target value for the next usage.

14.6.1. Features

- Three sets of 32-bit timer hardware
- One 90kHz timer
- One watchdog timer
- 32-bit timer hardware can be configured to timer or counter mode
- Supports timer/counter pulse

14.7. Real Time Clock

The Real Time Clock (RTC) can be operated by the backup battery while the system power is off. The RTC data includes the time by half second, minute, hour, and date. The RTC works with an external 32.768kHz crystal and also can perform an alarm function.

14.7.1. Features

- Accepts 32.768kHz clock input
- Hex number data: Half-second, minute, hour, and date
- Programmable enable/disable half-second, minute, hour, date, and alarm interrupt
- Alarm function for system memory record
- RTC accuracy: 20ppm (under 60 seconds per month)
- Operating voltage: 1.5V up to 3.4V
- Low power consumption (2μA @ 3.3V)
- Supports reset function

14.7.2. RTC Block External Pin Description

Table 25. RTC Block External Pin Description

Pin Name	Type	Description
RTC_XI	AI	Real-Time Clock 32.768kHz
RTC_XO	AO	Real-Time Clock 32.768kHz
RTC_VDD	PWR	Power for Real Time Clock

14.8. LSADC (Low Speed ADC)

The RTD1296 provides a two-channel Low-speed ADC for keypad detection.

- 6-bit ADC
- Frequency: < 1MHz

Table 26. LSADC Interface

Pin Name	Type	Description
LSADC0	AI	Low Speed ADC0
LSADC1	AI	Low Speed ADC1

14.9. PWM (Pulse Width Modulation)

The RTD1296 provides four set Pulse Width Modulation (PWM) at two locations.

- Max/Min Frequency: 6.75MHz/1.6Hz

14.10. Smart Card Interface

The RTD1296 provides ISO 7816 compliant Smart Card Interfaces (each has a 32-byte FIFO) that support embedded Conditional Access (CA) applications.

14.10.1. Features

- Supports T=0, T=1 and T=14 protocol.

14.10.2. Smart Card Controller External Pin Description

Table 27. Smart Card Controller External Pin Description

Pin Name	Type	Description
SC_DATA	DB	Smart Card Input or Output for Serial Data
SC_RST#	DO	Smart Card Reset Signal
SC_CLK	DO	Smart Card Clock Signal
SC_CD	DI	Smart Card Card Detect Signal

14.11. DC Fan Control

The DC FAN rotation detect controller is made up of three parts; a de-bounce circuit, a timer, and a counter. The timer counts at 90KHz. Software can setup the timer target value to store the counter value.

When the timer value equals the set target value, the counter value will be stored in registers and the counter cleared. The counter counts via a FAN tachometer pulse signal. The FAN tachometer pulse signal has de-bounce to filter noise. Figure 6 shows the interface of a 4-wire DC Fan.

14.11.1. Features

- Supports 3/4-wire fan with tachometer input
- 32-bit timer for precision control
- Configurable de-bounce time for noise filtering
- 5V tolerance for tachometer input

14.11.2. DC Fan Control External Pin Description

Table 28. DC Fan Control External Pin Description

Pin Name	Type	Description
FAN_IN	DI	Fan speed detect (Tachometer input)

14.11.3. Typical 4-Wire Fan Interface

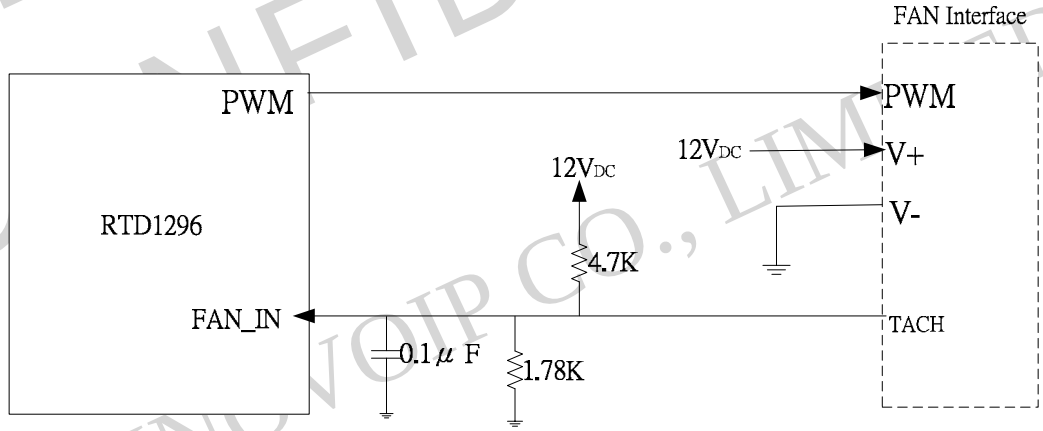


Figure 6. Typical 4-Wire Fan Interface

15. TV Encoder

The TV encoder encodes digital Y-Cb-Cr video data (4:2:2) to standard TV signal formats (NTSC or PAL) for CVBS. The supported TV formats are NTSC (M,J,4.43) or PAL (B, D, G, H, I, M, N, NC, 60).

The TV encoder supports multiple VBI encodings: Wide-Screen Signaling (WSS) or Teletext B for PAL, Copy Generation Management System (CGMS) for NTSC and Close Caption (CC) for both NTSC and PAL.

The TV encoder includes a 10-bit voltage output DAC.

15.1. Features

- On-chip 10-bit Digital-to-Analog Converter
- Supports VBI encoding: Wide-Screen Signaling (WSS), Teletext B, Copy Generation Management System (CGMS) and Close Caption (CC)
- Video encoding supports multi-composite format that includes NTSC[M, J, 4.43] and PAL [B, D, G, H, I, M, N, NC, 60]

15.2. TV Encoder Analog Output Interface

Table 29. TV Encoder Analog Output Interface

Pin Name	Type	Description
CVBS	AO	Composite Output

16. HDMI Transmitter

The RTD1296 incorporates a High-Definition Multimedia Interface (HDMI) transmitter; a fully functional single-link transmitter with High-bandwidth Digital Content Protection (HDCP). It transmits studio-quality video/audio to any HDMI/DVI/HDCP-enabled digital receiver. This module is compliant with the HDMI2.0, DVI 1.0, and HDCP specifications. The RTD1296 HDMI transmitter can also carry control and status information.

16.1. Features

- HDMI2.0a, HDCP, and DVI 1.0 compliant transmitter
  - Video Support

    Standard-Definition Video Format Timing:
    - -720 (1440) x 480i @ 59.94/60Hz
    - -720 (1440) x 576i @ 50Hz
    - -720 x 480p @ 59.94/60Hz
    - -720 x 576p @ 50Hz

    High-Definition Video Format Timing:
    - -1280 x 720p @ 59.94/60Hz
    - -1280 x 720p @ 50Hz
    - -1920 x 1080i @ 59.94/60Hz
    - -1920 x 1080i @ 50Hz
    - -1920 x 1080p @ 23.98/24Hz
    - -1920 x 1080p @ 59.94/60Hz
    - -1920 x 1080p @ 50Hz
    - -4K x 2K@23.98/24Hz
    - -4K x 2K@25Hz
    - -4K x 2K@29.97/30Hz
    - -4K x 2K@59.94/60Hz
    - -4K x 2K@50Hz

    Pixel Encoding:
    - -YCbCr 4:2:2
    - -YCbCr 4:4:4
    - -RGB 4:4:4

    Color Depth:
    - -Deep Color 24-bit
    - -Deep Color 30-bit
    - -Deep Color 36-bit

    3D Video Format Structure
    - -Frame Packing
    - -Top-and-Bottom
    - -Side-by-Side (Half)

- Audio Support
  -Audio sample rate: 32~192k
  -Sample size: 16~24 bits
  -Up to 8-channel
  -Supports PCM, Dolby Digital, DTS digital audio transmission
  -IEC 60958 and IEC61937 compatible
  -Supports High-Bit-Rate Audio

- Master I2C interface for DDC Connection
- Supports Consumer Electronics Control (CEC)

16.2. HDMI Block External Pin Description

Table 30. HDMI Block External Pin Description

Pin Name	I/O	Description
HDMITX_CKN	AO	HDMI Output Clock Pair-
HDMITX_CKP	AO	HDMI Output Clock Pair+
HDMITX_D0N	AO	HDMI Output Data Pair 0-
HDMITX_D0P	AO	HDMI Output Data Pair 0+
HDMITX_D1N	AO	HDMI Output Data Pair 1-
HDMITX_D1P	AO	HDMI Output Data Pair 1+
HDMITX_D2N	AO	HDMI Output Data Pair 2-
HDMITX_D2P	AO	HDMI Output Data Pair 2+
HDMITX_CEC	AB	HDMI Consumer Electronics Control
HDMITX_HPD	DI	HDMI Hot Plug-In

17. HDMI Receiver

The RTD1296 integrates a 1-channel High-Definition Multimedia Interface (HDMI) receiver.

17.1. Features

- One-channel HDMI 2.0a compliant receiver
- Supports video format up to 4K x 2K@59.94/60Hz
- Supports audio 2-channel PCM format with sampling rate up to 192 kHz. PCM bit number support 16, 18, 20, and 24-bit
- Integrated HDCP decryption engine for receiving protected audio and video content
- Supports Consumer Electronics Control (CEC) interface
- DDC bus connection with 5V tolerance
- On-chip high-performance PLLs

17.2. HDMI Receiver Block External Pin Description

Table 31. HDMI Receiver Block External Pin Description

Pin Name	Type	Description
HDMIRX_CKN	AI	HDMI clock input pair-
HDMIRX_CKP	AI	HDMI clock input pair+
HDMIRX_D0N	AI	HDMI data input pair0-
HDMIRX_D0P	AI	HDMI data input pair0+
HDMIRX_D1N	AI	HDMI data input pair1-
HDMIRX_D1P	AI	HDMI data input pair1+
HDMIRX_D2N	AI	HDMI data input pair2-
HDMIRX_D2P	AI	HDMI data input pair2+
HDMIRX_CEC	AB	HDMI Consumer Electronics Control

18. Audio-In Interface

The audio-in interface transfers audio PCM data. A 2-channel default I2S interface is supported. For Karaoke application, HW has an I2S input loopback function. The input data of I2S input could be mixed into PCM output data. The data will be modulated and mixed into the PCM output L or R channel. Only the 2ch I2S input would be looped back. The loopback L channel can be added to both output L and R channels, as can the loopback R channel.

18.1. Features

- Digital Interface
  - One I2S for AI
    -Sample Rate: 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 176.4k, and 192kHz
    -Supports Master and Slave modes
    -PCM bit number: 16, 18, 20, and 24-bit
    -Mute function for left or right channel
    -Supports Karaoke application
  - Digital MIC

- Analog Interface
  - Internal Audio ADC
    -1Vrms line-level driver
    -Sample rate: 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 176.4k, and 192kHz
    -PCM bit number: 16, 18, 20, and 24 bit
    -Independent mute control for left and right channels
    -Stereo differential analog microphone inputs with boost pre-amplifiers and low noise microphone bias

18.2. Audio External Signal Descriptions

AICK and AI_BCLK are the reference clock signals related to the input sampling rate.

AICK is not output as slave mode, so an external crystal is needed for ADC.

AI_LRCK is used as the Word Select line to identify the signal source.

Figure 7 shows the I2S audio-in configuration.

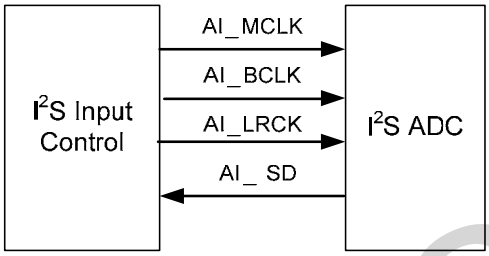


Figure 7. I2S Audio-In Interface Configuration

Table 32. Audio IN Block Pin Description

Pin Name	Type	Description
AIOCK	DO	Main Clock Output to ADC as Master Mode
AIO_BCLK	DO	I2S Bit Clock Output to ADC
AIO_LRCK	DO	I2S Word Select Clock Output to ADC
AI_SDO	DI	I2S Serial Data Input for Audio L/R Input
DMIC_DATA	DI	Digital MIC data in
DMIC_CLK	DO	Digital MIC clock output
AIL	AI	Audio ADC Input Left Channel
AIR	AI	Audio ADC Input Right Channel
MIC1L	AI	Analog microphone left channel (differential pad)
MIC2L	AI	Analog microphone left channel (differential pad)
MIC1R	AI	Analog microphone right channel (differential pad)
MIC2R	AI	Analog microphone right channel (differential pad)
MICBIAS	AO	MICBIAS output (3.3V)

19. Audio-Out Interface

The audio-out interface transfers audio PCM data or non-PCM bit-stream data. Two digital audio IO interfaces, I2S and SPDIF, are supported. Three I2S output protocols are supported: Default I2S, left justified, and right justified. A 2-channel audio DAC (includes a 1Vrms line-level driver) is embedded in this chip. For HDMI output, the RTD1296's HDMI interface can send the PCM data from audio-out to the HDMI TX module.

19.1. Features

- Digital Interface
  - Four I2S for AO
    -Three protocol types: Default I2S, left justified, and right justified
    -Sample rate: 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 176.4k, and 192kHz
    -PCM bit number: 16, 18, 20, and 24 bit
    -Variable WS period
    -Mute function for left or right channel
  - SPDIF
    -Designed in accordance with IEC 60958 (both PCM and non-PCM are supported)
    -Sample rate: 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 176.4k, and 192kHz
    -PCM bit number: 16, 18, 20, and 24 bit
    -Independent mute control for left and right channels
- Analog Interface
  - Internal Audio DAC
    -1Vrms line-level driver
    -Sample rate: 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 176.4k, and 192kHz
    -PCM bit number: 16, 18, 20, and 24 bit
    -Pop-noise-free design on power on/off
    -Independent DAC filter gain for left and right channels
    -Independent mute control for left and right channels

19.2. Audio External Signal Descriptions

AO_MCLK and AO_BCLK are the reference clock signals related to the output sampling rate.

AO_LRCK is used as the Word Select line to identify the signal source.

Figure 8 shows the I2S audio-out configuration. The RTD1296 supports master mode only, meaning AO_MCLK/AO_BCLK/AO_LRCK are from the RTD1296 to an external DAC.

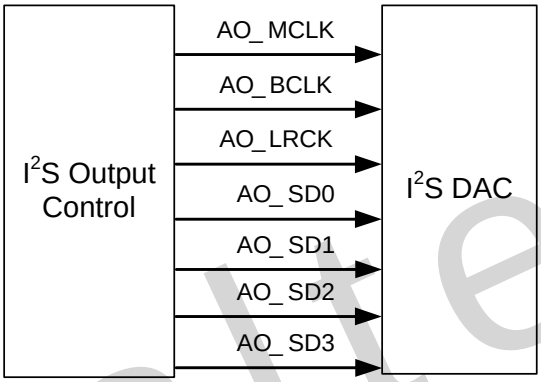


Figure 8. I2S Audio-Out Interface Configuration

Table 33. Audio OUT Block Pin Description

Pin Name	Type	Description
AIOCK	DO	Main Clock Output to DAC
AIO_BCLK	DO	I2S Bit Clock Output to DAC
AIO_LRCK	DO	I2S Word Select Clock Output to DAC
AO_SD0	DO	I2S Serial Data Output for Downmixing Channels
AO_SD1	DO	I2S Serial Data Output for Downmixing Channels
AO_SD2	DO	I2S Serial Data Output for Downmixing Channels
AO_SD3	DO	I2S Serial Data Output for Downmixing Channels
ADAC_AOL	AO	Audio DAC Output Left Channel
ADAC_AOR	AO	Audio DAC Output Right Channel
VREF	PWR	Common Mode Reference Voltage for Audio DAC (10µF Cap to GND)
VREF+	PWR	Common mode voltage output
SPDIF	DO	IEC 60958 (SPDIF) Output

20. SATA Controller

The RTD1296 integrates Two Serial ATA AHCI host controller. The Serial ATA AHCI host controller provides an interface between a host and device. This interface is a peer-to-peer connection and the data is transmitted or received from one Serial ATA compatible device. It is designed to meet the Serial ATA 3.0 standard and designed synchronously with two clock domains – system clock and SATA PHY clock.

20.1. Features

- The Host controller complies with the SATA II extension specification
  - Registers are backward compatible with PATA
  - Supports only one port PHY
  - Supports serial-ATA 3.1 Spec
  - Supports SATA III (1.5G/3G/6G) Spec
  - Supports SATA AHCI 1.31 Spec (first-party DMA)
  - Supports PIO transfer
  - Supports NCQ (Native Command Queuing)
  - Supports Power management including automatic partial-to-slumber transition
  - Any sector size (2 bytes alignment)
  - Internal DMA engine per port
  - AMBA 2.0 for AHB transfer
- PHY Layer (analog) function module complies with 1.0a Specification
  - Transmits a 1.5Gbps (3Gb) differential NRZ serial stream
  - Receives a 1.5Gbps (3Gb) +350/-5000ppm differential NRZ serial stream
  - Supports 5000ppm clock down-spread spectrum function
  - Supports Out-of-Band signal generator and detector
  - Supports speed transition between 1.5Gbps and 3Gbps and 6Gbps
  - Supports Low Power Mode (Partial or Slumber) at PHY Layer
  - Supports MDIO interface to configure internal PHY layer registers setting
  - Supports 32-bit/75MHz (3.0Gbps) or 32-bit/37.5MHz (1.5Gbps) parallel interface with
  - Serial-ATA Mac Layer
- Transmits/extracts data with/without Spread Spectrum Clocking (SSC)
- Device status detection and auto speed negotiation
- Supports low power mode

20.2. SATA Block External Pin Description

Table 34. SATA Block External Pin Description

Pin Name	Type	Description
SATA0_OP	AO	SATA TX+ Signal
SATA0_ON	AO	SATA TX- Signal
SATA0_IP	AI	SATA RX+ Signal
SATA0_IN	AI	SATA RX- Signal
SATA1_OP	AO	SATA TX+ Signal
SATA1_ON	AO	SATA TX- Signal
SATA1_IP	AI	SATA RX+ Signal
SATA2_IN	AI	SATA RX- Signal

20.3. Typical SATA Application

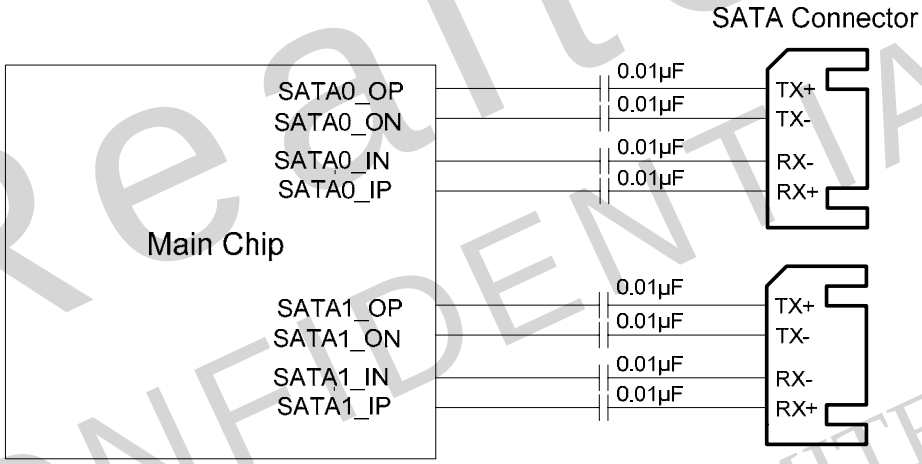


Figure 9. Typical SATA Application

21. PCI Express 1.1

The RTD1296 complies with the PCI Express Base Specification Revision 1.1, and runs at 2.5GHz signal rate with 1x lane. PCI Express lane polarity reversal is also supported to ease PCB layout constraints.

PCI Express is used for extension cards such as 802.11n and Gigabit Ethernet cards.

21.1. Features

- Refer to PCI Express Base Specification Revision 1.1
- Integrated PHY
- PCI Express Gen1.0 (2.5Gbps) in Root Complex (RC) mode
- Built-in 100MHz reference clock (PCIE_CKP, PCIE_CKN)
- Supports 1x lane and polarity reversal
- Supports 256 bytes payload size
- Supports full address translation from PCI Express address space to on-chip memory space

21.2. PCI Express Block External Pin Description

Table 35. PCI Express Block External Pin Description

Pin Name	Type	Description
PCIE1_TXP	AO	Differential Transmit Output
PCIE1_TXN	AO	Differential Transmit Output
PCIE1_RXP	AI	Differential Receive Input
PCIE1_RXN	AI	Differential Receive Input
PCIE1_CKP	AO	Differential Reference Clock
PCIE1_CKN	AO	Differential Reference Clock

21.3. Typical PCI Express 1.1 Application

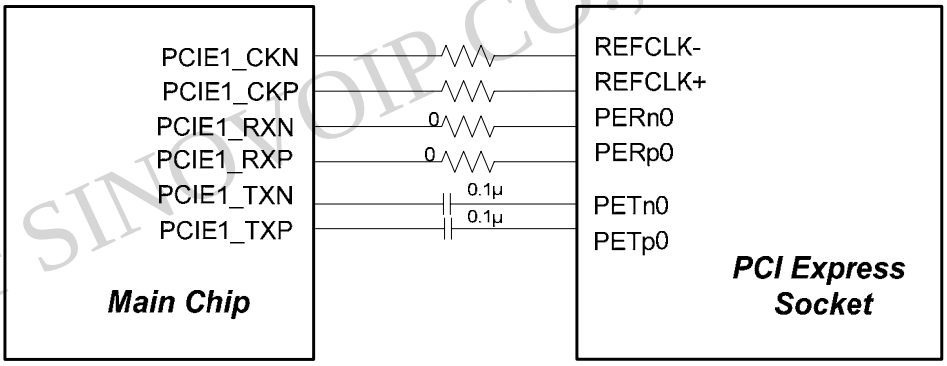


Figure 10. Typical PCI Express 1.1 Application

22. PCI Express 2.0

The RTD1296 complies with the PCI Express Base Specification Revision 2.0, and runs at 5GHz signal rate with 1x lane. PCI Express lane polarity reversal is also supported to ease PCB layout constraints.

PCI Express is used for extension cards such as 802.11n, 802.11ac, and Gigabit Ethernet cards.

22.1. Features

- Refer to PCI Express Base Specification Revision 2.0
- Integrated PHY
- PCI Express Gen2.0(5Gbps) in Root Complex (RC) mode
- Built-in 100MHz reference clock (PCIE_CKP, PCIE_CKN)
- Supports 1x lane and polarity reversal
- Supports 256 bytes payload size
- Supports full address translation from PCI Express address space to on-chip memory space

22.2. PCI Express 2.0 Block External Pin Description

Table 36. PCI Express 2.0 Block External Pin Description

Pin Name	IO Standard	Type	Description
PCIE2_TXP	Analog	AO	Differential Transmit Output
PCIE2_TXN	Analog	AO	Differential Transmit Output
PCIE2_RXP	Analog	AI	Differential Receive Input
PCIE2_RXN	Analog	AI	Differential Receive Input
PCIE2_CKP	Analog	AO	Differential Reference Clock
PCIE2_CKN	Analog	AO	Differential Reference Clock

22.3. Typical PCI Express 2.0 Application

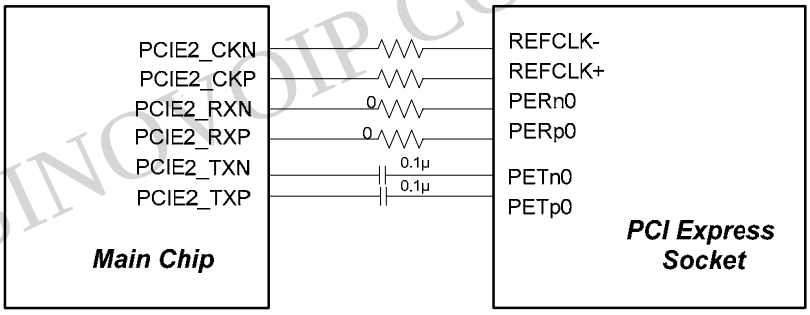


Figure 11. Typical PCI Express 2.0 Application

23. Gigabit Ethernet Controller

The RTD1296 integrates a 10/100/1000M Ethernet MAC, PHY, and transceiver. It provides full compliance with IEEE 802.3 compliant Media Access Controller and IEEE 802.3x Full Duplex Flow Control.

23.1. Features

- 10M, 100Mbps, and 1000Mbps operation
- Auto-Negotiation with Next Page capability
- Supports pair swap/polarity/skew correction
- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az -2010 (EEE)
- Supports power down/link down power saving

23.2. Ethernet 10/100/1000M Block External Pin Description

Table 37. Ethernet 10/100/1000M Block External Pin Description

Pin Name	Type	Description
ETN_MDIP0 ETN_MDIN0	AB AB	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
ETN_MDIP1 ETN_MDIN1	AB AB	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
ETN_MDIP2 ETN_MDIN2	AB AB	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
ETN_MDIP3 ETN_MDIN3	AB AB	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
ETN_LED0	DO	Customized Ethernet LED0
ETN_LED1	DO	Customized Ethernet LED1

23.3. Typical Gigabit Ethernet Application

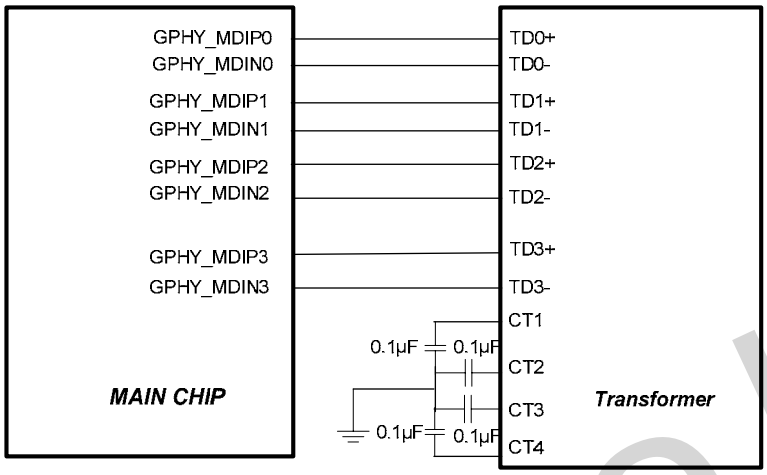


Figure 12. Typical Gigabit Ethernet Application

24. HW NAT

The Realtek RTD1296 HW NAT implements a L2 switch, L3 routing, and L4 NAT functions. Via table configuration and look-up, the RTD1296 can perform hard-wired network traffic forwarding. The CPU may be used to handle upper layer functions, such as DHCP, HTTP, and some other protocols, and to operate with a hard-wired forwarding engine. Due to its powerful protocol parser, the RTD1296 can recognize and hard-wire-forward VLAN-tagged, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP, IGMP, and PPTP packets. Layer 2, 3, and 4 information is stored in look-up tables. For VLAN and PPPoE protocols, the RTD1296 can automatically encapsulate and decapsulate VLAN tagged frames and PPPoE headers.

24.1. Features

- Three Gigabit Ethernet MACs switch with:
  - MAC4: Embedded IEEE 802.3 10/100/1000Mbps physical layer UTP transceiver; shared with Gigabit Ethernet Controller
  - MAC5: Supports dedicated RGMII interface to connect to an external MAC or PHY
  - MAC0: Supports an optional mode to operate at SGMII mode instead of RGMII interface; shares pins with SATA
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
- Internal 512Kbit SRAM for Ethernet switch core packet buffer
- Internal 1024 entry 4 way hash L2 look-up table
- Supports source and destination MAC address filtering
- Supports IPv4 HW NAT

- Supports IPv6 HW Routing, including DS-Lite, 6RD, and IPv6 HW multicasting
- Supports HW QoS:
  - Per port 8 HW output queues with strict and WFQ scheduling
  - The priority of packet can be decided based on port-based, 802.1p tag, DSCP, ACL and VID based
  - Supports ingress and egress bandwidth control with 1Kbps scale resolution
- Supports TSO (TCP Segmentation Offload)
- Supports low cost LED display

24.2. NAT Block External Pin Description

Table 38. NAT Block External Pin Description

Pin Name	Type	Description
RGMII0_VDD	PWR	Power pin for MAC5 RGMII interface and RGMII0_MDC/RGMII0_MDIO
RGMII0_MDC	DO	Management Data Clock. This pin provides a clock synchronous to the RGMII0_MDIO.
RGMII0_MDIO	DB	Management Data Input/Output. This pin provides a bi-directional signal used to transfer management information.
RGMII0_RXC	DI	MAC5 RGMII Receive Clock Input. RGMII0_RXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RGMII0_RXD [3:0] and RGMII0_RXCTL synchronization at both RGMII0_RXC rising and falling edges.
RGMII0_RXCTL	DI	MAC5 RGMII Receive Control signal Input The RGMII0_RXCTL indicates RX_DV at the rising of RGMII0_RXC and RX_ER at the falling edge of RG0_RXCLK.. At RGMII0_RXC falling edge, RGMII0_RXCTL=RX_DV (xor) RX_ER.
RGMII0_RXD[3:0]	DI	MAC5 RGMII Receive Data Input. Received data is received synchronously by RGMII0_RXC.
RGMII0_TXC	DO	MAC5 RGMII Transmit Clock Output RGMII0_TXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG0_TXD[3:0] and RG0_TXCTL synchronization at RGMII0_TXC on both rising and falling edges.
RGMII0_TXCTL	DO	MAC5 RGMII Transmit Control signal Output. The RG0_TXCTL indicates TX_EN at the rising edge of RGMII0_TXC, and TX_ER at the falling edge of RGMII0_TXC At the RGMII0_TXC falling edge, RG0_TXCTL=TX_EN (xor) TX_ER.
RGMII0_TXD[3:0]	DO	MAC5 RGMII Transmit Data Output. Transmitted data is sent synchronously to RGMII0_TXC
RGMII1_VDD	PWR	Power pin for MAC0 RGMII interface
RGMII1_RXC	DI	MAC0 RGMII Receive Clock Input. RGMII1_RXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RGMII1_RXD [3:0] and RGMII1_RXCTL synchronization at both RGMII1_RXC rising and falling edges.

Pin Name	Type	Description
RGMII1_RXCTL	DI	MAC0 RGMII Receive Control signal Input The RGMII1_RXCTL indicates RX_DV at the rising of RGMII1_RXC and RX_ER at the falling edge of RG1_RXCLK. At RGMII1_RXC falling edge, RGMII1_RXCTL = RX_DV (xor) RX_ER.
RGMII1_RXD[3:0]	DI	MAC0 RGMII Receive Data Input. Received data is received synchronously by RGMII1_RXC.
RGMII1_TXC	DO	MAC0 RGMII Transmit Clock Output RGMII1_TXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RGMII1_TXC on both rising and falling edges.
RGMII1_TXCTL	DO	MAC0 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RGMII0_TXC, and TX_ER at the falling edge of RGMII0_TXC At the RGMII0_TXC falling edge, RG0_TXCTL= TX_EN (xor) TX_ER.
RGMII1_TXD[3:0]	DO	MAC0 RGMII Transmit Data Output. Transmitted data is sent synchronously to RGMII0_TXC
NAT_LED0	DB	MAC4 LED indicator
NAT_LED1	DB	MAC5 LED indicator
NAT_LED2	DB	LED control signal in scan mode
NAT_LED3	DB	MAC0 LED indicator
HSIP	AI	SERDES differential input
HSIN	AI	SERDES differential input
HSOP	AO	SERDES differential output
HSON	AO	SERDES differential output

24.3. Typical Gigabit Ethernet Application

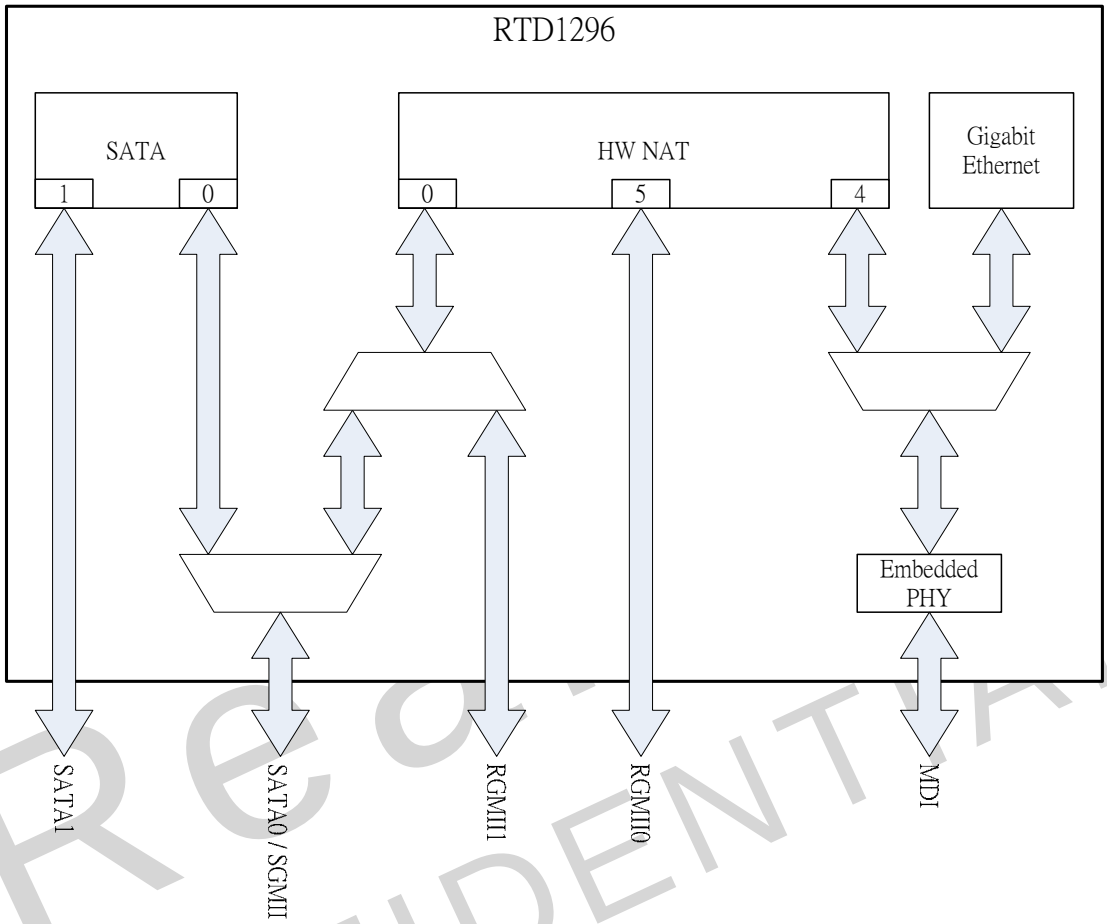


Figure 13. Flexible Interface of HW NAT

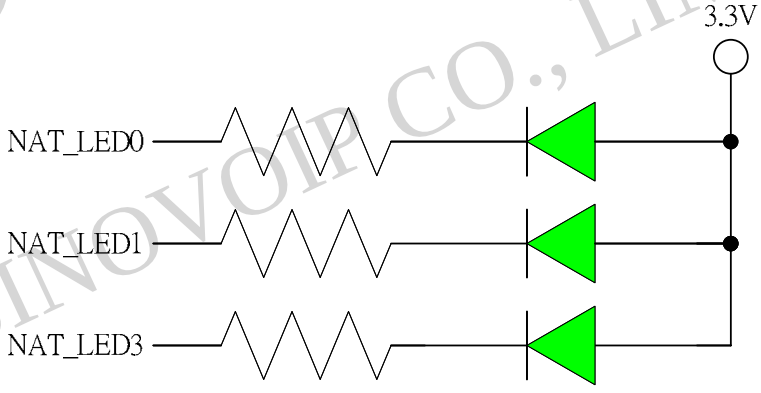


Figure 14. LED Indicator in Direct Mode

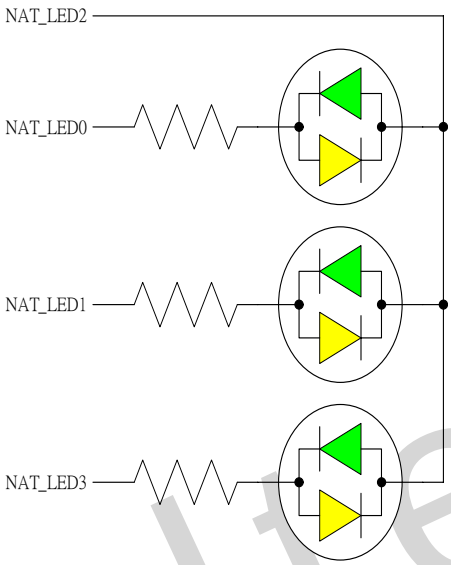


Figure 15. LED Indicator in Scan Mode

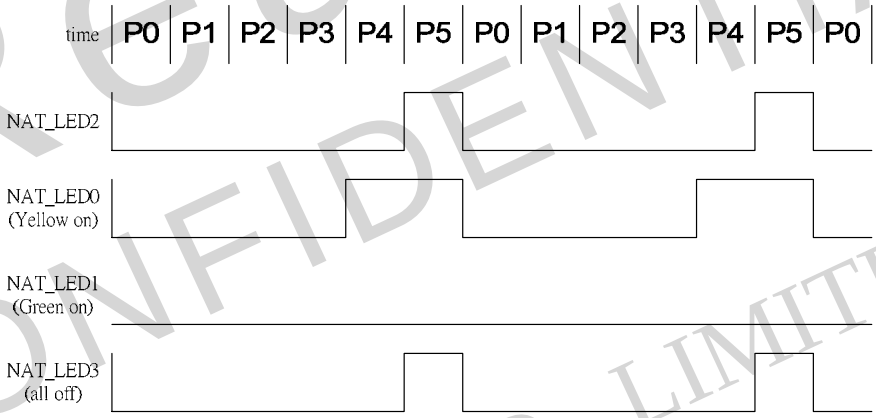


Figure 16. Scan Mode Timing Chart (Example)

SERDES

HSIP/HSIN – SERDES differential input: 1.25GHz serial interface to receive data from an external device that supports the SGMII interface.

HSOP/HSON – SERDES differential output: 1.25GHz serial interface to transfer data from an external device that supports the SGMII interface

25. USB 2.0/USB 3.0 Host/Device Controller

The RTD1296 complies with the USB 2.0 and USB 3.0 standards. Of the two USB 3.0 ports, the one for type C connector is configured as host or device by CC pin and the other supports host only. Of the two USB 2.0 ports, one supports host only and the other is configured as host or device by the operating system.

25.1. Features

- Type-C port detects plug orientation with CC pin to determine USB 3.0 signal path.
- Complies with the XHCI specification and with the USB 3.0 specification
- Complies with EHCI and OHCI specifications and with the USB 2.0 specification
- XHCI compliant host for Super-Speed.EHCI compliant host for High-Speed
- OHCI compliant host for Full/Low-Speed/Super/High/Full-Speed device capability
- Built-in termination resistor to reduce system cost
- Supports power management for downstream port devices

25.2. USB Block External Pin Description

Table 39. USB Block External Pin Description

Pin Name	Type	Description
TYPEC_TX1+	AO	USB3 TC TX D+ signal.
TYPEC_TX1-	AO	USB3 TC TX D- signal.
TYPEC_TX2+	AO	USB3 TC TX D+ signal.
TYPEC_TX2-	AO	USB3 TC TX D- signal.
TYPEC_RX1+	AI	USB3 TC RX D+ signal.
TYPEC_RX1-	AI	USB3 TC RX D- signal.
TYPEC_RX2+	AI	USB3 TC RX D+ signal.
TYPEC_RX2-	AI	USB3 TC RX D- signal.
TYPEC_CC1	AB	USB3 TC Configuration Channel
TYPEC_CC2	AB	USB3 TC Configuration Channel
TYPEC_D+	AB	USB2 D+ signal (USB3 TC)
TYPEC_D-	AB	USB2 D- signal (USB3 TC)
USB3_HSOP	AO	USB3 Host TX D+ signal
USB3_HSON	AO	USB3 Host TX D- signal
USB3_HSIP	AI	USB3 Host RX D+ signal
USB3_HSIN	AI	USB3 Host RX D- signal
USB_DP3	AB	USB2 D+ signal (USB3 Host)
USB_DM3	AB	USB2 D- signal (USB3 Host)
USB_DP1	AB	USB2 D+ signal (USB2 HOST)
USB_DM1	AB	USB2 D- signal (USB2 HOST)
USB_DP2	AB	USB2 D+ signal (USB2 Host/ Device)
USB_DM2	AB	USB2 D- signal (USB2 Host/ Device)
USB_ID	DI	USB Identification. Denotes the pin on the USB Micro connectors that is used to differentiate a Micro-A plug from a Micro-B plug attached.

26. Transport Module

The transport module provides basic support for MPEG Transport Streams (TS) from transport interfaces. It supports several modern digital TV services. Two transport interfaces are supported in the RTD1296; both of which can operate simultaneously.

26.1. Features

- Supports terrestrial, cable, and satellite DTV
- Supports two serial inputs

26.2. Transport Module External Pin Description

Table 40. Transport Module External Pin Description

Pin Name	Type	Description
TP0_SYNC	DI	Primary Transport Stream Input SYNC
TP0_VALID	DI	Primary Transport Stream Input Data Valid
TP0_CLK	DI	Primary Transport Stream Input Clock
TP0_DATA	DI	Primary Transport Stream Input Data
TP1_SYNC	DI	Secondary Transport Stream Input SYNC
TP1_VALID	DI	Secondary Transport Stream Input Data Valid
TP1_CLK	DI	Secondary Transport Stream Input Clock
TP1_DATA	DI	Secondary Transport Stream Input Data

27. Card Reader Controller

There are two card reader controllers: one supports SDIO embedded devices; the other supports SD/MMC cards. Note that the SD/MMC controller cannot sense the interrupt signal on DATA[1], so the SD/MMC controller cannot handle SDIO devices.

27.1. Features

- SDIO 3.0 (4-bit bus width, clock frequency up to 100 MHz)
- SD 3.0 (4-bit bus width, clock frequency up to 208 MHz)

27.2. Card Reader Block External Pin Description

Table 41. Card Reader Block External Pin Description

Pin Name	Type	Description
SDIO_CLK	DO	SDIO Clock Output
SDIO_CMD	DB	SDIO Command Line
SDIO_D[3:0]	DB	SDIO Data[3:0]
SD_WP	DI	SD/MMC Write Protect
SD_CD	DI	SD/MMC Card Detect
SD_CLK	DO	SD/MMC Clock Output
SD_CMD	DB	SD/MMC Command Line
SD_D[3:0]	DB	SD/MMC Data[3:0]

28. LVDS (Flat Panel Display Link)

The RTD1296 can display onto flat panels, e.g., an LCD, through its LVDS interface.

28.1. Features

- Supports 1-channel LVDS, up to 1366x768 panels
- Supports 6-bit and 8-bit color
- Supports Gamma and Dither functions

28.2. Transport Module External Pin Description

Table 42. Transport Module External Pin Description

Pin Name	Type	Description
DP_LANE0P	AO	LVDS Output Channel A Data Pair 0+
DP_LANE0N	AO	LVDS Output Channel A Data Pair 0-
DP_LANE1P	AO	LVDS Output Channel A Data Pair 1+
DP_LANE1N	AO	LVDS Output Channel A Data Pair 1-
DP_LANE2P	AO	LVDS Output Channel A Data Pair 2+
DP_LANE2N	AO	LVDS Output Channel A Data Pair 2-
DP_LANE3P	AO	LVDS Output Channel A Clock Pair+
DP_LANE3N	AO	LVDS Output Channel A Clock Pair-
DP_LANE4P	AO	LVDS Output Channel A Data Pair 3+
DP_LANE4N	AO	LVDS Output Channel A Data Pair 3-

29. DisplayPort

The DisplayPort interface of the RTD1296 can output digital video and audio to monitors and TVs with DP interfaces. It also can display onto flat panels such as an LCD with an eDP interface.

29.1. Features

- Supports 4-lane, 2.7G HBR; up to 4KP30 resolutions
- Supports AUX channel; 1 Mbit/s
- Supports 2-ch and 8-ch audio
- Supports HDCP2.2

29.2. Transport Module External Pin Description

Table 43. Transport Module External Pin Description

Pin Name	Type	Description
DP_LANE0P	AO	DP lane 0+
DP_LANE0N	AO	DP lane 0-
DP_LANE1P	AO	DP lane 1+
DP_LANE1N	AO	DP lane 1-
DP_LANE2P	AO	DP lane 2+
DP_LANE2N	AO	DP lane 2-
DP_LANE3P	AO	DP lane 3+
DP_LANE3N	AO	DP lane 3-
DP_AUXP	AIO	AUX channel +
DP_AUXN	AIO	AUX channel -

30. Soldering Reflow Profile

The reflow profile is for MSL classification only, not a recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs, and should not exceed the parameters in Table 44.

Table 44. Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (T_L to T_P)	3°C/second max
Preheat Ts_{min} Ts_{max} t_S	 150°C min 200°C max 60~120 seconds
Time Maintained Above T_L t_L	 217°C 60~150 seconds
Peak Package Body Temperature (T_P)	260°C max
Time (t_P) within 5°C of Actual Peak Temperature	30 seconds
Ramp-Down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

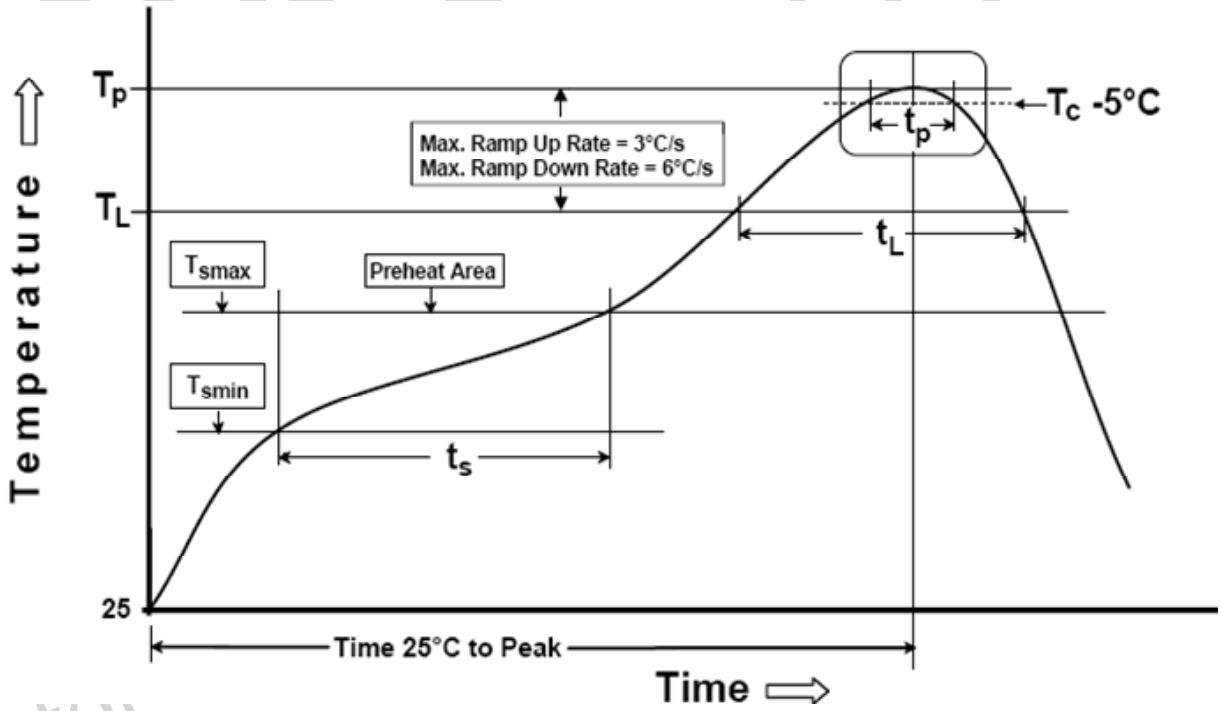
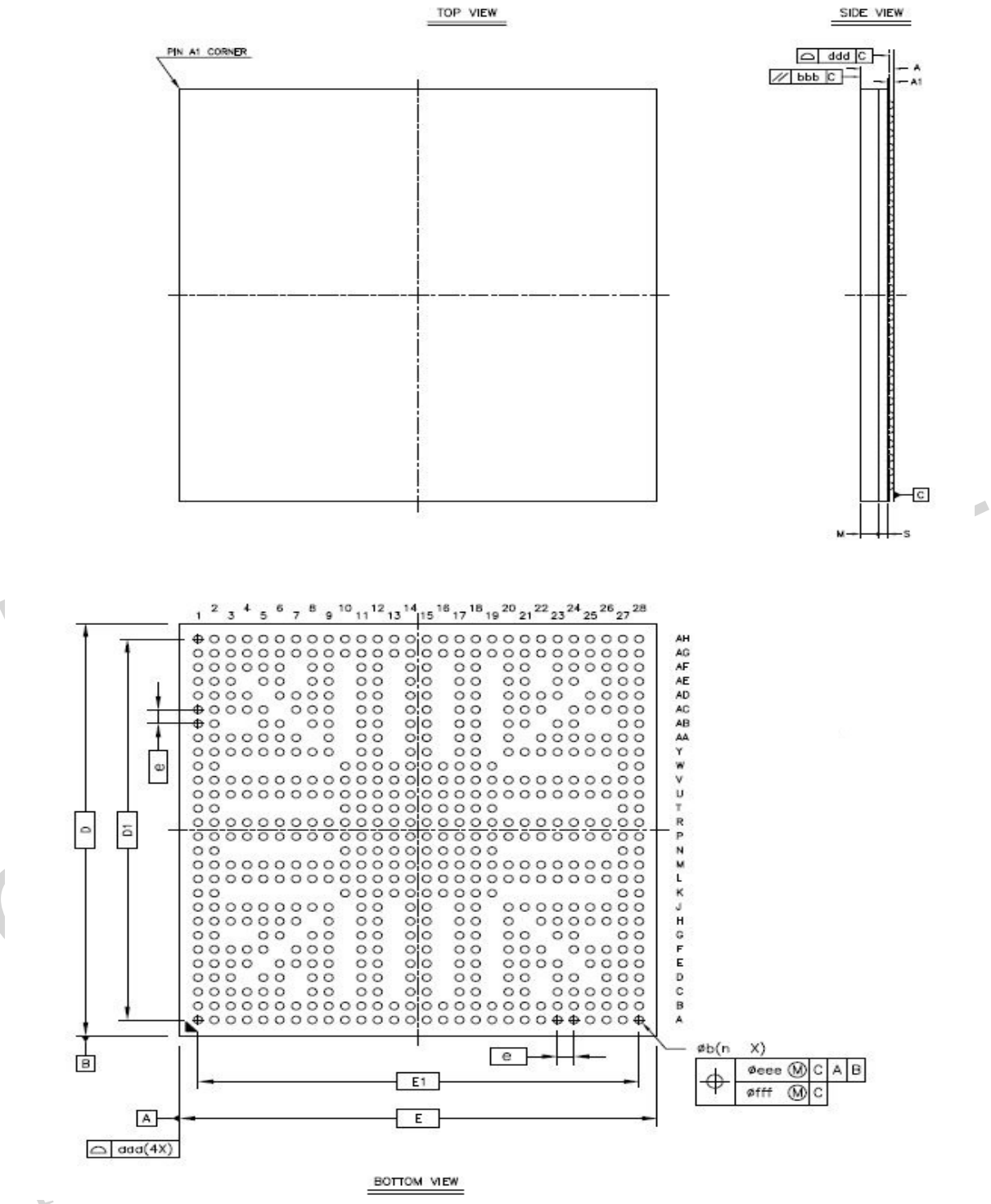


Figure 17. Soldering Temperature Profile

31. Mechanical Dimensions



31.1. Mechanical Dimensions Notes

		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			LFBGA		
Body Size:	X	E	19.000		
	Y	D	19.000		
Ball Pitch :		e	0.650		
Total Thickness :		A	1.120	1.260	1.400
Mold Thickness :		M	0.700 Ref.		
Substrate Thickness :		S	0.360 Ref.		
Ball Diameter :			0.350		
Stand Off :		A1	0.220	0.270	0.320
Ball Width :		b	0.320	0.370	0.420
Package Edge Tolerance :		aaa	0.150		
Mold Flatness :		bbb	0.350		
Coplanarity:		ddd	0.200		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	636		
Edge Ball Center to Center :	X	E1	17.550		
	Y	D1	17.550		

Note: Dimensions Unit: mm.

32. Ordering Information

Table 45. Ordering Information

Part Number	Description	Status
RTD1296DB-VA1-CG	636-Pin TFBGA. Dolby and DTS certified	-
RTD1296DC-VA1-CG	636-Pin TFBGA. Dolby certified	-
RTD1296PB-VA1-CG	636-Pin TFBGA.	-

Note: Only licensees certified by the original licensor(s) are eligible to purchase these products.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan.
Tel: 886-3-5780211 Fax: 886-3-577-6047
www.realtek.com