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**UNICORN-CR-ARCH**

**Specification for Unicorn Project**



# Specification for Unicorn: Card Reader Architecture Specification

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| SD | Address Index (SYS) | Address Index (IP) |
|---|---|---|
| wrapper control register | 0x1801_0400~0x1801_04FF | NA |
| IP sys_sel | 0x1801_0500~0x1801_050F | FD50~FD5F |
| | 0x1801_0510~0x1801_051F | FD60~FD6F |
| | 0x1801_0520~0x1801_052F | FD70~FD7F |
| | 0x1801_0530~0x1801_053F | FD30~FD3F |
| IP ocp_sel | 0x1801_0540~0x1801_054F | FDA0~FDAF |
| IP sd_mux_sel | 0x1801_0550~0x1801_055F | FDC0~FDCF |
| | 0x1801_0560~0x1801_056F | FDD0~FDDF |
| | 0x1801_0570~0x1801_057F | FDE0~FDEF |
| IP sd_sel | 0x1801_0580~0x1801_058F | FF00~FF0F |
| | 0x1801_0590~0x1801_059F | FF10~FF1F |
| | 0x1801_05A0~0x1801_05AF | FF20~FF2F |
| IP ppb_sel | 0x1801_0600~0x1801_06FF | F800~F8FF |
| | 0x1801_0700~0x1801_07FF | F900~F9FF |
| | 0x1801_0800~0x1801_08FF | FA00~FAFF |
| | 0x1801_0900~0x1801_09FF | FB00~FBFF |

| SDIO | Address Index (SYS) | Address Index (IP) |
|---|---|---|
| wrapper control register | 0x9801_0A00~0x9801_0AFF | NA |
| SDIO pcie if register | 0x9801_0B00~0x9801_0BFF | FE00~FEFF |
| SDIO host standard register | 0x9801_0C00~0x9801_0CFF | FF00~FFFF |
| SDIO ring buffer access | 0x9801_0B00~0x9801_0EFF | |

| eMMC | Address Index (SYS) | Address Index (IP) |
|---|---|---|
| wrapper control register | 0x1801_2000~0x1801_20FF | NA |
| IP sys_sel | 0x1801_2100~0x1801_210F | FD50~FD5F |
| | 0x1801_2110~0x1801_211F | FD60~FD6F |
| | 0x1801_2120~0x1801_212F | FD70~FD7F |
| | 0x1801_2130~0x1801_213F | FD30~FD3F |
| IP ocp_sel | 0x1801_2140~0x1801_214F | FDA0~FDAF |
| IP sd_mux_sel | 0x1801_2150~0x1801_215F | FDC0~FDCF |
| | 0x1801_2160~0x1801_216F | FDD0~FDDF |
| | 0x1801_2170~0x1801_217F | FDE0~FDEF |
| IP sd_sel | 0x1801_2180~0x1801_218F | FF00~FF0F |
| | 0x1801_2190~0x1801_219F | FF10~FF1F |
| | 0x1801_21A0~0x1801_21AF | FF20~FF2F |
| IP ppb_sel | 0x1801_2200~0x1801_22FF | F800~F8FF |
| | 0x1801_2300~0x1801_23FF | F900~F9FF |
| | 0x1801_2400~0x1801_24FF | FA00~FAFF |
| | 0x1801_2500~0x1801_25FF | FB00~FBFF |

SD wrapper control register

| Module::sd | Register:: DMA_CTL1 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0404 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..30 | - | - | - | | |
| dram_sa | 29..0 | R/W | ‘h0000 000 | Dram start address for DMA transfer. This information will be map to addcmd. (8 Bytes Unit, 1 means 8B) | | |

| Module::sd | Register::DMA_CTL2 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0408 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..16 | - | - | - | | |
| dma_len | 15..0 | R/W | ‘h0000 | Transfer length for DMA transfer between DMA buffer and DDR. (512B Unit, 1 means 512B) | | |

| Module::sd | Register::DMA_CTL3 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_040C |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..6 | - | - | - | | |
| dat64_sel | 5 | R/W | ‘b0 | For CMD6 case, read data length is 64byte (less than 256 byte)<br>‘1’: dma count to 64byte and send sb1_req.<br>‘0’: normal case. | | |
| rsp17_sel | 4 | R/W | ‘b0 | For response is R2 case, reponse will transfer by dma and not store in register.<br>‘1’: dma count to 16byte and send sb1_req.<br>‘0’: normal case. | | |
| Rvd | 3..2 | - | - | - | | |
| ddr_wr | 1 | R/W | ‘b0 | ‘1’: Move data from DMA buffer to DDR.<br>‘0’: Move data from DDR to DMA Buffer.<br>This information will be map to addcmd. | | |

| | | | | |
|---|---|---|---|---|
| | | | | When target_sel |
| dma_xfer | 0 | R/W | ‘b0 | Set this bit to transfer data between DRAM and DMA buffer. Direction must be set at next bit. The transfer length is reference to DMA_CTL2[24:1215:0].<br>This bit will be auto clear when transfer done. |

| Module::sd | Register::SYS_LOW_PWR | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0410 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..7 | - | - | - | | |
| sys_clk_gate_ena | 6 | R/W | ‘b1 | DMA clk_sys gating enable | | |
| Rvd | 5 | - | - | - | | |
| dma_sram_lp_ena | 4 | R/W | ‘b0 | dma sram low power enable | | |
| dma_sram_rdy_num | 3:0 | R/W | ‘d10 | dma sram ready cycle (leave sleep mode)<br>(N+1) * clk_sys period | | |

| Module::sd | Register:: DMA_RST | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0420 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | - | - | - | | |
| Dbus_endian_sel | 2 | R/W | ‘b0 | 0: little; 1: Big | | |
| L4_gated_disable | 1 | R/W | ‘b0 | Disable L4 clock gated | | |
| dma_rstn | 0 | R/W | ‘b1 | dma soft reset. | | |

| Module::sd | Register:: ISR | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0424 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..5 | - | - | - | | |
| Int4 | 4 | R/W | ‘b0 | SD Int4. DMA transfer done INT. | | |
| Int3 | 3 | R/W | ‘b0 | SD Int3.SB1 wlast/rlast. | | |
| Int2 | 2 | R/W | ‘b0 | SD Int2. Card Error. | | |

| | | | | |
|---|---|---|---|---|
| Int1 | 1 | R/W | ‘b0 | SD Int1. Card End. |
| write_data | 0 | W | - | 1 to set, 0 to clear bit with 1. |

| Module::sd | Register:: ISREN | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0428 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..9 | - | - | - | | |
| Rvd | 8..5 | - | - | - | | |
| Int4En | 4 | R/W | ‘b0 | SD Int4 Enable<br>dma_clr INT Enable. | | |
| Int3En | 3 | R/W | ‘b0 | SD Int3 Enable<br>SB1 wlast/rlast INT Enable. | | |
| Int2En | 2 | R/W | ‘b0 | SD Int2 Enable<br>Card Error INT Enable. | | |
| Int1En | 1 | R/W | ‘b0 | SD Int1 Enable<br>Card End INT Enable. | | |
| write_data | 0 | W | - | 1 to set, 0 to clear bit with 1. | | |

| Module::sd | Register:: DUMMY_SYS | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_042C |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| dmy | 31..0 | R/W | ‘h0000 0000 | Dummy bit. | | |

| Module::sd | Register:: DBG | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0444 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..13 | - | - | - | | |
| write_enable4 | 12 | W | - | Write enable for bit[11..10] | | |
| cr_dbg_sel | 11..10 | R/W | ‘h0 | CR dbg select | | |

| | | | | |
|---|---|---|---|---|
| write_enable3 | 9 | W | - | Write enable for bit[8..6] |
| sel1 | 8..6 | R/W | ‘h0 | Select control of dbg_sel1. |
| write_enable2 | 5 | W | - | Write enable for bit[4..2] |
| sel0 | 4..2 | R/W | ‘h0 | Select control of dbg_sel0. |
| write_enable1 | 1 | W | - | Write enable for bit0. |
| enable | 0 | R/W | ‘b0 | Debug Enable.<br>If set to 1, the debug port will be switched to the selected probed signals for observation.<br>If clear to 0 (default), the scpu_dbg_out0 and scpu_dbg_out1 are both static at 16’h0. |

| Module::sd | Register::IP_BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0460 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..17 | R/W | - | - |
| bist_cr_ppb_rme_1 | 16 | R/W | ‘b0 | RM1 enable |
| bist_cr_ppb_rm_1 | 15..12 | R/W | ‘h0 | RM1 value |
| Rvd | 11..9 | R/W | - | - |
| bist_cr_ppb_rme_0 | 8 | R/W | ‘b0 | RM0 enable |
| bist_cr_ppb_rm_0 | 7..4 | R/W | ‘h0 | RM0 value |
| bist_drf_test_resume | 3 | R/W | ‘b0 | Bist drf test resume bit. |
| bist_drf_mode | 2 | R/W | ‘b0 | Bist drf enable bit. |
| bist_en | 1 | R/W | ‘b0 | Bist enable bit. |
| bist_ls | 0 | R/W | ‘b0 | Bist ls bist |

| Module::sd | Register::IP_BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0464 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..7 | R | - | - |
| bist_drf_start_pause | 6 | R | ‘b0 | IP DRF start pause |

| | | | | |
|---|---|---|---|---|
| bist_drf_fail_1 | 5 | R | ‘b0 | IP BIST DER 1 fail |
| bist_drf_fail_0 | 4 | R | ‘b0 | IP BIST DER 0 fail |
| bist_drf_done | 3 | R | ‘b0 | IP BIST DRF done |
| bist_1_fail | 2 | R | ‘b0 | IP BIST 1 fail |
| bist_0_fail | 1 | R | ‘b0 | IP BIST 0 fail |
| bist_done | 0 | R | ‘b0 | IP BIST finishing signal |

| Module::sd | Register::BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0468 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..17 | R/W | - | - |
| cr_bist2_rme_1 | 16 | R/W | ‘b0 | BIST2 RM1 enable |
| cr_bist2_rm_1 | 15..12 | R/W | ‘h0 | BIST2 RM1 value |
| Rvd | 11..9 | R/W | - | - |
| cr_bist2_rme_0 | 8 | R/W | ‘b0 | BIST2 RM0 enable |
| cr_bist2_rm_0 | 7..4 | R/W | ‘h0 | BIST2 RM0 value |
| cr_bist2_drf_test_resume | 3 | R/W | ‘b0 | BIST group1 fail signal. |
| cr_drf_bist2_mode | 2 | R/W | ‘b0 | CR DRF BIST2 enable |
| cr_bist2_mode | 1 | R/W | ‘b0 | CR BIST2 enable |
| cr_bist2_ls | 0 | R/W | ‘b0 | CR BIST2 ls mode |

| Module::sd | Register::BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_046C |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..22 | R | - | - |
| drf_bist2_fail_3 | 21 | R | ‘b0 | BIST2 DRF 3 fail |
| drf_bist2_fail_2 | 20 | R | ‘b0 | BIST2 DRF 2 fail |

| | | | | |
|---|---|---|---|---|
| drf_bist2_fail_1 | 19 | R | ‘b0 | BIST2 DRF 1 fail |
| drf_bist2_fail_0 | 18 | R | ‘b0 | BIST2 DRF 0 fail |
| bist2_drf_start_pause | 17 | R | ‘b0 | BIST2 DRF start pause |
| drf_bist2_done | 16 | R | ‘b0 | DRF BIST2 finishing signal. |
| Rvd | 15..5 | R | | |
| bist2_fail_3 | 4 | R | ‘b0 | BIST2 3 fail |
| bist2_fail_2 | 3 | R | ‘b0 | BIST2 2 fail |
| bist2_fail_1 | 2 | R | ‘b0 | BIST2 1 fail |
| bist2_fail_0 | 1 | R | ‘b0 | BIST2 0 fail |
| bist2_done | 0 | R | ‘b0 | BIST2 finishing signal |

| Module::sd | Register::IP_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0470 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..16 | R/W | - | - |
| asic_crc_dbgo_sel | 15..8 | R/W | ‘h0 | IP dbug page sel 1 |
| Rvd | 7 | R/W | - | - |
| crc_dbgo_sel | 6..3 | R/W | ‘h0 | IP dbug page sel 2 |
| ip_ea_flash | 2 | R/W | ‘b0 | IP ea flash |
| crc_clk_disable_trig | 1 | R/W | ‘b0 | IP auto disable crc_clk triggle |
| mcu_time_1_us | 0 | R/W | ‘b0 | IP mcu control |

| Module::sd | Register::PAD_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0474 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..1 | - | - | - |
| tune3318 | 0 | R/W | ‘b1 | Pad select 3.3v or 1.8v,<br>1: 3.3v<br>0: 1.8v |

| Module::sd | Register::CKGEN_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0478 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..19 | R/W | - | - |
| sd30_sample_change | 18 | R/W | ‘b0 | 0: from sd30_sample_clk_src<br>1: clk4M |
| sd30_push_change | 17 | R/W | ‘b0 | 0: from sd30_push_clk_src<br>1: clk4M |
| crc_clk_change | 16 | R/W | ‘b0 | 0: from crc_clk_src<br>1: clk4M |
| Rvd | 15..14 | R/W | - | - |
| sd30_sample_clk_src | 13:12 | R/W | ‘b10 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 11..10 | R/W | - | - |
| sd30_push_clk_src | 9:8 | R/W | ‘b01 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 7..6 | R/W | - | - |
| crc_clk_src | 5:4 | R/W | ‘b00 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 3 | - | - | - |
| clk_div | 2..0 | R/W | ‘h0 | 000: div1<br>001: div2<br>010: div4<br>011: div8 |

| Module::sd | Register::SDIO_BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0480 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..9 | R/W | - | - |
| bist_dbus_buf_rme | 8 | R/W | ‘b0 | RM enable |
| bist_dbus_buf_rm | 7..4 | R/W | ‘h0 | RM value |
| bist_drf_test_resume | 3 | R/W | ‘b0 | Bist drf test resume bit. |
| bist_drf_mode | 2 | R/W | ‘b0 | Bist drf enable bit. |
| bist_en | 1 | R/W | ‘b0 | Bist enable bit. |
| bist_ls | 0 | R/W | ‘b0 | Bist ls bit. |

| Module::sd | Register::SDIO_BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0484 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..7 | R | - | - |
| bist_drf_start_pause | 6 | R | ‘b0 | DBUS BUF DRF start pause |
| bist_drf_fail_1 | 5 | R | ‘b0 | DBUS BUF BIST DER 1 fail |
| bist_drf_fail_0 | 4 | R | ‘b0 | DBUS BUF BIST DER 0 fail |
| bist_drf_done | 3 | R | ‘b0 | DBUS BUF BIST DRF done |
| bist_1_fail | 2 | R | ‘b0 | DBUS BUF BIST 1 fail |
| bist_0_fail | 1 | R | ‘b0 | DBUS BUF BIST 0 fail |
| bist_done | 0 | R | ‘b0 | DBUS BUF BIST finishing signal |

| Module::sd | Register::SDIO_IP_BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0488 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..9 | R/W | - | - |
| bist_ring_buf_rme_0 | 8 | R/W | ‘b0 | RM0 enable |
| bist_ring_buf_rm_0 | 7..4 | R/W | ‘h0 | RM0 value |

| | | | | |
|---|---|---|---|---|
| bist_drf_test_resume | 3 | R/W | ‘b0 | Bist drf test resume bit. |
| bist_drf_mode | 2 | R/W | ‘b0 | Bist drf enable bit. |
| bist_en | 1 | R/W | ‘b0 | Bist enable bit. |
| bist_ls | 0 | R/W | ‘b0 | Bist ls bit. |

| Module::sd | Register::SDIO_IP_BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_048C |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..5 | R | - | - |
| bist_drf_start_pause | 4 | R | ‘b0 | IP DRF start pause |
| bist_drf_fail | 3 | R | ‘b0 | IP BIST DRF fail |
| bist_drf_done | 2 | R | ‘b0 | IP BIST DRF done |
| bist_fail | 1 | R | ‘b0 | IP BIST fail |
| bist_done | 0 | R | ‘b0 | IP BIST finishing signal |

| Module::sd | Register::SPEED_SENSOR_CTRL | Set::2 | ATTR::ctrl | Type::SR | ADDR::0x9801_0490 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..27 | - | - | |
| sensor_clk_en | 26 | R/W | ‘b0 | speed sensor clock enable |
| speed_en | 25 | R/W | ‘b0 | enable |
| daya_in | 24..5 | R/W | ‘b0 | data in |
| wire_sel | 4 | R/W | ‘b0 | interconnect (metal) selection |
| ro_sel | 3..1 | R/W | ‘b0 | select ring osc |
| rstn | 0 | R/W | ‘b0 | reset |

| Module::sd | Register::SPEED_SENSOR_OUT1 | Set::2 | ATTR::nor | Type::SR | ADDR::0x9801_049c |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..21 | - | - | |
| count_out | 20..1 | R | ‘b0 | data out (valid if ready is high) |
| ready | 0 | R | ‘b0 | indicate the test is done |

| Module::sd | Register::SPEED_SENSOR_OUT2 | Set::2 | ATTR::nor | Type::SR | ADDR::0x9801_04a4 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| Rvd | 31..17 | - | - | |
| dbgo | 16..1 | R | 'b0 | debug output |
| wsort_go | 0 | R | 'b0 | go/no-go for wafer test |

SDIO wrapper control register

| Module::sdio | Register::SRAM_CTL | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A00 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | - | - | - | | |
| mcu_buf_access | 2..1 | R/W | 'h0 | in bit[0] = 1 condition,<br>bit[2:1] = 'b00 : buf access disable.<br>bit[2:1] = 'b01 : buf abs access enable, ring buffer address is direct mapping to 0x9801_0B00 ~ 0x9801_0EFF.<br>bit[2:1] = 'b10: buf auto access enable, ring buffer could be access by register<br>0x9801_0B30 (sram data [7:0]),<br>0x9801_0B31 (sram data [15:8]),<br>0x9801_0B32 (sram data [23:16]),<br>0x9801_0B33 (sram data [31:24]),<br>address will auto increase by 4.<br>bit[2:1] = 'b11 : buf access disable. | | |
| mcu_sel | 0 | R/W | 'b0 | 0: elbi I/F<br>1: mcu I/F | | |

Note: In MCU reg mode(mcu_sel = 1, mcu_buf_access = 2'b01/2'b10), Data always accessed to rbus_wdata[7:0] / from rbus_rdata[7:0], data[31:8] will be 0.

Note: MCU mode is used for debug, normal function covered in elbi mode totally.

| Module::sdio | Register::IP_CTL | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A10 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | R/W | - | - | | |
| Dbus_endian_sel | 2 | R/W | 'b0 | 0: little; 1: Big | | |
| L4_gated_disable | 1 | R/W | 'b0 | Disable L4 clock gated | | |
| suspend_n | 0 | R/W | 'b1 | suspend, low active | | |

| Module::sdio | Register:: DBG_1 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0A20 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..10 | - | - | - | | |
| write_enable3 | 9 | W | - | Write enable for bit[8..6] | | |
| sel1 | 8..6 | R/W | 'h0 | Select control of dbg_sel1. | | |
| write_enable2 | 5 | W | - | Write enable for bit[4..2] | | |
| sel0 | 4..2 | R/W | 'h0 | Select control of dbg_sel0. | | |
| write_enable1 | 1 | W | - | Write enable for bit0. | | |
| enable | 0 | R/W | 'b0 | Debug Enable.<br>If set to 1, the debug port will be switched to the selected probed signals for observation.<br>If clear to 0 (default), the scpu_dbg_out0 and scpu_dbg_out1 are both static at 16'h0. | | |

| Module::sdio | Register:: DBG_2 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0A24 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | - | - | - | | |
| dbus_dbg_sel | 2..0 | R/W | 'h0 | sdio dbus dbg select | | |

| Module::sdio | Register:: DBG_3 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0A28 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..8 | - | - | - | | |
| ip_dbg_sel | 7..0 | R/W | 'h0 | sdio ip dbg select | | |

| Module::sdio | Register:: ISR | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_0A30 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..5 | - | - | - | | |
| Int4 | 4 | R/W | 'b0 | SDIO Int4. SDIO IP Int. | | |

| | | | | |
|---|---|---|---|---|
| Int3 | 3 | R/W | ‘b0 | SD Int3.SB1 wlast/rlast. |
| Rvd | 2 | - | - | - |
| Int1 | 1 | R/W | ‘b0 | SDIO Int1. DMA done. |
| write_data | 0 | W | - | 1 to set, 0 to clear bit with 1. |

| Module::sdio | Register:: ISREN | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A34 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..5 | - | - | - | | |
| Int4En | 4 | R/W | ‘b0 | SDIO Int4 Enable<br>IP Int Enable | | |
| Int3En | 3 | R/W | ‘b0 | SDIO Int3 Enable<br>SB1 wlast/rlast Int Enable | | |
| Rvd | 2 | - | - | - | | |
| Int1En | 1 | R/W | ‘b0 | SDIO Int1 Enable<br>Dma done Int Enable | | |
| write_data | 0 | W | - | 1 to set, 0 to clear bit with 1. | | |

| Module::sdio | Register::PAD_CTL | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A40 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..1 | R/W | - | - | | |
| tune3318 | 0 | R/W | ‘b1 | Pad select 3.3v or 1.8v,<br>1: 3.3v<br>0: 1.8v | | |

| Module::sdio | Register::CKGEN_CTL | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A44 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..19 | R/W | - | - | | |
| sd30_sample_change | 18 | R/W | ‘b0 | 0: from sd30_sample_clk_src | | |

| | | | | |
|---|---|---|---|---|
| | | | | 1: clk4M |
| sd30_push_change | 17 | R/W | 'b0 | 0: from sd30_push_clk_src<br>1: clk4M |
| crc_clk_change | 16 | R/W | 'b0 | 0: from crc_clk_src<br>1: clk4M |
| Rvd | 15..14 | R/W | - | - |
| sd30_sample_clk_src | 13:12 | R/W | 'b10 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 11..10 | R/W | - | - |
| sd30_push_clk_src | 9:8 | R/W | 'b01 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 7..6 | R/W | - | - |
| crc_clk_src | 5:4 | R/W | 'b00 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 3 | - | - | - |
| clk_div | 2..0 | R/W | 'h0 | 000: div1<br>001: div2<br>010: div4<br>011: div8 |

| Module::sdio | Register:: DMA_RST | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A50 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..1 | - | - | - | | |
| dma_rstn | 0 | R/W | 'b1 | dma soft reset. | | |

| Module::sdio | Register:: PAD_DRIVE | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_0A54 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..24 | - | - | - |
| dat_pad_pmos_drive | 23..20 | R/W | 'h0 | SDIO_DAT PAD PMOS drive select<br>bit[23]: NE4<br>bit[22]: NE3<br>bit[21]: NE2<br>bit[20]: NE5 |
| dat_pad_nmos_drive | 19..16 | R/W | 'h0 | SDIO_DAT PAD NMOS drive select<br>bit[19]: NE4<br>bit[18]: NE3<br>bit[17]: NE2<br>bit[16]: NE5 |
| cmd_pad_pmos_drive | 15..12 | R/W | 'h0 | SDIO_CMD PAD PMOS drive select<br>bit[15]: NE4<br>bit[14]: NE3<br>bit[13]: NE2<br>bit[12]: NE5 |
| cmd_pad_nmos_drive | 11..8 | R/W | 'h0 | SDIO_CMD PAD NMOS drive select<br>bit[11]: NE4<br>bit[10]: NE3<br>bit[9]: NE2<br>bit[8]: NE5 |
| clk_pad_pmos_drive | 7..4 | R/W | 'h0 | SDIO_CLK PAD PMOS drive select<br>bit[7]: NE4<br>bit[6]: NE3<br>bit[5]: NE2<br>bit[4]: NE5 |
| clk_pad_nmos_drive | 3..0 | R/W | 'h0 | SDIO_CLK PAD NMOS drive select<br>bit[3]: NE4<br>bit[2]: NE3<br>bit[1]: NE2<br>bit[0]: NE5 |

**※ PAD Drive Table**

eMMC wrapper control register

※SWC register, SWC access only!!! sb2 will block this register if from NWC access.

software need to set to 0 after rom code flow done.

| Module::emmc | Register:: DESC_CTL0 | | Set::1 | ATTR:: ctrl | Type::SR | ADDR::0x9801_2400 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..30 | - | - | - | | |
| base | 29:0 | R/W | ‘h0000 0000 | Descriptor base address (8B align) | | |

| Module::emmc | Register:: DESC_CTL1 | | Set::1 | ATTR:: ctrl | Type::SR | ADDR::0x9801_2404 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..30 | - | - | - | | |
| limit | 29..0 | R/W | ‘h0000 0000 | Descriptor limit address (8B align) | | |

| Module::emmc | Register::DESC_CTL2 | | Set::1 | ATTR:: nor_up | Type::SR | ADDR::0x9801_2408 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| desc_int_clr | 31 | R/W | ‘h0 | Descriptor interrupt clear | | |
| desc_go | 30 | R/W | ‘h0 | Trigger state machine | | |
| wptr | 29..0 | R/W | ‘h0 | Descriptor write pointer (8B align) | | |

| Module::emmc | Register::DESC_CTL3 | | Set::1 | ATTR:: nor_up | Type::SR | ADDR::0x9801_240C |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..30 | - | - | - | | |
| rptr | 29..0 | R/W | ‘h0 | Descriptor write pointer (8B align) | | |

Emmc wrapper descriptor format

DES0

| Name | bit field | Remarks |
|---|---|---|
| OWN | 31 | |
| Card Error Summary (CES) | 30 | |
| **IP cmd arg** | **29:6** | **IP cmd arg [23:0]** |
| End of Ring (ER) | 5 | |
| Second Address Chained (CH) | 4 | |
| First Descriptor (FS) | 3 | |
| Last Descriptor (LD) | 2 | |
| Disable Interrupt on Completion (DIC) | 1 | |
| reserved | 0 | |

DES1

| Name | bit field | Remarks |
|---|---|---|
| reserved | 31 | reserved |
| **IP cmd[12]** | 30 | **IP cmd [12]** |
| **IP cmd[11]** | 29 | **IP cmd [11]** |
| **IP cmd[10]** | 28 | **IP cmd [10]** |
| **IP cmd[9]** | 27 | **IP cmd [9]** |
| **IP cmd arg** | **26:19** | **IP cmd arg [31:24]** |
| **IP cmd** | **18:13** | **IP cmd [5:0]** |
| Buffer 1 Size | 12:0 | |

DES2

| Name | bit field | Remarks |
|---|---|---|
| Buffer Address Pointer 1 | 31:0 | |

DES3

| Name | bit field | Remarks |
|---|---|---|
| **IP byte count** | 31:0 | |



| Module::emmc | Register::DESC_STS | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_2410 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..16 | - | - | - | | |
| desc_sts | 15..0 | R | ‘h0 | Descriptor status = {9’h0, ptr_mis, desc_timeout, | | |

| | | | | |
|---|---|---|---|---|
| | | | | desc_state} |

Sts description

```
case(1'b1)
ps_desc_idle:           emmc_desc_status <= 0;
ps_desc_ptr:            emmc_desc_status <= 1;
ps_desc_fetch:          emmc_desc_status <= 2;
ps_desc_read1:          emmc_desc_status <= 3;
ps_desc_read2:          emmc_desc_status <= 4;
ps_desc_deco:           emmc_desc_status <= 5;
ps_desc_clr_int:        emmc_desc_status <= 6;
ps_desc_bytecnt:        emmc_desc_status <= 7;
ps_desc_cmd_arg:        emmc_desc_status <= 8;
ps_desc_cmd:            emmc_desc_status <= 9;
ps_desc_cmd_wait:       emmc_desc_status <= 10;
ps_desc_fake_dbus:      emmc_desc_status <= 11;
ps_desc_cmd_done:       emmc_desc_status <= 12;
ps_desc_xfer_wait:      emmc_desc_status <= 13;
ps_desc_xfer_done:      emmc_desc_status <= 14;
ps_desc_timeout:        emmc_desc_status <= 15;
ps_desc_int_chk:        emmc_desc_status <= 16;
ps_desc_int:            emmc_desc_status <= 17;
ps_desc_sts_chk:        emmc_desc_status <= 18;
```

Desc_int 發生條件 ：ps_desc_timeout or ps_desc_int or {ps_desc_sts_chk & read/write pointer equal (and the state machine will be idle)}

| Module::emmc | Register::DESC_THD | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2414 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| desc_timeout_bypass | 31 | R/W | ‘h0 | Descriptor timeout state bypass | | |
| desc_timeout_thd | 30..0 | R/W | ‘h3ffff | Descriptor timeout threshold | | |

| Module::emmc | Register::SYS_LOW_PWR | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2418 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..8 | - | - | - | | |
| mcu_pp_sram_lp_ena | 7 | R/W | ‘b0 | clk_sys domain MCU access pp_sram low power enable | | |
| sys_clk_gate_ena | 6 | R/W | ‘b1 | DMA clk_sys gating enable | | |
| cp_clk_gate_ena | 5 | R/W | ‘b1 | DMA cp part clk_sys gating enable | | |

| | | | | |
|---|---|---|---|---|
| dma_sram_lp_ena | 4 | R/W | ‘b0 | dma sram low power enable |
| dma_sram_rdy_num | 3:0 | R/W | ‘d10 | dma sram ready cycle (leave sleep mode)<br>(N+1) * clk_sys period |

| Module::emmc | Register:: CP | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_241c |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..26 | - | - | - | | |
| cp_de_en | 25 | R/W | ‘h0 | Cp decode enable | | |
| cp_length | 24..9 | R/W | ‘h00001 | NF <-> CP scramble/descramble length. | | |
| cp_first | 8 | R/W | ‘h0 | Cp first | | |
| cp_enable | 7 | R/W | ‘h0 | | | |
| cp_sram_sel | 6 | R/W | ‘h0 | | | |
| Rvd | 5..1 | - | - | - | | |
| cp_desc_sram_sel | 0 | R/W | ‘h0 | 0 : descriptor from DDR, 1: descriptor from cp sbuf | | |

| Module::emmc | Register:: OTHER1 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2420 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..2 | - | - | - | | |
| Dbus_endian_sel | 1 | R/W | ‘b0 | 0: little; 1: Big | | |
| l4_gated_disable | 0 | R/W | ‘b1 | Disable L4 gated clock | | |

| Module::emmc | Register:: ISR | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_2424 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..5 | - | - | - | | |
| ip_int_mask | 4 | R/W | ‘b0 | 0 : unmask, 1:mask | | |

| | | | | |
|---|---|---|---|---|
| desc_int_mask | 3 | R/W | ‘b0 | 0 : unmask, 1:mask |
| Dma_int_mask | 2 | R/W | ‘b0 | 0 : unmask, 1:mask |
| dma_done_int | 1 | R/W | ‘b0 | Dma done status |
| write_data | 0 | W | - | 1 to set, 0 to clear bit with 1. |

| Module::emmc | Register:: ISREN | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2428 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| dmy | 31..0 | R/W | ‘h0000 0000 | Dummy bit. | | |

| Module::emmc | Register:: DUMMY_SYS | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_242C |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| dmy | 31..0 | R/W | ‘h0000 0000 | Dummy bit. | | |

| Module::emmc | Register:: AHB | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2430 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | - | - | - | | |
| EMMC_ahb_m_big_endian | 2 | R/W | ‘b0 | Emmc ip dbus endian | | |
| EMMC_ahb_s_big_endian | 1 | R/W | ‘b0 | Emmc ip rbus endian | | |
| Rvd | 0 | - | - | - | | |

| Module::emmc | Register:: DBG | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_2444 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |

| | | | | |
|---|---|---|---|---|
| Rvd | 31..14 | - | - | - |
| write_enable3 | 13 | W | - | Write enable for bit[8..6] |
| sel1 | 12..8 | R/W | ‘h0 | Select control of dbg_sel1. |
| write_enable2 | 7 | W | - | Write enable for bit[4..2] |
| sel0 | 6..2 | R/W | ‘h0 | Select control of dbg_sel0. |
| write_enable1 | 1 | W | - | Write enable for bit0. |
| enable | 0 | R/W | ‘b0 | Debug Enable.<br>If set to 1, the debug port will be switched to the selected probed signals for observation.<br>If clear to 0 (default), the scpu_dbg_out0 and scpu_dbg_out1 are both static at 16’h0. |

| Module::emmc | Register::PP_BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2460 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..25 | R/W | - | - |
| bist_cr_desc_rme_0 | 24 | R/W | ‘b0 | Desc RM enable |
| bist_cr_desc_rm_0 | 23..20 | R/W | ‘h0 | Desc RM value |
| Rvd | 19..17 | R/W | - | - |
| bist_cr_ppb_rme_1 | 16 | R/W | ‘b0 | RM1 enable |
| bist_cr_ppb_rm_1 | 15..12 | R/W | ‘h0 | RM1 value |
| Rvd | 11..9 | R/W | - | - |
| bist_cr_ppb_rme_0 | 8 | R/W | ‘b0 | RM0 enable |
| bist_cr_ppb_rm_0 | 7..4 | R/W | ‘h0 | RM0 value |
| bist_drf_test_resume | 3 | R/W | ‘b0 | Bist drf test resume bit. |
| bist_drf_mode | 2 | R/W | ‘b0 | Bist drf enable bit. |
| bist_en | 1 | R/W | ‘b0 | Bist enable bit. |
| bist_ls | 0 | R/W | ‘b0 | Bist reset bist |

| Module::emmc | Register::IP_BIST_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2464 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..17 | R/W | - | - |
| bist_cr_ip_rme_1 | 16 | R/W | ‘b0 | RM1 enable |
| bist_cr_ip_rm_1 | 15..12 | R/W | ‘h0 | RM1 value |
| Rvd | 11..9 | R/W | - | - |
| bist_cr_ip_rme_0 | 8 | R/W | ‘b0 | RM0 enable |
| bist_cr_ip_rm_0 | 7..4 | R/W | ‘h0 | RM0 value |
| bist_drf_test_resume | 3 | R/W | ‘b0 | Bist drf test resume bit. |
| bist_drf_mode | 2 | R/W | ‘b0 | Bist drf enable bit. |
| bist_en | 1 | R/W | ‘b0 | Bist enable bit. |
| bist_ls | 0 | R/W | ‘b0 | Bist reset bist |

| Module::emmc | Register::PP_BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_2468 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..11 | R | - | - |
| bist_drf_start_pause | 10 | R | ‘b0 | IP DRF start pause |
| Rvd | 9 | R/W | - | - |
| bist_drf_fail_2 | 8 | R | ‘b0 | IP BIST DER 2 fail |
| bist_drf_fail_1 | 7 | R | ‘b0 | IP BIST DER 1 fail |
| bist_drf_fail_0 | 6 | R | ‘b0 | IP BIST DER 0 fail |
| bist_drf_done | 5 | R | ‘b0 | IP BIST DRF done |
| Rvd | 4 | R/W | - | - |

| | | | | |
|---|---|---|---|---|
| bist_2_fail | 3 | R | ‘b0 | IP BIST 2 fail |
| bist_1_fail | 2 | R | ‘b0 | IP BIST 1 fail |
| bist_0_fail | 1 | R | ‘b0 | IP BIST 0 fail |
| bist_done | 0 | R | ‘b0 | IP BIST finishing signal |

| Module::emmc | Register::IP_BIST_STS | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_246c |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..11 | R | - | - |
| bist_drf_start_pause | 10 | R | ‘b0 | IP DRF start pause |
| Rvd | 9 | R/W | - | - |
| Rvd | 8 | R/W | - | - |
| bist_drf_fail_1 | 7 | R | ‘b0 | IP BIST DER 1 fail |
| bist_drf_fail_0 | 6 | R | ‘b0 | IP BIST DER 0 fail |
| bist_drf_done | 5 | R | ‘b0 | IP BIST DRF done |
| Rvd | 4 | R/W | - | - |
| Rvd | 3 | R/W | - | - |
| bist_1_fail | 2 | R | ‘b0 | IP BIST 1 fail |
| bist_0_fail | 1 | R | ‘b0 | IP BIST 0 fail |
| bist_done | 0 | R | ‘b0 | IP BIST finishing signal |

| Module::emmc | Register::IP_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2470 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..16 | R/W | - | - |
| asic_crc_dbgo_sel | 15..8 | R/W | ‘h0 | IP dbug page sel 1 |
| Rvd | 7 | R/W | - | - |

| | | | | |
|---|---|---|---|---|
| crc_dbgo_sel | 6..3 | R/W | ‘h0 | IP dbug page sel 2 |
| ip_ea_flash | 2 | R/W | ‘b0 | IP ea flash |
| crc_clk_disable_trig | 1 | R/W | ‘b0 | IP auto disable crc_clk triggle |
| mcu_time_1_us | 0 | R/W | ‘b0 | IP mcu control |

| Module::emmc | Register::PAD_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2474 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..1 | R/W | - | - |
| tune3318 | 0 | R/W | ‘b1 | Pad select 3.3v or 1.8v,<br>1: 3.3v<br>0: 1.8v |

| Module::emmc | Register::CKGEN_CTL | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2478 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..19 | R/W | - | - |
| sd30_sample_change | 18 | R/W | ‘b0 | 0: from sd30_sample_clk_src<br>1: clk4M |
| sd30_push_change | 17 | R/W | ‘b0 | 0: from sd30_push_clk_src<br>1: clk4M |
| crc_clk_change | 16 | R/W | ‘b0 | 0: from crc_clk_src<br>1: clk4M |
| Rvd | 15..14 | R/W | - | - |
| sd30_sample_clk_src | 13:12 | R/W | ‘b10 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 11..10 | R/W | - | - |
| sd30_push_clk_src | 9:8 | R/W | ‘b01 | 00: ssc_clk |

| | | | | |
|---|---|---|---|---|
| | | | | 01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 7..6 | R/W | - | - |
| crc_clk_src | 5:4 | R/W | 'b00 | 00: ssc_clk<br>01: ssc_clk_vp0<br>10: ssc_clk_vp1 |
| Rvd | 3 | - | - | - |
| clk_div | 2..0 | R/W | 'h0 | 000: div1<br>001: div2<br>010: div4<br>011: div8 |

| ~~Module::emmc~~ | ~~Register::CPU_ACC_CTRL~~ | | ~~Set::1~~ | ~~ATTR::nor~~ | ~~Type::SR~~ | ~~ADDR::0x9801_2480~~ |
|---|---|---|---|---|---|---|
| ~~Name~~ | ~~Bits~~ | ~~R/W~~ | ~~Default~~ | ~~Comments~~ | | |
| ~~Rvd~~ | ~~31..3~~ | ~~-~~ | ~~-~~ | ~~-~~ | | |
| ~~buf_full~~ | ~~2~~ | ~~R~~ | ~~'b0~~ | ~~buf_full flag.~~ | | |
| ~~buf_sw~~ | ~~1~~ | ~~R/W~~ | ~~'b0~~ | ~~if buf_sw set to 1, hw will load next 512bytes data in dma_buffer0/1. this register will auto-clear.~~ | | |
| ~~cpu_mode~~ | ~~0~~ | ~~R/W~~ | ~~'b0~~ | ~~if cpu_mode = 1, cpu can access dma_buffer0 and dma_buffer1 data via rbus.~~<br>~~dma_buffer0 range : 0x18012200 ~ 0x180122FF and bit[2] = 0 means data[31:0],~~<br>~~bit[2] = 1 means data[63:32].~~<br>~~dma_buffer1 range : 0x18012300 ~ 0x180123FF and bit[2] = 0 means data[31:0],~~<br>~~bit[2] = 1 means data[63:32].~~ | | |

| Module::emmc | Register::CARD_SIG | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2484 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |

| | | | | |
|---|---|---|---|---|
| Rvd | 31..1 | R/W | - | - |
| EMMC_RST_n | 0 | R/W | ‘b1 | EMMC_RST_n |

| Module::emmc | Register::CARD_DRV | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2490 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| EMMC_card_drive | 31..24 | R/W | ‘b0101 0101 | - |
| EMMC_dat_n_drive | 23:20 | R/W | ‘b0000 | **SD_DATA PAD NMOS drive select**<br>**bit[3]: NE4**<br>**bit[2]: NE3**<br>**bit[1]: NE2**<br>bit[0]: NE5 |
| EMMC_dat_p_drive | 19:16 | R/W | ‘b0000 | **SD_DATA PAD PMOS drive select**<br>**bit[7]: PE4**<br>**bit[6]: PE3**<br>**bit[5]: PE2**<br>**bit[4]: PE5** |
| EMMC_cmd_n_drive | 15:12 | R/W | ‘b0000 | **SD_CMD PAD NMOS drive select**<br>**bit[3]: NE4**<br>**bit[2]: NE3**<br>**bit[1]: NE2**<br>bit[0]: NE5 |
| EMMC_cmd_p_drive | 11:8 | R/W | ‘b0000 | **SD_CMD PAD PMOS drive select**<br>**bit[7]: PE4**<br>**bit[6]: PE3**<br>**bit[5]: PE2**<br>**bit[4]: PE5** |
| EMMC_clk_n_drive | 7:4 | R/W | ‘b0000 | **SD_CLK PAD NMOS drive select**<br>**bit[3]: NE4**<br>**bit[2]: NE3**<br>**bit[1]: NE2**<br>bit[0]: NE5 |
| EMMC_clk_p_drive | 3:0 | R/W | ‘b0000 | **SD_CLK PAD PMOS drive select** |

| | | | | |
|---|---|---|---|---|
| | | | | **bit[7]: PE4**<br>**bit[6]: PE3**<br>**bit[5]: PE2**<br>**bit[4]: PE5** |

| Module::emmc | Register::CARD_DRV1 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2494 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..9 | R/W | - | - |
| EMMC_sd_pupdc | 8:6 | R/W | ‘b001 | |
| EMMC_card_output_en | 5:0 | R/W | ‘b000000 | |

| Module::emmc | Register::DQS_CTRL1 | Set::1 | ATTR::nor_up | Type::SR | ADDR::0x9801_2498 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..8 | - | - | - |
| fw_set | 7 | R/W | ‘b0 | 1’b1 : set dqs delay value by fireware, auto clear to 0. |
| fw_dlyn | 6..0 | R/W | ‘h00 | dqs delay value |

| Module::emmc | Register::DQS_CTRL2 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_249c |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..8 | - | - | - |
| auto_cal | 7 | R/W | ‘h0 | auto calibration enable |
| Rvd | 6 | - | - | - |
| pos_trig_sel | 5..3 | R/W | ‘h00 | dq calibration range selection.<br>000: 2 tap<br>001: 3 tap<br>010: 4 tap<br>011: 5 tap<br>100: 6 tap<br>101: 8 tap<br>110: 6 tap<br>111: 8 tap |
| pre_trig_sel | 2..0 | R/W | ‘h00 | dq calibration range selection.<br>000: 2 tap<br>001: 3 tap<br>010: 4 tap |

| | | | | |
|---|---|---|---|---|
| | | | | 011: 5 tap<br>100: 6 tap<br>101: 8 tap<br>110: 6 tap<br>111: 8 tap |

| Module::emmc | Register::IP_DESC0 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24a0 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Desc0 | 31..0 | R | 'h0 | Descriptor 0 | | |

| Module::emmc | Register::IP_DESC1 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24a4 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Desc1 | 31..0 | R | 'h0 | Descriptor 1 | | |

| Module::emmc | Register::IP_DESC2 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24a8 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Desc2 | 31..0 | R | 'h0 | Descriptor 2 | | |

| Module::emmc | Register::IP_DESC3 | | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24ac |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Desc3 | 31..0 | R | 'h0 | Descriptor 3 | | |

| Module::emmc | Register::main2_dbg | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24b0 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..3 | R/W | - | - | | |

| | | | | |
|---|---|---|---|---|
| main2_dbg_en | 2 | R/W | ‘b0 | Main2 block debug enable |
| main2_dbg_sel | 1:0 | R/W | ‘b000 | 0 : NF<br>1: CR<br>2: PCIE0<br>3: PCIE1 |

| Module::emmc | Register::tm_sensor_ctrl0 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24b4 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..29 | R/W | - | - |
| reg_a | 28..0 | R/W | ‘b0100000011111110000000000000 | - |

| Module::emmc | Register::tm_sensor_ctrl1 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24b8 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..29 | R/W | - | - |
| reg_chopen | 28 | R/W | ‘b0 | |
| reg_cal_en | 27 | R/W | ‘b0 | |
| reg_biasdem_sel | 26 | R/W | ‘b1 | |
| reg_biaschop | 25 | R/W | ‘b0 | |
| reg_adccksel | 24..22 | R/W | ‘b101 | |
| reg_b | 21..0 | R/W | ‘b1101110010000000000000 | |

| Module::emmc | Register::tm_sensor_ctrl2 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24bc |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..25 | R/W | - | - |
| reg_vbe_biassel | 24..23 | R/W | ‘b11 | |
| reg_sdm_test_en | 22 | R/W | ‘b0 | |
| reg_sdm_test | 21 | R/W | ‘b0 | |
| reg_rstb | 20 | R/W | ‘b0 | |
| reg_resol | 19..18 | R/W | ‘b00 | |
| reg_ppow | 17 | R/W | ‘b1 | |
| reg_osccursel | 16..15 | R/W | ‘b00 | |
| reg_order3 | 14 | R/W | ‘b1 | |
| reg_opcursel | 13..12 | R/W | ‘b00 | |
| reg_hold_en | 11 | R/W | ‘b0 | |
| reg_hold_dly | 10..9 | R/W | ‘b00 | |
| reg_filteredgesel | 8 | R/W | ‘b0 | |
| reg_dsr | 7..5 | R/W | ‘b010 | |
| reg_cksourcesel | 4 | R/W | ‘b0 | |
| reg_chopfreqsel | 3..0 | R/W | ‘b0111 | |

| Module::emmc | Register::tm_sensor_ctrl3 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24c0 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..22 | R/W | - | - |
| reg_offset | 21..0 | R/W | ‘b10000000000 | - |

| | | | | |
|---|---|---|---|---|
| | | | 00000000 | |

| Module::emmc | Register::tm_sensor_ctrl4 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24c4 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..24 | R/W | - | - |
| reg_r | 23..0 | R/W | ‘b001111000000000000000 | - |

| Module::emmc | Register::tm_sensor_ctrl5 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24c8 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..23 | R/W | - | - |
| reg_s | 22..0 | R/W | ‘b010000000000000000000 | - |

| Module::emmc | Register::tm_sensor_status1 | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24cc |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..19 | - | - | - |
| ct_out | 18..0 | R | - | |

| Module::emmc | Register::tm_sensor_status2 | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24d0 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..22 | - | - | - |
| u_out | 21..0 | R | - | |

| Module::emmc | Register:: swc_sel | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24d4 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..1 | - | - | - | | |
| swc_sel | 0 | R/W | ‘h0 | | | |

| Module::emmc | Register:: dss_c30_7t_ctrl | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24dc |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..28 | - | - | |
| c30_data_in | 27..8 | R/W | ‘b0 | Input data for speed comparison |
| Rvd | 7..6 | - | - | |
| c30_speed_en | 5 | R/W | ‘b0 | Speed sensor enable<br>0: disable<br>1: enable |
| c30_wire_sel | 4 | R/W | ‘b0 | Wire selection<br>0 : long wire/delay cell/clock buffer<br>1 : short wire |
| c30_ro_sel | 3..1 | R/W | ‘b0 | Ring Oscillator selection<br>000: select dss_clk (for test mode)<br>001 : select 1st ring oscillator<br>010 : select 2nd ring oscillator<br>011 : select 3rd ring oscillator<br>100 : select 4th ring oscillator<br>101 : select multi-library ring oscillator<br>Others : not used |
| c30_dss_rst_n | 0 | R/W | ‘b0 | Reset signal of Speed-Sensor (low active)<br>(Software control reset) |

| Module::emmc | Register:: dss_c30_7t_status | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24e0 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..24 | - | - | |
| c30_count_out | 23..4 | R | - | Counter value indicates the speed of selected ring oscillator<br>Cycle time = (count_out*dss_clk period)/ 16384 |

| | | | | |
|---|---|---|---|---|
| Rvd | 3..2 | - | - | |
| c30_wsort_go | 1 | R | - | 0: measured speed slower than expected.<br>1: measured speed faster than expected. |
| c30_ready | 0 | R | - | Ready strobe to read count_out value |

| Module::emmc | Register:: dss_c30_7t_debug | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24e4 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..16 | - | - | |
| c30_dbgo | 15..0 | R | - | Debug signal |

| Module::emmc | Register:: dss_c35_7t_ctrl | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24e8 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..28 | - | - | |
| c35_data_in | 27..8 | R/W | 'b0 | Input data for speed comparison |
| Rvd | 7..6 | - | - | |
| c35_speed_en | 5 | R/W | 'b0 | Speed sensor enable<br>0: disable<br>1: enable |
| c35_wire_sel | 4 | R/W | 'b0 | Wire selection<br>0 : long wire/delay cell/clock buffer<br>1 : short wire |
| c35_ro_sel | 3..1 | R/W | 'b0 | Ring Oscillator selection<br>000: select dss_clk (for test mode)<br>001 : select 1st ring oscillator<br>010 : select 2nd ring oscillator<br>011 : select 3rd ring oscillator<br>100 : select 4th ring oscillator<br>101 : select multi-library ring oscillator<br>Others : not used |
| c35_dss_rst_n | 0 | R/W | 'b0 | Reset signal of Speed-Sensor (low active)<br>(Software control reset) |

| Module::emmc | Register:: dss_c35_7t_status | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24ec |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..24 | - | - | |
| c35_count_out | 23..4 | R | - | Counter value indicates the speed of selected ring oscillator<br>Cycle time = (count_out*dss_clk period)/ 16384 |
| Rvd | 3..2 | - | - | |
| c35_wsort_go | 1 | R | - | 0: measured speed slower than expected.<br>1: measured speed faster than expected. |
| c35_ready | 0 | R | - | Ready strobe to read count_out value |

| Module::emmc | Register:: dss_c35_7t_debug | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24f0 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..16 | - | - | |
| c35_dbgo | 15..0 | R | - | Debug signal |

| Module::emmc | Register:: dss_c40_7t_ctrl | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_24f4 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..28 | - | - | |
| c40_data_in | 27..8 | R/W | 'b0 | Input data for speed comparison |
| Rvd | 7..6 | - | - | |
| c40_speed_en | 5 | R/W | 'b0 | Speed sensor enable<br>0: disable<br>1: enable |
| c40_wire_sel | 4 | R/W | 'b0 | Wire selection<br>0 : long wire/delay cell/clock buffer<br>1 : short wire |
| c40_ro_sel | 3..1 | R/W | 'b0 | Ring Oscillator selection<br>000: select dss_clk (for test mode)<br>001 : select 1st ring oscillator<br>010 : select 2nd ring oscillator<br>011 : select 3rd ring oscillator<br>100 : select 4th ring oscillator<br>101 : select multi-library ring oscillator<br>Others : not used |
| c40_dss_rst_n | 0 | R/W | 'b0 | Reset signal of Speed-Sensor (low active)<br>(Software control reset) |

| Module::emmc | Register:: dss_c40_7t_status | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24f8 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..24 | - | - | |
| c40_count_out | 23..4 | R | - | Counter value indicates the speed of selected ring oscillator<br>Cycle time = (count_out*dss_clk period)/ 16384 |
| Rvd | 3..2 | - | - | |
| c40_wsort_go | 1 | R | - | 0: measured speed slower than expected.<br>1: measured speed faster than expected. |
| c40_ready | 0 | R | - | Ready strobe to read count_out value |

| Module::emmc | Register:: dss_c40_7t_debug | Set::1 | ATTR::nor | Type::SR | ADDR::0x9801_24fc |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..16 | - | - | |

| | | | | |
|---|---|---|---|---|
| c40_dbgo | 15..0 | R | - | Debug signal |

PadFunction and PadMux Control Register

**Register Summary**

| *Physical Address* | *Name* | *R/W* | *Description* |
|---|---|---|---|
| 0x9801_2600 | main2_muxpad0 | R/W | pad mux Register 0 |
| 0x9801_2604 | mian2_muxpad1 | R/W | pad mux Register 1 |
| 0x9801_2608 | main2_pfunc_nf0 | R/W | pad function nf0 |
| 0x9801_260C | main2_pfunc_nf1 | R/W | pad function nf1 |
| 0x9801_2610 | main2_pfunc_cr | R/W | pad function cr |
| 0x9801_2614 | main2_pfunc_sdio | R/W | pad function sdio |
| 0x9801_2618 | main2_pfunc_nf2 | R/W | pad function emmc |
| 0x9801_261C | main2_muxpad2 | R/W | pad mux Register 2 |
| 0x9801_2620 | main2_pdrive_nf0 | R/W | Pad driving for NF/EMMC |
| 0x9801_2624 | main2_pdrive_nf1 | R/W | Pad driving for NF/EMMC |
| 0x9801_2628 | main2_pdrive_nf2 | R/W | Pad driving for NF/EMMC |
| 0x9801_262C | main2_pdrive_nf3 | R/W | Pad driving for NF/EMMC |
| 0x9801_2630 | main2_pdrive_nf4 | R/W | Pad driving for NF/EMMC |
| 0x9801_2634 | main2_pdrive_cr0 | R/W | Pad driving for CR |
| 0x9801_2638 | main2_pdrive_cr1 | R/W | Pad driving for CR |
| 0x9801_263C | main2_pdrive_sdio0 | R/W | Pad driving for SDIO |
| 0x9801_2640 | main2_pdrive_sdio1 | R/W | Pad driving for SDIO |
| ~0x9801_27FF | Reserved | - | - |

| **NF/CR pin mux plan** | | |
|---|---|---|
| NAND flash pin | EMMC card pin | SDIO pin |
| MMC_CMD | | SDIO_CMD |
| MMC_CLK | | SDIO_CLK |
| MMC_WP | | X |
| MMC_CD | | X |
| MMC_DAT[0] | | SDIO_DATA[0] |
| MMC_DAT[1] | | SDIO_DATA[1] |
| MMC_DAT[2] | | SDIO_DATA[2] |
| MMC_DAT[3] | | SDIO_DATA[3] |
| NF_CLE | EMMC_CLK | |
| NF_ALE | x | |
| NF_RD_N | EMMC_CMD | |
| NF_WR_N | x | |
| NF_RDY | EMMC_RST_N | |
| NF_DD[7] | EMMC_DATA[7] | |
| NF_DD[6] | EMMC_DATA[6] | |
| NF_DD[5] | EMMC_DATA[5] | |
| NF_DD[4] | EMMC_DATA[4] | |
| NF_DD[3] | EMMC_DATA[3] | |
| NF_DD[2] | EMMC_DATA[2] | |
| NF_DD[1] | EMMC_DATA[1] | |
| NF_DD[0] | EMMC_DATA[0] | |
| X | EMMC_DD_SB | |
| NF_CE_N[1] | X | |

| | | |
|---|---|---|
| NF_CE_N[0] | | |

| SDIO pin mux plan |
|---|
| NAND flash pin |
| SDIO_CMD |
| SDIO_CLK |
| SDIO_DATA[0] |
| SDIO_DATA[1] |
| SDIO_DATA[2] |
| SDIO_DATA[3] |
| ~~SDIO_DATA[4]~~ |
| ~~SDIO_DATA[5]~~ |
| ~~SDIO_DATA[6]~~ |
| ~~SDIO_DATA[7]~~ |

| Module::emmc | Register::muxpad0 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2600 |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| nf_dd_7 | 31..30 | R/W | ‘b01 | 00 : Mux to gpio[69]/main2_gpio[5]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[7]<br>11 : Mux to AVCPU EJ_TCLK (location 2)<br>Others : Revised |
| nf_dd_6 | 29..28 | R/W | ‘b01 | 00 : Mux to gpio[70]/main2_gpio[6]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[6]<br>11 : Mux to AVCPU EJ_TMS (location 2)<br>Others : Revised |
| nf_dd_5 | 27..26 | R/W | ‘b01 | 00 : Mux to gpio[71]/main2_gpio[7]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[5]<br>11 : Mux to AVCPU EJ_RST_N (location 2)<br>Others : Revised |
| nf_dd_4 | 25..24 | R/W | ‘b01 | 00 : Mux to gpio[72]/main2_gpio[8]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[4]<br>11 : Mux to HIF_EN (location 2)<br>Others : Revised |
| nf_dd_3 | 23..22 | R/W | ‘b01 | 00 : Mux to gpio[73]/main2_gpio[9]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[3]<br>Others : Revised |
| nf_dd_2 | 21..20 | R/W | ‘b01 | 00 : Mux to gpio[74]/main2_gpio[10]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[2]<br>Others : Revised |
| nf_dd_1 | 19..18 | R/W | ‘b01 | 00 : Mux to gpio[75]/main2_gpio[11]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[1] |

| | | | | |
|---|---|---|---|---|
| | | | | Others : Revised |
| nf_dd_0 | 17..16 | R/W | 'b01 | 00 : Mux to gpio[76]/main2_gpio[12]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to eMMC DATA[0]<br>Others : Revised |
| nf_ce_n_1 | 15..14 | R/W | 'b01 | 00 : Mux to gpio[79]/main2_gpio[15]<br>01 : Mux to NAND flash I/F.<br>Others : Revised |
| nf_ce_n_0 | 13..12 | R/W | 'b01 | 00 : Mux to gpio[78]/main2_gpio[14]<br>01 : Mux to NAND flash I/F<br>10 : N/A<br>Others : Revised |
| nf_cle | 11..10 | R/W | 'b01 | 00 : Mux to gpio[64]/main2_gpio[0]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to EMMC CLK (location1)<br>11 : Mux to HIF_DATA (location 2)<br>Others : Revised |
| nf_ale | 9..8 | R/W | 'b01 | 00 : Mux to gpio[65]/main2_gpio[1]<br>01 : Mux to NAND flash I/F.<br>~~10: Mux to EMMC CD~~<br>11 : Mux to HIF_RDY (location 2)<br>Others : Revised |
| nf_wr_n | 7..6 | R/W | 'b01 | 00 : Mux to gpio[67]/main2_gpio[3]<br>01 : Mux to NAND flash I/F.<br>~~10 : Mux toEMMC write protect~~<br>11 : Mux to HIF_CLK (location 2)<br>Others : Revised |
| nf_rd_n | 5..4 | R/W | 'b01 | 00 : Mux to gpio[66]/main2_gpio[2]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to EMMC CMD<br>11 : Mux to AVCPU EJ_TDI (location 2)<br>Others : Revised |
| nf_rdy | 3..2 | R/W | 'b01 | 00 : Mux to gpio[68]/main2_gpio[4]<br>01 : Mux to NAND flash I/F.<br>10 : Mux to EMMC RST N<br>11 : Mux to AVCPU EJ_TDO (location 2)<br>Others : Revised |
| nf_dqs | 1..0 | R/W | 'b01 | 00 : Mux to gpio[77]/main2_gpio[13]<br>01 : Mux to NAND flash I/F.<br>10 : N/A<br>11 : N/A<br>Others : Revised |

| Module::emmc | Register::muxpad1 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2604 |
|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | |
| mmc_data_3 | 31..30 | R/W | 'b01 | 00 : Mux to gpio[88]/main2_gpio[24]<br>01 : Mux to SD card I/F (mmc_data[3])<br>10: Mux to SDIO I/F (sdio_data[3])<br>11 : Mux to SCPU EJTAG I/F (ej_tclk location2)<br>Others : Revised | |

| | | | | |
|---|---|---|---|---|
| mmc_data_2 | 29..28 | R/W | ‘b01 | 00 : Mux to gpio[87]/main2_gpio[23]<br>01 : Mux to SD card I/F (mmc_data[2])<br>10: Mux to SDIO I/F (sdio_data[2])<br>Others : Revised |
| mmc_data_1 | 27..26 | R/W | ‘b01 | 00 : Mux to gpio[86]/main2_gpio[22]<br>01 : Mux to SD card I/F (mmc_data[1])<br>10: Mux to SDIO I/F (sdio_data[1])<br>Others : Revised |
| mmc_data_0 | 25..24 | R/W | ‘b01 | 00 : Mux to gpio[85]/main2_gpio[21]<br>01 : Mux to SD card I/F (mmc_data[0])<br>10: Mux to SDIO I/F (sdio_data[0])<br>11 : Mux to SCPU EJTAG I/F (ej_rst_n location 2)<br>Others : Revised |
| mmc_cd | 23..22 | R/W | ‘b00 | 00 : Mux to gpio[84]/main2_gpio[20]<br>01 : Mux to SD card I/F (sd_card_detect)<br>Others : Revised |
| mmc_wp | 21..20 | R/W | ‘b00 | 00 : Mux to gpio[83]/main2_gpio[19]<br>01 : Mux to SD card I/F (sd_write_protect)<br>11 : Mux to SCPU EJTAG I/F (ej_tdi location 2)<br>Others : Revised |
| mmc_clk | 19..18 | R/W | ‘b01 | 00 : Mux to gpio[82]/main2_gpio[18]<br>01 : Mux to SD card I/F (sd_clk)<br>10: Mux to SDIO I/F (sdio_clk)<br>11 : Mux to SCPU EJTAG I/F (ej_tdo location 2)<br>Others : Revised |
| mmc_cmd | 17..16 | R/W | ‘b01 | 00 : Mux to gpio[81]/main2_gpio[17]<br>01 : Mux to SD card I/F (sd_cmd)<br>10: Mux to SDIO I/F (sdio_cmd)<br>11 : Mux to SCPU EJTAG I/F (ej_tms location 2)<br>Others : Revised |
| Rvd | 15..14 | - | - | - |
| emmc_dd_sb | 13..12 | R/W | ‘b00 | 00 : Mux to gpio[80]/main2_gpio[16]<br>01 : N/A<br>10 : Mux to EMMC Data Strobe (DI)<br>11 : N/A<br>Others : Revised |
| sdio_data_3 | 11..10 | R/W | ‘b01 | 00 : Mux to gpio[94]/main2_gpio[30]<br>01 : Mux to SDIO I/F (sdio_data[3])<br>10 : N/A<br>11 : N/A<br>Others : Revised |
| sdio_data_2 | 9..8 | R/W | ‘b01 | 00 : Mux to gpio[93]/main2_gpio[29]<br>01 : Mux to SDIO I/F (sdio_data[2])<br>10 : N/A<br>11 : N/A<br>Others : Revised |
| sdio_data_1 | 7..6 | R/W | ‘b01 | 00 : Mux to gpio[92]/main2_gpio[28]<br>01 : Mux to SDIO I/F (sdio_data[1])<br>10 : N/A<br>11 : N/A<br>Others : Revised |

| | | | | |
|---|---|---|---|---|
| sdio_data_0 | 5..4 | R/W | ‘b01 | 00 : Mux to gpio[91]/main2_gpio[27]<br>01 : Mux to SDIO I/F (sdio_data[0])<br>10 : N/A<br>11 : N/A<br>Others : Revised |
| sdio_clk | 3..2 | R/W | ‘b01 | 00 : Mux to gpio[90]/main2_gpio[26]<br>01 : Mux to SD card I/F (sdio_clk)<br>10 : N/A<br>11 : N/A<br>Others : Revised |
| sdio_cmd | 1..0 | R/W | ‘b01 | 00 : Mux to gpio[89]/main2_gpio[25]<br>01 : Mux to SDIO I/F (sdio_cmd)<br>10 : N/A<br>11 : N/A<br>Others : Revised |



- NAND Flash pad function selection

| Module::emmc | Register::pfunc_nf0 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2608 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| nf_cle_smt | 31 | R/W | ‘b0 | NF_CLE pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 30 | - | - | - | | |
| nf_cle_pud_en | 29 | R/W | ‘b0 | NF_CLE pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| nf_cle_pud_sel | 28 | R/W | ‘b0 | NF_CLE pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| nf_wr_n _smt | 27 | R/W | ‘b0 | NF_WR_N pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 26 | - | - | - | | |
| nf_wr_n _pud_en | 25 | R/W | ‘b1 | NF_WR_N pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| nf_wr_n _pud_sel | 24 | R/W | ‘b1 | NF_WR_N pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| nf_rd_n _smt | 23 | R/W | ‘b0 | NF_RD_N pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 22 | - | - | - | | |
| nf_rd_n _pud_en | 21 | R/W | ‘b1 | NF_RD_N pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| nf_rd_n_pud_sel | 20 | R/W | ‘b1 | NF_RD_N pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| nf_rdy _smt | 19 | R/W | ‘b0 | NF_RDY pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |

| | | | | |
|---|---|---|---|---|
| Rvd | 18 | - | - | - |
| nf_rdy _pud_en | 17 | R/W | ‘b1 | NF_RDY pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_rdy_pud_sel | 16 | R/W | ‘b1 | NF_RDY pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_ce_n_1_smt | 15 | R/W | ‘b0 | NF_CE_N_1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 14 | - | - | - |
| nf_ce_n_1_pud_en | 13 | R/W | ‘b1 | NF_CE_N_1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_ce_n_1_pud_sel | 12 | R/W | ‘b1 | NF_CE_N_1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_ce_n_0_smt | 11 | R/W | ‘b0 | NF_CE_N_0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 10 | - | - | - |
| nf_ce_n_0_pud_en | 9 | R/W | ‘b1 | NF_CE_N_0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_ce_n_0_pud_sel | 8 | R/W | ‘b1 | NF_CE_N_0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_ale_smt | 7 | R/W | ‘b0 | NF_ALE pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 6 | - | - | - |
| nf_ale_pud_en | 5 | R/W | ‘b0 | NF_ALE pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_ale_pud_sel | 4 | R/W | ‘b0 | NF_ALE pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dqs_smt | 3 | R/W | ‘b0 | NF_DQS pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 2 | - | - | - |
| nf_dqs_pud_en | 1 | R/W | ‘b0 | NF_DQS pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dqs_pud_sel | 0 | R/W | ‘b0 | NF_DQS pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |

| Module::emmc | Register::pfunc_nf1 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_260C |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| nf_dd_7_smt | 31 | R/W | ‘b0 | NF_DD_7 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 30 | - | - | - | | |
| nf_dd_7_pud_en | 29 | R/W | ‘b1 | NF_DD_7 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| nf_dd_7_pud_sel | 28 | R/W | ‘b1 | NF_DD_7 pad pull-up /pull-down function selection. | | |

| | | | | |
|---|---|---|---|---|
| | | | | 1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_6_smt | 27 | R/W | ‘b0 | NF_DD_6 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 26 | - | - | - |
| nf_dd_6_pud_en | 25 | R/W | ‘b1 | NF_DD_6 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_6_pud_sel | 24 | R/W | ‘b1 | NF_DD_6 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_5_smt | 23 | R/W | ‘b0 | NF_DD_5 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 22 | - | - | - |
| nf_dd_5_pud_en | 21 | R/W | ‘b1 | NF_DD_5 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_5_pud_sel | 20 | R/W | ‘b1 | NF_DD_5 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_4_smt | 19 | R/W | ‘b0 | NF_DD_4 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 18 | - | - | - |
| nf_dd_4_pud_en | 17 | R/W | ‘b1 | NF_DD_4 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_4_pud_sel | 16 | R/W | ‘b1 | NF_DD_4 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_3_smt | 15 | R/W | ‘b0 | NF_DD_3 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 14 | - | - | - |
| nf_dd_3_pud_en | 13 | R/W | ‘b1 | NF_DD_3 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_3_pud_sel | 12 | R/W | ‘b1 | NF_DD_3 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_2_smt | 11 | R/W | ‘b0 | NF_DD_2 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 10 | - | - | - |
| nf_dd_2_pud_en | 9 | R/W | ‘b1 | NF_DD_2 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_2_pud_sel | 8 | R/W | ‘b1 | NF_DD_2 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| nf_dd_1_smt | 7 | R/W | ‘b0 | NF_DD_1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 6 | - | - | - |
| nf_dd_1_pud_en | 5 | R/W | ‘b1 | NF_DD_1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable (Kylin ECOB fix) |
| nf_dd_1_pud_sel | 4 | R/W | ‘b1 | NF_DD_1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up (Kylin ECOB fix) |
| nf_dd_0_smt | 3 | R/W | ‘b0 | NF_DD_0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |

| | | | | |
|---|---|---|---|---|
| Rvd | 2 | - | - | - |
| nf_dd_0_pud_en | 1 | R/W | ‘b1 | NF_DD_0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| nf_dd_0_pud_sel | 0 | R/W | ‘b1 | NF_DD_0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |

| Module::emmc | Register::pfunc_cr | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2610 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| mmc_data_3_smt | 31 | R/W | ‘b0 | MMC_DATA3 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 30 | - | - | - | | |
| mmc_data_3_pud_en | 29 | R/W | ‘b1 | MMC_DATA3 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| mmc_data_3_pud_sel | 28 | R/W | ‘b0 | MMC_DATA3 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| mmc_data_2_smt | 27 | R/W | ‘b0 | MMC_DATA2 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 26 | - | - | - | | |
| mmc_data_2_pud_en | 25 | R/W | ‘b1 | MMC_DATA2 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| mmc_data_2_pud_sel | 24 | R/W | ‘b0 | MMC_DATA2 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| mmc_data_1_smt | 23 | R/W | ‘b0 | MMC_DATA1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 22 | - | - | - | | |
| mmc_data_1_pud_en | 21 | R/W | ‘b1 | MMC_DATA1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| mmc_data_1_pud_sel | 20 | R/W | ‘b0 | MMC_DATA1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| mmc_data_0_smt | 19 | R/W | ‘b0 | MMC_DATA0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| Rvd | 18 | - | - | - | | |
| mmc_data_0_pud_en | 17 | R/W | ‘b1 | MMC_DATA0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| mmc_data_0_pud_sel | 16 | R/W | ‘b0 | MMC_DATA0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| mmc_cd_smt | 15 | R/W | ‘b0 | MMC_CD pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| mmc_cd_e2 | 14 | R/W | ‘b0 | MMC_CD pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA | | |
| mmc_cd_pud_en | 13 | R/W | ‘b1 | MMC_CD pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |

| | | | | |
|---|---|---|---|---|
| mmc_cd_pud_sel | 12 | R/W | ‘b1 | MMC_CD pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| mmc_wp_smt | 11 | R/W | ‘b0 | MMC_WP pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| mmc_wp_e2 | 10 | R/W | ‘b0 | MMC_WP pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA |
| mmc_wp_pud_en | 9 | R/W | ‘b1 | MMC_WP pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| mmc_wp_pud_sel | 8 | R/W | ‘b1 | MMC_WP pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| mmc_clk_smt | 7 | R/W | ‘b0 | MMC_CLK pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 6 | - | - | - |
| mmc_clk_pud_en | 5 | R/W | ‘b1 | MMC_CLK pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| mmc_clk_pud_sel | 4 | R/W | ‘b0 | MMC_CLK pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| mmc_cmd_smt | 3 | R/W | ‘b0 | MMC_CMD pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 2 | - | - | - |
| mmc_cmd_pud_en | 1 | R/W | ‘b1 | MMC_CMD pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| mmc_cmd_pud_sel | 0 | R/W | ‘b0 | MMC_CMD pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |

| Module::emmc | Register::pfunc_sdio | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2614 |
|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | |
| sdio_data_3_smt | 31 | R/W | ‘b0 | SDIO_DATA3 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | |
| Rvd | 30 | - | - | - | |
| sdio_data_3_pud_en | 29 | R/W | ‘b1 | SDIO_DATA3 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | |
| sdio_data_3_pud_sel | 28 | R/W | ‘b1 | SDIO_DATA3 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | |
| sdio_data_2_smt | 27 | R/W | ‘b0 | SDIO_DATA2 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | |
| Rvd | 26 | - | - | - | |
| sdio_data_2_pud_en | 25 | R/W | ‘b1 | SDIO_DATA2 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | |
| sdio_data_2_pud_sel | 24 | R/W | ‘b1 | SDIO_DATA2 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | |
| sdio_data_1_smt | 23 | R/W | ‘b0 | SDIO_DATA1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | |
| Rvd | 22 | - | - | - | |

| | | | | |
|---|---|---|---|---|
| sdio_data_1_pud_en | 21 | R/W | ‘b1 | SDIO_DATA1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| sdio_data_1_pud_sel | 20 | R/W | ‘b1 | SDIO_DATA1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| sdio_data_0_smt | 19 | R/W | ‘b0 | SDIO_DATA0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 18 | - | - | - |
| sdio_data_0_pud_en | 17 | R/W | ‘b1 | SDIO_DATA0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| sdio_data_0_pud_sel | 16 | R/W | ‘b1 | SDIO_DATA0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| Rvd | 15..8 | - | - | - |
| sdio_clk_smt | 7 | R/W | ‘b0 | SDIO_CLK pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 6 | - | - | - |
| sdio_clk_pud_en | 5 | R/W | ‘b1 | SDIO_CLK pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| sdio_clk_pud_sel | 4 | R/W | ‘b0 | SDIO_CLK pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| sdio_cmd_smt | 3 | R/W | ‘b0 | SDIO_CMD pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 2 | - | - | - |
| sdio_cmd_pud_en | 1 | R/W | ‘b1 | SDIO_CMD pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| sdio_cmd_pud_sel | 0 | R/W | ‘b1 | SDIO_CMD pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |

| Module::emmc | Register::pfunc_nf2 | | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_2618 |
|---|---|---|---|---|---|---|
| Name | Bits | R/W | Default | Comments | | |
| Rvd | 31..28 | - | - | - | | |
| prob_3_smt | 27 | R/W | ‘b0 | PROB_3 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| prob_3_e2 | 26 | R/W | ‘b0 | PROB_3 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA | | |
| prob_3_pud_en | 25 | R/W | ‘b1 | PROB_3 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| prob_3_pud_sel | 24 | R/W | ‘b1 | PROB_3 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up | | |
| prob_2_smt | 23 | R/W | ‘b0 | PROB_2 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |
| prob_2_e2 | 22 | R/W | ‘b0 | PROB_2 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA | | |
| prob_2_pud_en | 21 | R/W | ‘b1 | PROB_2 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable | | |

| | | | | |
|---|---|---|---|---|
| prob_2_pud_sel | 20 | R/W | ‘b1 | PROB_2 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| prob_1_smt | 19 | R/W | ‘b0 | PROB_1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| prob_1_e2 | 18 | R/W | ‘b0 | PROB_1 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA |
| prob_1_pud_en | 17 | R/W | ‘b0 | PROB_1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| prob_1_pud_sel | 16 | R/W | ‘b0 | PROB_1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| prob_0_smt | 15 | R/W | ‘b0 | PROB_0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| prob_0_e2 | 14 | R/W | ‘b0 | PROB_0 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA |
| prob_0_pud_en | 13 | R/W | ‘b0 | PROB_0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| prob_0_pud_sel | 12 | R/W | ‘b0 | PROB_0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| pcie_clkreq_1_smt | 11 | R/W | ‘b0 | PCIE_CLKREQ_1 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| pcie_clkreq_1_e2 | 10 | R/W | ‘b0 | PCIE_CLKREQ_1 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA |
| pcie_clkreq_1_pud_en | 9 | R/W | ‘b1 | PCIE_CLKREQ_1 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| pcie_clkreq_1_pud_sel | 8 | R/W | ‘b1 | PCIE_CLKREQ_1 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| pcie_clkreq_0_smt | 7 | R/W | ‘b0 | PCIE_CLKREQ_0 pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| pcie_clkreq_0_e2 | 6 | R/W | ‘b0 | PCIE_CLKREQ_0 pad driven current selection.<br>1‘b0 : 4mA , 1‘b1 : 8mA |
| pcie_clkreq_0_pud_en | 5 | R/W | ‘b1 | PCIE_CLKREQ_0 pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| pcie_clkreq_0_pud_sel | 4 | R/W | ‘b1 | PCIE_CLKREQ_0 pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |
| emmc_dd_sb_smt | 3 | R/W | ‘b0 | EMMC_DD_SB pad Schmitt-trigger enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| Rvd | 2 | - | - | - |
| emmc_dd_sb_pud_en | 1 | R/W | ‘b1 | EMMC_DD_SB pad pull-up /pull-down function enable.<br>1‘b0 : Disable , 1‘b1 : Enable |
| emmc_dd_sb_pud_sel | 0 | R/W | ‘b0 | EMMC_DD_SB pad pull-up /pull-down function selection.<br>1‘b0 : Pull-down , 1‘b1 : Pull-up |

| Module::emmc | Register::muxpad2 | Set::1 | ATTR::ctrl | Type::SR | ADDR::0x9801_261C |
|---|---|---|---|---|---|

| Name | Bits | R/W | Default | Comments |
|---|---|---|---|---|
| Rvd | 31..14 | - | - | - |
| prob_3 | 13..12 | R/W | ‘b00 | 00 : Mux to gpio[100]/main2_gpio[36]<br>01: Mux to pll_test_out_loc1[1]<br>Others: Input tri-state |
| prob_2 | 11..10 | R/W | ‘b00 | 00 : Mux to gpio[99]/main2_gpio[35]<br>01: Mux to pll_test_out_loc1[0]<br>Others: Input tri-state |
| prob_1 | 9..8 | R/W | ‘b10 | 00 : Mux to gpio[98]/main2_gpio[34]<br>01: Mux to pll_test_out_loc0[1]<br>10: Mux to P2S_O<br>Others: Input tri-state |
| prob_0 | 7..6 | R/W | ‘b10 | 00 : Mux to gpio[97]/main2_gpio[33]<br>01: Mux to pll_test_out_loc0[0]<br>10: Mux to P2S_TRIG_O<br>Others: Input tri-state |
| pcie_clkreq_1 | 5..4 | R/W | ‘b00 | 00 : Mux to gpio[96]/main2_gpio[32]<br>01: Mux to PCIE_CLKREQ_1<br>Others: Input tri-state |
| pcie_clkreq_0 | 3..2 | R/W | ‘b00 | 00 : Mux to gpio[95]/main2_gpio[31]<br>01: Mux to PCIE_CLKREQ_0<br>Others: Input tri-state |
| sdio_loc | 1..0 | R/W | ‘b01 | 2'b01 : SDIO data from SDIO pad<br>2'b10 : SDIO data form MMC pad<br>Others: Disable |

LSADC register

LSADC0

| *Physical Address* | *Name* | *R/W* | *Description* |
|---|---|---|---|
| 0x9801_2800 | **LSADC0_pad0** | R/W | PAD 0 control |
| 0x9801_2804 | **LSADC0_pad1** | R/W | PAD 1 control register |
| 0x9801_2808 ~ 0x9801_281C | Reserved | | |
| 0x9801_2820 | **LSADC0_ctrl** | R/W | LSADC control register |
| 0x9801_2824 | **LSADC0_status** | R/W | LSADC status register |
| 0x9801_2828 | **LSADC0_analog_ctrl** | R/W | LSADC ANALOG control register |
| 0x9801_282C | LSADC0_peri_top_debug | R/W | Debug port selection |
| 0x9801_2830 | **LSADC0_pad0_level_set0** | R/W | LSADC PAD 0 compare set0 |
| 0x9801_2834 | **LSADC0_pad0_level_set1** | R/W | LSADC PAD 0 compare set1 |
| 0x9801_2838 | **LSADC0_pad0_level_set2** | R/W | LSADC PAD 0 compare set2 |
| 0x9801_283C | **LSADC0_pad0_level_set3** | R/W | LSADC PAD 0 compare set3 |
| 0x9801_2840 | **LSADC0_pad0_level_set4** | R/W | LSADC PAD 0 compare set4 |
| 0x9801_2844 | **LSADC0_pad0_level_set5** | R/W | LSADC PAD 0 compare set5 |
| 0x9801_2848 | **LSADC0_pad1_level_set0** | R/W | LSADC PAD 1 compare set0 |
| 0x9801_284C | **LSADC0_pad1_level_set1** | R/W | LSADC PAD 1 compare set1 |
| 0x9801_2850 | **LSADC0_pad1_level_set2** | R/W | LSADC PAD 1 compare set2 |
| 0x9801_2854 | **LSADC0_pad1_level_set3** | R/W | LSADC PAD 1 compare set3 |
| 0x9801_2858 | **LSADC0_pad1_level_set4** | R/W | LSADC PAD 1 compare set4 |
| 0x9801_285C | **LSADC0_pad1_level_set5** | R/W | LSADC PAD 1 compare set5 |
| 0x9801_2860 ~ 0x9801_2874 | **Reserved** | | |
| 0x9801_2878 | **LSADC0_INT_PAD0** | R/W | LSADC PAD0 compare status |
| 0x9801_287C | **LSADC0_INT_PAD1** | R/W | LSADC PAD1 compare status |
| 0x9801_2880 | **LSADC0_POWER** | R/W | LSADC power setting |

LSADC1

| *Physical Address* | *Name* | *R/W* | *Description* |
|---|---|---|---|
| 0x9801_2900 | **LSADC1_pad0** | R/W | PAD 0 control |
| 0x9801_2904 | **LSADC1_pad1** | R/W | PAD 1 control register |
| 0x9801_2908 ~ 0x9801_291C | Reserved | | |
| 0x9801_2920 | **LSADC1_ctrl** | R/W | LSADC control register |
| 0x9801_2924 | **LSADC1_status** | R/W | LSADC status register |
| 0x9801_2928 | **LSADC1_analog_ctrl** | R/W | LSADC ANALOG control register |
| 0x9801_292C | LSADC1_peri_top_debug | R/W | Debug port selection |

| | | | |
|---|---|---|---|
| 0x9801_2930 | **LSADC1_pad0_level_set0** | R/W | LSADC PAD 0 compare set0 |
| 0x9801_2934 | **LSADC1_pad0_level_set1** | R/W | LSADC PAD 0 compare set1 |
| 0x9801_2938 | **LSADC1_pad0_level_set2** | R/W | LSADC PAD 0 compare set2 |
| 0x9801_293C | **LSADC1_pad0_level_set3** | R/W | LSADC PAD 0 compare set3 |
| 0x9801_2940 | **LSADC1_pad0_level_set4** | R/W | LSADC PAD 0 compare set4 |
| 0x9801_2944 | **LSADC1_pad0_level_set5** | R/W | LSADC PAD 0 compare set5 |
| 0x9801_2948 | **LSADC1_pad1_level_set0** | R/W | LSADC PAD 1 compare set0 |
| 0x9801_294C | **LSADC1_pad1_level_set1** | R/W | LSADC PAD 1 compare set1 |
| 0x9801_2950 | **LSADC1_pad1_level_set2** | R/W | LSADC PAD 1 compare set2 |
| 0x9801_2954 | **LSADC1_pad1_level_set3** | R/W | LSADC PAD 1 compare set3 |
| 0x9801_2958 | **LSADC1_pad1_level_set4** | R/W | LSADC PAD 1 compare set4 |
| 0x9801_295C | **LSADC1_pad1_level_set5** | R/W | LSADC PAD 1 compare set5 |
| 0x9801_2960 ~ 0x9801_2974 | **Reserved** | | |
| 0x9801_2978 | **LSADC1_INT_PAD0** | R/W | LSADC PAD0 compare status |
| 0x9801_297C | **LSADC1_INT_PAD1** | R/W | LSADC PAD1 compare status |
| 0x9801_2980 | **LSADC1_POWER** | R/W | LSADC power setting |

Register Description

LSADC0

| Module::emmc | Register:: **LSADC0_pad0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2800 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| pad0_active | 31 | R/W | 'b0 | **PAD Active Control Bit**<br>1: active<br>0: de-active |
| Rvd | 30:24 | - | - | - |
| pad0_thred | 23:16 | R/W | 'h0 | **LS ADC Threshold Value**<br>As the difference between current LSADC value and previous LSADC value is larger than **Thred**, the corresponding **Pad_status** will be asserted.<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |
| pad0_sw | 15:12 | R/W | 'h0 | **Pad Switch**<br>0x2 ~ 0xf : reserved<br>0x1 : External input pin 1<br>0x0 : External input pin 0 |
| Rvd | 11:9 | - | - | - |
| pad0_ctrl | 8 | R/W | 'b0 | **Mode Control Bit**<br>0: Voltage Mode<br>1: Current Mode<br>ctrl_0 = ctrl_4 = **pad_ctrl** (refer to block diagram) |
| Rvd | 7:6 | - | - | - |
| adc_val0 | 5:0 | R/W | - | **Current LS ADC value of this configured pad**<br>In order to enhance the robustness, the difference |

| | | | | |
|---|---|---|---|---|
| | | | | checking will be performed for (**debounce_cnt** +1) times. |

| Module::emmc | Register:: **LSADC0_pad1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2804 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| pad1_active | 31 | R/W | 'b0 | **PAD Active Control Bit**<br>1: active<br>0: de-active |
| Rvd | 30:24 | - | - | - |
| Pad1_thred | 23:16 | R/W | 'h0 | **LS ADC Threshold Value**<br>As the difference between current LSADC value and previous LSADC value is larger than **Thred**, the corresponding **Pad_status** will be asserted.<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |
| Pad1_sw | 15:12 | R/W | 'h0 | **Pad Switch**<br>0x2 ~ 0xf : reserved<br>0x1 : External input pin 1<br>0x0 : External input pin 0 |
| Rvd | 11:9 | - | - | - |
| Pad1_ctrl | 8 | R/W | 'b0 | **Mode Control Bit**<br>0: Voltage Mode<br>1: Current Mode<br>ctrl_0 = ctrl_4 = **pad_ctrl** (refer to block diagram) |
| Rvd | 7:6 | - | - | - |
| adc_val0 | 5:0 | R/W | - | **Current LS ADC value of this configured pad**<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |

| Module::emmc | Register:: **LSADC0_ctrl** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2820 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Sel_wait | 31:28 | R/W | 'h1 | **OPAMP settling time**<br>After changing the multiplexer setting for LSADC, hardware will wait **sel_wait** and start A-to-D conversion<br>Legal value: 0x0~0xB and others are forbidden<br>Wait time = 10* 2^(6+sel_wait+1)/xtal_clk (us) |
| Sel_adc_ck | 27:24 | R/W | 'h6 | **ADC clock rate**<br>Legal value: 0x0~0xB and others are forbidden<br>adc_ck = (xtal_clk)/2^(2+sel_adc_ck+1) MHz<br>Note : The ADC clock rate shall be less than 1MHz for proper operation. |
| Debounce_cnt | 23:20 | R/W | 'h0 | **Debounce_Count**<br>debounce length = **Deboutce_cnt** +1 |
| Rvd | 19:16 | - | - | - |
| Dout_Test_IN | 15:8 | R/W | 'h0 | **Dout Test Input** |
| Rvd | 7:2 | - | - | - |
| Test_en | 1 | R/W | 'b0 | **Test mode enable bit**<br>Test enable: write 1 to enable test mode. In test mode software can write value into **Dout_Test_IN** to let LSADC work.<br>1 : Enable<br>0 : Disable |

| | | | | |
|---|---|---|---|---|
| Enable | 0 | R/W | 'b0 | **Module enable bit**<br>1 : Enable<br>0 : Disable |

| Module::emmc | Register:: **LSADC0_status** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2824 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| IRQ_En | 31:24 | R/W | 'h0 | **Interrupt Enable of each pad**<br>bit[31:26] = reserved<br>:<br>bit[25] = pad1<br>bit[24] = pad0<br>1: Enable<br>0: Disable |
| PAD_CNT | 23:20 | R | - | **PAD counter value**<br>**PAD_CNT** indicates which PAD status is checked by hardware now. |
| ADC_busy | 19 | R | - | **Status of low-speed ADC**<br>1: busy<br>0: ready |
| Rvd | 18:17 | - | - | - |
| pad_ctrl | 16:12 | R | - | **Current PAD_CTRL value**<br>This is used for debug only.<br>**CurPAD_CTRL** indicates the **PAD_CTRL** value of current checked PAD.<br>[16:12]=[Ctrl_4, Ctrl_3=0, Ctrl_2=0, Ctrl_1=0, Ctrl_0] |
| Rvd | 11:2 | - | - | - |
| Pad1_status | 1 | R | - | **Pad1_status**<br>1 : PAD status is changed<br>0 : PAD status is the same as before<br>Write 1 to clear |
| Pad0_status | 0 | R | - | **Pad0_status**<br>1 : PAD status is changed<br>0 : PAD status is the same as before<br>Write 1 to clear |

| Module::emmc | Register:: **LSADC0_analog_ctrl** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2828 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Rvd | 31:24 | - | - | - |
| DUMMY2 | 23:20 | R/W | 'h0 | Dummy |
| Rvd | 19:18 | - | - | - |
| JD_sbias | 17:16 | R/W | 'h0 | **Jack Detection bias current control, for debug use.**<br>00:5u<br>01:10u<br>10:15u<br>11:20u |
| Rvd | 15:14 | - | - | - |
| JD_adsbias | 13:12 | R/W | 'h0 | **ADC bias current select**<br>00:5u<br>01:10u<br>10:15u<br>11:20u |
| JD_DUMMY | 11:10 | R/W | 'h0 | JD Dummy |

| | | | | |
|---|---|---|---|---|
| Rvd | 9 | - | - | - |
| JD_svr | 8 | R/W | 'b0 | **Jack Detection OPAMP 1.65V reference voltage select**<br>0: 0.5*VDD from BB<br>1: 0.5*VDD from JD |
| Rvd | 7:5 | - | - | - |
| JD_adcksel | 4 | R/W | 'b0 | **ADC clock pos/neg edge select for data latch**<br>0: positive edge<br>1: negative edge |
| Rvd | 3:1 | - | - | - |
| JD_power | 0 | R/W | 'b0 | **Power down control of Jack Detection**<br>0: power down<br>1: power on |

| Module::emmc | Register::<br>**LSADC0_peri_top_debug** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_282C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31:19 | - | - | - |
| Lsadc_2_ifd_data_sel | 18:16 | R/W | 'h0 | Lsadc_2_ifd_data source selection<br>3'h0: pad0;<br>3'h1: pad1;<br>3'h2 ~ 3'h7: reserved |
| Rvd | 15 | - | - | - |
| Power_saving_enable | 14 | W | 'h0 | - |
| Power_saving_cycle_time | 13:11 | W | 'h0 | - |
| Power_saving_disable_time | 10:8 | W | 'h0 | - |
| peri_top_debug | 7:0 | R/W | 'h0 | **Peripheral Top Debug Register** |

| Module::emmc | Register::<br>**LSADC0_pad0_level_set0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2830 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_0_top_bound | 31:24 | R/W | 'h0 | **Level_0 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_0 low bound value** |
| Block0_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en0 | 1 | R/W | 'h0 | **INT0 enable** |
| INT_pending_bit0 | 0 | R | 'h0 | **INT0 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC0_pad0_level_set1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2834 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_1_t | 31:24 | R/W | 'h0 | **Level_1 top bound value** |

| | | | | |
|---|---|---|---|---|
| op_bound | | | | |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_1 low bound value** |
| Block1_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en1 | 1 | R/W | 'h0 | **INT1 enable** |
| INT_pending_bit1 | 0 | R | 'h0 | **INT1 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC0_pad0_level_set2** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2838 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_2_top_bound | 31:24 | R/W | 'h0 | **Level_2 top bound value** |
| Level_2_low_bound | 23:16 | R/W | 'h0 | **Level_2 low bound value** |
| Block2_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en2 | 1 | R/W | 'h0 | **INT2 enable** |
| INT_pending_bit2 | 0 | R | 'h0 | **INT2 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC0_pad0_level_set3** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_283C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_3_top_bound | 31:24 | R/W | 'h0 | **Level_3 top bound value** |
| Level_3_low_bound | 23:16 | R/W | 'h0 | **Level_3 low bound value** |
| Block3_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en3 | 1 | R/W | 'h0 | **INT3 enable** |
| INT_pending_bit3 | 0 | R | 'h0 | **INT3 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC0_pad0_level_set4** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2840 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_4_top_bound | 31:24 | R/W | 'h0 | **Level_4 top bound value** |
| Level_4_low_bound | 23:16 | R/W | 'h0 | **Level_4 low bound value** |
| Block4_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en4 | 1 | R/W | 'h0 | **INT4 enable** |
| INT_pending_bit4 | 0 | R | 'h0 | **INT4 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad0_level_set5** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2844 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_5_top_bound | 31:24 | R/W | 'h0 | **Level_5 top bound value** |
| Level_5_low_bound | 23:16 | R/W | 'h0 | **Level_5 low bound value** |
| Block5_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en5 | 1 | R/W | 'h0 | **INT5 enable** |
| INT_pending_bit5 | 0 | R | 'h0 | **INT5 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2848 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_0_top_bound | 31:24 | R/W | 'h0 | **Level_0 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_0 low bound value** |
| Block0_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en0 | 1 | R/W | 'h0 | **INT0 enable** |
| INT_pending_bit0 | 0 | R | 'h0 | **INT0 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_284C |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_1_top_bound | 31:24 | R/W | 'h0 | **Level_1 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_1 low bound value** |
| Block1_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en1 | 1 | R/W | 'h0 | **INT1 enable** |
| INT_pending_bit1 | 0 | R | 'h0 | **INT1 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set2** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2850 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_2_top_bound | 31:24 | R/W | 'h0 | **Level_2 top bound value** |
| Level_2_low_bound | 23:16 | R/W | 'h0 | **Level_2 low bound value** |
| Block2_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en2 | 1 | R/W | 'h0 | **INT2 enable** |
| INT_pending_bit2 | 0 | R | 'h0 | **INT2 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set3** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2854 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_3_top_bound | 31:24 | R/W | 'h0 | **Level_3 top bound value** |
| Level_3_low_bound | 23:16 | R/W | 'h0 | **Level_3 low bound value** |
| Block3_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en3 | 1 | R/W | 'h0 | **INT3 enable** |

| | | | | |
|---|---|---|---|---|
| INT_pending_bit3 | 0 | R | 'h0 | **INT3 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set4** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2858 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_4_top_bound | 31:24 | R/W | 'h0 | **Level_4 top bound value** |
| Level_4_low_bound | 23:16 | R/W | 'h0 | **Level_4 low bound value** |
| Block4_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en4 | 1 | R/W | 'h0 | **INT4 enable** |
| INT_pending_bit4 | 0 | R | 'h0 | **INT4 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC0_pad1_level_set5** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_285C |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Level_5_top_bound | 31:24 | R/W | 'h0 | **Level_5 top bound value** |
| Level_5_low_bound | 23:16 | R/W | 'h0 | **Level_5 low bound value** |
| Block5_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en5 | 1 | R/W | 'h0 | **INT5 enable** |
| INT_pending_bit5 | 0 | R | 'h0 | **INT5 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: LSADC0_INT_pad0 | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2878 |
|---|---|---|---|---|---|

| Name | Bits | Read/Write | Reset State | Comments |
|---|---|---|---|---|
| Rvd | 31:16 | - | - | - |
| Rvd | 15:14 | - | - | - |
| ADC_value0 latch | 13:8 | R | 'h0 | **ADC value latch at first pad0 interrupt happen**<br>**R_bus and HW can write this register** |
| Rvd | 7:1 | - | - | - |
| INT_latch status | 0 | R | 'h0 | **Latch INT pending bit at first pad0 interrupt happen**<br>**R_bus and HW can write this register** |

| Module::emmc | Register:: LSADC0_INT_pad1 | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_287C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31:16 | - | - | - |
| Rvd | 15:14 | - | - | - |
| ADC_value1 latch | 13:8 | R | 'h0 | **ADC value latch at first pad1 interrupt happen R_bus and HW can write this register** |
| Rvd | 7:1 | - | - | - |
| INT_latch status | 0 | R | 'h0 | **Latch INT pending bit at first pad1 interrupt happen R_bus and HW can write this register** |

| Module::emmc | Register:: LSADC_POWER | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2880 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31..2 | - | - | - |
| lsadc1_clk_gating_en | 1 | R/W | 'b1 | Enable LSADC1 clock gating function. |
| lsadc0_clk_gating_en | 0 | R/W | 'b1 | Enable LSADC0 clock gating function. |

| Module::emmc | Register:: LSADC_DBG | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2884 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31..2 | - | - | - |
| sel | 1 | R/W | 'b0 | debug selection<br>1'b0: LSADC0 (JD_TOP)<br>1'b1: LSADC1 (LSADC_TOP) |
| enable | 0 | R/W | 'b0 | Enable the LSADC debug port output, when enable = 0, the output would be 16'd0 |

| Module::emmc | Register:: LSADC_ANA_TEST | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2888 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31..1 | - | - | - |
| sel | 0 | R/W | 'b0 | Analog test selection (DOUT, ADCKOUT)<br>1'b0: JD_TOP<br>1'b1: LSADC_TOP |

LSADC1

| Module::emmc | Register:: **LSADC1_pad0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2900 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| pad0_active | 31 | R/W | ‘b0 | **PAD Active Control Bit**<br>1: active<br>0: de-active |
| Rvd | 30:25 | - | - | - |
| pad0_vref_sel | 24 | R/W | ‘h0 | LSADC detect range control<br>A00：1LSB=8mV<br>0: 0V ~ 1.024V<br>1: 0.5V ~ 1.524V<br><br>A01/B00：1LSB=6.1mV<br>0: 0V ~ 0.7812V<br>1: 0.6559V ~ 1.4371V |
| pad0_thred | 23:16 | R/W | ‘h0 | **LS ADC Threshold Value**<br>As the difference between current LSADC value and previous LSADC value is larger than **Thred**, the corresponding **Pad_status** will be asserted.<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |
| DUMMY | 15..13 | R/W | ‘h0 | **Dummy** |
| pad0_sw | 12 | R/W | ‘h0 | **LSADC 2 to 1 input MUX select:**<br>**0: VDD**<br>**1: GND** |
| Rvd | 11:9 | - | - | - |
| pad0_ctrl | 8 | R/W | ‘b0 | **Mode Control Bit**<br>0: Voltage Mode<br>1: Current Mode<br>ctrl_0 = ctrl_4 = **pad_ctrl** (refer to block diagram) |
| Rvd | 7 | - | - | - |
| adc_val0 | 6:0 | R/W | - | **Current LS ADC value of this configured pad**<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |

| Module::emmc | Register:: **LSADC1_pad1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2904 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| pad1_active | 31 | R/W | ‘b0 | **PAD Active Control Bit**<br>1: active<br>0: de-active |
| Rvd | 30:25 | - | - | - |
| Pad1_vref_sel | 24 | R/W | ‘h0 | LSADC detect range control<br>A00：1LSB=8mV<br>0: 0V ~ 1.024V<br>1: 0.5V ~ 1.524V<br><br>A01/B00：1LSB=6.1mV<br>0: 0V ~ 0.7812V<br>1: 0.6559V ~ 1.4371V |
| Pad1_thred | 23:16 | R/W | ‘h0 | **LS ADC Threshold Value**<br>As the difference between current LSADC value and previous LSADC value is larger than **Thred**, the corresponding **Pad_status** will be asserted.<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |
| DUMMY1 | 15..13 | R/W | ‘h0 | **Dummy** |
| Pad1_sw | 12 | R/W | ‘h0 | **LSADC 2 to 1 input MUX select:**<br>**0: VDD** |

| | | | | |
|---|---|---|---|---|
| | | | | **1: GND** |
| Rvd | 11:9 | - | - | - |
| Pad1_ctrl | 8 | R/W | ‘b0 | **Mode Control Bit**<br>0: Voltage Mode<br>1: Current Mode<br>ctrl_0 = ctrl_4 = **pad_ctrl** (refer to block diagram) |
| Rvd | 7 | - | - | - |
| adc_val0 | 6:0 | R/W | - | **Current LS ADC value of this configured pad**<br>In order to enhance the robustness, the difference checking will be performed for (**debounce_cnt** +1) times. |

| Module::emmc | Register:: **LSADC1_ctrl** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2920 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Sel_wait | 31:28 | R/W | ‘h0 | **OPAMP settling time**<br>After changing the multiplexer setting for LSADC, hardware will wait **sel_wait** and start A-to-D conversion<br>Legal value: 0x0~0xB and others are forbidden<br>Wait time = 10* 2^(2+sel_wait)/xtal_clk (us) |
| Sel_adc_ck | 27:24 | R/W | ‘h0 | **ADC clock rate**<br>Legal value: 0x0~0xB and others are forbidden<br>adc_ck = (xtal_clk)/2^(2+sel_adc_ck) MHz |
| Debounce_cnt | 23:16 | R/W | ‘ha | **Debounce_Count**<br>debounce length = **Deboutce_cnt** +1<br>the debounce length shall be above than 10 for proper operation. |
| Dout_Test_IN | 15:8 | R/W | ‘h0 | **Dout Test Input** |
| Rvd | 7:6 | - | - | - |
| vdd_gnd_sel | 5 | R/W | ‘b0 | **VDD/GND select mode bit**<br>1 : VDD1/VDD2<br>0 : GND1/GND2 |
| vdd_gnd_en | 4 | R/W | ‘b0 | **VDD/GND select mode enable bit**<br>VDD/GND select mode enable: write 1 to enable.<br>In select mode, LSADC detect VDD1 and VDD2 voltage (or GND1 and GND2).<br>1 : Enable<br>0 : Disable |
| Rvd | 3:2 | - | - | - |
| Test_en | 1 | R/W | ‘b0 | **Test mode enable bit**<br>Test enable: write 1 to enable test mode. In test mode software can write value into **Dout_Test_IN** to let LSADC work.<br>1 : Enable<br>0 : Disable |
| Enable | 0 | R/W | ‘b0 | **Module enable bit**<br>1 : Enable<br>0 : Disable |

| Module::emmc | Register:: **LSADC1_status** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2924 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| IRQ_En | 31:24 | R/W | ‘h0 | **Interrupt Enable of each pad**<br>bit[31:26] = reserved<br>: |

| | | | | |
|---|---|---|---|---|
| | | | | bit[25] = pad1<br>bit[24] = pad0<br>1: Enable<br>0: Disable |
| PAD_CNT | 23:20 | R | - | **PAD counter value**<br>**PAD_CNT** indicates which PAD status is checked by hardware now. |
| ADC_busy | 19 | R | - | **Status of low-speed ADC**<br>1: busy<br>0: ready |
| Rvd | 18:17 | - | - | - |
| pad_ctrl | 16:12 | R | - | **Current PAD_CTRL value**<br>This is used for debug only.<br>**CurPAD_CTRL** indicates the **PAD_CTRL** value of current checked PAD.<br>[16:12]=[Ctrl_4, Ctrl_3=0, Ctrl_2=0, Ctrl_1=0, Ctrl_0] |
| Rvd | 11:2 | - | - | - |
| Pad1_status | 1 | R | - | **Pad1_status**<br>1 : PAD status is changed<br>0 : PAD status is the same as before<br>Write 1 to clear |
| Pad0_status | 0 | R | - | **Pad0_status**<br>1 : PAD status is changed<br>0 : PAD status is the same as before<br>Write 1 to clear |

| Module::emmc | Register::<br>**LSADC1_analog_ctrl** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2928 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| test_in_en | 31 | R/W | 'h0 | LSADC test input enable<br>0: disable<br>1: enable |
| Rvd | 30:24 | - | - | - |
| DUMMY2 | 23:20 | R/W | 'h0 | Dummy |
| Rvd | 19:18 | - | - | - |
| JD_sbias | 17:16 | R/W | 'h1 | **Jack Detection bias current control, for debug use.**<br>00:37.5u<br>01:40u<br>10:42.5u<br>11:45u |
| Rvd | 15:14 | - | - | - |
| JD_adsbias | 13:12 | R/W | 'h1 | **ADC bias current select**<br>00:2.5u<br>01:5u<br>10:7.5u<br>11:10u |
| JD_DUMMY | 11:10 | R/W | 'h0 | JD Dummy |
| Rvd | 9 | - | - | - |
| JD_svr | 8 | R/W | 'b0 | **Jack Detection OPAMP 1.65V reference voltage select**<br>0: 0.5*VDD from BB<br>1: 0.5*VDD from JD |
| Rvd | 7:5 | - | - | - |
| JD_adcksel | 4 | R/W | 'b0 | **ADC clock pos/neg edge select for data latch**<br>0: positive edge<br>1: negative edge |
| Rvd | 3:1 | - | - | - |
| JD_power | 0 | R/W | 'b0 | **Power down control of Jack Detection**<br>0: power down |

| | | | | |
|---|---|---|---|---|
| | | | | 1: power on |

| Module::emmc | Register:: **LSADC1_peri_top_debug** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_292C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31:19 | - | - | - |
| Lsadc_2_ifd_data_sel | 18:16 | R/W | 'h0 | Lsadc_2_ifd_data source selection<br>3'h0: pad0;<br>3'h1: pad1;<br>3'h2 ~ 3'h7: reserved |
| Rvd | 15 | - | - | - |
| Power_saving_enable | 14 | W | 'h0 | - |
| Power_saving_cycle_time | 13:11 | W | 'h0 | - |
| Power_saving_disable_time | 10:8 | W | 'h0 | - |
| peri_top_debug | 7:0 | R/W | 'h0 | **Peripheral Top Debug Register** |

| Module::emmc | Register:: **LSADC1_pad0_level_set0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2930 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_0_top_bound | 31:24 | R/W | 'h0 | **Level_0 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_0 low bound value** |
| Block0_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en0 | 1 | R/W | 'h0 | **INT0 enable** |
| INT_pending_bit0 | 0 | R | 'h0 | **INT0 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad0_level_set1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2934 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_1_top_bound | 31:24 | R/W | 'h0 | **Level_1 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_1 low bound value** |
| Block1_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en1 | 1 | R/W | 'h0 | **INT1 enable** |

| | | | | |
|---|---|---|---|---|
| INT_pending_bit1 | 0 | R | 'h0 | **INT1 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad0_level_set2** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2938 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_2_top_bound | 31:24 | R/W | 'h0 | **Level_2 top bound value** |
| Level_2_low_bound | 23:16 | R/W | 'h0 | **Level_2 low bound value** |
| Block2_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en2 | 1 | R/W | 'h0 | **INT2 enable** |
| INT_pending_bit2 | 0 | R | 'h0 | **INT2 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad0_level_set3** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_293C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_3_top_bound | 31:24 | R/W | 'h0 | **Level_3 top bound value** |
| Level_3_low_bound | 23:16 | R/W | 'h0 | **Level_3 low bound value** |
| Block3_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en3 | 1 | R/W | 'h0 | **INT3 enable** |
| INT_pending_bit3 | 0 | R | 'h0 | **INT3 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad0_level_set4** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2940 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_4_top_bound | 31:24 | R/W | 'h0 | **Level_4 top bound value** |
| Level_4_low_bound | 23:16 | R/W | 'h0 | **Level_4 low bound value** |
| Block4_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |

| | | | | |
|---|---|---|---|---|
| Rvd | 14:2 | - | - | - |
| INT_en4 | 1 | R/W | 'h0 | **INT4 enable** |
| INT_pending_bit4 | 0 | R | 'h0 | **INT4 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad0_level_set5** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2944 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_5_top_bound | 31:24 | R/W | 'h0 | **Level_5 top bound value** |
| Level_5_low_bound | 23:16 | R/W | 'h0 | **Level_5 low bound value** |
| Block5_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en5 | 1 | R/W | 'h0 | **INT5 enable** |
| INT_pending_bit5 | 0 | R | 'h0 | **INT5 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad1_level_set0** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2948 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_0_top_bound | 31:24 | R/W | 'h0 | **Level_0 top bound value** |
| Level_0_low_bound | 23:16 | R/W | 'h0 | **Level_0 low bound value** |
| Block0_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en0 | 1 | R/W | 'h0 | **INT0 enable** |
| INT_pending_bit0 | 0 | R | 'h0 | **INT0 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register:: **LSADC1_pad1_level_set1** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_294C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_1_top_bound | 31:24 | R/W | 'h0 | **Level_1 top bound value** |
| Level_0_l | 23:16 | R/W | 'h0 | **Level_1 low bound value** |

| | | | | |
|---|---|---|---|---|
| ow_bound | | | | |
| Block1_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en1 | 1 | R/W | 'h0 | **INT1 enable** |
| INT_pending_bit1 | 0 | R | 'h0 | **INT1 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC1_pad1_level_set2** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2950 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_2_top_bound | 31:24 | R/W | 'h0 | **Level_2 top bound value** |
| Level_2_low_bound | 23:16 | R/W | 'h0 | **Level_2 low bound value** |
| Block2_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en2 | 1 | R/W | 'h0 | **INT2 enable** |
| INT_pending_bit2 | 0 | R | 'h0 | **INT2 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC1_pad1_level_set3** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2954 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_3_top_bound | 31:24 | R/W | 'h0 | **Level_3 top bound value** |
| Level_3_low_bound | 23:16 | R/W | 'h0 | **Level_3 low bound value** |
| Block3_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en3 | 1 | R/W | 'h0 | **INT3 enable** |
| INT_pending_bit3 | 0 | R | 'h0 | **INT3 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC1_pad1_level_set4** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2958 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| Level_4_top_bound | 31:24 | R/W | 'h0 | **Level_4 top bound value** |
| Level_4_low_bound | 23:16 | R/W | 'h0 | **Level_4 low bound value** |
| Block4_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en4 | 1 | R/W | 'h0 | **INT4 enable** |
| INT_pending_bit4 | 0 | R | 'h0 | **INT4 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>**LSADC1_pad1_level_set5** | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_295C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Level_5_top_bound | 31:24 | R/W | 'h0 | **Level_5 top bound value** |
| Level_5_low_bound | 23:16 | R/W | 'h0 | **Level_5 low bound value** |
| Block5_en | 15 | R/W | 'h0 | **Level compare block enable bit**<br>**0: diable**<br>**1; enable** |
| Rvd | 14:2 | - | - | - |
| INT_en5 | 1 | R/W | 'h0 | **INT5 enable** |
| INT_pending_bit5 | 0 | R | 'h0 | **INT5 pending bit, Write "1" to clear the interrupt** |

| Module::emmc | Register::<br>LSADC1_INT_pad0 | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_2978 |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31:16 | - | - | - |
| Rvd | 15:14 | - | - | - |
| ADC_value0 latch | 13:8 | R | 'h0 | **ADC value latch at first pad0 interrupt happen**<br>**R_bus and HW can write this register** |
| Rvd | 7:1 | - | - | - |
| INT_latch status | 0 | R | 'h0 | **Latch INT pending bit at first pad0 interrupt happen**<br>**R_bus and HW can write this register** |

| Module::emmc | Register::<br>LSADC1_INT_pad1 | Set::1 | **ATTR::**sfdf | Type::SR | ADDR::0x9801_297C |
|---|---|---|---|---|---|

| **Name** | **Bits** | **Read/Write** | **Reset State** | **Comments** |
|---|---|---|---|---|
| Rvd | 31:16 | - | - | - |
| Rvd | 15:14 | - | - | - |

| | | | | |
|---|---|---|---|---|
| ADC_value1 latch | 13:8 | R | 'h0 | **ADC value latch at first pad1 interrupt happen**<br>**R_bus and HW can write this register** |
| Rvd | 7:1 | - | - | - |
| INT_latch status | 0 | R | 'h0 | **Latch INT pending bit at first pad1 interrupt happen**<br>**R_bus and HW can write this register** |