/Standard for RealTek DVD Recordable

Date: 2009-04-23

Kylin USB

RealTek specification on DVD Recordable Technology

Specification for Kylin: USB Specification

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1 Register description

Mode	Adress Index (SYS)	Adress Index (MAC)	Register type
EHCI	0x9801_3000~0x9801_30FF		EHCI register
OHCI	0x9801_3400~0x9801_34FF		OHCI register
USB2 Wrapper	0x9801_3800~0x9801_3FFF	NA	wrapper register
OTG	0x981E_0000~0x981E_FFFF	0x0000h~0xFFFFh	CSR register

1.1 REGISTER:: Wrapp_reg 0x9801_3800

Module::**usb**	Register:: **Wrapp_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3800**

Name	Bits	R/W	Default	Comments
Status_err	31..30	R	'b00	Error status [31]: bus_err (When rbus AHB slave asserts ERROR, RETRY or SPLIT, this bit will be asserted) [30]: wrap_err (When rbus access wrong address in wrapper, this bit will be asserted)
Rvd	29..7	-	-	-
suspend_r	6	R/W	'b0	1: wake up 0: depend on IP's utmi_suspend_n_o signal when set '1', PHY will turn on all clocks (UTMI_CLK, 12M and 48M) to host, then suspend_r will be auto turned to '0' when utmi_suspend_n_o asserted.
Debug_mux	5..1	R/W	5'b00000	The debug ports mux for fpga 000: ahb_ohci_rd_debug 001: ahb_ohci_wr_debug 010: ahb_ehci_rd_debug 011: ahb_ehci_wr_debug 100: sb1_rd_debug 101: sb1_wr_debug 110: utmi_debug
packing	0	R/W	'b1	Packing OHCI packet

1.2 REGISTER:: VSTATUS_reg (un-used) 0x9801_3804

Module::**usb**	Register:: **VSTATUS_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3804**

Name	Bits	R/W	Default	Comments
Rvd	**31..8**	-	-	-
Vstatus_out	7..0	R/W	'h00	Vstatus output (It's used to configure PHY's control register)

The process of configuring PHY control register:

1. write VSTATUS_reg (0x9801_3804), (data output to PHY)
2. write INSNREG05 (0x9801_30a4)
   [17]: vBusy
   [16:13] : port number = 0001
   [12]: vload (low active)
   [11:8]: vcontrol
   [7:0]: vstatus_in (data input from PHY)
3. polling [17]: vBusy, if [17]=0, then vstatus_in is valid

Example for RealTek PHY:
Vcontrol[3]: low/high address, 0: low, 1: high
Vcontrol[2:0]: address
The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.3 REGISTER:: USBIPINPUT_reg 0x9801_3808

Module::**usb**	Register:: **USBIPINPUT_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3808**

Name	Bits	R/W	Default	Comments
pwr_mux	**31**	**R/W**	'b0	**0: high active of power control output signal** **1: low active of power control output signal**
ovrcur_mux	30	R/W	'b1	1: select low active of over current input signal 0: select high active of over current input signal
ss_resume_utmi_pls_dis_I	29	R/W	'b0	
ss_utmi_backward_enb_i	28	R/W	'b0	0: select original from IP
utmi_suspend_mux	27	R/W	'b0	Due to phy_clk should be suspended in RUN=0 1: select gatting with RUN=0 0: select original from IP
~~app_prt_ovrcur~~	~~26~~	~~R/W~~	~~'b0~~	~~Only for FPGA, when ASIC it's from PCB~~
host_disc_mux	26	R/W	'b1	0: utmi_discon_det_i => tie 0 1: utmi_discon_det_i => from PHY (HostDisconnect)
sys_interrupt_i	25	R/W	'b0	
ohci_0_app_irq12_i	24	R/W	'b0	
ohci_0_app_irq1_	23	R/W	'b0	

i				
ohci_0_app_io_hit_i	22	R/W	'b0	
ss_nxt_power_state_valid_I	21	R/W	'b0	
ss_next_power_state_i	20..19	R/W	'b00	
ss_power_state_i	18..17	R/W	'b00	
ohci_0_cntsel_i_n	16	R/W	'b0	
ohci_0_clkcktrst_i_n	15	R/W	'b1	
~~ohci_0_scanmode_i_n~~	14	R	'b0	
ss_fladj_val_5_i	13	R/W	'b1	
ss_fladj_val_4_i	12	R/W	'b0	
ss_fladj_val_3_i	11	R/W	'b0	
ss_fladj_val_2_i	10	R/W	'b0	
ss_fladj_val_1_i	9	R/W	'b0	
ss_fladj_val_0_i	8	R/W	'b0	
ss_fladj_val_host_i	7..2	R/W	'h20	
ss_simulation_mode_i	1	R/W	'b0	
ss_word_if_i	0	R/W	'b1	1: utmi 16 bits interface (utmi_clk=30MHz) 0: umti 8 bits interface (utmi_clk=60MHz)

1.4 REGISTER:: RESET_UTMI_reg 0x9801_380c

Module::**usb**	Register:: **RESET_UTMI_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_380c**

Name	Bits	R/W	Default	Comments
Rvd	**31..3**	-	-	-
Test_rst	2	R/W	'b0	Self_loop_back reset
Test_en	1	R/W	'b0	Self_loop_back enable
Reset_UTMI	0	R/W	'b0	UTMI reset (to PHY) (It's a sync. reset in PHY) When set high, it'll return to low automatically.

1.5 REGISTER:: SELF_LOOP_BACK_reg 0x9801_3810

Module::**usb**	Register:: **SELF_LOOP_BACK_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3810**

Name	Bits	R/W	Default	Comments
Rvd	**31..18**	-	-	-
Simulation_mode	17	R/W	'b0	Reduce counter for entering High-Speed mode
Force_hs_mode	16	R/W	'b0	Force HOST IP enter High-Speed mode 1: enable, 0: disable
Reserved	15-14	-	-	-
Test_done	13	R	'b0	Self_loop_back done
Test_fail	12	R	'b0	Self_loop_back result fail
Test_speed	11-10	R/W	'b00	When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2'b01: force PHY in HS 2'b10: force PHY in FS/LS 2'b00/2'b11: normal mode
Test_seed	9-2	R/W	'h00	Self_loop_back Random generator seed
Test_psl	1-0	R/W	'b00	Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter

Slef_loop_back procedure:

(1) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	F0	DBNC_EN	DISCON_ENABLE	EN_ERR_UNDERRUN	LATE_DL LEN	INTG	SOP_KK	SLB_INNER	SLB_EN	
			1	1	1	1	1	1	0: digital & analog 1: digital only	1	

(2) set test_psl, test_seed and test_speed
(3) set test_rst=1 & test_en=0 (reset)
(4) set test_rst=0 & test_en=0 (reset)
(5) set test_rst=0 & test_en=1 (enable)
(6) polling test_done
(7) check test_fail

Force MAC to enter High-Speed procedure:
(1) In simulation mode: force_hs_mode=1 & simulation_mode=1
(2) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
(3) In normal mode: force_hs_mode=0 & simulation_mode=0

1.6 REGISTER:: VERSION_reg 0x9801_3814

Module::**usb**	Register:: **TWO_PORT_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3814**

Name	Bits	R/W	Default	Comments
Rvd	**31..12**	-	-	-
trans_flag_host	11	R	'b0	When HOST issue sb1_req & write, this bit will be asserted and it'll be de-asserted if sb1_done is asserted. 1: HOST write transfer isn't complete
trans_flag_otg	10	R	'b0	When OTG issue sb1_req & write, this bit will be asserted and it'll be de-asserted if sb1_done is asserted. 1: OTG write transfer isn't complete
Dummy_reg	9..2	R/W	8'h00	Dummy registers For FPGA: Dummy[0]: gateing port0 VLOADM Dummy[1]: gateing port1 VLOADM Dummy[2]: control VSTATUS output enable
Nouse_done	1	R/W	'b0	1: Interrupt doesn't gatting sb1_usb_done signal 0: interrupt gatting with sb1_usb_done signal (It's only used to generate a mux selection.)
Wrap_version	0	R/W	'b0	It's used to identify wrapper version 1: Venus version 0: Neptune version

Note1: The interrupt should not need to gate with sb1_usb_done, so bit1 (nouse_done) should set “high”.
Note2: When interrupt happens, SW should polling trans_flag_host or trans_flag_otg to ensure data have been written to DDR.

1.7 REGISTER:: Wrapp_2port_reg 0x9801_3820

Module::**usb**	Register:: **Wrapp_2port_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3820**

Name	Bits	R/W	Default	Comments
Rvd	29..7	-	-	-
suspend_r	6	R/W	‘b0	1: wake up 0: depend on IP’s utmi_suspend_n_o signal when set ‘1’, PHY will turn on all clocks (UTMI_CLK, 12M and 48M) to host, then suspend_r will be auto turned to ‘0’ when utmi_suspend_n_o asserted.
Rvd	5..0	-	-	-

1.8 REGISTER:: VSTATUS_2port_reg 0x9801_3824

Module::**usb**	Register:: **VSTATUS_2port_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3824**

Name	Bits	R/W	Default	Comments
Rvd	**31..8**	-	-	-
Vstatus_out	7..0	R/W	‘h00	Vstatus output (It’s used to configure PHY’s control register)

The process of configuring PHY control register:

3. write VSTATUS_reg (0x9801_3824), (data output to PHY)
4. write INSNREG05 (0x9801_30a4)
   [17]: vBusy
   [16:13] : port number = 0001
   [12]: vload (low active)
   [11:8]: vcontrol

[7:0]: vstatus_in (data input from PHY)

3. polling [17]: vBusy, if [17]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.9 REGISTER:: USBIPINPUT_2port_reg 0x9801_3828

Module::**usb**	Register:: **USBIPINPUT_2port_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3828**

Name	Bits	R/W	Default	Comments
pwr_mux	**31**	**R/W**	'b0	**0: high active of power control output signal** **1: low active of power control output signal**
ovrcur_mux	30	R/W	'b1	1: select low active of over current input signal 0: select high active of over current input signal
Rvd	29..28	-	-	-
utmi_suspend_mux	27	R/W	'b0	Due to phy_clk should be suspended in RUN=0 1: select gatting with RUN=0 0: select original from IP
host_disc_mux	26	R/W	'b1	0: utmi_discon_det_i => tie 0 1: utmi_discon_det_i => from PHY (HostDisconnect)
Rvd	25..14	-	-	-
ss_fladj_val_5_i	13	R/W	'b1	
ss_fladj_val_4_i	12	R/W	'b0	
ss_fladj_val_3_i	11	R/W	'b0	
ss_fladj_val_2_i	10	R/W	'b0	
ss_fladj_val_1_i	9	R/W	'b0	
ss_fladj_val_0_i	8	R/W	'b0	
Rvd	7..0	-	-	-

1.10 REGISTER:: RESET_UTMI_2port_reg 0x9801_382c

Module::**usb**	Register:: **RESET_UTMI_2port_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_382c**

Name	Bits	R/W	Default	Comments
Rvd	**31..3**	-	-	-
Test_rst	2	R/W	'b0	Self_loop_back reset
Test_en	1	R/W	'b0	Self_loop_back enable
Reset_UTMI	0	R/W	'b0	UTMI reset (to PHY) (It's a sync. reset in PHY) When set high, it'll return to low automatically.

1.11 REGISTER:: SELF_LOOP_BACK_2port_reg 0x9801_3830

Module::**usb**	Register:: **SELF_LOOP_BACK_2port_reg**	Set::**1**	ATTR::**nor**	Type::**SR**	ADDR::**0x9801_3830**

Name	Bits	R/W	Default	Comments
Rvd	**31..18**	-	-	-
Simulation_mode	17	R/W	'b0	Reduce counter for entering High-Speed mode
Force_hs_mode	16	R/W	'b0	Force HOST IP enter High-Speed mode 1: enable, 0: disable
Reserved	15-14	-	-	-
Test_done	13	R	'b0	Self_loop_back done
Test_fail	12	R	'b0	Self_loop_back result fail
Test_speed	11-10	R/W	'b00	When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2'b01: force PHY in HS 2'b10: force PHY in FS/LS 2'b00/2'b11: normal mode
Test_seed	9-2	R/W	'h00	Self_loop_back Random generator seed
Test_psl	1-0	R/W	'b00	Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter

1.12 REGISTER:: IPNEWINPUT_2port_reg 0x9801_3834

Module::**usb**	Register:: **IPNEWINPUT_2port_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3834**

Name	Bits	R/W	Default	Comments
Rvd	**31..4**	-	-	-
ss_ulpi_pp2vbus_i	3	R/W	'b0	IP input
ss_autoppd_on_overcur_en_i	2	R/W	'b0	IP input
ss_power_state_valid_i	1	R/W	'b0	IP input
reg_usb_ck27m_sel	0	R/W	'b0	It's used to select clock source for usbphy PLL 1: select 1.2V 27MHz clock for PLL 0: select 3.3V 27MHz clock for PLL

1.13 REGISTER:: USBPHY_SLB0_reg 0x9801_3838

Module::**usb**	Register:: **USBPHY_SLB0_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3838**

Name	Bits	R/W	Default	Comments
Rvd	**31..4**	-	-	-
usbphy_slb_done	3	R	'b0	Usbphy port0 self loop back done
usbphy_slb_fail	2	R	'b0	Usbphy port0 self loop back fail
usbphy_slb_hs	1	R/W	'b0	Usbphy port0 self loop back hs mode
usbphy_force_slb	0	R/W	'b0	Usbphy port0 self loop back start

1.14 REGISTER:: USBPHY_SLB1_reg 0x9801_383c

Module::**usb**	Register:: **USBPHY_SLB1_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_383c**

Name	Bits	R/W	Default	Comments
Rvd	**31..4**	-	-	-
usbphy_slb_done	3	R	'b0	Usbphy port1 self loop back done

usbphy_slb_fail	2	R	‘b0	Usbphy port1 self loop back fail
usbphy_slb_hs	1	R/W	‘b0	Usbphy port1 self loop back hs mode
usbphy_force_slb	0	R/W	‘b0	Usbphy port1 self loop back start

1.15 REGISTER:: USB_OTG_reg 0x9801_3840

Module::**usb**	Register:: **USB_OTG_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3840**

Name	Bits	R/W	Default	Comments
Rvd	**31..6**	**-**	**-**	-
iopdcr_reserved_12	6	R/W	‘b0	Synopsys modify OTG IP, it’s used to do a mux selection.
ss_scaledown_mode	5..4	R/W	‘b00	For OTG IP simulation scale down
m_hbigendian	3	R/W	‘b0	OTG master (dbus) endian
s_hbigendian	2	R/W	‘b0	OTG slave (rbus) endian
from_frchs	1	R/W	‘b0	Select linestate signals to OTG IP 1: linestate signals from the output of forcehs module 0: linestate signals from the signals before forcehs module
otg_enable	0	R/W	‘b0	1: enable OTG, 0: disable OTG

1.16 REGISTER:: USB_OTGMUX_reg 0x9801_3844

Module::**usb**	Register:: **USB_OTGMUX_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3844**

Name	Bits	R/W	Default	Comments
Rvd	**31..25**	**-**	**-**	-

data_value[8]	24	R/W	‘b0	Value of P1_DmPulldown (device=1’b0)
data_value[7]	23	R/W	‘b0	Value of P1_DpPulldown (device=1’b0)
data_value[6]	22	R/W	‘b0	Value of P1_IDPULLUP (device=1’b0)
data_value[5]	21	R/W	‘b0	Value of otg_sessend (device=1’b0)
data_value[4]	20	R/W	‘b0	Value of otg_vbusvalid (device=1’b1)
data_value[3]	19	R/W	‘b0	Value of otg_bvalid (device=1’b1)
data_value[2]	18	R/W	‘b0	Value of otg_avalid (device=1’b1)
data_value[1]	17	R/W	‘b0	Value of otg_iddig (device=1’b1)
data_value[0]	16	R/W	‘b0	Value of otg_hostdisconnect (device=1’b0)
Rvd	15..9	-	-	-
data_mux[8]	8	R/W	‘b0	P1_DmPulldown=~otg_enable ? 1’b1 : data_mux[8] ? data_value[8] : otg_dmpulldown;
data_mux[7]	7	R/W	‘b0	P1_DpPulldown=~otg_enable ? 1’b1 : data_mux[7] ? data_value[7] : otg_dppulldown;
data_mux[6]	6	R/W	‘b0	P1_IDPULLUP=~otg_enable ? 1’b0 : data_mux[6] ? data_value[6] : otg_idpullup;
data_mux[5]	5	R/W	‘b0	0: otg_sessend from port1 PHY 1: otg_sessend from data_value[5]
data_mux[4]	4	R/W	‘b0	0: otg_vbusvalid from port1 PHY 1: otg_vbusvalid from data_value[4]
data_mux[3]	3	R/W	‘b0	0: otg_bvalid from port1 PHY 1: otg_bvalid from data_value[3]
data_mux[2]	2	R/W	‘b0	0: otg_avalid from port1 PHY 1: otg_avalid from data_value[2]
data_mux[1]	1	R/W	‘b0	0: otg_iddig from port1 PHY 1: otg_iddig from data_value[1]
data_mux[0]	0	R/W	‘b0	0: otg_hostdisconnect from port1 PHY 1: otg_hostdisconnect from data_value[0]

Note: When OTG device mode, this register should set 0x001e_01ff.

1.17 REGISTER:: USB_dummy0_reg 0x9801_3848

Module::**usb**	Register:: **USB_dummy3848_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3848**

Name	Bits	R/W	Default	Comments
Rvd	**31..9**	**-**	**-**	**-**
prt_pwren_reg_ds	8..7	R/W	‘b0	

prt_pwren_ctrl	6..5	R/W	'b0	
prt_ovrcur_reg_ds	4..3	R/W	'b0	
prt_ovrcur_ctrl	2..1	R/W	'b0	
usb_dbg_ctrl	0	R/W	'b0	

1.18 REGISTER:: USB_dummy1_reg 0x9801_384c

Module::**usb**	Register:: **USB_dummy384c_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_384c**

Name	Bits	R/W	Default	Comments
Rvd	**31..2**	**-**	**-**	**-**
usb_ldo_en	1	R/W	'b0	enable UPHY LDO ,default:disable
usb3_isolate_mac2phy	0	R/W	'b0	Isolate enable U3PHY when disable USB3

1.19 REGISTER:: USB_BIST_CTRL_reg 0x9801_3850

Module::**usb**	Register:: **USB_BIST_CTRL_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3850**

Name	Bits	R/W	Default	Comments
Rvd	**31..23**	**-**	**-**	**-**
usb2_bist1_rme_1	22	R/W	'b0	Bist1 RM1 enable
usb2_bist1_rm_1	21..18	R/W	3'h0	Bist1 RM1 value
usb2_bist1_rme_0	17	R/W	'b0	Bist1 RM0 enable
usb2_bist1_rm_0	16..13	R/W	3'h0	Bist1 RM0 value
usb2_drf_bist1_test_resume	12	R/W	'b0	Bist1 drf resume
usb2_drf_bist1_en	11	R/W	'b0	Bist1 drf enable
usb2_bist1_en	10	R/W	'b0	Bist1 enable
usb2_bist1_mode	9	R/W	'b0	Bist1 test mode
usb2_bist2_rme	8	R/W	'b0	bist2 RM enable
usb2_bist2_rm	7..4	R/W	3'h0	bist2 RM value
usb2_drf_bist2_test_resume	3	R/W	'b0	bist2 drf resume

usb2_drf_bist2_en	2	R/W	‘b0	bist2 drf enable
usb2_bist2_en	1	R/W	‘b0	bist2 enable
usb2_bist2_mode	0	R/W	‘b0	bist2 test mode

1.20 REGISTER:: USB_BIST_STS_reg 0x9801_3854

Module::**usb**	Register:: **USB_BIST_STS_reg**	Set::**1**	ATTR::**ctrl**	Type::**SR**	ADDR::**0x9801_3854**

Name	Bits	R/W	Default	Comments
Rvd	**31..12**	**-**	**-**	**-**
usb2_drf_bist2_fail_1	11	R	‘b0	Bist1 1 drf test fail
usb2_drf_bist2_fail_0	10	R	‘b0	Bist1 0 drf test fail
usb2_drf_bist2_start_pause	9	R	‘b0	Bist1 drf test start pause
usb2_drf_bist1_done	8	R	‘b0	Bist1 drf test done
usb2_bist1_fail_1	7	R	‘b0	Bist1 1 test fail
usb2_bist1_fail_0	6	R	‘b0	Bist1 0 test fail
usb2_bist1_done	5	R	‘b0	Bist1 test done
usb2_drf_bist2_fail	4	R	‘b0	Bist2 drf test fail
usb2_drf_bist2_start_pause	3	R	‘b0	Bist2 drf test start pause
usb2_drf_bist2_done	2	R	‘b0	Bist2 drf test done

usb2_bist2_fail	1	R	‘b0	Bist2 test fail
usb2_bist2_done	0	R	‘b0	Bist2 test done

1.21 REGISTER:: USB2_BC_CTL_REG 0x9801_3858

Module::usb	Register::USB2_BC_CTL_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3858

Name	Bits	R/W	Default	Comments
Rvd	31..15	-	-	-
hst_pow_charge_1_usb2	13	R/W	‘b0	Enable charge, high enable
hst_vdm_src_en_1_usb2	12	R/W	‘b0	Enable VDM_SRC output, high enable
hst_idp_sink_en_1_usb2	11	R/W	‘b0	Enable DP current sink, high enable
hst_app_div_en_1_usb2	10	R/W	‘b0	Enable Apple mode, high enable
hst_app_div_sel_1_usb2	9	R/W	‘b0	Select Apple charge current 2.1A/1A 0: DP=2.0V, DM=2.7V 1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_1_usb2	8	R/W	‘b0	Enable comparator for detect Apple/DCP mode, high enable
hst_note_div_en_1_usb2	7	R/W	‘b0	Enable NOTE mode, high enable, DP=1.25V
hst_dcp_en_1_usb2	6	R/W	‘b0	Enable DCP mode, high enable, short DP and DM.
dev_pow_charge_1_usb2	5	R/W	‘b0	Enable charger, high enable
dev_dcp_chg_mode_1_usb2	4	R/W	‘b0	0: select CHG_DET detect 1: select DCP_DET detect
dev_vdp_src_en_1_usb2	3	R/W	‘b0	Enable DP output voltage, high enable
dev_vdm_src_en_1_usb2	2	R/W	‘b0	Enable DM output voltage, high enable
dev_idp_sink_en_1_usb2	1	R/W	‘b0	Enable DP current sink, high enable
dev_idm_sink_en_1_usb2	0	R/W	‘b0	Enable DM current sink, high enable

1.22 REGISTER:: USB2_BC_STS2_REG 0x9801_385C

Module::usb	Register::USB2_BC_STS2_REG	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_385c

Name	Bits	R/W	Default	Comments
Rvd	31..8	-	-	-
hst_prtbl_det_1_usb2	7	R	‘b0	
hst_comp_out_1_usb2	6	R	‘b0	Debug signal
hst_sh_out_1_usb2	5	R	‘b0	Debug signal
hst_v0p07_out_1_usb2	4	R	‘b0	DP>0.35V, output=low, DP<0.35V, output=high
hst_v0p41_out_1_usb2	3	R	‘b0	DM>THD, output=low, DM<THD, output=high
hst_v0p46_out_1_usb2	2	R	‘b1	don't care. Output=high.
dev_chg_det_1_usb2	1	R	‘b0	Detector result

dev_dcp_det_1_usb2	0	R	'b0	Detector result

1.23 REGISTER:: USB2_dummy_0_REG 0x9801_3860

Module::usb	Register::USB2_dummy_0_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3860
Name	Bits	R/W	Default	Comments	
dummy_60	31..0	R/W	32'h0	dummy register , default=0	

1.24 REGISTER:: USB2_dummy_1_REG 0x9801_3864

Module::usb	Register::USB2_dummy_1_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3864
Name	Bits	R/W	Default	Comments	
dummy_64	31..0	R/W	32'hFFFF_FFFF	dummy register , default=1	

1.25 REGISTER:: USB2_DBUS_PWR_CTRL_REG 0x9801_3868

Module::usb	Register::USB2_DBUS_PWR_CTRL_REG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3868
Name	Bits	R/W	Default	Comments	
Rvd	31..12	-	-	-	
clk_en_gap	11..10	R/W	2'h0		
sram_ls_gap	9..8	R/W	2'h0		
Rvd	7..2	-	-	-	
dbus_pwr_ctrl_sw_rst	1	R/W	1'b0		
dbus_pwr_ctrl_en	0	R/W	1'b0		

1.26 REGISTER:: HCCAPBASE 0x9801_3000

1.27 REGISTER:: HCSPARAMS 0x9801_3004

1.28 REGISTER:: HCCPARAMS 0x9801_3008

1.29 REGISTER:: USBCMD 0x9801_3010

1.30 REGISTER:: USBSTS 0x9801_3014

1.31 REGISTER:: USBINTR 0x9801_3018

1.32 REGISTER:: FRINDEX 0x9801_301c

1.33 REGISTER:: CTRLDSSEGMENT 0x9801_3020

1.34 REGISTER:: PERIODICLISTBASE 0x9801_3024

1.35 REGISTER:: ASYNCLISTADDR 0x9801_3028

1.36 REGISTER:: CONFIGFLAG 0x9801_3050

1.37 REGISTER:: PORTSC_0 0x9801_3054

1.38 REGISTER:: INSNREG00 0x9801_3090

Name	bits	Read/Write	Reset State	Comments
Microframe length	31-1	R/W	31'b0	
select	0	R/W	1'b0	0: from input, 1: from [31:1]

1.39 REGISTER:: INSNREG01 0x9801_3094

Name	bits	Read/Write	Reset State	Comments
OUT threshold	31-16	R/W	0040	0100=256x4B=1024B
IN threshold	15-0	R/W	0040	0040=64x4B=256B

1.40 REGISTER:: INSNREG02 0x9801_3098

1.41 REGISTER:: INSNREG03 0x9801_309c

Name	bits	Read/Write	Reset State	Comments
Reserved	31-1	-	-	

Break Memory Transfer	0	R/W	0	1: enable, 0: disable

1.42 REGISTER:: INSNREG04 0x9801_30a0

1.43 REGISTER:: INSNREG05 0x9801_30a4

Name	bits	Read/Write	Reset State	Comments
Reserved	31-18	-	-	-
vBusy	17	R/W	1'b0	
Port number	16-13	R/W	4'b0	0001
vload	12	R/W	1'b1	Low active
vcontrol	11-8	R/W	4'b0	
Vstatus_in	7-0	R/W	8'b0	

1.66 OTG REGISTERS 0x981E_0000 ~ 0x981E_ffff

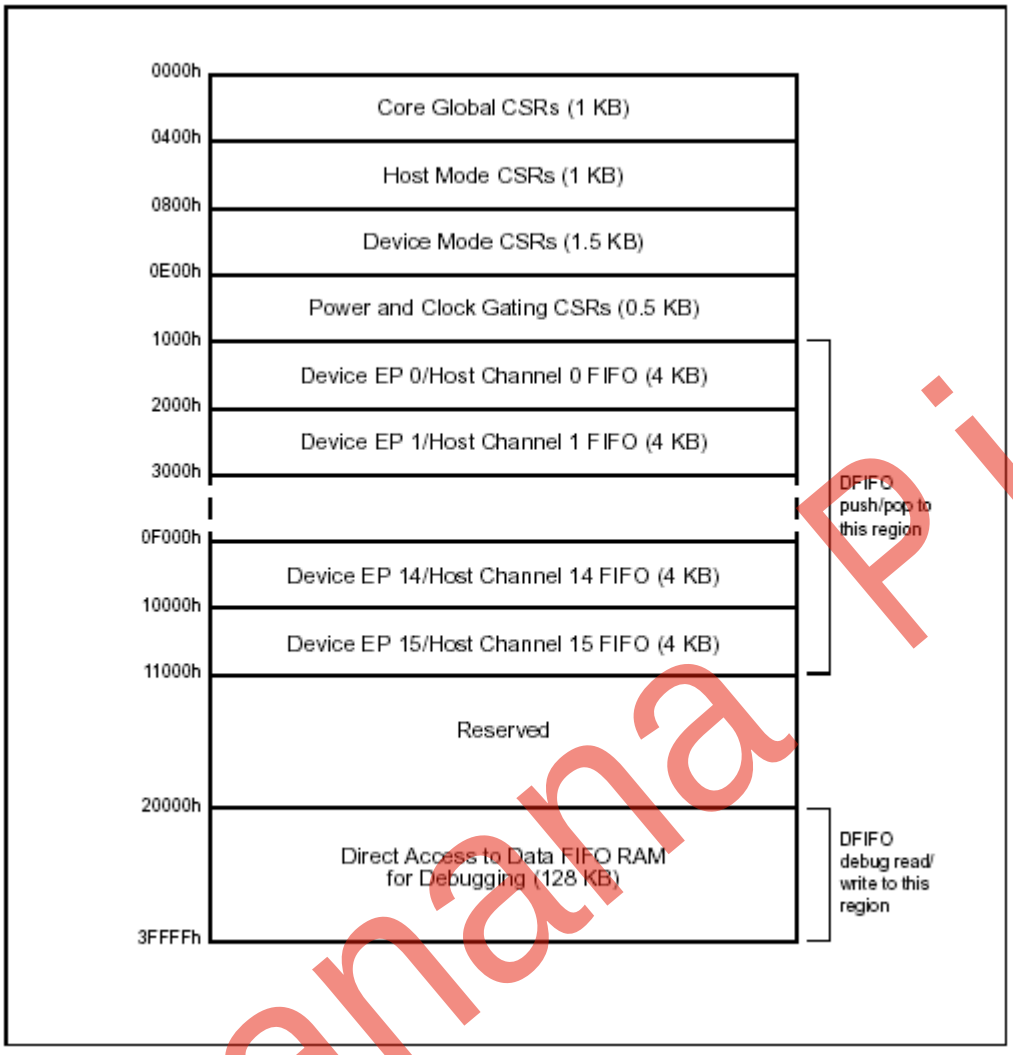

FIGURE 5-1 OTG CSR Memory Map