

Standard for RealTek DVD Recordable

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Kylin USB3.0

RealTek specification on DVD Recordable Technology



Specification for Kylin: USB3.0 Specification

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1.1 REGISTER:: WRAP_CTR_reg

0x9801_3200

Module::usb Register::W	RAP_CTR	Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3200		
Name	Bits	R/W	Default		Comments		
Rvd	317			-			
rxdetect_value	6	R/W	'b0				
rxdetect_sel	5	R/W	'b0				
resume_cycle_sel	4	R/W	'b0				
sram_debug_sel	3	R/W	'b0	Select sram			
				1: host			
				0: device			
sram_debug_mode	2	R/W	'b0	Enable sran	n de <mark>bu</mark> g mode		
dbus_multi_req_disable	1	R/W	'b0		ltiple request for Dbus		
				0: enable m	ultiple request		
				1: disable m	nultiple request		
dev_mode	0	R/W	'b0	Enable peek on AHB burst length			
				0: host (2)			
				1: host/dev			

1.2 REGISTER:: GNT_INT_reg

0x9801_3204

Module::usb Register::GN	NR_INT	Set::	1 ATTR::nor	Type::SR ADDR::0x9801_3204	
Name	Bits	R/W	Default	Comments	
Rvd	312		-	-	
device_int	1	R	'b0	USB3 Device MAC interrupt	
host_int	0	R	'b0	USB3 Host MAC interrupt	

1.3 REGISTER:: USB2_PHY_UTMI

0x9801_3208

Module::usb	Register:	:USB2_PHY	_UTMI Set	::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3208
Na	me	Bits	R/W Default Comme		Comments	
Rvd		311	_	-	-	
reset_utmi_p0		0	R/W	'b0	UTMI rese	t to PHY1 (sync and
					automatical	lly return to low)

1.4 REGISTER:: USB3_PHY_PIPE

0x9801_320c

Module::usb	Register::US	SB3_PHY_PIPE Set::1			ATTR::ctrl	Type::SR	ADDR::0x9801_320c	
Name		Bits	R/V	W	Default	Comments		
Rvd	311	-		=	-			
reset_pipe3_p0		0	R/V	W	'b0	PIPE3 reset to PHY1 (sync and		
						automatica	lly return to low)	

1.5 REGISTER:: MDIO_CTR_reg



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Module::usb			Set	t::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3210		
Na	me	Bits	R/W	Default	Comments			
data		3116	R/W	'h0	Write data or read data.			
phy_addr		1513	R/W	'd0	MDIO PH	Y addressing value.		
phy_reg_addr		128	R/W	'd0	MDIO Register addressing value			
mdio_busy		7	R/W	'd0	-			
mdio_st		65	R/W	'd0	MDIO host	t controller state Monitor		
mdio_rdy		4	R/W	'd0	MDIO Pre-	amble signal Monitor		
mclk_rate		32	R/W	'd0	MDIO clock rate selection:			
					2'b00: clk_	_sys/32		
					2'b01: clk_	_sys/16		
					2'b10: clk_	_sys/8		
					2'b11: clk_sys/4			
mdio_srst		1	R/W	R/W 'd0 Ass		/W 'd0 Assert 1'b1 to do soft reset		
mdio rdwr		0	R/W	/ 'd0 1'b0: read . 1'b1: write				

1.6 REGISTER:: VSTATUS_port0_reg

0x9801_3214

Module::usb	Register::VS	TATUS0_C	OUT	Set::1 ATTR::ctrl			Ty	Type::SR ADDR::0x9801_3214		
Nar	Bits	R/W		Default		Comments				
Rvd		318	-	-	7		1			
p0_vstatus_out		70	R/	W	'h00				put for port1 (It's used to	
							C	onfigure P	HY's control register)	

The process of configuring PHY control register:

- 1. write VSTATUS_reg (0x9801_3214), (data output to PHY)
- 2. write GUSB2PHYAccn (0x1802_8280)

[25]: vload

[23]: vBusy

[11:8]: vcontrol

[7:0]: vstatus_in (data input from PHY)



0x9801_3218

Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'b0	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. Note: This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. Note: These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.7 REGISTER:: SLP_BACK_EN_port0_reg

Module::usb	Register::SLP_BACK0_EN		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3218	
Nam	ne	Bits	R/	W	Default		Comments



Rvd	314	-	-	-
simulation_mode_p0	3	R/W	'b0	Reduce counter for entering HS
force_hs_mode_p0	2	R/W	'b 0	Force HOST IP enter high speed mode 0: disable 1: enable
test_rst_p0	1	R/W	'b0	Self loop back reset
test_en_p0	0	R/W	'b0	Self loop back enable

1.8 REGISTER:: SLP_BACK_CTR_port0_reg

0x9801_321c

Module::usb Register::	SLP_BACK0_0	CTR Set:	:1 ATTR::ctrl	Type::SR ADDR::0x9801_321c
Name	Bits	R/W	Default	Comments
Rvd	3112	-	-	-
test_speed_p0	1110	R/W	'h0	When Self_loop_back, force PHY
				enter High Speed or Full Speed
				mode
				(HS: utmi_xver_select=0,
				utmi_term_select[1:0]=00)
				(FS: utmi_xver_select=1,
				utmi_term_select[1:0]=01,
				FsLsSerialMode=0)
				2'b01: force PHY in HS
				2'b10: force PHY in FS/LS
				2'b00/2'b11: normal mode
test_seed_p0	92	R/W	ʻh0	Self_loop_back
				Random generator seed
test_psl_p0	10	R/W	ʻh0	Select self_loop_back pattern
			•	00: all zeros
				01: load from seed
				10: pseudo random pattern
				11: incremental counter

1.9 REGISTER::SLP_BACK_ST_port0_reg

0x9801_3220

Module::usb	Register::SL	LP_BACK0_ST Set::		Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3220	
Nan	Name			W	Default	Comments		
Rvd		312	-			-		
test_fail_p0		1	R	1	'b0	Self loop back fail		
test_done_p0		0	R		'b0	Self loop back done		

Slef_loop_back procedure:

(1) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	ΕO	DDNC E	DISCON E	EN EDD IIN	LATE DI	INITO	SOD KK	CLD ININIED	CLD EN	
K/VV	ುಂ	ΓU	DDINC_E	DISCON_E	EIN_EKK_UIN	LAIE DL	IIN I G	SUP_KK	SLB_INNER	OLD EIN	



N	NABLE	DERRUN	LEN					
1	1	1	1	1	1	0: digital &	1	
						analog		
						1: digital only		

- (2) set test_psl, test_seed and test_speed
- (3) set test_rst=1 & test_en=0 (reset)
- (4) set test_rst=0 & test_en=0 (reset)
- (5) set test_rst=0 & test_en=1 (enable)
- (6) polling test_done
- (7) check test_fail

Force MAC to enter High-Speed procedure:

- (1) In simulation mode: force_hs_mode=1 & simulation_mode=1
- (2) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
- (3) In normal mode: force_hs_mode=0 & simulation_mode=0

1.10 REGISTER:: PHY2_SLB0_EN_reg

0x9801_3224

Module::usb	Register::PHY2_SLB_EN			N Set::1 ATTR::c		ATTR::ctrl	Type::SR	ADDR::0x9801_3224		
Nam	ne	Bits		R/W		1	Default	Comments		
Rvd		312		(-)			-	-		
p0_usb2phy_sl	p0_usb2phy_slb_hs		R/W		'b0	Usbphy port0 self loop back hs				
								mode		
p0_usb2phy_fo	rce_slb	0		R/W			'b0	Usbphy por	rt0 self loop back start	

1.11 REGISTER: PHY2 SLB0 ST reg

0x9801 3228

Module::usb Register::PI	IY2_SLB_S	ST Set:	:1 ATTR::nor	Type::SR ADDR::0x9801_3228	
Name	Bits	R/W	Default	Comments	
Rvd	312	-	=	-	
p0_usb2phy_slb_fail 1		R	'b0	Usbphy port0 self loop back done	
p0_usb2phy_slb_done			'b0	Usbphy port0 self loop back fail	

1.12 REGISTER:: USB2_SPD_CTR

0x9801_322C

Module::usb	Register::US	egister::USB2_SPD_CTR			ATTR::ctrl	Type::SR	ADDR::0x9801_322c
Name Bits		R/V	W	Default	Comments		
Rvd		311	-		-	-	
p0 suspend r		0	R/V	W	'b0	-	



1.13 REGISTER:: USB3_ SLB_EN_reg

0x9801_3230

Module::usb	Register:: PI	HY3_SLB_EN		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3230	
Nar	ne	Bits	R/W	·	Default		Comments	
Rvd		313	-		-	-		
p0_pipe_bist_s	sel	21	R/W		'b0	Self loop back select:		
						00:counter		
						01:tseq		
						10:ts1		
						11:ts2		
p0_pipe_bist_e	en	0	R/W	r	'b0 Self loop back enable			

1.14 REGISTER:: PHY3_ SLB_CT_reg

0x9801_3234

Module::usb	Register::PH	Y3_SLB_C	T Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3234
Naı	me	Bits	R/W	Default		Comments
Rvd		311	-	=	-	
p0_usb3phy_s	lb_go	0	R/W	'b0	Usb3phy	port0 self loop back start
					transfer	

1.15 REGISTER:: PHY3_ SLB_ST_reg

0x9801_3238

Module::usb Register::PF	ST Set::1	ATTR::nor_up	Type::SR ADDR::0x9801_3238	
Name	Bits	R/W	Default	Comments
Rvd	312	-	-	-
p0_usb3phy_slb_fail	1	R	'b0	Usb3phy port0 self loop back done
p0_usb3phy_slb_done	0	R	'b0	Usb3phy port0 self loop back
				enable

1.16 REGISTER:: USB_DBG_reg

Module::usb	Register::US	SB_DBG	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3240		
Nam	ne	Bits	R/W	Default		Comments		
Rvd		3113	-	-	-			
dbg_sel1		127	R/W	'b0	Select deb	oug signal sets to be		
					-	probed via usb_dbg_out1		
dbg_sel0		61	R/W	'b0	Select debug signal sets to be			
					probed via	a usb_dbg_out0		
dbg_en		0	R/W	'b0	Debug ena			
						selected signals can be		
					probed via debug ports. When clear			
					both usb_dbg_out0 and			
					usb_dbg_	out1 are static 16'h0.		



1.17 REGISTER:: USB_STCH_reg

0x9801_3244

Module::usb	Register::US	SB_SCTCH	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3244	
Nam	Name Bits R		R/W	Default	Comments		
reg1		3116	R/W	'hffff	Dummy register with value 1		
reg0 150 I		R/W	'd0	Dummy register with value 0			

1.18 REGISTER:: USB_TMP_SP_reg _0

0x9801_3248

Module::usb Register::USI	3_TMP_SP	Set::1	ATTR::nor	Type::SR ADDR::0x9801_3248		
Name	Bits	R/W	Default	Comments		
test_sp_reg_0	3112	R/W	'd0	Dummy test register		
int_inact_status	11	R/W	'd0	Itssm change to ss inactive state		
int_ss_dis_status	10	R/W	'd0	ltssm change to ss disabled state		
int_hreset_status	9	R/W	'd0	Itssm change to hot reset state		
int_recov_status	8	R/W	'd0	Itssm change to recovery state		
int_rx_det_status	7	R/W	'd0	Itssm change to rx detect state		
int_poll_status	6	R/W	'd0	Itssm change to polling state		
int_u3_status	5	R/W	'd0	Itssm change to u3 state		
int_u2_status	4	R/W	'd0	Itssm change to u2 state		
int_u1_status	3	R/W	'd0	Itssm change to u1 state		
int_u0_status	2	R/W	'd0	ltssm change to u0 state		
int_loopbk_status	1	R/W	'd0	Itssm change to loopback state		
int_comp_status	0	R/W	,q0	Itssm change to compliance state		

1.19 REGISTER:: USB_TMP_SP_reg_

0x9801_324C

Module::usb Register::USI	Set::1	ATTR::nor	Type::SR ADDR::0x9801_3248	
Name Bits		R/W	Default	Comments
test_sp_reg_1 310		R/W	'd0	Dummy test register

1.20 REGISTER:: USB_TMP_reg

Module::usb	Iodule::usb Register::USB_TMP			Set::3	ATTR::ctrl	Type::SR	ADDR::0x9801_3250	
Nam	e		Bits	R	/W	Default		Comments
test_reg	7		310	R	/W	'd0	Dummy tes	st register



1.21 REGISTER:: USB_TMP_reg_3

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0x9801_325C

Module::usb Register::US	SB_TMP	Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3250	
Name	Bits	R/W	Default	Comments		
test_reg_3	3113	R/W	'd0	Dummy test register		
int_inact_en	12	R/W	'd0		ge to ss inactive state	
				interrupt er		
int_ss_dis_en	11	R/W	'd0		ge to ss disable state	
				interrupt er		
int_hreset_en	10	R/W	'd0		ge to hot reset state	
			(10	interrupt er		
int_recov_en	9	R/W	'd0		ge to recovery state	
	0	D/W	6.10	interrupt er		
int_rx_det_en	8	R/W	'd0		ge to rx detect state	
5 m 4 m 2 11 m m	7	D/W	6.10	interrupt er		
int_poll_en	/	R/W	'd0	ltssm change to polling state interrupt enable		
int_u3_en	6	R/W	'd0		ge to u3 state interrupt	
Int_us_en	U	IX/ VV	uo	enable	ge to us state interrupt	
int_u2_en	5	R/W	'd0	0111110110	ge to u2 state interrupt	
Int_u2_cn	3	IX/ VV	do	enable	ge to uz state interrupt	
int_u1_en	4	R/W	'd0		ge to u1 state interrupt	
1110_01_011		20 11		enable	so to all state interrupt	
int_u0_en	3	R/W	'd0	ltssm chans	ge to u0 state interrupt	
				enable	1	
int_loopbk_en	2	R/W	d0 ltssm change to loopback s		ge to loopback state	
_			interrupt enable		nable	
int_comp_en	1	R/W	'd0	'd0 ltssm change to compliance sta		
				interrupt enable		
Rvd	0	-	_	-		

1.22 REGISTER:: USB_HMAC_CTR0_reg

Module::usb Register::HN	MAC_CTRO	Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3260
Name	Bits	R/W	Default		Comments
Rvd	31	-	-	-	
host_ utmiotg_vbusvalid	30	R/W	'b1	-	
host_fladj_30mhz	2924	R/W	'd32	-	
host_ppc_present	23	R/W	'b0	-	
host_msi_enable	22	R/W	'b0		
host_pm_pw_state_req	2120	R/W	'b0		
hub_port_over_current	1916	R/W	'b0		
Rvd	1514	-	-	-	
hub_port_perm_attach	1312	R/W	'b0		
Rvd	1110	-	-		
host_u2_port_disable	9	R/W	'b0		
host_u3_port_disable	8	R/W	'b0		
host_num_u2_port	74	R/W	'd1		
host_num_u3_port	30	R/W	'd1		



1.23 REGISTER:: MAC3_HST_ST_reg

0x9801_3264

Module::usb	Register::MA	C3_HST_S	T Set::1	ATTR::nor	Type::SR ADDR::0x9801_3264		
Name Bits		R/W	Default	Comments			
Rvd		314	-	=	-		
host_current_power_state		32	R	'b0	Current xHC power state		
host_hub_vbus_ctrl		10	R	'b0	Vbus active indication		

1.24 REGISTER::DMAC_CTR0_reg

0x9801_3268

Module::usb Register::DN	MAC_CTR(Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3268
Name	Bits	R/W	Default		Comments
Rvd	3127	-	-	-	
xhc_bme	26	R/W	'b1		
dev_vbus_value	25	R/W	'b0		
dev_utmiotg_vbusvalid	24	R/W	'b0		
dev_pm_pw_state_req	2322	R/W	'b0		
dev_fladj_30mhz	2116	R/W	'd32		
dev_usb_outep_pkt_buff	150	R/W	'hffff		

1.25 REGISTER:: MAC3_DEV_ST_reg

0x9801_326C

Module::usb Register::MA	.C3_DEV_S	ST Set::1	ATTR::nor	Type::SR ADDR::0x9801_326c		
Name Bits R			Default	Comments		
Rvd	312	-	-	-		
dev_current_power_state	10	R	'b0	Current xHC power state		

1.26 REGISTER: USB2_PHY_reg

Module::usb Register::US	:USB2_PHY Set::1 ATTR		1 ATTR::ct	rl Type::SR ADDR::0x9801_3270
Name	Bits	R/W	Default	Comments
Rvd	3112	1	-	-
p0_by_pass_on_0	11	R/W	'b0	isolation A→D
p0_DmPulldown	10	R/W	'b0	Device = 1'b0
p0_DpPulldown	9	R/W	'b0	Device = 1'b0
p0_IDPULLUP	8	R/W	'b0	Device = 1'b0
Rvd	73	-	-	-
p0_DmPulldown_sel	2	R/W	'b0	p0_dmpulldown =~dev_mode ? 1'b1:
				p0_DmPulldown_sel ?
				p0_DmPulldown: 1'b0
p0_DpPulldown_sel	1	R/W	'b0	p0_dppulldown =~dev_mode ? 1'b1:
				p0_DpPulldown_sel ?
				p0_DpPulldown: 1'b0
p0_IDPULLUP_sel	0	R/W	'b0	p0_dmpulldown =~dev_mode ? 1'b1:
				p0_IDPULLUP_sel ?
				p0_IDPULLUP: 1'b0



1.27 REGISTER:: USB_RAM_CTR_reg

0x9801_3274

Module::usb	Register::RA	egister::RAM_CTR		ATTR::nor_up	Type::SR	ADDR::0x9801_3274		
Nan	ne	Bits	R/W	Default	Comments			
Rvd		3117	-	-	-			
done_st		16	R/W	'b0	Write 1 to	Write 1 to clear		
Rvd		151	-	=	-			
go_ct		0	R/W	'b0	Start DMA transfer, clear after done			

1.28 REGISTER:: USB_RAM_ADDR_reg

0x9801_3278

Module::usb	Register::RAM_ADDR			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3278	
Name		Bits	R/W		Default	Comments		
sram_addr		310	R/	W	'd0	SRAM address, 4-byte align.		
						Bit[0] = us	e for write/read bit	
					0: read			
						1: write		

1.29 REGISTER:: USB_RAM_WDATA_reg

0x9801_327C

Module::usb	Register::RAM_WDATA			Set::1	ATTR::	ctrl	Type:	:SR	ADDR::0x9801_	327C
Name Bits R/		R/V	V	Default				Comments		
ram_wdata		310	R/V	V	'd0		RAM	write o	data to be write	

1.30 REGISTER:: USB3_RAM_RDATA_reg

0x9801_3280

Module::usb	Register::RA	M_RDATA	A Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3280
Name		Bits	R/W	Default		Comments
ram_rdata		310	R/W	'd0	USB read d	ata to be read back

1.31 REGISTER:: USB3_PHY0_ST_reg

0x9801_3284

Module::usb	Register::PHY0_ST			et::1	ATTR::nor	Type::SR	ADDR::0x9801_3284
Name Bits R/		R/W		Default	Comments		
Rvd		3119	-		-	-	
p0_count_num		180	R		'b0	USB3 PHY count number value	

1.32 REGISTER:: USB3_OVR_CT_reg

Module::usb	Register::US	SB3_OVR_CT		Set::1 ATTR::ctrl		Type::SR	ADDR::0x9801_3288
Name		Bits	R/W D		Default	Comments	
Rvd	312 R/W -		-	-			
phy3_lperiod	phy3_lperiod 97 R/W		'd1	Connect to PHY3			
phy3_hperiod		64	R/W	V	'd3	Connect to PHY3	



phy3_last	32	R/W	'd2	Connect to PHY3
host_ovr_current_value	1	R/W	'b0	
host_ovr_current_sel	0	R/W	'b0	

Host MAC register

1.33 REGISTER:: SOFT_Reset

0x9801_3300

Module::usb Register::SC	FT_RESE	Γ Set::	1 ATTR::ctrl	Type::SR ADDR::0x9801_3300	
Name	Bits	R/W	Default	Comments	
Rvd	313			-	
rstn_usb2_phy1	2	R/W	'b0	USB2 PHY1 reset for USB2 IP	
rstn_usb2_phy0	1	R/W	'b0	USB2 PHY0 reset for USB2 IP	
rstn_usb2	0	R/W	'b0	USB2 IP system reset	

1.34 REGISTER:: GBL_USB_CT

0x9801_3304

Module::usb	Register::GBL_USB_CT			Set::1	ATTR:	:ctrl	Type::SR	ADDR::0x9801_3304
Nan	Name Bits R		/W	Default Comments			Comments	
usb_mac_ctrl		310	R	/W	'd0		Register us	e for usb_mac_ctrl

1.35 REGISTER:: GBL_USB_ARB

0x9801_3308

Module::usb	Register::GF	BL_USB_A	RB Set:	:1 ATTR::ctrl	Type::SR	ADDR::0x9801_3308	
Name Bits			R/W	Default	Comments		
Rvd		314	-				
dbus_robin_ena	able	3	R/W	'b0			
cmd_full_numb	er	21	R/W	'd3			
dbus_arb_prior	ity	0	R/W	'b0			

1.36 REGISTER:: UNUSED

0x9801_330C

1.37 REGISTER:: USB3_OTG_STS

Module::usb	Register::USB3_OTG_STS		Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3310		
					e			
Name Bits R/W			Default	Comment	Comments			
Rvd 311 -			-	-	-			
otg_interrupt		0	R	'b0	OTG inter	rupt from US	B3 MAC	



1.38 REGISTER:: USB_BC_STS

0x9801_3314

Module::usb	lle::usb Register::USB_BC_STS		Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3314			
Name		Bits	R/W	Defau lt	Comments				
Rvd		312	-	-	-				
chirp_on		1	R	'b0	battery charging chirp signal from USB3 MAC				
bc_interrupt		0	R	'b0	battery charging interrupt from USB3 MAC				

1.39 REGISTER:: USB3_BIST1_CTRL

0x9801_3318

Module::usb	Register::	USB3_BI	ST1_CT	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3318	
RL								
Name		Bits	R/W	Default	Comments			
Rvd		3128	-	_	-			
usb3_bist1_ls[2:	:0]	2725	R/W	3'h0	IP SRAM 0~	·2 LS value		
usb3_bist1_rm_;	3	2421	R/W	4'h0	SRAM3 RM	value	·	
usb3_bist1_rme_	_3	20	R/W	'b0	SRAM3 RM	enable		
usb3_bist1_rm_2	2	1916	R/W	4'h0	SRAM2 RM	value		
usb3_bist1_rme_	_2	15	R/W	'b0	SRAM2 RM	enable	•	
usb3_bist1_rm_	1	1411	R/W	4'h0	SRAM1 RM	value		
usb3_bist1_rme_	_1	10	R/W	'b0	SRAM1 RM	enable		
usb3_bist1_rm_0	0	96	R/W	4'h0	SRAM0 RM	value		
usb3_bist1_rme_	_0	5	R/W	'b0	SRAM0 RM	enable		
usb3_drf_1_test	_resume	4	W/R	'b0	USB3 DRF	BIST1 trigger	resume signal	
usb3_drf_bist1_	en	3	W/R	'b0	USB3 DRF BIST1 enable			
usb3_bist1_en		2	W/R	'b0	USB3 BIST	enable		
Rvd	_	1		F	-			
usb3_bist1_test_	_mode	0	W/R	'b0	USB3 BIST	test mode en	able	

1.40 REGISTER: USB3_BIST2_CTRL

0x9801_331c

Module::usb Register::USF L	BIST2_	CTR	Set::1 A	TTR::ctrl	Type::SR	ADDR::0x9801_331c
Name	Bits	R/W	Default	Commen	its	
Rvd	3117	-	-	-		
usb3_bist2_ls[1:0]	1615	R/W	2'h0	Pp SRAM	I LS value	
usb3_bist2_rm_1	1411	R/W	4'h0	SRAM5 l	RM value	
usb3_bist2_rme_1	10	R/W	'b0	SRAM5 RM enable		
usb3_bist2_rm_0	96	R/W	4'h0	SRAM4 l	RM value	
usb3_bist2_rme_0	5	R/W	'b0	SRAM4 l	RM enable	
usb3_drf_2_test_resume	4	W/R	'b0	USB3 DF	RF BIST2 trig	ger resume signal
usb3_drf_bist2_en	3	W/R	'b0	USB3 DF	RF BIST2 ena	ble
usb3_bist2_en	2	W/R	'b0	USB3 BIST2 enable		
Rvd	1	-	-	-		
usb3_bist2_test_mode	0	W/R	'b0	USB3 BI	ST2 test mode	e enable



1.41 REGISTER:: USB3_BIST1_STS

0x9801_3320

Module::usb Register::USB3_BIST1_STS			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3320	
Name	Bits	R/W	Default	t Comments			
Rvd	3111	-	-	-			
usb3_drf_bist1_fail_3	10	R	'b0	USB3 DRF	1 SRAM3 fa	il signal	
usb3_bist1_fail_3	9	R	'b0	USB3 BIST	1 SRAM3 fa	il signal	
usb3_drf_bist1_fail_2	8	R	'b0	USB3 DRF	1 SRAM2 fa	il signal	
usb3_bist1_fail_2	7	R	'b0	USB3 BIST	1 SRAM2 fa	il signal	
usb3_drf_bist1_fail_1	6	R	'b0	USB3 DRF	1 SRAM1 fa	il signal	
usb3_bist1_fail_1	5	R	'b0	USB3 BIST	'l SRAM1 fa	il signal	
usb3_drf_bist1_fail_0	4	R	'b0	USB3 DRF	1 SRAM0 fa	il signal	
usb3_bist1_fail_0	3	R	'b0	USB3 BIST	'1 SRAM0 fa	il signal	
usb3_drf_1_start_pause	2	R	'b0	USB3 DRF	1 start pause	signal	
usb3_drf_bist1_done	1	R	'b0	USB3 DRF	1 done		
usb3_bist1_done	0	R	'b0	USB3 BIST	1 done		

1.42 REGISTER:: USB3_BIST2_STS

0x9801_3324

Module:: usb Register::U	ISB3_BI	ST2_S	Set::1	ATTR::nor Type::SR ADDR::0x9801_3324
Name	Bits	R/W	Default	Comments
Rvd	317	-	-	
usb3_drf_bist2_fail_1	6	R	'b0	USB3 DRF2 SRAM5 fail signal
usb3_bist2_fail_1	5	R	'b0	USB3 BIST2 SRAM5 fail signal
usb3_drf_bist2_fail_0	4	R	'b0	USB3 DRF2 SRAM4 fail signal
usb3_bist2_fail_0	3	R	'b0	USB3 BIST2 SRAM4 fail signal
usb3_drf_2_start_pause	2	R	'b0	USB3 DRF2 start pause signal
usb3_drf_bist2_done	1	R	'b0	USB3 DRF2 done
usb3_bist2_done	0	R	'b0	USB3 BIST2 done

1.43 REGISTER:: USB3_APHY_REG

0x9801_3328

Module::usb Regist	er::USB3_APHY	_RE Set:	::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3328	
Name	Bits	R/W	Default	Default Comments		
Rvd	315	-	-	-		
usb3_clk_mode_sel	43	R/W	'b00	"11": Diff.	. 100MHz in, else	
V				CKIN_XT	AL in.	
				IN RL6227 .CKREF comes from		
				CKIN_XTAL, tie "00".		
usb3_ckbuf_en	2	R/W	'b0	CKREF Bu	uffer Enable tie 0	
usb3_mbias_en	1	R/W	'b1	Bias Circuit Enable.		
				1: Bias Circuit enable		
				0: Bias Circuit disable		
usb3_bg_en	0	R/W	'b0	Bandgap Enable. IN RL6227,no		
				BG inside	the USB3.0 block, tie 0	

1.44 REGISTER:: USB3_BC_STS2_REG

0x9801_332C

Module::usb	Register::USB3_BC_STS2_	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_332c
	REG				



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				A Substituti y of Reutier Group
Name	Bits	R/W	Default	Comments
Rvd	318	-	-	-
hst_prtbl_det_0_usb3	7	R	'b0	
hst_comp_out_0_usb3	6	R	'b0	Debug signal
hst_sh_out_0_usb3	5	R	'b0	Debug signal
hst_v0p07_out_0_usb3	4	R	'b0	DP>0.35V, output=low,
				DP<0.35V, output=high
hst_v0p41_out_0_usb3	3	R	'b0	DM>THD, output=low,
_				DM <thd, output="high</td"></thd,>
hst_v0p46_out_0_usb3	2	R	'b1	don't care. Output=high.
dev_chg_det_0_usb3	1	R	'b0	Detector result
dev_dcp_det_0_usb3	0	R	'b0	Detector result

1.45 REGISTER:: USB3_BC_CTL_REG

0x9801_3330

Module::usb Register::US	B3_BC_C	ΓL_ Set:	:1 ATTR::ctrl	Type::SR ADDR::0x9801_3330
REG				
Name	Bits	R/W	Default	Comments
Rvd	3115	-	-	-
LF_PD_R_en	14	R/W	'b1	
hst_pow_charge_0_usb3	13	R/W	'b0	Enable charge, high enable
hst_vdm_src_en_0_usb3	12	R/W	'b0	Enable VDM_SRC output, high enable
hst_idp_sink_en_0_usb3	11	R/W	'b0	Enable DP current sink, high enable
hst_app_div_en_0_usb3	10	R/W	'b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	'b0	Select Apple charge current
				2.1A/1A
				0: DP=2.0V, DM=2.7V
				1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_u	8	R/W	'b0	Enable comparator for detect
sb3				Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	'b0	Enable NOTE mode, high enable, DP=1.25V
hst_dcp_en_0_usb3	6	R/W	'b0	Enable DCP mode, high enable, short DP and DM.
dev_pow_charge_0_usb3	5	R/W	'b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb	4	R/W	'b0	0: select CHG_DET detect
3				1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	'b0	Enable DP output voltage, high
				enable
dev_vdm_src_en_0_usb3	2	R/W	'b0	Enable DM output voltage, high
				enable
dev_idp_sink_en_0_usb3	1	R/W	'b0	Enable DP current sink, high
				enable
dev_idm_sink_en_0_usb3	0	R/W	'b0	Enable DM current sink, high
				enable

1.46 REGISTER:: USB3_DUMMY_0_REG

Module::usb	Register::USB3_DUMMY_ 0_REG			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3334
Name Bits R/V		W	Default		Comments		
dummy_0 310 R/W		W	32'h0	Dummy re	gister,default:0		



1.47 REGISTER:: USB3_DUMMY_1_REG

0x9801_3338

Module::usb	Register::US 1_REG	SB3_DUMMY_		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3338
Nan	Name Bits R/		W	Default		Comments	
dummy_1		310 R/V		W 3	2'hFFFF_FFF	Dummy reg	gister,default:1
					F		

1.48 REGISTER:: USB3_LTSSM_STS

0x9801_333C

Module::usb	Register::USB3_LTSSM_S			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_333c
	TS						
Nan	ne	Bits R/		W	Default		Comments
Rvd		314	314 -		-	-	
Ltdb_sub_state	state 30 R			'b0	Ltssm sub-	state from USB3 IP	

1.49 REGISTER:: USB_PHY_CTRL

0x9801_3340

Module::usb	Register::US	B_PHY_C	TRL Set	::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3340
Nan	ne	Bits	R/W	Default		Comments
Rvd		316	-	-	-	
usb_ldo_en		52	R/W	'b0	U2phy0~U2	2phy3 ldo enable
usb3_isolate_n	nac2phy	10	R/W	'b0	isolate UPF	IY A → D

1.50 REGISTER:: USB_PWR_CTRL

0x9801_3344

Module::usb	Register::USB_PWR_CTR Set::			:1 ATTR::ctrl	Type::SR	ADDR::0x9801_3344
	L					
Nan	ne	Bits	R/W	Default		Comments
u3_det_time_v	al	3116	R/W	ʻhfa	u3_det_tim	ne_val
u2_det_time_v	al	159	R/W	ʻh3	u2_det_time_val	
u3_ip_clk_en		87	R/W	'h3	u3_ip_clk_en	
u3_ip_rstn		65	R/W	ʻh3	u3_ip_rstn	
mac_phy_pll_e	en	43	R/W	'h3	mac_phy_p	oll_en
u2_det_deboun	ice_en	2	R/W	'b0	u2_det_debounce_en	
recv_det_start_	hst	1	R/W	'b0	recv_det_start_hst	
recv_det_start_	drd	0	R/W	'b0	recv_det_s	tart_drd

1.51 REGISTER:: USB_PWR_STS

Module::usb	Register::US	B_PWR_S	TS	Set::1 ATTR::ctrl		Type::SR	ADDR::0x9801_3348
Nan	ne	Bits	R/V	W	Default		Comments
usb_pwr_ctrl_e	en	31	R/V	W	'h0	usb_pwr_c	trl_en
sw_reset_pwr_	fsm	3029	R/V	W	'h0	sw_reset_p	wr_fsm
rxterm_dly_en		28	R/V	W	ʻb1	rxterm_dly	_en
Rvd		2710	-		-	-	
recv_det_int_er	n_hst	9	R/V	W	'b0	recv_det_ii	nt_en_hst
recv_det_int_er	n_drd	8	R/V	W	'b0	recv_det_ii	nt_en_drd
Rvd		72	-		-	-	
recv_det_int_st	ts_hst	1	R/	W	'b0	recv_det_ii	nt_sts_hst
recv_det_int_st	ts_drd	0	R/	W	'b0	recv_det_ii	nt_sts_drd



1.52 REGISTER:: USB_TYPEC_CTRL_CC1_0 0x9801_334C

Module::usb Register::US RL_CC1_0	B_TYPEC	_CT Set:	:1 ATTR::ctrl	Type::SR ADDR::0x9801_334C
Name	Bits	R/W	Default	Comments
Rvd	3130	-	-	-
EN_SWITCH	29	R/W	'h0	En switch
Txout_sel	28	R/W	'h0	Txout_sel
Rxin_sel	27	R/W	'h0	Rxin_sel
Reg_cc1_rp4pk_code	2622	R/W	'h0	Reg_cc1_rp4pk_code
Reg_cc1_rp36k_code	2117	R/W	'h0	Reg_cc1_rp36k_code
Reg_cc1_rp12k_code	1612	R/W	'h0	Reg_cc1_rp12k_code
Reg_cc1_rd_code	117	R/W	'h0	Reg_cc1_rd_code
Reg_cc1_mode	65	R/W	'h0	Reg_cc1_mode
En_cc1_rp4p7k	4	R/W	'h0	En_cc1_rp4p7k
En_cc1_rp36k	3	R/W	'h0	En_cc1_rp36k
En_cc1_rp12k	2	R/W	'h0	En_cc1_rp12k
En_cc1_rd	1	R/W	'h0	En_ccl_rd
En_cc1_det	0	R/W	ʻh0	En_cc1_det

Module::usb Register::US RL_CC1_1	B_TYPEC	_CT Set:	::1 ATTR::ctrl	Type::SR ADDR::0x9801_3350
Name	Bits	R/W	Default	Comments
Rvd	3129		-	-
Reg_cc1_ vref_2p6v	2826	R/W	'h0	Reg_cc1_ vref_2p6v
Reg_cc1_ vref_1p23v	25.22	R/W	ʻh0	Reg_cc1_ vref_1p23v
Reg_cc1_ vref_0p8v	2118	R/W	'h0	Reg_cc1_ vref_0p8v
Reg_cc1_ vref_0p66v	1714	R/W	ʻh0	Reg_cc1_ vref_0p66v
Reg_cc1_ vref_0p4v	13.11	R/W	'h0	Reg_cc1_ vref_0p4v
Reg_cc1_vref_0p2v	108	R/W	'h0	Reg_cc1_vref_0p2v
Reg_cc1_ vref1_1p6v	74	R/W	'h0	Reg_cc1_ vref1_1p6v
Reg_cc1_vref0_1p6v	30	R/W	'h0	Reg_cc1_vref0_1p6v

1.54 REGISTER:: USB_TYPEC_CTRL_CC2_0 0x9801_3354

Module::usb Register::US RL_CC2_0	B_TYPEC	_CT Set:	:1 ATTR::ctrl	Type::SR ADDR::0x9801_3354
Name	Bits	R/W	Default	Comments
Rvd	3127	-	=	-
Reg_CC2_rp4pk_code	2622	R/W	'h0	Reg_CC2_rp4pk_code
Reg_CC2_rp36k_code	2117	R/W	'h0	Reg_CC2_rp36k_code
Reg_CC2_rp12k_code	1612	R/W	'h0	Reg_CC2_rp12k_code
Reg_CC2_rd_code	117	R/W	'h0	Reg_CC2_rd_code
Reg_CC2_mode	65	R/W	'h0	Reg_CC2_mode
En_CC2_rp4p7k	4	R/W	'h0	En_CC2_rp4p7k
En_CC2_rp36k	3	R/W	'h0	En_CC2_rp36k
En_CC2_rp12k	2	R/W	'h0	En_CC2_rp12k
En_CC2_rd	1	R/W	'h0	En_CC2_rd



En_CC2_det	0	R/W	ʻh0	En_CC2_det	

Module::usb	Register::US RL_CC2_1	B_TYPEC	_CT Set:	::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3358
Name	e	Bits	R/W	Default		Comments
Rvd		3129	-	-	-	
Reg_CC2_ vref_	_2p6v	2826	R/W	'h0	Reg_CC2_	vref_2p6v
Reg_CC2_ vref_	_1p23v	25.22	R/W	'h0	Reg_CC2_	vref_1p23v
Reg_CC2_ vref_	_0p8v	2118	R/W	'h0	Reg_CC2_	vref_0p8v
Reg_CC2_ vref_	_0p66v	1714	R/W	'h0	Reg_CC2_	vref_0p66v
Reg_CC2_ vref_	_0p4v	13.11	R/W	'h0	Reg_CC2_	vref_0p4v
Reg_CC2_vref_	0p2v	108	R/W	'h0 Reg_CC2_vref_0p2v		vref_0p2v
Reg_CC2_ vref	l_1p6v	74	R/W	'h0 Reg_CC2_vref1_1p6v		
Reg_CC2_vref0	_1p6v	30	R/W	'h0	Reg_CC2_	vref0_1p6v

1.56 REGISTER:: USB_TYPEC_STS

0x9801_335C

Module::usb	Register::USB_TYPEC_ST S			Set::1	ATTR::	nor	Type::SR	ADDR::0x9801_335C
Name Bits R/			R/	W	Default			Comments
Rvd		316	-					
cc2_det 53		RO	O	'h7 CC2_det				
cc1_det 20		RO	О	'h7		CC1_det		

1.57 REGISTER:: USB_TYPEC_CTRL

0x9801_3360

Module::usb Register::URL	SB_TYPEC	_CT Set:	ATTR::ctrl	Type::SR ADDR::0x9801_3360
Name	Bits	R/W	Default	Comments
Rvd	3112	1	-	-
cc2_det_int_en	11	R/W	'h0	cc2 det interrupt en
cc1_det_int_en	10	R/W	'h0	cc1 det interrupt en
cc2_det_int	9	R/W	'h0	cc2 det interrupt sts
cc1_det_int	8	R/W	'h0	cc1 det interrupt sts
cc_detect_time_value	71	R/W	ʻh3	debounce time scale
cc_det_debounce_en	0	R/W	ʻh1	cc detect debounce en

1.58 REGISTER:: USB_DBUS_PWR_CTRL 0x9801_3364

Module::usb	Register::USB_DBUS_PW R_CTRL			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3364
Nan	Name Bits R/			W	Default		Comments
Rvd		3112 -			-	-	
clk_en_gap		1110	R/V	W	'h0	00:50ns	
						01:300ns	
						10:500ns	
						11:1us	



sram_ls_gap	98	R/W	'h0	00:200ns
				01:300ns
				10:100ns
				11:500ns
Rvd	72	-	-	-
dbus_pwr_ctrl_sw_rst	1	R/W	'h0	dbus power ctrl software reset to
				idle
dbus_pwr_ctrl_en	0	R/W	'h0	dbus power ctrl enable

1.59 REGISTER:: USB3_HOST_WRAP_CTR_reg 0x9801_3C00

Module::usb Register:: USB3_HOS	T_WRAP_	CT Set::	1 ATTR::ctrl	Type::SR ADDR::0x9801_3C00	
Name	Bits	R/W	Default	Comments	
		K/ W	Deraun	Comments	
Rvd	317	-	-	-	
rxdetect_value	6	R/W	'b0		
rxdetect_sel	5	R/W	'b0		
resume_cycle_sel	4	R/W	'b0		
sram_debug_sel	3	R/W	'b0	Select sram	
				1: host	
				0: device	
sram_debug_mode	2	R/W	, p0	Enable sram debug mode	
dbus_multi_req_disable	1	R/W	'b0	Disable multiple request for Dbus	
				0: enable multiple request	
				1: disable multiple request	
dev_mode	_mode 0 R		'b0	Enable peek on AHB burst length	
				0: host (2)	
				1: host/dev	

1.60 REGISTER:: USB3_HOST_GNT_INT_reg 0x9801_3C04

Module::usb Register::USB3_HOST_GN R_INT			::1 ATTR::nor	Type::SR	ADDR::0x9801_3C04
Name	Name Bits R/		Default		Comments
Rvd	312	-	-	-	
device_int 1		R	'b0	USB3 Device MAC interrupt	
host_int 0		R	'b0	USB3 Host MAC interrupt	

1.61 REGISTER:: USB3_HOST_USB2_PHY_UTMI 0x9801_3C08

Module::	usb Register:: USB3_HOST UTMI	_USB2_PH		::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3C08
	Name	Bits	R/W	Default		Comments
Rvd		311	-	-	-	



reset_utmi_p0	0	R/W	'b0	UTMI reset to PHY0 (sync and
				automatically return to low)

1.62 REGISTER:: USB3_HOST_VSTATUS_port0_reg 0x9801_3C14

Module::usb	Register:: USB3_HOS7 _OUT	Γ_VSTATU	JS0	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C14
Nar	ne	Bits	R	/W	Default		Comments
Rvd	Rvd 318		-	-	-		
p0_vstatus_ou	p0_vstatus_out 70 R		/W	V 'h00 Vstatus output for port0 (It's		put for port0 (It's used to	
						configure P	HY's control register)

The process of configuring PHY control register:

3. write VSTATUS_reg (0x9801_3C14), (data output to PHY)

4. write GUSB2PHYAccn (p0:0x9803_1280)

[25]: vload [23]: vBusy [11:8]: vcontrol

[7:0]: vstatus_in (data input from PHY)



Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'b0	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. Note: This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. Note: These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address

The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.63 REGISTER:: USB3_HOST_SLP_BACK_EN_port0_reg 0x9801_3C18

Module::usb	Register::USB3 HOST SL	Set::1	ATTR::ctrl Type::SR	ADDR::0x9801 3C18



P_BACK0_1	EN			A substituty of Reutek Group		
Name	Bits	R/W	Default	Comments		
Rvd	314	-	-	-		
simulation_mode_p0	3	R/W	'b0	Port0 Reduce counter for entering		
				HS		
force_hs_mode_p0	2	R/W	'b0	Port0 Force HOST IP enter high		
				speed mode		
				0: disable		
				1: enable		
test_rst_p0	1	R/W	'b0	Port0 Self loop back reset		
test_en_p0	0	R/W	'b0	Port0 Self loop back enable		

1.64 REGISTER:: USB3_HOST_SLP_BACK_CTR_port0_reg 0x9801_3C1c

Module::usb	Register::			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C1c	
		SB3_HOST_SLP_BACK0_				71	_	
	CTR							
Na	me	Bits	R/V	V	Default		Comments	
Rvd		3112	-			-		
test_speed_p0		1110	R/V	V	'h0	When Self_	loop_back, force PHY	
						enter High	Speed or Full Speed	
						mode		
						(HS:	utmi_xver_select=0,	
						utmi_term_s	select[1:0]=00)	
						(FS:	utmi_x ver_select=1,	
						utmi_term_s	select[1:0]=01,	
						FsLsSerialN	Mode=0)	
						2'b01: force	PHY in HS	
						2'b10: force	PHY in FS/LS	
			•			2'b00/2'b11: normal mode		
test_seed_p0		92	R/V	V	'h0	Self_loop_b	oack	
						Random ger	nerator seed	
test_psl_p0		10	R/V	V	'h0	Select self_l	loop_back pattern	
						00: all zeros	1	
						01: load from	m seed	
						10: pseudo r	random pattern	
	•					11: incremen	ntal counter	

1.65 REGISTER:: USB3_HOST_SLP_BACK_ST_port0_reg 0x9801_3C20

Module::usb	USB3_HOST_SLP_BACK 0_ST		Set Set	::1 A	ATTR::nor	Type::SR	ADDR::0x9801_3C20
Nan	Name Bits		R/W		Default	Comments	
Rvd		312	-		-	1	



test_fail_p0	1	R	'b0	Port0 Self loop back fail
test_done_p0	0	R	'b0	Port0 Self loop back done

Slef_loop_back procedure:

(8) Configure PHY as self_loop_back mode (by vloadM interface)

		,				, ,			,		
R/W	38	F0	DBNC_E	DISCON_E	EN_ERR_UN	LATE_DL	INTG	SOP_KK	SLB_INNER	SLB_EN	
			N	NABLE	DERRUN	LEN					
			1	1	1	1	1	1	0: digital &	1	
									analog		
									1: digital only		

- (9) set test_psl, test_seed and test_speed
- (10) set test_rst=1 & test_en=0 (reset)
- (11) set test_rst=0 & test_en=0 (reset)
- (12) set test_rst=0 & test_en=1 (enable)
- (13) polling test_done
- (14) check test fail

Force MAC to enter High-Speed procedure:

- (4) In simulation mode: force_hs_mode=1 & simulation_mode=1
- (5) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation_mode=0
- (6) In normal mode: force_hs_mode=0 & simulation_mode=0

1.66 REGISTER:: USB3_HOST_PHY2_SLB0_EN_reg 0x9801_3C24

Module::usb Register:: USB3_HOS EN	T_PHY2_S	Set:	::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3C24	
Name	Bits	R/W	Default	ılt Comments		
Rvd	312	-	-	-		
p0_usb2phy_slb_hs	1	R/W	'b0	Usbphy port0 self loop back hs		
				mode		
p0_usb2phy_force_slb	0	R/W	'b0	Usbphy po	rt0 self loop back start	

1.67 REGISTER:: USB3_HOST_PHY2_SLB0_ST_reg 0x9801_3C28

Module::usb	Register::	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C28
	USB3_HOST_PHY2_SLB_				
	ST				



Name	Bits	R/W	Default	Comments
Rvd	312	-	-	-
p0_usb2phy_slb_fail	1	R	'b0	Usbphy port0 self loop back done
p0_usb2phy_slb_done	0	R	'b0	Usbphy port0 self loop back fail

1.68 REGISTER:: USB3_HOST_USB2_SPD_CTR 0x9801_3C2C

Module::usb	Register:: USB3_HOST_USB2_SPD _CTR ne Bits R/		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C2c	
Nan	Name		R/	W	Default		Comments
Rvd	312 -		-	-	-		
p0_suspend_r		0	R/	W	'b0	-	

1.69 REGISTER:: USB3_HOST_USB_DBG_reg 0x9801_3C40

Module::usb	Register::			:1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C40		
	USB3_HOS	T_USB_DI	BG						
Nam	ie	Bits	R/W		Default		Comments		
Rvd		3113			-	-			
dbg_sel1		127	R/W	1	'b0		oug signal sets to be		
						probed via	usb_dbg_out1		
dbg_sel0	dbg_sel0		R/W		'b0		Select debug signal sets to be		
						probed via	probed via usb_dbg_out0		
dbg_en		0	R/W		'b0		Debug enable		
							selected signals can be		
							debug ports. When clear,		
						both usb_	dbg_out0 and		
						usb_dbg_	out1 are static 16'h0.		

1.70 REGISTER: USB3_HOST_USB_STCH_reg 0x9801_3C44

Module::usb	Register:: USB3_HOST_USB_SCT CH			:1 ATTR::ctrl	Type::SR	ADDR::0x9801_3C44	
Nam	Name Bits		R/W	Default		Comments	
reg1	reg1 3116		R/W	'hffff	Dummy r	egister with value 1	
		R/W	'd0	Dummy r	egister with value 0		



1.71 REGISTER:: USB3_HOST_USB_TMP_SP_reg_0 0x9801_3C48

Module::usb	Register:: USB3_HOST P_SP	_USB_TM		ATTR::nor	Type::SR	ADDR::0x9801_3C48
Name		Bits	R/W	Default		Comments
test_sp_reg_0		310	R/W	'd0	Dummy tes	st register

1.72 REGISTER:: USB3_HOST_USB_TMP_SP_reg_1 0x9801_3C4C

Module::usb Register:: USB3_HOS7 P_SP	Register:: USB3_HOST_USB_TM P_SP		ATTR::nor	Type::SR ADDR::0x9801_3C48
Name	Bits	R/W	Default	Comments
test_sp_reg_1	310	R/W	'd0	Dummy test register

1.73 REGISTER:: USB3_HOST_USB_TMP_reg _2 0x9801_3C50

Module::usb	Register:: USB3_HOS	egister:: SB3_HOST_USB_ <mark>TMP</mark>			ATTR::	ctrl	Type::SR	ADDR::0x9801_3850
Name		Bits	R/W	41	Default			Comments
test_reg_2		310	R/W		'd0		Dummy tes	t register

1.74 REGISTER:: USB3_HOST_USB_TMP_reg_3 0x9801_3C5C

Module::usb Register:: USB3_H0	OST_USB_TN	Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3C5C
Name	Bits	R/W	Default		Comments
test_reg_3	310	R/W	'd0	Dummy tes	st register

1.75 REGISTER:: USB3_HOST_USB_HMAC_CTR0_reg 0x9801_3C60

Module::usb	Register:: USB3_HOS R0	USB3_HOST_HMAC_CT			ATTR::ctrl	Type::SR	ADDR::0x9801_3C60
Name		Bits	R/W		Default		Comments
Rvd		3130	-		-	-	
host_fladj_30n	nhz	2924	R	/W	'd32	-	
host_ppc_prese	ent	23	R	/W	'b0	-	
host_msi_enab	le	22	R	/W	'b0		
host_pm_pw_state_req		2120	R	/W	'b0		
hub_port_over	_current	1916	R	/W	'b0		



hub_port_perm_attach	1512	R/W	'b0	
host_u2_port_disable	119	R/W	'b0	
host_u3_port_disable	8	R/W	'b0	
host_num_u2_port	74	R/W	'd1	
host_num_u3_port	30	R/W	'd0	

1.76 REGISTER:: USB3_HOST_MAC3_HST_ST_reg 0x9801_3C64

Module::usb	Register:: USB3_HOST T_ST	_MAC3_H	S Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C64	
Na	me	Bits	R/W	Default	Comments		
Rvd		316	-	=	-		
host_current_power_state 54			R	'b0	Current xHC power state		
host_hub_vbus_ctrl 30			R	'b0	Vbus active	e indication	

1.77 REGISTER:: USB3_HOST_DMAC_CTR0_reg 0x9801_3C68

Module::usb	Register:: USB3_HOST_DMAC_CT R0			Set::	1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C68
Nam	Bits	R	/W		Default		Comments	
Rvd		3127		-	1	-	-	
host_xhc_bme		26	R	/W		ʻb1		
Rvd		253				<u>-</u>	-	
host_utmiotg_vl	20	R	/W		ʻh7			

1.78 REGISTER:: USB3_HOST_MAC3_DEV_ST_reg 0x9801_3C6C

Module::usb Register:: USB3_HOST V_ST	E Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3C6c	
Name	Bits	R/W	Default	Comments	
Rvd 312		-	=	-	
dev_current_power_state	10	R	'b0	Current xH	IC power state

1.79 REGISTER:: USB3_HOST_USB2_PHY_reg 0x9801_3C70

ľ	Module::usb	Register:: USB3_HOST_USB2_PHY			Set::1	ATTR::ct	rl Type::SR	ADDR::0x9801_3C70
	Name		Bits	R	/W	Default	(Comments



Rvd	3113	-	-	-
phy_pll_en	12	R/W	ʻb1	1:phy pll always on(for CR 480MHz)
p0_by_pass_on_1	11	R/W	'b0	Isolation A→D
p0_DmPulldown	10	R/W	'b0	Device = 1'b0
p0_DpPulldown	9	R/W	'b0	Device = 1'b0
p0_IDPULLUP	8	R/W	'b0	Device = 1'b0
Rvd	73	-	-	-
p0_DmPulldown_sel	2	R/W	'b0	p0_DmPulldown_sel ?
				p0_DmPulldown: 1'b0
p0_DpPulldown_sel	1	R/W	'b0	p0_DpPulldown_sel ?
				p0_DpPulldown: 1'b0
p0_IDPULLUP_sel	0	R/W	'b0	p0_IDPULLUP_sel ?
				p0_IDPULLUP: 1'b0

1.80 REGISTER:: USB3_HOST_USB_RAM_CTR_reg 0x9801_3C74

USB3_HOST_RAM_ CTR			Set::1	ATTR::nor_up	Type::SR ADDR::0x9801_3C	274
Name		Bits	R/W	Default	Comments	
Rvd		3117	-	-	-	
done_st	done_st		R/W	'b0	Write 1 to clear	
Rvd		151	-	-	7	
go_ct		0	R/W	6 0	Start DMA transfer, clear after of	done

1.81 REGISTER:: USB3_HOST_USB_RAM_ADDR_reg 0x9801_3C78

Module::usb Regis USB3	ter:: 8_HOST_RAM_A	Set:	:1 ATTR::ctrl	Type::SR	ADDR::0x9801_3C78
Name	Bits	R/W	Default		Comments
sram_addr	310	R/W	'd0		dress, 4-byte align. e for write/read bit

1.82 REGISTER:: USB3_HOST_USB_RAM_WDATA_reg 0x9801_3C87C

Module::usb	Register:: USB3_HOS TA	T_RAM_W	VDA	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3C87 C
Name Bi		Bits	R/W		Default	Comments	
ram_wdata 310 R/W		V	'd0	RAM write data to be write			



1.83 REGISTER:: USB3_HOST_RAM_RDATA_reg 0x9801_3C80

Module::usb	Register:: USB3_HOST ATA	Γ_RAM_RI		ATTR::nor_up	Type::SR	ADDR::0x9801_3C80	
Nan	Name Bits		R/W	Default	Comments		
ram_rdata	ram_rdata 310		R/W	'd0	USB read data to be read back		

1.84 REGISTER:: USB3_HOST_PHY0_ST_reg 0x9801_3C84

Module::usb	Register:: USB3_HOS	T_PHY0_S		et::1	ATTR::nor	Type::S	R AI	DDR::0x98	301_3C84
Name Bits R/V			R/W		Default		Co	mments	
Rvd		3119	-		-	-			
p0_count_num 180 R			R		'b0	USB3 F	PHY cou	unt numbei	r value

1.85 REGISTER:: USB3_HOST_OVR_CT_reg 0x9801_3C88

	Register::USB3_HOST_OV R_CT				ATTR::ctrl	Type::SR	ADDR::0x9801_3C88
Name		Bits	R/W		Default		Comments
Rvd		312	R/W		-	-	
phy3_lperiod		97	R/W		'd1	Connect to	PHY3
phy3_hperiod		64	R/W	7	'd3	Connect to	PHY3
phy3_last		32	R/W		'd2	Connect to	PHY3
host_ovr_current_	value	1	R/W		'b0		
host_ovr_current_	sel	0	R/W		'b0		

1.86 REGISTER:: USB3_HOST_SOFT_Reset 0x9801_3D00

Module::usb	Register:: USB3_HOST_SOFT_RES ET			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D00
Nan	Bits	R	/W	W Default C		Comments	
Rvd		313		-	-	-	
rstn_usb2_phy	rstn_usb2_phy1 2		R	/W	'b0	USB2 PHY1 reset for USB2 IP	
rstn_usb2_phy0 1 R		/W	'b0	USB2 PHY0 reset for USB2 IP			
rstn_usb2			R	/W	'b0	USB2 IP system reset	

1.87 REGISTER:: USB3_HOST_GBL_USB_CT 0x9801_3D04

Modulovush	Dogistor	Cat. 1	A TTDotrl	TymouCD	ADDR::0x9801 3D04
Module::usb	Register::	Sethi	ATTR::ctrl	Type::SR	ADDR::0x9801 3D04



USB3_HOS CT	T_GBL_U	SB_		A Substatury of Reattek Group
Name	Bits	R/W	Default	Comments
usb_mac_ctrl 310 R/		R/W	'd0	Register use for usb_mac_ctrl

1.88 REGISTER:: USB3_HOST_GBL_USB_ARB 0x9801_3D08

Module::usb	Register:: USB3_HOS ARB	3_HOST_GBL_USB_			ATTR::ctrl	Type::SR	ADDR::0x9801_3D08
Nan	Bits	R/W		Default	Comments		
Rvd		314		-			
dbus_robin_ena	able	3	R	/W	'b0		
cmd_full_number 21		R	/W	'd3			
dbus_arb_prior	dbus_arb_priority 0 R		R	/W	'b0		

1.89 REGISTER:: UNUSED 0x9801_3D0C

1.90 REGISTER:: USB3_HOST_OTG_STS 0x9801_3D10

Module::usb	Register::USB3_HOST_OTG			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3D10
	_STS				e		
Name		Bits	R/W	Default	Comment	S	
Rvd		311	-	-	-		
otg_interrupt		0	R	'b0	OTG inter	rupt from US	B3 MAC

1.91 REGISTER:: USB3_HOST_USB_BC_STS 0x9801_3D14

Module::usb	Registe USB3_ STS	er:: _HOST_U	SB_BC_	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3D14	
Name Bits R/W		Defau lt	Comments					
Rvd		312	-	-	-			
chirp_on		1	R	'b0	battery charg	ing chirp sign	al from USB3 MAC	
bc_interrupt		0	R	'b0	battery charging interrupt from USB3 MAC			



1.92 REGISTER:: USB3_HOST_BIST1_CTRL 0x9801_3D18 (IP sram)

Module::usb Register::	USB3_HC	OST_BIS	Set::1	ATTR::ctrl Type::SR ADDR::0x9801_3D18
T1_CTRI				
Name	Bits	R/W	Default	Comments
Rvd	3128	-	-	-
usb3_bist1_ls[2:0]	2725	R/W	3'h0	SRAM0~2 LS value
usb3_bist1_rm_3	2421	R/W	4'h0	SRAM3 RM value
usb3_bist1_rme_3	20	R/W	'b0	SRAM3 RM enable
usb3_bist1_rm_2	1916	R/W	4'h0	SRAM2 RM value
usb3_bist1_rme_2	15	R/W	'b0	SRAM2 RM enable
usb3_bist1_rm_1	1411	R/W	4'h0	SRAM1 RM value
usb3_bist1_rme_1	10	R/W	'b0	SRAM1 RM enable
usb3_bist1_rm_0	96	R/W	4'h0	SRAM0 RM value
usb3_bist1_rme_0	5	R/W	'b0	SRAM0 RM enable
usb3_drf_1_test_resume	4	W/R	'b0	USB3 DRF BIST1 trigger resume signal
usb3_drf_bist1_en	3	W/R	'b0	USB3 DRF BIST1 enable
usb3_bist1_en	2	W/R	'b0	USB3 BIST1 enable
Rvd	1	=	=	-
usb3_bist1_test_mode	0	W/R	'b0	USB3 BIST1 test mode enable

1.93 REGISTER:: USB3_HOST_BIST2_CTRL 0x9801_3D1c (PPsram)

Module::usb			Set::1	ΑΊ	TR::ctrl	Type::SR	ADDR::0x9801_3D1c			
	T2_CTRL									
Name		Bits	R/W	Defa	ult	Comme	Comments			
Rvd		3117	-	_		-				
usb3_bist2_ls[[1:0]	1615	R/W	2'h0		SRAM4	~5 LS value			
usb3_bist2_rm	1_1	1411	R/W	4'h0		SRAM5	RM value			
usb3_bist2_rm	ne_1	10	R/W	'b0		SRAM5 RM enable				
usb3_bist2_rm	1_0	96	R/W	4'h0		SRAM4	RM value			
usb3_bist2_rm	ne_0	5	R/W	'b0		SRAM4	RM enable			
usb3_drf_2_te	st_resume	4	W/R	'b0		USB3 D	RF BIST2 trig	ger resume signal		
usb3_drf_bist2	2_en	3	W/R	'b0		USB3 D	RF BIST2 ena	ble		
usb3_bist2_en		2	W/R	'b0		USB3 B	IST2 enable			
Rvd		1	-	-		=				
usb3_bist2_tes	st_mode	0	W/R	'b0		USB3 B	IST2 test mode	e enable		

Module::usb	Register::USB3_HOST_BIST1 _STS			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3D20	
Name Bits R/W		Default	Comments					
Rvd		3111	-	=	-	-		
usb3_drf_bist1_fail_3 10 R		'b0	USB3 DRI	USB3 DRF1 SRAM3 fail signal				
usb3_bist1_fail_3 9 R		'b0	USB3 BIST1 SRAM3 fail signal					



usb3_drf_bist1_fail_2	8	R	'b0	USB3 DRF1 SRAM2 fail signal
usb3_bist1_fail_2	7	R	'b0	USB3 BIST1 SRAM2 fail signal
usb3_drf_bist1_fail_1	6	R	'b0	USB3 DRF1 SRAM1 fail signal
usb3_bist1_fail_1	5	R	'b0	USB3 BIST1 SRAM1 fail signal
usb3_drf_bist1_fail_0	4	R	'b0	USB3 DRF1 SRAM0 fail signal
usb3_bist1_fail_0	3	R	'b0	USB3 BIST1 SRAM0 fail signal
usb3_drf_1_start_pause	2	R	'b0	USB3 DRF1 start pause signal
usb3_drf_bist1_done	1	R	'b0	USB3 DRF1 done
usb3_bist1_done	0	R	'b0	USB3 BIST1 done

1.95 REGISTER:: USB3_HOST_BIST2_STS 0x9801_3D24

	le:: usb Register::USB3_HOST_B IST2_STS			ATTR::nor Type::SR ADDR::0x9801_3D24
Name	Bits	R/W	Default	Comments
Rvd	317	-	=.	-
usb3_drf_bist2_fail_1	6	R	'b0	USB3 DRF2 SRAM5 fail signal
usb3_bist2_fail_1	5	R	'b0	USB3 BIST2 SRAM5 fail signal
usb3_drf_bist2_fail_0	4	R	'b0	USB3 DRF2 SRAM4 fail signal
usb3_bist2_fail_0	3	R	'b0	USB3 BIST2 SRAM4 fail signal
usb3_drf_2_start_pau	se 2	R	'b0	USB3 DRF2 start pause signal
usb3_drf_bist2_done	1	R	'b0	USB3 DRF2 done
usb3_bist2_done	0	R	'b0	USB3 BIST2 done

	Register::US STS2 REC		BC Set:	:1 ATTR::nor	Type::SR	ADDR::0x9801_3D2 C	
Name		Bits	R/W	Default		Comments	
Rvd		318	-	-	-		
hst_prtbl_det_0_u	usb3	7	R	'b0			
hst_comp_out_0_	_usb3	6	R	'b0	Debug sign	ıal	
hst_sh_out_0_ush	53	5	R	'b0	Debug signal		
hst_v0p07_out_0	_usb3	4	R	'b0	DP>0.35V, output=low,		
						, output=high	
hst_v0p41_out_0	_usb3	3	R	'b0		output=low,	
					DM <thd,< td=""><td>output=high</td></thd,<>	output=high	
hst_v0p46_out_0	_usb3	2	R	'b1	don't care. Output=high.		
dev_chg_det_0_u	ısb3	1	R	'b0	Detector result		
dev_dcp_det_0_u	ısb3	0	R	'b0	Detector re	sult	

1.97 REGISTER:: USB3_HOST_BC_CTL_REG 0x9801_3D30

Module::usb	Register::US _CTL_REG	ter::USB3_HOST_BC _REG			ATTR::ctrl	Type::SR	ADDR::0x9801_3D30
Nam	Bits	R/W		Default	Comments		
Rvd		3115	3115 -		-	-	
lf_pd_r_en_0_u	lf_pd_r_en_0_usb3 14		R/V	V	'b1		
hst_pow_charge_0_usb3		13	R/V	V	'b0	Enable charge, high enable	
hst_vdm_src_er	n_0_usb3	12	R/V	V	'b0	Enable VDM_SRC output, high	



				enable
			(1.0	*******
hst_idp_sink_en_0_usb3	11	R/W	'b0	Enable DP current sink, high
				enable
hst_app_div_en_0_usb3	10	R/W	'b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	'b0	Select Apple charge current
				2.1A/1A
				0: DP=2.0V, DM=2.7V
				1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_u	8	R/W	'b0	Enable comparator for detect
sb3				Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	'b0	Enable NOTE mode, high enable,
				DP=1.25V
hst_dcp_en_0_usb3	6	R/W	'b0	Enable DCP mode, high enable,
_				short DP and DM.
dev_pow_charge_0_usb3	5	R/W	'b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb	4	R/W	'b0	0: select CHG_DET detect
3				1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	'b0	Enable DP output voltage, high
_				enable
dev_vdm_src_en_0_usb3	2	R/W	'b0	Enable DM output voltage, high
				enable
dev_idp_sink_en_0_usb3	1	R/W	'b0	Enable DP current sink, high
_				enable
dev_idm_sink_en_0_usb3	0	R/W	'b0	Enable DM current sink, high
				enable

1.98 REGISTER:: USB3_HOST_DUMMY_0_REG 0x9801_3D34

Module::usb	Register::US	DU Set:	:1	ATTR::ctrl	Type::SR	ADDR::0x9801_3D34	
	MMY_0_RI	EG					
Name Bits		R/W		Default		Comments	
dummy_0		310	R/W		32'h0	Dummy reg	gister,default:0

1.99 REGISTER:: USB3_HOST_DUMMY_1_REG 0x9801_3D38

Module::usb	Register MMY_	r::US 1_RI	B3_HOST_DU EG		Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3D38
Nam	Name Bits R/		W	Default	Comments			
dummy_1		/	310	R/	W	32'hFFFF_FFF	Dummy reg	gister,default:1
						F		

1.100 REGISTER:: USB3_HOST_USB_DBUS_PWR_CTRL 0x9801_3D60

Module::usb	_	egister:: SB3_HOST_USB_DBUS WR_CTRL			ATTR::ctrl	Type::SR	ADDR::0x9801_3D60
Name Bits R/V			R/W	V	Default Comments		
Rvd		3112 -			-	-	
clk_en_gap		R/W	V	'h0	00:50ns		
						01:300ns	



				10:500ns
				11:1us
sram_ls_gap	98	R/W	'h0	00:200ns
				01:300ns
				10:100ns
				11:500ns
Rvd	72	-	=	-
dbus_pwr_ctrl_sw_rst	1	R/W	'h0	dbus power ctrl software reset to
				idle
dbus_pwr_ctrl_en	0	R/W	ʻh0	dbus power ctrl enable

3.6 1.1 1 D			Set::1	A TOTO (1	T
Module::usb Register::				ATTR::ctrl	Type::SR ADDR::0x9801_3E00
USB3_U3_	HOST_WR	AP_			
CTR					
Name	Bits	R/	W	Default	Comments
Rvd	317	-		-	-
rxdetect_value	6	R/	W	'b0	
rxdetect_sel	5	R/	W	'b0	•
resume_cycle_sel	4	R/	W	'b0	
sram_debug_sel	3	R/	W	'b0	Select sram
					1: host
					0: device
sram_debug_mode	2	R/	W	,p0	Enable sram debug mode
dbus_multi_req_disable	1	R/	W	'b0	Disable multiple request for Dbus
_					0: enable multiple request
			7		1: disable multiple request
dev_mode	0	R/	W	'b0	Enable peek on AHB burst length
					0: host (2)
					1: host/dev

1.102 REGISTER:: USB3_U3_HOST_GNT_INT_reg 0x9801_3E04

Module::usb	Register::USB3_U3_HOST _GNR_INT			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E04
Name		Bits	R/W		Default	Comments	
Rvd	Rvd 312		-		-	-	
device_int		1	R		'b0	USB3 Device MAC interrupt	
host_int		0	R		'b0	USB3 Host MAC interrupt	

Module::usb	Register::	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E08
	USB3_U3_HOST_USB2_PH				
	Y_UTMI				



Name	Bits	R/W	Default	Comments
Rvd	311	-	-	-
reset_utmi_p0	0	R/W	'b0	UTMI reset to PHY0 (sync and
				automatically return to low)

1.104 REGISTER:: USB3_U3_HOST_PHY_PIPE 0x9801_3E0c

Module::usb	Register::USB3_U3_HOST _PHY_PIPE		OST	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E0c
Name		Bits	R/W	7	Default	Comments	
Rvd		311	-		-	-	
reset_pipe3_p0		0	R/W		'b0	PIPE3 reset to PHY1 (sync and	
						automatica	lly return to low)

1.105 REGISTER:: USB3_U3_HOST_MDIO_CTR_reg 0x9801_3E10

Module::usb Register:: USB3_U3_HOST_MDIO_C TR		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E10		
Name	Bits	R/W		Default	Comments		
data	3116	R/W		'h0	Write data or read data.		
phy_addr	1513	R/W		'd0	MDIO PHY	addressing value.	
phy_reg_addr	128	R/W		'd0	MDIO Register addressing value		
mdio_busy	7	R/W		'd0	-		
mdio_st	65	R/W		'd0	MDIO host controller state Monitor		
mdio_rdy	4	R/W		'd0	MDIO Pre-a	amble signal Monitor	
mclk_rate	32	R/W		'd0	MDIO clock rate selection:		
					2'b00: clk_s		
					2'b01: clk_sys/16		
					2'b10: clk_s	sys/8	
					2'b11: clk_sys/4		
mdio_srst	mdio_srst 1			'd0	Assert 1'b1 to do soft reset		
mdio_rdwr	0	R/W		'd0	1'b0: read, 1'b1: write		

1.106 REGISTER:: USB3_U3_HOST_VSTATUS_port0_reg 0x9801_3E14

Module::usb	Register:: USB3_U3_HOST_VSTAT US0_OUT			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E14
Name		Bits	R/W		Default	Comments	
Rvd	Rvd 318		-		-	-	
p0_vstatus_out		70	R/W		'h00	Vstatus output for port0 (It's used to	
						configure P	HY's control register)



The process of configuring PHY control register:

5. write VSTATUS_reg (0x9801_3E14), (data output to PHY)

6. write GUSB2PHYAccn (p0:0x981F_8280)

[25]: vload [23]: vBusy [11:8]: vcontrol

[7:0]: vstatus_in (data input from PHY)

Field	Description	Reset	Access
25	New Register Request (NewRegReq) The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.	1'b0	R_WS_SC
24	VStatus Done (VStsDone) The core sets this bit when the vendor control access is done. The core clears this bit when the application sets the New Register Request bit (bit 25).	1'60	R_SS_SC
23	VStatus Busy (VStsBsy) The core sets this bit when the vendor control access is in progress and clears this bit when done.	1'b0	RU
22	Register Write (RegWr) The application sets this bit for register writes and clears it for register reads. Note: This bit is applicable for ULPI register read/write access only.	1'b0	R_W
21:16	Register Address (RegAddr) The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. Note: These bits are applicable for ULPI only.	6'h0	R_W
15:8	Vendor Control Register Address (VCtrl)/Extended Register Address (ExtRegAddr) ■ UTMI+ interface: Vendor Control Register Address (VCtrl) This field contains the 4-bit register address, and the vendor-defined 4-bit parallel output bus. Bits [11:8] of this field are also placed on bits [3:0] of the utmi_vcontrol output signal. ■ ULPI interface: Extended Register Address (ExtRegAddr) This field contains the 8-bit PHY-extended register address.	8'h0	R_W
7:0	Register Data (RegData) UTMI interface: This field contains the data on utmi_vstatus bus, when VStatus Done is set. ULPI interface: This field contains the write data for ULPI register write. It contains the read data for ULPI register read, valid when VStatus Done is set.	8'h0	R_W

3. polling [23]: vBusy, if [23]=0, then vstatus_in is valid

Example for RealTek PHY:

Vcontrol[3]: low/high address, 0: low, 1: high

Vcontrol[2:0]: address



The control address in RealTek PHY is 6 bits, so it needs to send 2 vcontrol address. For example, vcontrol=1110 (high address) and 0000 (low address) means 110000=0x30.

1.107 REGISTER:: USB3_U3_HOST_SLP_BACK_EN_port0_reg 0x9801_3E18

Module::usb	Register::US _SLP_BAC	SB3_U3_HOST K0_EN		::1 ATTR::ctr	:l Type::SR ADDR::0x9801_3E18	
Nan	ne	Bits	R/W	Default	Comments	
Rvd		314	-	-	-	
simulation_mo	simulation_mode_p0		R/W	'b0	Port0 Reduce counter for entering	
	_				HS	
force_hs_mode	_p0	2	R/W	'b0	Port0 Force HOST IP enter high	
					speed mode	
					0: disable	
					1: enable	
test_rst_p0		1	R/W	'b0	Port0 Self loop back reset	
test_en_p0		0	R/W	'b0 Port0 Self loop back enable		

1.108 REGISTER:: USB3_U3_HOST_SLP_BACK_CTR_port0_reg 0x9801_3E1c

Module::usb	Register:: USB3_U3_He K0_CTR	OST_SLP_I	Set:	:1 AT	TR::ctrl	Type::SR	ADDR::0x9801_3E1c	
Na	me	Bits	R/W	Def	ault		Comments	
Rvd		3112	-		=	-		
		11.,10	R/W	'h0		When Self_loop_back, force PHY enter High Speed or Full Speed mode (HS: utmi_xver_select=0, utmi_term_select[1:0]=00) (FS: utmi_xver_select=1, utmi_term_select[1:0]=01, FsLsSerialMode=0) 2'b01: force PHY in HS 2'b10: force PHY in FS/LS 2'b00/2'b11: normal mode		
test_seed_p0	test_seed_p0 92		R/W	'ł	10	Self_loop_ Random ge	back enerator seed	
test_psl_p0 10		R/W	'h0		Select self_loop_back pattern 00: all zeros 01: load from seed 10: pseudo random pattern 11: incremental counter			

1.109 REGISTER:: USB3_U3_HOST_SLP_BACK_ST_port0_reg 0x9801_3E20

Module::usb	Register:: USB3_U3_HOST_SLP_BA CK0_ST			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E20
Name Bits R/V		W	Default Comments		Comments		
Rvd		312	-		-	-	
test_fail_p0 1 R			'b0	Port0 Self loop back fail			
test_done_p0 0 R			'b0	'b0 Port0 Self loop back done			

Slef_loop_back procedure:

(15) Configure PHY as self_loop_back mode (by vloadM interface)

R/W	38	F0	DBNC_E	DISCON_E	EN_ERR_UN	LATE_DL	INTG	SOF	KK	SLB_INNER	SLB_EN	
			N	NABLE	DERRUN	LEN						
			1	1	1	1	1		1	0: digital &	1	
										analog		
										1: digital only		

- (16) set test_psl, test_seed and test_speed
- (17) set test_rst=1 & test_en=0 (reset)
- (18) set test rst=0 & test en=0 (reset)
- (19) set test_rst=0 & test_en=1 (enable)
- (20) polling test_done
- (21) check test_fail

Force MAC to enter High-Speed procedure:

- (7) In simulation mode: force_hs_mode=1 & simulation_mode=1
- (8) In non-simulation mode (don't reduce counter): force_hs_mode=1 & simulation mode=0
- (9) In normal mode: force hs mode=0 & simulation mode=0

Module::usb	Register:: USB3_U3_HOST_PHY2_S LB_EN			Set::	1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E24
Nan	Name Bits R/		W		Default	Comments		
Rvd		312	-			-	-	
p0_usb2phy_slb_hs		1	R/W			'b0	Usbphy port0 self loop back hs mode	



p0_usb2phy_force_slb	0	R/W	'b0	Usbphy port0 self loop back start

Module::usb	Register:: USB3_U3_H LB_ST	HOST_PHY	Z2_S Set	::1 ATTR::nor	Type::SR	ADDR::0x9801_3E28	
Nan	Name Bits R/V		R/W	Default	Comments		
Rvd		312	-	-	-		
p0_usb2phy_slb_fail 1 R		R	'b0	Usbphy port0 self loop back done			
p0_usb2phy_slb_done 0 R		R	'b0	Usbphy por	rt0 self loop back fail		

1.112 REGISTER:: USB3_U3_HOST_USB2_SPD_CTR 0x9801_3E2C

Module::usb	USB3_U3_HOST_USB2_ SPD_CTR			Set::1	ATTR	ctrl	Тур	pe::SR	ADDR::0x9801_3E2c
Nam	ne	Bits	R/	W	Defau	lt			Comments
Rvd		312	-	-	-		1		
p0_suspend_r		0	R/	W	'b0		7	>	

1.113 REGISTER:: USB3_U3_HOST_SLB_EN_reg 0x9801_3E30

Module::usb Register: USB3_U LB EN	:: J3_HOST_PHY	Set:	:1 ATTR::ctrl	Type::SR	ADDR::0x9801_3E30	
Name	Bits	R/W	Default		Comments	
Rvd	313	-	-	-		
p0_pipe_bist_sel 21		R/W	'b0	Self loop back select:		
				00:counter		
				01:tseq		
				10:ts1		
*				11:ts2		
p0_pipe_bist_en	0	R/W	'b0	Self loop b	ack enable	

Module::usb	Register:: USB3_U3_H _SLB_CT	OST_PHY3		ATTR::nor_up	Type::SR	ADDR::0x9801_3E34
Name Bits		R/W	Default		Comments	
Rvd		311	-	-	-	



				A Substituty of Rediter Group
p0_usb3phy_slb_go	0	R/W	'b0	Usb3phy port0 self loop back start
				transfer

Module::usb	Register:: USB3_U3_H _SLB_ST	HOST_PHY	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E38	
Name Bits		R/W	Default	Comments			
Rvd		312	-	=	-		
p0_usb3phy_sl	b_fail	1	R	'b0	Usb3phy port0 self loop back done		
p0_usb3phy_slb_done		0	R	'b0	Usb3phy port0 self loop back		
					mode		

1.116 REGISTER:: USB3_U3_HOST_USB_DBG_reg 0x9801_3E40

Module::usb Register:: USB3_U3_U DBG	USB3_U3_HOST_USB_			Type::SR ADDR::0x9801_3E40
Name	Bits	R/W	Default	Comments
Rvd	3113	-	-	-
dbg_sel1	127	R/W	'b0	Select debug signal sets to be probed via usb_dbg_out1
dbg_sel0	61	R/W	'b0	Select debug signal sets to be probed via usb_dbg_out0
dbg_en 0		R/W	'b0	Debug enable When set, selected signals can be probed via debug ports. When clear, both usb_dbg_out0 and usb_dbg_out1 are static 16'h0.

1.117 REGISTER:: USB3_U3_HOST_USB_STCH_reg 0x9801_3E44

Module::usb	Register:: USB3_U3_I SCTCH	HOST_USE	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E44
Nam	Name Bits		R/W	Default		Comments
reg1		3116	R/W	'hffff	Dummy register with value 1	
reg0 150 F		R/W	'd0	Dummy re	egister with value 0	



1.118 REGISTER:: USB3_U3_HOST_USB_TMP_SP_reg _0 0x9801_3E48

Module::usb Register:: USB3_U3_H TMP_SP	USB3_U3_HOST_USB_ TMP_SP		ATTR::nor	Type::SR ADDR::0x9801_3E48		
Name	Bits	R/W	Default	Comments		
test_sp_reg_0	3112	R/W	'd0	Dummy test register		
int_inact_status	11	R/W	'd0	ltssm change to ss inactive state		
int_ss_dis_status	10	R/W	'd0	ltssm change to ss disabled state		
int_hreset_status	9	R/W	'd0	ltssm change to hot reset state		
int_recov_status	8	R/W	'd0	Itssm change to recovery state		
int_rx_det_status	7	R/W	'd0	ltssm change to rx detect state		
int_poll_status	6	R/W	'd0	ltssm change to polling state		
int_u3_status	5	R/W	'd0	ltssm change to u3 state		
int_u2_status	4	R/W	'd0	ltssm change to u2 state		
int_u1_status	3	R/W	'd0	ltssm change to u1 state		
int_u0_status	2	R/W	'd0	ltssm change to u0 state		
int_loopbk_status	1	R/W	'd0	ltssm change to loopback state		
int_comp_status	0	R/W	'd0	Itssm change to compliance state		

1.119 REGISTER:: USB3_U3_HOST_USB_TMP_SP_reg_1 0x9801_3E4C

Module::usb	Register:: USB3_U3_HOST_USB_ TMP_SP		- Se	et::1	АТ	TR::nor	Type::SR	ADDR::0x9801_3E48
Name Bits		R/	W		Default		Comments	
test_sp_reg_1	st_sp_reg_1 310		R/	W		'd0	Dummy test register	

Module::usb Register USB3_UMP	: 3_HOST_USE	Set:::	3 ATTR::ctrl	Type::SR	ADDR::0x9801_3850
Name	Bits	R/W	Default		Comments
test_reg_2	310	R/W	'd0	Dummy tes	st register

1.121 REGISTER:: USB3_U3_HOST_USB_TMP_reg_3 0x9801_3E5C

Module::usb	Register::			Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3E5C
	USB3_U3_HOST_USB_T						
	MP						
Name Bits R			R/W	V	Default	Comments	
test_reg_3		3113	R/W	V	'd0	Dummy test register	
int_inact_en 12 R		R/W	V	'd0	Itssm change to ss inactive state		
						interrupt er	able



R/W 'd0 int_ss_dis_en 11 ltssm change to ss disable state interrupt enable int_hreset_en 10 R/W 'd0 ltssm change to hot reset state interrupt enable int_recov_en 9 R/W 'd0 Itssm change to recovery state interrupt enable R/W 'd0 ltssm change to rx detect state int_rx_det_en 8 interrupt enable 7 ltssm change to polling state int_poll_en R/W 'd0 interrupt enable int_u3_en R/W 'd0 ltssm change to u3 state interrupt 6 enable ltssm change to u2 state interrupt int_u2_en 5 R/W 'd0 enable R/W 4 'd0 Itssm change to ul state interrupt int_u1_en enable R/W Itssm change to u0 state interrupt int_u0_en 3 'd0 enable 2 R/W 'd0 ltssm change to loopback state int_loopbk_en interrupt enable 1 R/W 'd0 Itssm change to compliance state int_comp_en interrupt enable 0 Rvd

Module::usb Register:: USB3_U3_I CTR0	HOST_HM	AC Set::	1 ATTR::ctrl	Type::SR	ADDR::0x9801_3E60
Name	Bits	R/W	Default		Comments
Rvd	3130	-	-	-	
host_fladj_30mhz	2924	R/W	'd32	-	
host_ppc_present	23	R/W	'b0	-	
host_msi_enable	22	R/W	'b0		
host_pm_pw_state_req	2120	R/W	'b0		
hub_port_over_current	1916	R/W	'b0		
hub_port_perm_attach	1512	R/W	'b0		
host_u2_port_disable	119	R/W	'b0		
host_u3_port_disable	8	R/W	'b0		
host_num_u2_port	74	R/W	'd1		
host_num_u3_port	30	R/W	'd1		

Module::usb	Register:: USB3_U3_H _HST_ST	OST_MAC	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3E64
N	ame Bits		R/W	Default		Comments



Rvd	316	-	-	-
host_current_power_state	54	R	'b0	Current xHC power state
host_hub_vbus_ctrl	30	R	'b0	Vbus active indication

1.124 REGISTER:: USB3_U3_HOST_DMAC_CTR0_reg 0x9801_3E68

Module::usb	USB3_U3_HOST_DMAC _CTR0			Set::	1 ATT	R::ctrl	Type::SR	ADDR::0x9801_3E68	
Nam	ne	Bits R			Def	ault	Comments		
Rvd		3127		-		-	-		
host_xhc_bme		26	26 R/V		'l	1			
Rvd		253		-		-	-		
host_utmiotg_v	busvalid	20	20 R/		'1	n7			

1.125 REGISTER:: USB3_U3_HOST_MAC3_DEV_ST_reg 0x9801_3E6C

Module::usb Register:: USB3_U3_H DEV_ST	OST_MAC	3_ Set::1	ATTR::nor	Type::SR ADDR::0	0x9801_3E6c
Name	Bits	R/W	Default	Commen	ts
Rvd 312		-	-	-	
dev_current_power_state	dev_current_power_state 10		'b0	Current xHC power st	tate

Module::usb Register:: USB3_U3_I PHY	USB3_U3_HOST_USB2_		1 ATTR::ct	rl Type::SR ADDR::0x9801_3E70	
Name	Bits	R/W	Default	Comments	
Rvd	3113	-	-	-	
phy_pll_en	12	R/W	'b1	1:phy pll always on(for CR 480MHz)	
p0_by_pass_on_1	11	R/W	'b0	Isolation A→D	
p0_DmPulldown	10	R/W 'b0		Device = 1'b0	
p0_DpPulldown	9	R/W	'b0	Device = 1'b0	
p0_IDPULLUP	8	R/W	'b0	Device = 1'b0	
Rvd	73	-	-	-	
p0_DmPulldown_sel	2	R/W	'b0	p0_DmPulldown_sel ?	
				p0_DmPulldown: 1'b0	
p0_DpPulldown_sel	1	R/W	'b0	p0_DpPulldown_sel ?	
				p0_DpPulldown: 1'b0	
p0_IDPULLUP_sel	0	R/W	'b0	p0_IDPULLUP_sel ?	
				p0_IDPULLUP: 1'b0	



1.127 REGISTER:: USB3_U3_HOST_USB_RAM_CTR_reg 0x9801_3E74

Module::usb	Register::		Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E874		
	USB3_U3_HOST_R							
	AM_CTR							
Nar	ne	Bits	R/W	Default		Comments		
Rvd		3117	-	-	-			
done_st		16	R/W	'b0	Write 1 to	Write 1 to clear		
Rvd		151	-	-	-			
go_ct 0		R/W	'b0	Start DM	A transfer, clear after done			

1.128 REGISTER:: USB3_U3_HOST_USB_RAM_ADDR_reg 0x9801_3E78

Module::usb	Register:: USB3_U3_HOST_RAM_ ADDR			Set::1	ATTR::ctrl	Type::SR ADDR::0x9801_3E78
Nam	Name Bits F		R/	W	Default	Comments
sram_addr		310	R/	W	'd0	SRAM address, 4-byte align.
						Bit[0]= use for write/read bit
						0: read
						1: write

1.129 REGISTER:: USB3_U3_HOST_USB_RAM_WDATA_reg 0x9801_3E87C

Module::usb	Register: USB3_U DATA		T_RA		t::1 ATTR::ctrl	Type::SR	ADDR::0x9801_3E87 C
Nam	ne	I	Bits	R/W	Default		Comments
ram_wdata		3	10	R/W	'd0	RAM write	data to be write

1.130 REGISTER:: USB3_U3_HOST_RAM_RDATA_reg 0x9801_3E80

Module::usb	Register:: USB3_U3_F _RDATA	IOST_RAM	Set::1	ATTR::nor_up	Type::SR	ADDR::0x9801_3E80
Name Bits		R/W	Default	Comments		
ram_rdata		310	R/W	'd0	USB read d	ata to be read back



USB3_U3_I T	HOST_PHY	70_S		A sunsuaury of Reuter Group
Name	Bits	R/W	Default	Comments
Rvd	3119	-	-	-
p0_count_num	180	R	'b0	USB3 PHY count number value

Module::usb Register: _OVR_C	:USB3_U3_H T	OST Se	t::1 ATTR::ctrl	Type::SR ADDR::0x9801_3E88
Name	Bits	R/W	Default	Comments
Rvd	312	R/W	-	-
phy3_lperiod	97	R/W	'd1	Connect to PHY3
phy3_hperiod	64	R/W	'd3	Connect to PHY3
phy3_last	32	R/W	'd2	Connect to PHY3
host_ovr_current_value	current_value 1 R/W 'b0		'b0	
host_ovr_current_sel	0	R/W	'b0	

1.133 REGISTER:: USB3_U3_HOST_SOFT_Reset 0x9801_3F00

Module::usb	Register:: USB3_U3_HOST_SOFT_ RESET				1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F00	
Nam	Name Bits R			W	1	Default	Comments		
Rvd		313				-	-		
rstn_usb2_phy1	1	2	R	/W		b0 USB2 PHY1 reset for USB2 IP		'1 reset for USB2 IP	
rstn_usb2_phy0 R		R	W 'b0		'b0	USB2 PHY0 reset for USB2 IP			
rstn_usb2 0 R/		W		'b0	USB2 IP sy	/stem reset			

1.134 REGISTER:: USB3_U3_HOST_GBL_USB_CT 0x9801_3F04

Module::usb	Register:: USB3_U3_H SB_CT	HOST_GBI	U Set	::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F04
Nam	ne	Bits	R/W		Default		Comments
usb_mac_ctrl		310	R/W		'd0	Register us	e for usb_mac_ctrl

1.135 REGISTER:: USB3_U3_HOST_GBL_USB_ARB 0x9801_3F08

Module::usb	Register::	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F08
	USB3_U3_HOST_GBL_U				
	SB_ARB				



Name	Bits	R/W	Default	Comments
Rvd	314	-		
dbus_robin_enable	3	R/W	'b0	
cmd_full_number	21	R/W	'd3	
dbus_arb_priority	0	R/W	'b0	

1.136 REGISTER:: UNUSED 0x9801 3F0C

Module::usb	Iodule::usb Register::USB3_U3_HOST_ OTG_STS			Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3F10
Name		Bits	R/W	Default	Comment	s	
Rvd		311	-	-	-		
otg_interrupt		0	R	'b0	OTG inter	rupt from US	B3 MAC

Module::usb Register:: USB3_U3_HOST_USB_ BC_STS			r_usb_	Set::1	ATTR::nor Type::SR ADDR::0x9801_3F14				
Name	Name Bits R/W			Defau lt	Comments				
Rvd		312	-	-	-				
chirp_on		1	R	,p0	battery charging chirp signal from USB3 MAC				
bc_interrupt		0	R	'b0	battery charging interrupt from USB3 MAC				

1.139 REGISTER:: USB3_U3_HOST_BIST1_CTRL 0x9801_3F18 (IP sram)

Module::usb	Register:: BIST1_C		_HOST_	Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F18	
Name		Bits	R/W	Default	Comments			
Rvd		3128	-	-	-			
usb3_bist1_ls[2	2:0]	2725	R/W	3'h0	SRAM0~2 L	S value		
usb3_bist1_rm	_3	2421	R/W	4'h0	SRAM3 RM value			
usb3_bist1_rme	e_3	20	R/W	'b0	SRAM3 RM	enable		
usb3_bist1_rm	_2	1916	R/W	4'h0	SRAM2 RM	value		
usb3_bist1_rme	e_2	15	R/W	'b0	SRAM2 RM	enable		
usb3_bist1_rm	_1	1411	R/W	4'h0	SRAM1 RM	value		
usb3_bist1_rme	usb3_bist1_rme_1		R/W	'b0	SRAM1 RM enable			
usb3_bist1_rm	_0	96	R/W	4'h0	SRAM0 RM	value		
usb3_bist1_rm	e_0	5	R/W	'b0	SRAM0 RM	enable		



usb3_drf_1_test_resume	4	W/R	'b0	USB3 DRF BIST1 trigger resume signal
usb3_drf_bist1_en	3	W/R	'b0	USB3 DRF BIST1 enable
usb3_bist1_en	2	W/R	'b0	USB3 BIST1 enable
Rvd	1	-	-	-
usb3_bist1_test_mode	0	W/R	'b0	USB3 BIST1 test mode enable

1.140 REGISTER:: USB3_U3_HOST_BIST2_CTRL 0x9801_3F1c (PPsram)

Module::usb	fodule:: usb Register::USB3_U3 BIST2_CTRL		ST_	Set::1	Set::1 AT		Type::SR	ADDR::0x9801_3F1c
Name		Bits	R/W	Defa	ult	Comme	nts	
Rvd		3117	-	-		-		
usb3_bist2_ls[1:0]	1615	R/W	2'h0		SRAM4	~5 LS value	
usb3_bist2_rm	_1	1411	R/W	4'h0		SRAM5	RM value	
usb3_bist2_rm	e_1	10	R/W	'b0		SRAM5	RM enable	
usb3_bist2_rm	_0	96	R/W	4'h0		SRAM4	RM value	
usb3_bist2_rm	e_0	5	R/W	'b0		SRAM4	RM enable	
usb3_drf_2_tes	st_resume	4	W/R	'b0		USB3 D	RF BIST2 trig	ger resume signal
usb3_drf_bist2	en .	3	W/R	'b0		USB3 D	RF BIST2 ena	ble
usb3_bist2_en		2	W/R	'b0		USB3 B	IST2 enable	
Rvd		1	-	-		\mathbf{A}		
usb3_bist2_tes	t_mode	0	W/R	'b0		USB3 B	IST2 test mode	e enable

_	SB3_U3_HO	ST_BI	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3F20
ST1_STS						
Name	Bits	R/W	Default	Comments	S	
Rvd	3111	-	-	-		
usb3_drf_bist1_fail_3	10	R	'b0	USB3 DRI	F1 SRAM3 fai	l signal
usb3_bist1_fail_3	9	R	'b0	USB3 BIS	Γ1 SRAM3 fa	il signal
usb3_drf_bist1_fail_2	8	R	'b0	USB3 DRI	F1 SRAM2 fai	l signal
usb3_bist1_fail_2	7	R	'b0	USB3 BIS	Γ1 SRAM2 fa	il signal
usb3_drf_bist1_fail_1	6	R	'b0	USB3 DRI	F1 SRAM1 fai	l signal
usb3_bist1_fail_1	5	R	'b0	USB3 BIS	Γ1 SRAM1 fa	il signal
usb3_drf_bist1_fail_0	4	R	'b0	USB3 DRI	F1 SRAM0 fai	l signal
usb3_bist1_fail_0	3	R	'b0	USB3 BIS	Γ1 SRAM0 fa	il signal
usb3_drf_1_start_pause	2	R	'b0	USB3 DRI	F1 start pause	signal
usb3_drf_bist1_done	1	R	'b0	USB3 DRI	F1 done	
usb3_bist1_done	0	R	'b0	USB3 BIS'	Γ1 done	

Module::usb	Register::USB3_U3_HOS	Set::1	ATTR::nor	Type::SR	ADDR::0x9801_3F24



T_BIST2_STS				A Saconnary of Actives Group
Name	Bits	R/W	Default	Comments
Rvd	317	-	-	-
usb3_drf_bist2_fail_1	6	R	'b0	USB3 DRF2 SRAM5 fail signal
usb3_bist2_fail_1	5	R	'b0	USB3 BIST2 SRAM5 fail signal
usb3_drf_bist2_fail_0	4	R	'b0	USB3 DRF2 SRAM4 fail signal
usb3_bist2_fail_0	3	R	'b0	USB3 BIST2 SRAM4 fail signal
usb3_drf_2_start_pause	2	R	'b0	USB3 DRF2 start pause signal
usb3_drf_bist2_done	1	R	'b0	USB3 DRF2 done
usb3_bist2_done	0	R	'b0	USB3 BIST2 done

	Iodule::usb Register::USB3_U3_HOST _APHY_REG		Set::1	ATTR::ctrl		Type::SR	ADDR::0x9801_3F28
Name	Bits	R/V	W	Default		Comments	
Rvd	315	-		-		-	
usb3_clk_mode_sel	43	R/V	W	'b00		"11" : Diff	. 100MHz in, else
						CKIN_XTAL in.	
						IN RL6227 CKREF comes from	
						CKIN_XTAL, tie "00".	
usb3_ckbuf_en	2	R/V	W	'b0		CKREF Buffer Enable tie 0	
usb3_mbias_en	1	R/V	W	'b1		Bias Circuit Enable.	
						1: Bias Circuit enable	
						0: Bias Cir	cuit disable
usb3_bg_en	0	R/V	W	,p0		Bandgap Enable. IN RL6227,no	
						BG inside	the USB3.0 block, tie 0

1.144 REGISTER:: USB3_U3_HOST_BC_STS2_REG 0x9801_3F2C

Module::usb Register::US _BC_STS2		OST Set:	:1 ATTR::nor	Type::SR ADDR::0x9801_3F2C		
Name	Bits	R/W	Default	Comments		
Rvd	318	-	-	-		
hst_prtbl_det_0_usb3	7	R	'b0			
hst_comp_out_0_usb3	6	R	'b0	Debug signal		
hst_sh_out_0_usb3	5	R	'b0	Debug signal		
hst_v0p07_out_0_usb3	4	R	'b0	DP>0.35V, output=low,		
				DP<0.35V, output=high		
hst_v0p41_out_0_usb3	3	R	'b0	DM>THD, output=low,		
				DM <thd, output="high</td"></thd,>		
hst_v0p46_out_0_usb3	2	R	'b1	don't care. Output=high.		
dev_chg_det_0_usb3	1	R	'b0	Detector result		
dev_dcp_det_0_usb3	0	R	'b0	Detector result		

1.145 REGISTER:: USB3_U3_HOST_BC_CTL_REG 0x9801_3F30

Module::usb	_	Register::USB3_U3_HOST _BC_CTL_REG		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F30
Name		Bits	R/	W	Default	Comments	
Rvd	Rvd 3115 -				-	-	
lf_pd_r_en_0_usb3 14		R/	W	'b1			



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hst_pow_charge_0_usb3	13	R/W	'b0	Enable charge, high enable
hst_vdm_src_en_0_usb3	12	R/W	'b0	Enable VDM_SRC output, high
				enable
hst_idp_sink_en_0_usb3	11	R/W	'b0	Enable DP current sink, high
				enable
hst_app_div_en_0_usb3	10	R/W	'b0	Enable Apple mode, high enable
hst_app_div_sel_0_usb3	9	R/W	'b0	Select Apple charge current
				2.1A/1A
				0: DP=2.0V, DM=2.7V
				1: DP=2.7V, DM=2.0V
hst_dcp_app_comp_en_0_u	8	R/W	'b0	Enable comparator for detect
sb3				Apple/DCP mode, high enable
hst_note_div_en_0_usb3	7	R/W	'b0	Enable NOTE mode, high enable,
				DP=1.25V
hst_dcp_en_0_usb3	6	R/W	'b0	Enable DCP mode, high enable,
				short DP and DM.
dev_pow_charge_0_usb3	5	R/W	'b0	Enable charger, high enable
dev_dcp_chg_mode_0_usb	4	R/W	'b0	0: select CHG_DET detect
3				1: select DCP_DET detect
dev_vdp_src_en_0_usb3	3	R/W	'b0	Enable DP output voltage, high
				enable
dev_vdm_src_en_0_usb3	2	R/W	'b0	Enable DM output voltage, high
				enable
dev_idp_sink_en_0_usb3	1	R/W	'b0	Enable DP current sink, high
_				enable
dev_idm_sink_en_0_usb3	0	R/W	'b0	Enable DM current sink, high
				enable

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	Module::usb	Register::US	SB3_U3_HOST		Set::	1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F34
		DUMMY	0_REG						
	Nan	ne	Bits	R/	W		Default		Comments
	dummy 0		310	R/	W	32'h0		32'h0 Dummy register,default:0	

1.147 REGISTER:: USB3_U3_HOST_DUMMY_1_REG 0x9801_3F38

Module::usb	Register::US _DUMMY_		OST Set	t::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F38
Name		Bits	R/W		Default	Comments	
dummy_1	dummy_1		R/W 32		hFFFF_FFF	Dummy register,default:1	
					F		

1.148 REGISTER:: USB3_U3_HOST_LTSSM_STS 0x9801_3F3C

Module::usb	Register::US _LTSSM_S		OST Set	::1 AT	R::nor	Type::SR	ADDR::0x9801_3F3C
Name		Bits	R/W	Def	ault	Comments	
Rvd		314	-			-	
Ltdb_sub_state		30	R	'b	0	Ltssm sub-state from USB3 IP	



1.149 REGISTER:: USB3_U3_HOST_USB_DBUS_PWR_CTRL 0x9801_3F60

Module::usb	Register:: USB3_U3_HOST_USB_D BUS_PWR_CTRL		Set::1	ATTR::ctrl	Type::SR	ADDR::0x9801_3F60	
Name		Bits	R/W		Default	Comments	
Rvd		3112			-		
clk_en_gap		1110	R/W		'h0	00:50ns	
						01:300ns	
						10:500ns	
						11:1us	
sram_ls_gap		98	R/W		'h0	00:200ns	
						01:300ns 10:100ns	
						11:500ns	
Rvd		72	-		=	-	
dbus_pwr_ctrl_sw_rst		1	R/	W	'h0	dbus power ctrl software reset to	
						idle	
dbus_pwr_ctrl_en		0	R/	W	'h0	dbus power ctrl enable	