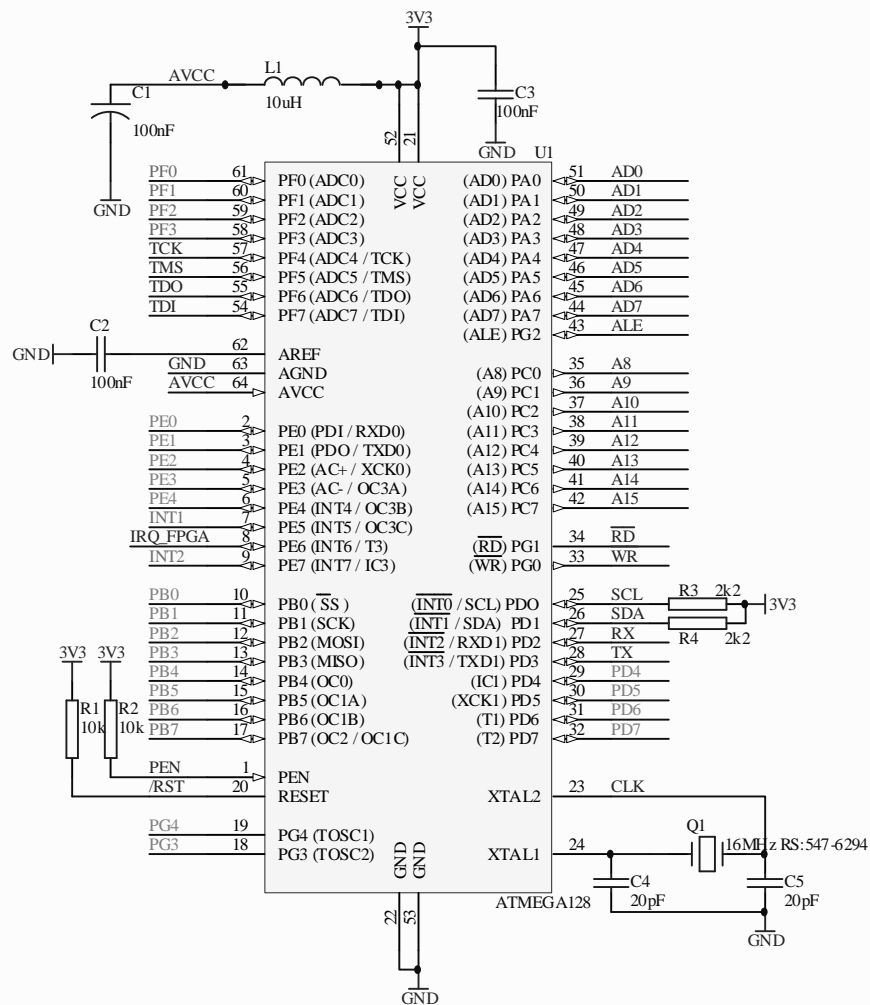
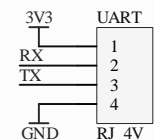
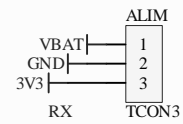


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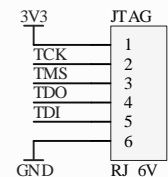
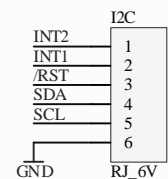
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134	13	134	14
136	15	136	16
139	17	139	18
143	19	143	20
3	21	3	22
7	23	7	24
9	25	9	26

UNIOC\_NG\_FPGA1



UNIOC_uC			
PD7	1	PD7	PD6
PD5	3	PD5	PD4
TX	5	TX	RX
SDA	7	SDA	SCL
/RST	9	RST	PG3
PB7	11	PB7	PB6
PB5	13	PB5	PB4
PB3	15	PB3	PB2
PB1	17	PB1	PB0
INT2	19	INT2	IRQ_FPGA
INT1	21	INT1	PE7
PE3	23	PE3	PE4
PE1	25	PE1	PE2
PEN	27	PEN	PE0
PF1	29	PF1	PF2
PF3	31	PF3	PF0
3V3	33	3V3	BAT

UNIOC\_NG\_uC



UNIOC_F2			
1	NC	NC	2
3	NC	NC	4
5	NC	NC	6
104	7	104	NC
99	9	99	103
96	11	96	100
93	13	93	97
91	15	91	94
89	17	89	92
87	19	87	90
79	21	79	88
74	23	74	86
25	NC	73	NC

UNIOC\_NG\_FPGA2

Title		
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