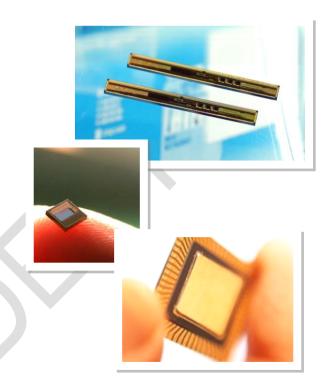
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RM67162 Data Sheet

Single Chip Driver with 16.7M color for 480RGBx480 OLED driver

Revision: 0.0

Date : May 16, 2016



Revision History

Version No.	Date	Description	Page	Modified By	Checked By
0.0	2016/03/07	First Release		Howard Hsiung	
	2016/05/16	Add RAD_ACL[1:0] function	101	Howard Hsiung	
		Add DA00,DB00,DC00 description	119~121	Howard Hsiung	
		Add CMD_READKEY[3:0] function	122	Howard Hsiung	



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1. General Description

The RM67162 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 400RGBx400, 360RGBx480, 320RGBx320, 320RGBx480, 272RGBx480, 240RGBx240, 240RGBx320, 180RGBx360, 180RGBx540, 128RGBx432with internal GRAM. It includes a 5,529,600 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The RM67162 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The RM67162 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 480-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for wearable device applications, including I-watch and smart band.

2. Features

■ Single chip AMOLED controller/driver with display RAM

Display resolution option

- 480RGB x 480 with 480x24-bits x 480 GRAM
- 400RGB x 400 with 400x24-bits x 400 GRAM
- > 360RGB x 480 with 360x24-bits x 480 GRAM
- 320RGB x 320 with 320x24-bits x 320 GRAM
- > 320RGB x 480 with 320x24-bits x 480 GRAM
- 272RGB x 480 with 272x24-bits x 480 GRAM
- 240RGB x 240 with 240x24-bits x 240 GRAM
- 240RGB x 320 with 240x24-bits x 320 GRAM
- 180RGB x 360 with 180x24-bits x 360 GRAM
- 180RGB x 540 with 180x24-bits x 540 GRAM
- > 128RGB x 432 with 128x24-bits x 432 GRAM

■ Display data RAM (frame memory): 480 x480 x 24-bits = 5,529,600 bits

■ Display mode (Color mode)

- Full color mode: 16.7M-colors
- ▶ Idle mode: 16.7M-colors, 4096-colors, 8-colors

■ Interface

- 8-bits 80-series MPU interface
- Serial peripheral interface (SPI)
- > Dual serial peripheral interface (Dual-SPI)
- MIPI Display Serial Interface (1 clock and 2 data lane pairs)
 - Support 1lane/2lane (1lane: 500Mbps)
 - Maximum total bit rate is 500Mbps of 2 data lanes 24-bit data format/ 360Mbps of 2 data lanes 18-bit data format/ 320Mbps of 2 data lanes 16-bit data format

Abundant color display and drawing functions

- Programmable y-correction function for 16.7 million color display
- Individual gamma correction setting for RGB dots
- Partial display function

■ Sunlight readable

■ Control power IC by one-wire interface

On chip

- VREFP5/VREFN5 voltage generator for panel voltage
- VGHR/VGLR voltage for gate control signal
- Internal oscillator for display clock
- Source output MUX 1-6 with 240ch source output pins
- Supports gate control signals to gate driver in the panel

Built-in OTP function to adjust panel setting

- Logic / interface power supply voltage VDDI = 1.65V ~ 3.3V
- Analog power supply voltage VDD = 2.7V ~ 3.6V



Output voltage levels

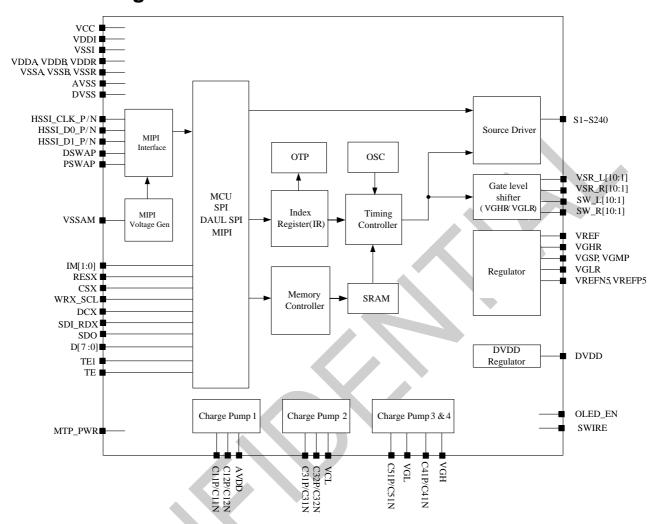
- Positive gate driver voltage range for VGHR: 3 ~ 10.5V
- Negative gate driver voltage range for VGLR: -2V ~ -15V
- VREFP5 panel voltage range : 0~5V
- VREFN5 panel voltage range : -0.5~-5V
- Step-up 1,2 output voltage range for AVDD: 4.5 ~ 6.5V, VCL: -3.5 ~ -5.0V
- Gamma high/low voltage range for VGMP: 2.0V ~ 6.0V (Max<=AVDD-0.5v) , VGSP: 0V, 0.3V ~ 4.5V</p>
- Package: COF/COG
- Chip size evaluation: 8300um x 2360um(including scribe line)



■ Power Supply Specifications

No.	Item		Description
1	Source Driver		240 pins (480 x RGB)
2	gate control timing Le	vel shift	VGHR-VGLR
5	Input Voltage	VDDI	1.65 ~ 3.3V
		VCC	Connect to VDDI or VDD(VCI)
		VDD (VDDA/VDDB/VDDR)	2.70 ~ 3.60V
6	OLED drive voltages	AVDD	4.5V ~ 6.5V
		VGHR	3V ~ 10.5V
		VGLR	-2V ~ -15V
		VREFP5	0V ~ 5V
		VREFN5	-0.5V ~ -5V
7	Internal step-up circuits	AVDD	VCI x2.0(dual), x3.0(single)
	onound	VCL	VCI x -1.0(dual), x-2.0(single)
		VGH	VCI x2, x3, x4
		VGL	VCI x-2, x-3, x-4

3. Block Diagram



Interface

The RM67162 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the y correction register. The RM67162 displays 16.7M colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

Timing Generating

The timing controller generates timing signals for internal circuits such as the display timing.

Oscillator

The RM67162 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The OLED display driver circuit consists of 240 source drivers (S1~S240). The gate signal consists of VSR_R/L[1:10], SW_R/L[1:10] and outputs either VGHR or VGLR level.



4. Pin Description

4.1 Power Supply Pins

4.1 Power Supp	<i>,</i> ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
Signal	I/O	Function
VDDB	Р	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	Р	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	Р	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDDI	Р	Power supply for interface system except MIPI interface
VCC	Р	Power supply for DVDD regulator
VSSB	Р	System ground for DC/DC converter
VSSA	Р	System ground for analog system
VSSR	Р	System ground for regulator system
VSSAM	Р	System ground for internal MIPI analog system
VSSI	Р	System ground for interface system except MIPI interface
DVSS	Р	System ground for internal digital system
AVSS	Р	System ground for source OP system.
MTP_PWR	Р	MTP programming power supply pin (7.5V typical) Must be left open or connected to DVSS in normal condition.



4.2 Interface Pins

Signal	I/O	Function
CSX	ı	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F.
		If not used, please connect to VSSI.
		WRX : Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F.
WRX_SCL	'	SCL: A synchronous clock signal in SPI I/F.
		If not used, please connect to VSSI.
		Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F.
D/CX	1	D/CX = "0" : Command
		D/CX = "1" : Display data or Parameter
		If not used, please connect to VSSI.
ODL DDV	1/0	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal.
SDI_RDX	I/O	RDX : Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface.
		If not used, please leave it Open.
		Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal.
SDO	0	If the host places the SDI line into high-impedance state during the read interval, the SDI and
		SDO can be tied together.
		If not used, please open this pin.
D[7:0]	I/O	8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F.
[]		These pins are not used for SPI, MIPI, please leave it Open.



4.3 MIPI Interface Pins

I/O	Function						
I							
I/O							
I/O							
	Pin Name	ect HSSI_D0 HSSI_D0_P	D/D1 data lan	e sequence HSSI_CLK_ P	and polarity i HSSI_CLK_ N	n high speed	HSSI_D1_N
	DSWAP=0 PSWAP=0	DSI D0+	DSI D0-	DSI CLK+	DSI CLK-	DSI D1+	DSI D1-
ı	DSWAP=0 PSWAP=1	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+
	DSWAP=1 PSWAP=0	DSI D1+	DSI D1-	DSI CLK+	DSI CLK-	DSI D0+	DSI D0-
	DSWAP=1 PSWAP=1	DSI D1-	DSI D1+	DSI CLK-	DSI CLK+	DSI D0-	DSI D0+
		-If not used, pl I/O -These pins ar -If not used, pl I/O -These pins ar -If not used, pl Input pin to sel Pin Name DSWAP=0 PSWAP=0 PSWAP=1 DSWAP=1 PSWAP=0 DSWAP=1 PSWAP=1	-If not used, please connect I/O -These pins are DSI-D0+/If not used, please connect I/O -These pins are DSI-D1+/If not used, please connect Input pin to select HSSI_D0 Pin Name HSSI_D0_P DSWAP=0 DSI PSWAP=0 DO- DSWAP=1 D0- DSWAP=1 DSI PSWAP=0 DSI PSWAP=1 D1- DSWAP=1 DSI PSWAP=1 D1-	-If not used, please connect these pins and I/O -These pins are DSI-D0+/- differential deliferential	-If not used, please connect these pins to VSSAM. I/O -These pins are DSI-D0+/- differential data signals if -If not used, please connect these pins to VSSAM. I/O -These pins are DSI-D1+/- differential data signals if -If not used, please connect these pins to VSSAM. Input pin to select HSSI_D0/D1 data lane sequence Pin Name	-If not used, please connect these pins to VSSAM. I/O -These pins are DSI-D0+/- differential data signals if MIPI interface -If not used, please connect these pins to VSSAM. I/O -These pins are DSI-D1+/- differential data signals if MIPI interface -If not used, please connect these pins to VSSAM. Input pin to select HSSI_D0/D1 data lane sequence and polarity in the pin Name HSSI_D0_P HSSI_D0_N HSSI_CLK_P HS	I/O

NOTE: "1" = VDDI level, "0" = VSSI level.



4.4 Interface Logic Pins

Signal	I/O	Function				
RESX	-	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.				
IM[1:0]	ı	Interface type selection. The connections of IM[1:0] which not shown in table are invalid. IM[1:0] Display Data Command				
BSTM	I	Boost mode selection pin. BSTM Mode 2 PWR(VDDI, VCI) 0 AVDD> internal CP VCL> internal CP				
TE	0	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.				
TE1	0	If not used, please open this pin.				
SWIRE	0	Swire protocol setting pin of Power IC, If not used, please open this pin.				
OLED_EN	0	Power IC enable control pin, If not used, please open this pin.				

NOTE: "1" = VDDI level, "0" = VSSI level.



4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S240	0	Pixel electrode driving output.
SDMY	0	Dummy Source, leave it Open.
VSR_L[10:1] VSR_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)
SW_L[10:1] SW_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)



4.6 DC/DC Convert Pins

Signal	I/O	Function
AVDD (DDVDH)	0	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
VCL	0	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	0	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	0	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N C12P, C12N	Ю	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	Ю	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	Ю	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	Ю	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitor as requirement.
VGHR	0	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	0	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	0	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	0	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VREF	0	Regulator output for internal reference voltage. Connect capacitor for stabilization.
DVDD	0	Regulator output for logic system power. Connect a capacitor for stabilization.
VREFP5	0	Regulator output for VREFP(0~5V)
VREFN5	0	Regulator output for VREFP(-0.5~-5V)



4.7 Test Pins

Signal	I/O	Function
ANALOG_TEST 1~2	0	Test pin, not accessible to user. Must be left open.
TEST1~3	Ю	Test pin, not accessible to user. Must be left open.
TESTEN	ı	Test pin, not accessible to user. Must be left open., Internal pull low
EXTCLK	I	Test pin, not accessible to user. Must be left open.
DUMMY	I	Dummy PAD, leave it open



5. Function Description

5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / Quad -SPI	MIPI / Quad -SPI
11	MCU 8-bit	MCU 8-bit





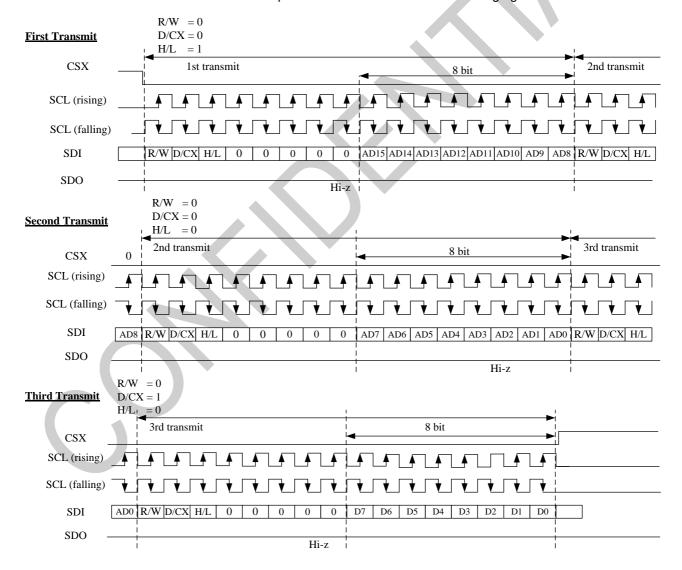
5.2 16-Bit Serial Interface

5.2.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The 16-Bit SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The 16-Bit SPI interface write command sequences are described in the following figure.



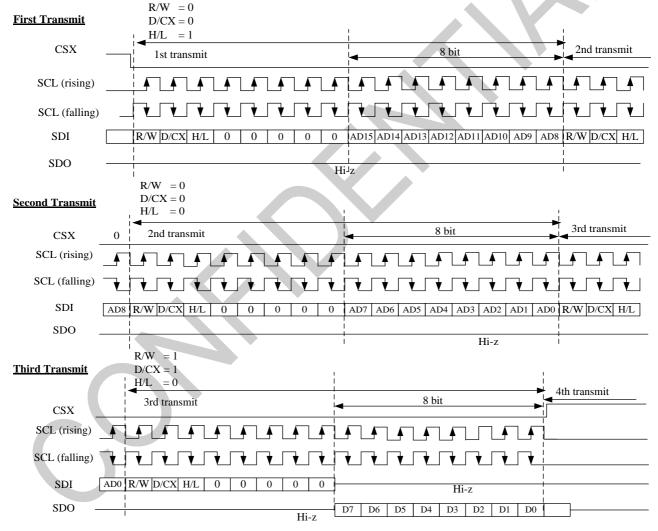


5.2.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The 16-Bit SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The 16-Bit SPI interface read command sequences are described in the following figure.





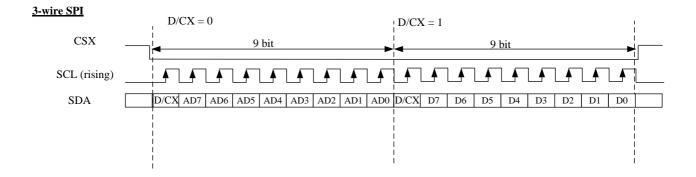
5.3 3-wire/4-wire SPI Interface

5.3.1 Write Cycle and Sequence

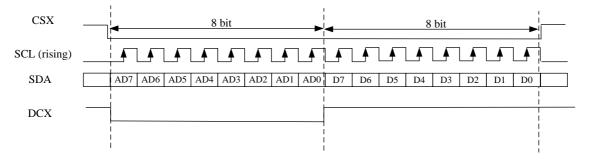
During a write cycle the host processor sends a single bit of data to the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX bit is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface write command sequences are described in the following figure.



4-wire SPI





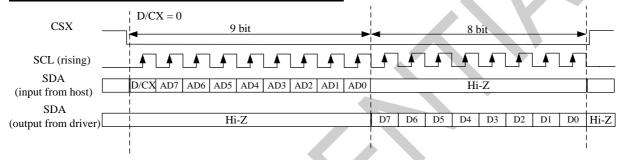
5.3.2 Read Cycle and Sequence

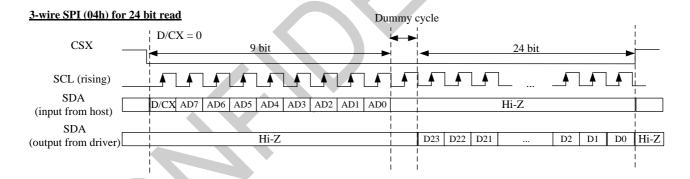
During a read cycle the host processor reads a single bit of data from the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface read command sequences are described in the following figure.

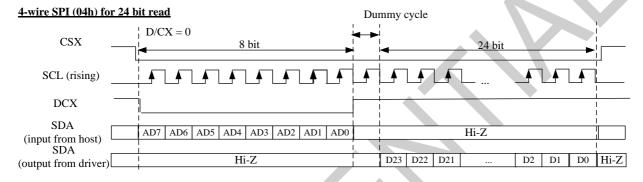
3-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read







4-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read D/CX = 0CSX 8 bit 8 bit SCL (rising) DCX SDA AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 Hi-Z (input from host) SDA Hi-Z D6 D5 D4 D3 D2 D1 D0 Hi-Z D7 (output from driver)

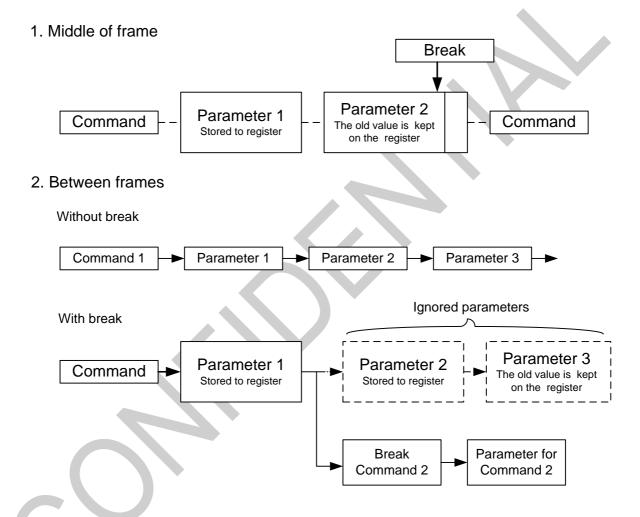




5.3.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.



Break can be e.g. another command or noise pulse.



5.4 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM67162 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller.

The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

RM67162 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

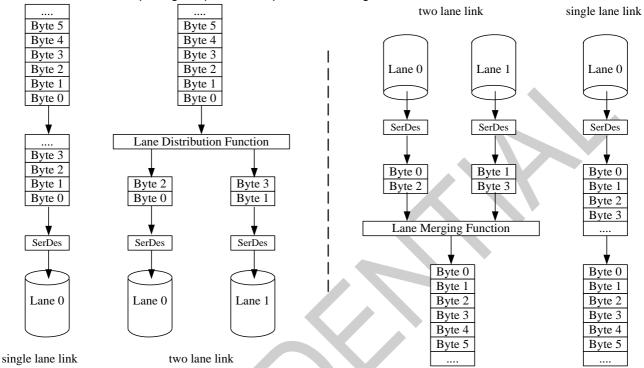
RM67162 Configuration:

ACIOI II	
Lane Pair	MCU(Master) RM67162(Slave)
Clock Lane	Unidirectional Lane
	Clock only
Data Lane 0	Bi-directional Lane
	Forward High-speed
	Bi-directional Escape Mode
	Bi-directional LPDT
Data Lane 1	Unidirectional Lane
	Forward High-Speed
	Escape Mode
	No LPDT



5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

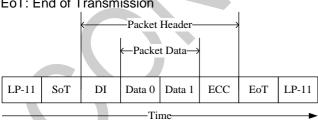


There are two kinds of packets, short packet and long packet.

Short packet structure: LP-11: low power mode

SoT: start of transmission
DI: data identification
Data 0, Data1: packet data

ECC: error correction code EoT: End of Transmission





DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

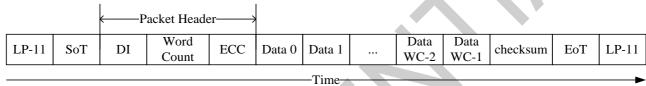
Long packet structure: LP-11: low power mode SoT: start of transmission DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission





5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type	Description	Packet
	binary		Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6	Long
		Format	
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long



Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM67162 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

DCS commands

DCS short write command

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

DCS read commands

The commands are used to request data from s display module.

DCS Long Write / write_LUT command

The commands are used to send larger blocks of data to a display module.

Maximum return packet size

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Null Packet

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

Blanking Packet

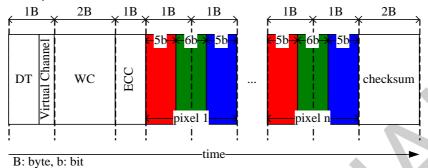
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

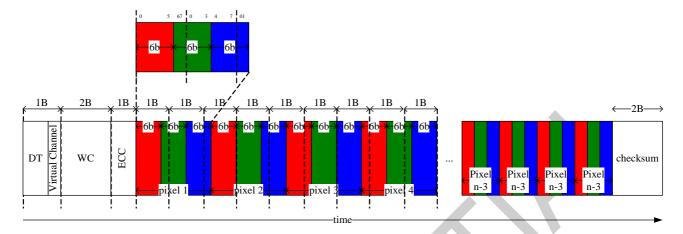
The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.





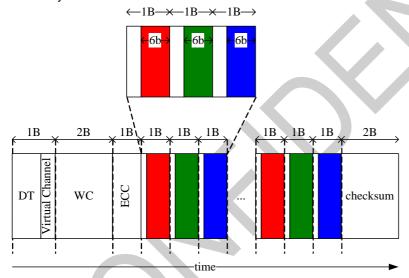
Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



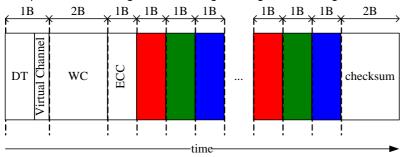
Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.





Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.





5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor. Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.

Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.



5.3.4 Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved



5.3.5 Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

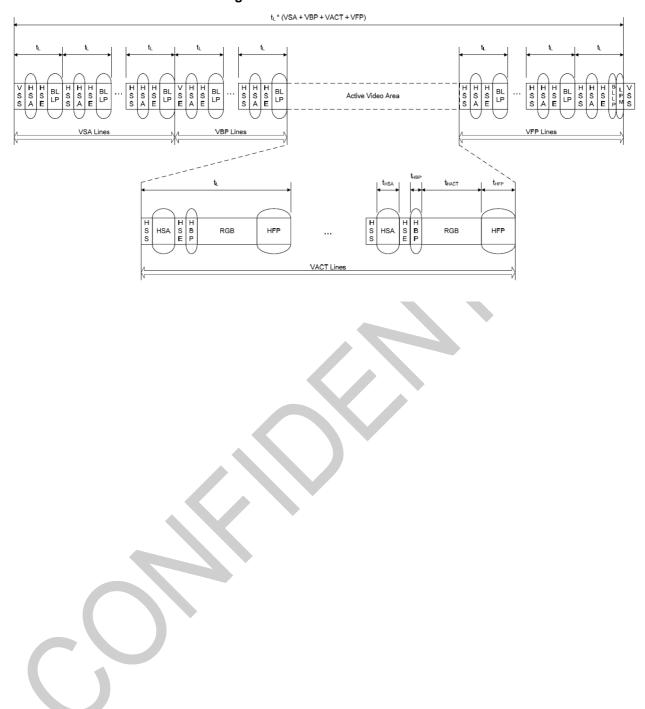
Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.



5.3.6 DSI Video Mode Interface Timing





5.3.7 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

ECC Parity Generation Rules:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B



5.3.8 Notice

- 1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
- 2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.



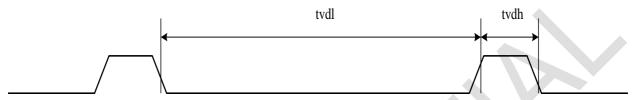


5.5 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



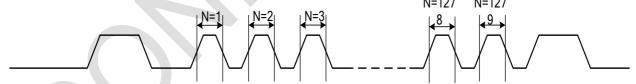
tvdh = The LCD display is not updated from the frame memory. tvdl = The LCD display is updated from the frame memory.

Mode 2, the tearing effect output signal consist of V-sync and H-sync information:



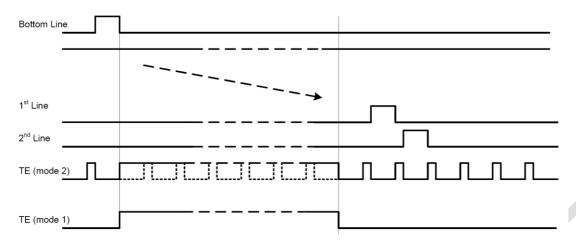
thdh = The LCD display is not updated from the frame memory. thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



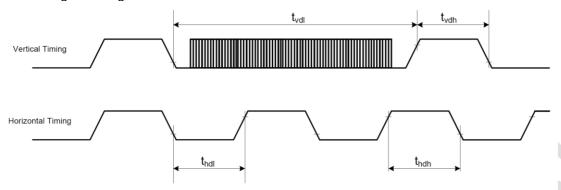


Note. During Sleep In mode, the tearing effect output signal is active low.



5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

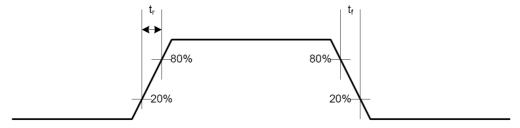


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Тур.	Unit	Description
tvdl	Vertical timing low duration			1*frame time- tvdh
tvdh	Vertical timing high duration			tvdh =V Porch time if STS[15:0]=0. tvdh =31* line time if STS[15:0] not equal to 0.
thdl	Horizontal timing low duration			1* line time- 32*PCLK
thdh	Horizontal timing high duration	1.45	us	32*PCLK

Notes:

- 1. The timings apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)



6. Command

6.1 Command List

<u>6.1</u>	Co	mn	nanc	d List										
Co	mmar	nd	W/P	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default	МТР
Page	Add.	Para.	**//	T direction	<i>D1</i>	D0	D3	D4	53	D2	D.	50	(hex)	
CMD1	00h	•	٧	NOP				No Arg	jument				-	-
CMD1	01h	·	8	Software reset				No Arg	jument				-	-
CMD1	04h	1st						ID1	7:0]				00h	-
CMD1	04h	2nd	R	Read display identification information				ID2	7:0]				80h	-
CMD1	04h	3rd						ID3	7:0]				00h	-
CMD1	05h	-	R	Read number of the errors on DSI				P[7	7:0]				00h	<u> </u>
CMD1	0Ah	1st	R	Read display power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	-	-	08h	-
CMD1	0Bh	1st	R	Read display MADCTR	MY	MX	MV	ML	RGB	-	RSMX	RSMY	00h	-
CMD1	0Ch	1st	R	Read display pixel format	-	1	1	1	-	IFPF2	IFPF1	IFPF0	77h	-
CMD1	0Dh	1st	R	Read display image mode	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h	-
CMD1	0Eh	1st	R	Read display signal mode	TEON	М	0	0	0	0	0	ERR	00h	-
CMD1	0Fh	1st	R	Read display self-diagnostic	0	0	0	0	0	0	0	checksum_	00h	-
CMD1	10h	-	w	result Sleep-in		Ů						comp	-	-
				-					jument				<u> </u>	
CMD1	11h	-	W	Sleep-out					jument				<u> </u>	-
CMD1	12h	•	W	Partial display mode on					jument				-	-
CMD1	13h	-	W	Normal display mode on					jument				-	-
CMD1	20h	-	W	Display inversion off					jument				-	-
CMD1	21h	•	W	Display inversion on					jument				-	-
CMD1	22h	•	W	All pixel off					jument				-	-
CMD1	23h	-	W	All pixel on					jument				-	-
CMD1	28h	-	W	Display off					jument				-	-
CMD1	29h	-	W	Display on					jument				-	-
CMD1		1st	W						9:8]				00h	-
CMD1	2Ah	2nd	W	Set column start address				sc	7:0]				00h	-
CMD1		3rd	W					EC	9:8]				01h	-
CMD1		4th	W					EC	7:0]				8Fh	-
CMD1		1st	W					SP[9:8]				00h	-
CMD1	2Bh	2nd	w	Set row start address				SP[7:0]				00h	-
CMD1	25	3rd	w	oct for start address				EP[9:8]				01h	-
CMD1		4th	W					EP[7:0]				8Fh	-
CMD1	2Ch	•	W	Memory write				No Arg	jument				-	-
CMD1	2Eh	-	W	Memory read				No Arg	jument				-	-
CMD1		1st	w					SR	9:8]				00h	-
CMD1	30h	2nd	w	Partial area				SR	7:0]				00h	-
CMD1	3011	3rd	W	raitiai alea				ER[9:8]				01h	-
CMD1		4th	w					ER[7:0]				8Fh	-
CMD1		1st	W					PSC	[9:8]				00h	-
CMD1		2nd	w					PSC	[7:0]				00h	-
CMD1	31h	3rd	W	Vertical partial area				PEC	[9:8]				01h	-
CMD1		4th	w					PEC	[7:0]				8Fh	-
CMD1	34h	-	W	Tearing effect line off				No Arg	jument				-	-
CMD1	35h		W	Tearing effect line on	0	0	0	0	0	0	TE_M	TELOM	00h	-
CMD1	36h	-	w	Scan direction control				MADC	TR[7:0]				00h	-
CMD1	38h	-	w	Idle mode off					jument				-	-
CMD1	39h	-	w	Enter idle mode					jument				-	-
CMD1	3Ah		w	Interface Pixel Format	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77h	-
CMD1	3Ch	-	w	Memory Continuous Write		<u> </u>	1		jument			1 6-4	-	-
CMD1	3Eh		w	Memory Continuous Read					jument				-	-
CMD1	44h	1st	w	Set tear scan-line					15:8]				00h	-
				l .					•				<u> </u>	



			1	1										
CMD1		2nd	W					STS	[7:0]				00h	-
CMD1	45h	1st	R	Get scan line				GTS	15:8]				00h	-
CMD1	4011	2nd	R	Get sour line				GTS	[7:0]				00h	-
CMD1	4Fh	-	W	Deep standby	0	0	0	0	0	0	0	DSTB	00h	-
CMD1	51h	-	W	Write display brightness				DBV	[7:0]				FFh	-
CMD1	52h	•	R	Read display brightness				DBV	[7:0]				FFh	-
CMD1	53h	•	8	Write CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-
CMD1	54h	•	R	Read CTRL display	0	0	BCTRL	0	DD	0	0	0	28h	-
CMD1	58h	-	w	Set color enhancement	0	0	0	0	0	SLR_EN	L1	SLR_LEVE L0	00h	-
CMD1	59h	-	R	Read color enhancement	0	0	0	0	0	SLR_EN	SLR_LEVE L1	SLR_LEVE L0	00h	-
CMD1	5Ah	,	w	Set color enhancement1	SLR_AMBI _IN7	_IN6	SLR_AMBI _IN5	_IN4-	SLR_AMBI _IN3	_IN2	SLR_AMBI _IN1	_IN0	00h	-
CMD1	5Bh		R	Read color enhancement1	SLR_AMBI IN7	SLR_AMBI IN6	SLR_AMBI IN5	SLR_AMBI IN4-	SLR_AMBI IN3	SLR_AMBI IN2	SLR_AMBI IN1	SLR_AMBI IN0	00h	<u> </u>
CMD1		1st	R					SID					D0h	-
CMD1		2nd	R					SID[15:8]				01h	-
CMD1	A1h	3rd	R	Read DDB				MID	[7:0]				80h	-
CMD1		4th	R					MID[15:8]				90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1		1st	R				•	SID	7:0]				D0h	-
CMD1		2nd	R					SID[15:8]				01h	-
CMD1	A8h	3rd	R	Read DDB Continuous				MID	[7:0]				80h	-
CMD1		4th	R					MID[15:8]				90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1	AAh		R	Read first checksum				FCS	[7:0]				00h	-
CMD1	AFh	-	R	Read continuous checksum				ccs	[7:0]				00h	-
	C2h			Set_DSI Mode	0	0	0	0	0	0	DM1	DM0	00h	-
	C4h			Set_DSPI Mode	0	0	DSPI_CFG 1	DSPI_CFG 0	0	0	0	DSPI_EN	00h	-
CMD1	DAh	-	R	Read display identification				ID1[7:0]				00h	-
CMD1	DBh		R	information	·			ID2[7:0]				80h	-
CMD1	DCh		R	(the same as 04h)	ID3[7:0]									-
CMD1	FEh	-	W	Write CMD mode page	0	0	0	0		CMD_P	age[3:0]		00h	-
CMD1	FFh	-	R	Read CMD page Status	0	0	0	0		CMD_St	atus[3:0]		00h	-



6.2 Command Description NOP (0000h)

0000H					NOP (No Op	eration	1)					
Inst/Para	R/W		Iress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other				<u> </u>						
NOP	W	00h	0000h				No Ar						
Description	Th	is comm	and is an	empty comn		does Don't		e any	effect o	on the o	display	modul	e.
Restriction	None												
Register Availability		No No Pa Pa	rmal Mod	de On, Idle M de On, Idle M e On, Idle M	Mode C	on, Sle	ep Out	Yes		Ey			
				atus ower On Sec	quence		Default N/A	Value					
			SV	V Reset		1	N/A						
Default			HV	V Reset		1	N/A						
Flow Chart	None												



SWRESET(0100h): Software Reset

0100H	SWRESET(Software Reset)													
		Add	Iress											
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
SWRESET	W	01h	0100h		I		No Arg	jumen	t	1	1	l		
Description				ommand is v set default v										
Doctriction		comman	d cannot l	cannot be se be sent for 1						enters	s Sleep	-In mod	de. Do	
			atus						ilabilit	y				
				le On, Idle I										
Register				le On, Idle I										
Availability			rtial Mod	Yes										
				e On, Idle M	lode O	n, Sle	ep Out	Yes						
		516	ep In					Yes	3					
					7									
			St	atus			Default	Value	!					
			Po	wer On Sec	quence) I	N/A							
Default			SV	V Reset		ı	N/A							
			HV	V Reset		ı	N/A							
						'				<u>'</u>				
Flow Chart		< < <	Display Set 0 to S	ESET (01h) / whole blank screen Commands //W Default Value ep In Mode						P2	Legend ommand aramete Display Action Mode equentia ransfer			



RDDID(0400h~0402h): Read Display ID

0400H		Oh~0402h) : Read Display ID RDDID													
		Add	Iress												
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
			0400h	х	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00		
RDDID	R	04h	0401h	х	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80		
			0402h	х	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00		
_ 000p	Note: Co	mmands	(ID1): the (ID2): the (ID3): the RDID1/2/spectively	Module's e Module/c Module/d 3 (DAh/DB	manufad river ver river ID h/DCh)	cture ID sion ID read da) ata corr	espon	d to the	e paran	neter 1	, 2, 3 o	f		
Restriction	-														
ı		Statu	IS					Avail	ability						
		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes													
Register	Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes														
Availability				•				Yes							
İ		Slee		On, Idle M	ode On,	Sieep	Out	Yes							
	Cloop III														
		Status			fault Val er MTP	lue	Befo	re MT	P						
Default			On Sequ		P value		-	:00h / I							
		SW Re			P value P value			:00h / I :00h / I							
		nw ke	set	IVI I	P value		=וטו	:00n / 1	D2=0U	11 / 103	=00n				
				_											
		RDDID	(04h)						 -	l ec	gend	7			
				_					_			┑┊			
		Send 1st	t paramet	er					-		mand				
		ID1[Para	meter				
Flow Chart		Ţ							<	Dis	play	$\supseteq \downarrow$			
i low Chart		Send 2nd	d parame	ter					<	Ac	tion	>			
			[7:0]							М	ode				
				_						<u></u>					
	i	<u>v</u>		~					' /	Sea	uentia	1 N 1 1			
		Send 3rd	d parame	ter					! (nsfer) :			



RDNUMED(0500h): Read Number of Errors on DSI

0500H						RDNU	MED								
		Ado	dress										Π		
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
RDNUMED	R	05h	0500h	х	D7	D6	D5	D4	D3	D2	D1	D0	00		
Description	the bits D[60] I D[7] is s D[70] I sent the	is below bits are to set to "1" bits are s e first par	. elling a nu if there is et to "0"s ameter in	ng a number umber of the overflow wit (as well as F formation (= MIPI DSI or	parity on the parity of the pa	errors. 0] bits. //(0Eh) ad fun	's D0 ar	e set ' compl	'0" at theted).	ne sam	e time) after t			
Restriction	_									X					
		Status Availability Normal Mode On Idle Mode Off Sleep Out Ves													
	Normal Mode On, Idle Mode Off, Sleep Out Yes														
Register		<u> </u>		ode On, Idle		 			es						
Availability		-		de On, Idle			<u> </u>		es						
			Partial Mo Bleep In	de On, Idle	Mode	On, SI	eep Ou		es es						
			пеер пі					''	5 3						
			S	tatus	_		Defaul	t Valu	e						
Datault				ower On Se	quenc		00h								
Default			S	W Reset			00h								
			Н	W Reset			00h								
	F	RDDID	(05h)				[Lege	end	7					
					Comm	nand									
	Send 1st parameter							Paran	neter	7					
Flow Chart	RDE	P[7:0]= DSM(0Eh)'				Actio	on de								
				_/				Seque trans							



RDDPM (0A00h): Read Display Power Mode

RDDPM (0A)	00h) : F	Read L	Displ												
0A00H				RDD	PM (R	lead D	isplay	Powe	r Mod	e)					
Inst/Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
	10,00	MIPI	Othe		<i>D</i> ,	50	50	D 4		52	<i>D</i> 1	20	TIEX		
RDDPM	R	0Ah	0A00	Oh x	D7	D6	D5	D4	D3	D2	D1	D0	08		
				tes the cur		atus of				cribed	in the	table b	elow:		
	Bit D7	Sym		Descripti Booster Vo		tatua		ommer =Booste							
	D6	IDMC		Idle Mode (ıaıus	'1'	=Booste = Idle N	lode Or	1,					
	D5	PTLC		Partial Mod		ff	'1'	= Idle M = Partia	I Mode	On,					
Description	D4	SLPC		Sleep In/Ou			'1'	= Partia	Out,	Off					
	D3	NOR		Display No		ode	'1'	'0' = Sleep In '1' = Normal Display,							
	D2	DISO		On/Off Display On	/Off		'1'	= Partial Display = Display On,							
	D1	Rese	rved	2.0p.u.y 0			0	= Displa	ay Off						
	D0	Rese	rved												
		Status Availability													
	Normal Mode On, Idle Mode Off, Sleep Out Yes														
Register			Norm	al Mode C	n, Idle	e Mode	On,	Sleep	Out	Yes					
Availability			Partia	al Mode O	Mode	Off, S	leep C	ut	Yes						
			_	al Mode O	n, Idle	Mode	On, S	leep C		Yes					
		L	Sleep	o In						Yes					
			S	Status			Det	fault V	alue						
Default			F	Power On	Seque	nce	180								
				W Reset			081								
			L	IW Reset			08ł	1							
		Serial I	/F Mo	de	Para	allel I/F	Mode	:		-	i	Legend			
		RDDP	M (0Al	h)	RI	DDPM (0Ah)		Host		С	omman			
	Send D[7:0] Dummy Read Display												er		
Flow Chart															
					_	Cond Di	7:01	_		 		Action	\geq		
				4	<u>/ </u>	Send D[, .UJ			! ! !		Mode	$\supset \Box$		
										 	S	equentia	al		
										 		ransfer			
										_					



RDDMADCTR (0B00h): Read Display MADCTR

0B00H			F	RDDMAD	CTR	Read	Displa	y MAI	OCTR)				
0_00		Λ حا دا ۰											
Inst/Para	R/W	Addı	1	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDMADCTR	R	0Bh	0B00h		D7	D6	D5	D4	D3	D2	D1	D0	00
	This com	nmand in	dicates	the curre	ent stat	us of t	he disp	olay as	descr	ibed in	the ta	ıble be	low:
	Bit	Symbo	ol	Description	on		Com	ment					
	D7	MY		Row Add	ress			creasin					
	D6	MX		Increment Column A		3		ecreasi creasin					
				Incremen				creasin ow/colun				\bigvee	
Description	D5	MV		Row/Colur	nn Orde	er (MV)	1: No	ormal					
	D4	ML		Vertical Re	efresh C	rder		D Refre					
	D3	RGB		RGB/BG	R Orde	r	'1' =l	BGR, "() }		
	D2	Reserv					,0, =	Norma	l disnla	v(36H-	D1='0')		
	D1	RSMX		Horizonta	al Flip		'1' =	Flipped	d displa	y(36H-	D1='1')		
	D0	RSMY		Vertical F	lip						D0='0') D0='1')		
		'									,		
		St	tatus						Av	ailabi	lity		
		N	ormal N	lode On	Idle N	lode C	Off, SI	ер Оі	ıt Ye	es .			
Register		N	ormal M	lode On	Idle I	On, Sle	ер Оц	ıt Ye	s				
Availability		Pa	artial M	ode On,	ldle M	ode O	ff, Sle	ep Ou	t Ye	es			
		P	artial M	ode On,	ldle M	ode O	n, Sle	ep Out	t Ye	es.			
		SI	leep In						Ye	es			
		01-1					D. (It M	-1			1	
		Statu						ault Va	aiue			1	
Default				equence	•		00h					1	
			Reset				00h						
		HW	Reset				00h						
									ī	_i	 _egend		7
	Se	erial I/F N	/lode	Р	arallel	I/F Mo	de				Ť		!
	PDF	OMADCTR	(OBb)	Ы	DMAD	CTR (0E	Rh)			5	ommano		ļ
	RDL	IMADOTR	(UDII)	RI	DIVIAD	T (UE	511)	Hos		Pa	aramete	er	
Flow Chart				~ <i>_</i>	•••••	1	············	Driv	er	<	Display		į
		Send D[7	:0]		Dumn	ny Read	/			<	Action	>	-
						<u> </u>					Mode		-
				\angle	Send	D[7:0]	/			(0)	equentia		-
									1				
1	transfer											i	



RDDCOLMOD (0C00h): Read Display Pixel Format

0C00H			R	DDCOLM	OD (R	ead Di	isplay	Pixel	Form	at)			
		Addı											
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	R	0Ch	0C00h	Х	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77
	This c	ommand	indicates	the curren	nt statu	s of th	e disp	lay as	descri	bed in	the ta	ble be	low:
	Bi			Descripti	on		Comr						
	D:							= SPI 1					
	D	1 IFPF	[1]	— DBI Pixe				= SPI 3 = SPI 2		pixei, ay / pixe	el.		
D				Format(Interface			'101'	= 16-bi	ts / pix	el,	,		
Description	D	0 IFPF	[0]	Format)		ı		= 18-bi					
								= 24-bi s are n					
		;	Status						Av	ailabil	ity		
		1	Normal I	Mode On, I	dle M	ode O	ff, Sle	ep Ou	t Ye	s			
Register		<u> </u>	Normal I	Mode On, I	dle M	ode O	n, Sle	ep Ou	t Ye	s			
Availability			Partial M	lode On, Id	dle Mo	de Of	f, Slee	p Out	Ye	s			
			Partial M	lode On, Id	de On	, Slee	p Out	Ye	s				
		;		Ye	S								
		St	atus				Defa	ault V	alue				
Default		Po	wer On	Sequence			77h						
Derault		SV	V Reset	>			77h						
		HV	V Reset				77h						
										 !	 Le	egend	
	Se	erial I/F M	lode	Paral	lel I/F	Mode							$\neg \mid$
	RDE	COLMOD	(0Ch)	RDDC	OLMOD	(0Ch)	1				_	mmand	
	<u> </u>		<u></u>				J	Host		/	$\overline{}$	ameter	<
Flow Chart		Send D[7:	nı /	Di	ummy Ro	ead.	7	Driver		<	=	isplay	\mathcal{O}
		Ocha D[7.	01		I	au					\leq _A	ction	<i>></i>
					end D[7:	01	7			į	\overline{N}	/lode	$) \mid$
					α <i>D</i> [/:	<u></u>	-			 	Sec	quential	
										 		ansfer	4 !
										<u>.</u>			



RDDIM (0D00h): Read Display Image Mode

0D00H				RDDIM	(Read	d Disp	lay Im	age M	ode)				
		Ad	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	R	0Dh	0D00h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
	The disp	olay mo	dule returr	ns the disp	olay im	age m	ode st	atus.					I
	Bit	Sym	bol	Descri	ption		Comr	nent					
	D7		erved				'0'						
	D6		erved				'0' "1" =	Inversi	on is C)n			
Description	D5	INVO	NC	Inversi	on On	/Off	"0" =	Inversi	on is C	Off			
Description	D4	ALLO	NC	All Pix	el On		'1' = V	Normal Vhite o	lisplay				
	D3	ALLO	OFF	All Pix	el Off			Normal Black d		ıy			
	D2~ D0	Rese	erved				'000'						
		'											
			Status	ada On I	dia M	ada O	t Clas	n 0.14		ilabilit	y		
		-	Normal M Normal M					•	Yes				
Register Availability		-	Partial Mo			\rightarrow		•	Yes				
		-	Partial Mo						Yes				
		_	Sleep In				<u>· </u>		Yes				
		_											
		Si	tatus				Def	ault Va	alue			1	
			ower On S	Sequence			00h		<u>uiuo</u>			1	
Default			W Reset	•			00h	l				_	
		H	W Reset				00h					_	
												_ 	
	Sei	ial I/F M	1ode	Para	llel I/F	Mode						gend	¬ ;
	R	DDIM (0D	Dh)	RI	DIM (0	Dh)	1					mand	
								Host			_	meter	
Flow Chart			0]	D	ummy R	ead	~ '	Oriver		<	`=	splay	\mathcal{I}
					Ī	/					\geq	tion	
				S	end D[7	:0]	7			; (M	ode	ノ
						/						uential	\
											trai	nsfer	<u> </u>



RDDSM (0E00h): Read Display Signal Mode

0E00H						ead Dis	play S	Signal	Mode)				
		Add	dress	T									
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	R	0Eh	0E00h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
				rns the D		Signal			•		•		
	Bit	Sym	bol	Descript Tearing E			Com	ment					
	D7	TEON	١	On/Off				On, "0"					
	D6	TELC	M	Tearing e mode	effect lin	ie		mode1 mode2					
Description	D5	Rese					'0'						
Boomption	D4 D3	Rese Rese					,0,						
	D2	Rese					,0,						
	D1	Rese	rved				'0'	Na Ewa					
	D0	Error	on DSI	Error on I	DSI		11' =	No Erro Error					
		5	Status						Ava	ailabili	ty		
		ı	Normal I	Mode On	, Idle N	/lode C	ff, Sle	ep Ou	t Yes	5			
Register		ı	Normal I	Mode On	, Idle N	Mode C	n, Sle	ep Ou	Yes	6			
Availability		F	Partial N	lode On,	Idle M	ode Of	f, Slee	p Out	Yes	3			
		F	Partial N	lode On,	ldle M	ode O	n, Slee	p Out	Yes	5			
			Sleep In						Yes	5			
		S	tatus				D	efault '	Value				
Default		P	ower O	n Sequen	ice		00)h					
		S	W Rese	t			00)h					
		H	IW Rese	t			00)h					
				_		.,				[L	egend	
	Se	erial I/F	Mode	Pa	arallel	l/F Mod	le —				Co	mmand	$\exists []$
	F	RDDSM (0)Eh)		RDDSN	И (0Eh)					Pai	rameter	
								Host Drive				Display	
Flow Chart		▼ Send D[7	7:0]		Dumm	y Read	7	שוועכו	L		\geq		$\langle \cdot \cdot $
	_											Action	<i>?</i>
					0 13	D[7.03	_			1		Mode	$) \mid \mid$
					Send	D[7:0]				į	95	quentia	
										į		quentia ansfer)
										į			<u> </u>



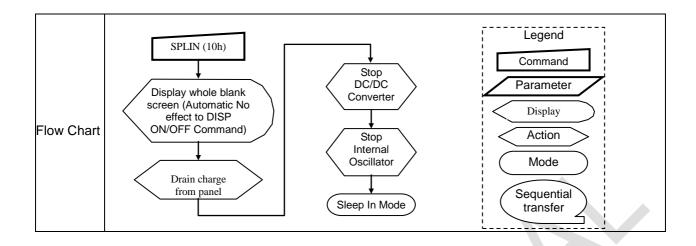
RDDSDR (0F00h): Read Display Self-Diagnostic Result

0F00H										agnost	tic Res	sult)		
		۸ ما ،	-lua a a							J				
Inst/Para	R/W		dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		HEX
RDDSDR	R	0Fh	0F00h	х	0	0	0	0	0	0	0	checksum_	_comp	00
	The	displa	ay mod	lule ret	urns th	ne self	-diagno	ostic re	esults f	ollowin	ig a Sl	eep Out cor	mmand	
		Bit	Symb	ol [Descrip	tion			(Comme	nt			
		D0	Rese	ved c	hecksı	um_cor	np		,	0'				
Description														
			S	status					_	_	Avai	lability		
				Iormal	Mode	On, l	dle Mo	de Of	f, Slee	p Out	Yes	,		
Register			N	Iormal	Mode	On, l	dle Mo	de On	, Slee	p Out	Yes			
Availability			F	artial	Mode	On, Id	le Mod	de Off,	Sleep	Out	Yes			
			P	artial	Mode	On, Id	le Mod	de On,	Sleep	Out	Yes			
			S	leep Ir	1						Yes			
			St	atus	_				Def	ault Va	ilue			
				wer O	n Seq	uence	<u>;</u>		00h					
Default			SV	V Rese	et				00h					
			н	V Rese	et				00h					
Flow Chart		RE	DDSDR (0Fh)		R	DDSTR Dummy I	(0Fh)		Host Driver		P	Display Action Mode equentiatransfer	



SLPIN (1000h): Sleep In

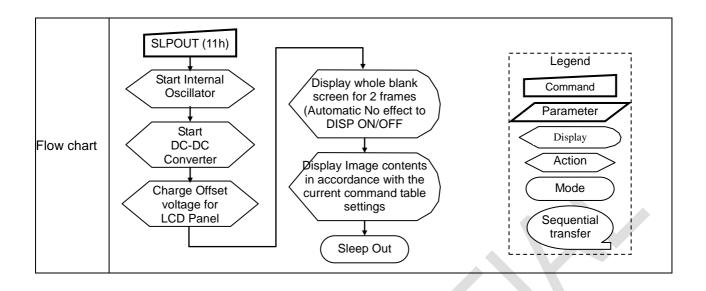
1000H					S	LPIN (Sleep	ln)					
		Ad	dress										
Inst/Para	R/W	MIDI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPIN	W	10h	1000h				No A	rgume	nt				
Description	In this m scannin values. After Sle display Out-mo	node the going is stoped to the good to be g	ne DC/DC opped. Th command s informa	he display converted e control l l, user car tion is vali	r is sto Interfac n send id durir	pped, I ce such PCLK, ng 2 fra	nterna n as reg HS an nmes if	l displa gisters id VS ii	y oscil is still nforma	lator is workin ation or	stoppi g and l	ed, and keeps i	l panel ts blank
Restriction	Sleep Ir It must v stabilize It must v	n Mode wait 5n e. wait 12	can only nsec befo	ffect when be exit by re sending ter sendin be sent.	the S g next	leep O comma	ut Com and for	mand the su	(11h). pply vo	oltages	and cl	ock cir	
		_											
			Status					_		ailabili	ty		
				Mode On			-	•		5			
Register			Normal I	Mode On	, Idle N	lode C	n, Sle	ep Ou	t Yes	3			
Availability			Partial N	lode On,	Idle M	ode O	ff, Slee	p Out	Yes	3			
			Partial M	lode On,	ldle M	ode O	n, Slee	p Out	Yes	5			
			Sleep In						Yes	5			
			Stat	us		ı	Default	Value					
Default				er On Se	quence		Sleep Ir)				
Default			SW	Reset		S	Sleep Ir	n Mode)				
			HW	Reset		S	Sleep Ir	n Mode)				





SLPOUT (1100h): Sleep Out

1100H		•			SLPO	UT (S	leep O	ut)					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	W	11h	1100h				No /	Argum	ent	•	•		
Description	This comi module a modules t	re enable	d. The ho	st proce	essor s	ends F	CLK, I	HS and	d VS in	format	ion to	display	,
Restriction	This coming not in Scommand circuits to The host sending at the registed display defor when the functions	Sleep mod I before so stabilize processo Sleep-Ir ers when evice who he displa	de. The hosending and the comman exiting the coding ymodule.	ost processors processors of the contract of t	essor r ommar nilliseco display mode. isters i	nust wand. This onds an modul on There of the fa	ait five s delay fter ser e loads shall r ctory c	millise / allow nding a s the d not be default	econds s the s a Sleep isplay any at and re	after supply of Out comodule on Out comodule o	sending voltage ommar e's defa Il visua values	y this s and o nd befo ault val I effect are the	clock ore lues to t on the e same
		Sto	tus						Avoil	obility.			
			rmal Mod	le On. lo	dle Mo	de Off	Sleen	Out	Yes	ability			
Register		-	rmal Mod		_				Yes				
Availability		Par	tial Mode	e On, Id	le Mod	le Off,	Sleep	Out	Yes				
		Pai	tial Mode	e On, Id	le Mod	le On,	Sleep	Out	Yes				
		Sle	ep In						Yes				
Default			SW	us er On S Reset Reset	equenc	е	Sleep Sleep	t Value In Mod In Mod In Mod	le le				





PTLON (1200h): Partial Display Mode On

1200H				PTI	LON (P	artial [Display	Mode	On)				
Inst/Para	R/W	Add MIPI	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	W	12h	1200h				No	 Argum	 ≏nt				
Description	This cor Display To leave written.	nmand Mode we Partial The hoses for two	causes t indow is Display	describ Mode, t sor cont	ed by the Northian	he Part mal Dis o send	enter th ial Area play M PCLK,	e Partia a (30h) ode Or HS and	al Displ comma (13h) d VS in	and. comma formati	and sho on to d	uld be isplay	
Restriction	This cor	mmand	has no e	ffect wh	en Part	tial Disp	olay Mc	de is a	Iready	active.			
Register Availability		1	Status Normal Normal Partial N Partial N Sleep In	Mode On lode On	n, Idle 1, Idle N	Mode (On, Sle	ep Out	t Yes	i i	У		
Default			Status Power SW R	On Sec	quence	No No	fault Varmal di rmal di rmal di	splay n splay n	node O	n			
Flow Chart	Refer to	Partial	Area (30)h)									



NORON (1300h): Normal Display Mode On

1300H				NORON (No	rmal	Displa	ay Mo	ode O	n)				
		Add	lress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	W	13h	1300h			No /	Argun	nent					
Description	as Parti	al Displate	ay mode ssor sen	he display modulo ds PCLK, HS and nand is sent whe	l VS i	nform	ation	to Ty _l	oe 2 d	display	/ mod	lules t	wo
Restriction	This cor	mmand	has no e	ffect when Norma	al Dis	play r	node	is alre	eady a	active.			
			Status						Avail	abilit	v		
				Mode On, Idle M	ode (Off, S	leep (Yes	abilit	y		
Register			Normal	Mode On, Idle M	ode (On, SI	leep (Out	Yes				
Availability		I	Partial N	lode On, Idle Mo	de O	ff, Sle	еер О	ut	Yes				
		I	Partial M	lode On, Idle Mo	de O	n, Sle	ер О	ut	Yes				
		:	Sleep In						Yes				
			04-			14	\/-l						
			Sta	tus ver On Sequence			Value Displ		nde O	ın			
Default				Reset			Displ						
			HW	Reset			Displ						
Flow Chart	Refer to	the des	scription	of Partial Area (3	000h)							

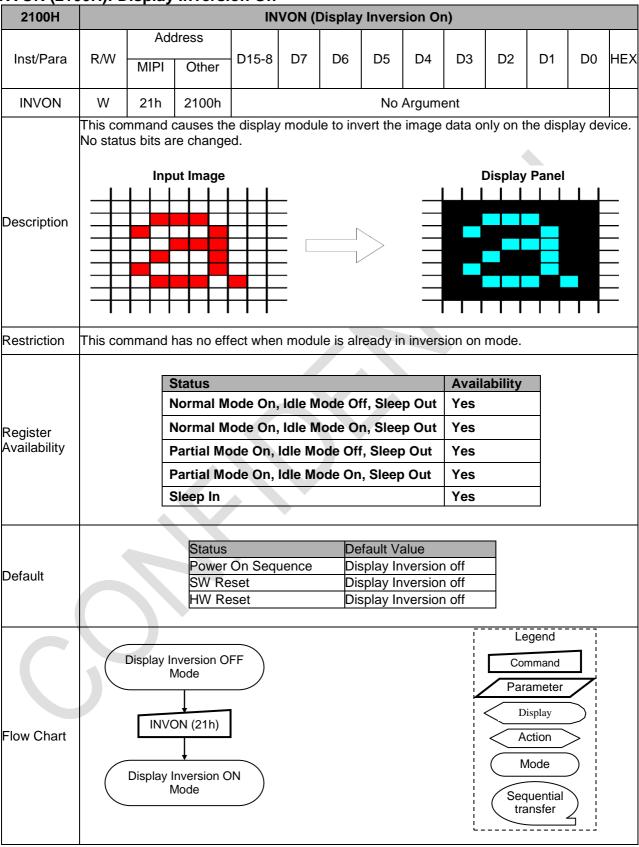


INVOFF (2000H): Display Inversion Off

2000H				INV	OFF (D	isplay	Inver	sion O	ff)				
		Addres	SS										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	W	20h	2000h				No Ar	gumen	t				
				the display are changed.		to sto	p inver	ting the	e imag	e data	on the	displa	у
		ļ	Input Ima	age .						Dis	splay F	Panel	
Description								- - - - -					
	T 1. '	11	111	1 1 1	<u> </u>	. 1		_		11	1 1	-	
Restriction	I his c	commar	nd has no	effect when	the dis	play m	odule	is not ii	nvertin	g the d	ıspıay	ımage.	i
			Status						Avail	ability	,		
				I Mode On, I	dle Mo	de Off	f, Slee	p Out	Yes	,			
Register			Norma	l Mode On, I	dle Mo	de On	, Slee	p Out	Yes				
Availability			Partial	Mode On, Id	dle Mo	de Off,	Sleep	Out	Yes				
			-	Mode On, Id	dle Mo	de On,	Sleep	Out	Yes				
			Sleep I	n					Yes				
Default		7	P S	tatus ower On Sec W Reset W Reset	quence	Di:	splay lı	'alue nversio nversio	n off				
Flow Chart			INVC	nversion On Mode DFF (20h)							Pa I Se	egend ommand rametel Display Action Mode quentia ansfer	



INVON (2100H): Display Inversion On

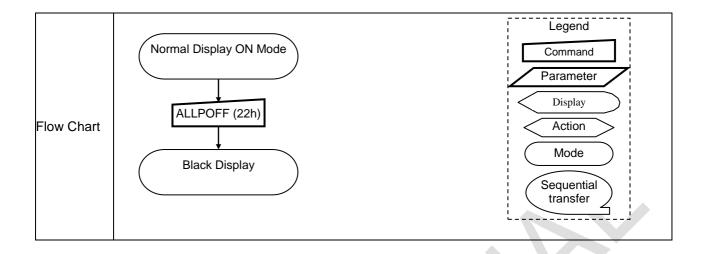




ALLPOFF (2200H): All Pixel Off

						ALLPO	OFF						
		Ac	dress										
Inst/Para	R/W	MIDI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPOFF	W	22h	2200h		•		No A	rgumer	nt	•			
	On/Of	f registe	er can be c	e display pa on or off. t change an			·	ut mod	e and a	status	of the	Displa	y
		Ir	nput Ima	ge					Disp	lay P	anel		
Description	-				_	-							
	this m	ode. Th	ne display p	Display Mo panel is sho On" comma	wing th								
Restriction	this m	ode. Th	ne display p	panel is sho	wing th								
Restriction	this m	ode. Th	ne display p	panel is sho	wing th								
Restriction	this m	ode. Th	ne display p	panel is sho	wing th					e after			
Restriction	this m	ode. Th	ne display p tial Mode (panel is sho	owing th	ne cont	ent of t	he Inpo	ut Imag	e after			
Register	this m	ode. Th	status Normal	oanel is sho On" commai	owing that the second s	ne cont	ent of t	o Out	ut Imag	e after			
	this m	ode. Th	Status Normal	oanel is sho On" commai	dle Mo	ode Off	, Sleep	Out	Availa Yes	e after			
Register	this m	ode. Th	Status Normal Partial N	Mode On, I	dle Modle Modle Modle Modle Mod	ode Off,	, Sleep Sleep	Out Out	Availa Yes Yes	e after			
Register	this m	ode. Th	Status Normal Partial N	Mode On, I Mode On, I Mode On, I Mode On, I Mode On, I	dle Modle Modle Modle Modle Mod	ode Off,	, Sleep Sleep	Out Out	Availa Yes Yes	e after			



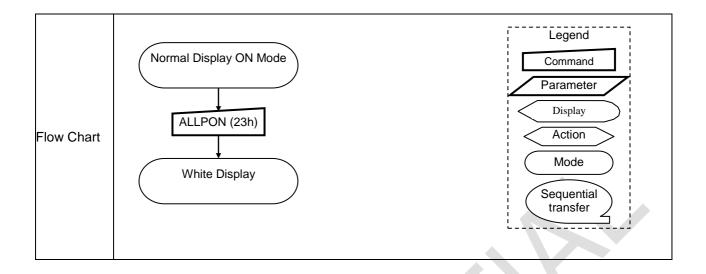




ALLPON (2300H): All Pixel On

2300H						ALLP	ON						
Inst/Para	R/W	Ad	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPON	W	23h	2300h				No .	Argum	ent				
Description	On/Off r This cor	egister of mand of Input	curns the discan be on codoes not characteristics. It Image 'Normal Discher before a constant of the constan	or off. lange an	ode On	status	rtial M	ode Or	Displa " comr	nands	nel	ed to le	ave
Restriction	-												
Register Availability		N F F	Status Normal Mo Normal Mo Partial Mod Partial Mod Sleep In	de On, I le On, Ic	dle Mo	de On de Off,	, Sleep Sleep	Out Out	Availa Yes Yes Yes Yes	ability			
Default			Status Power C SW Res HW Res	et	ence	Disp Disp	olay Inv	lue version version version	off				





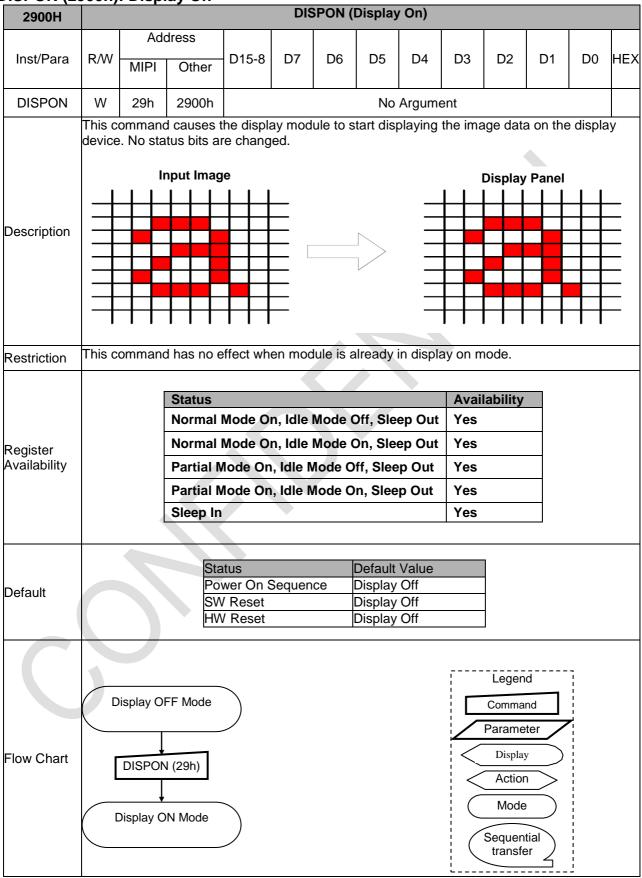


DISPOFF (2800h): Display Off

2800H					DISP	OFF (E	isplay	Off)					
		Ad	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	W	28h	2800h				No A	1 Argume	ent			1	
			d causes t tus bits a			le to sto	op disp	laying t	he ima	ge data	on the	displa	у
		Inp	out Image						D	isplay	Panel		
Description													- - - -
					_		-	\exists	\blacksquare	#		+	_
Restriction	This c	omman	d has no e	effect whe	n modu	ıle is alı	eady ir	n displa	y off m	ode.			
Register Availability			Normal Partial N	Mode On Mode On Mode On, Mode On,	, Idle M	lode O	n, Slee f, Sleep	p Out	Yes Yes Yes Yes Yes Yes	ability			
Default			SW	tus ver On Se Reset Reset	quence	e Dis	fault Va splay O splay O splay O	off off					
Flow Chart			DISPOFF (28h))						Legen Comma Parame Display Action Mode	nd ter	



DISPON (2900h): Display On



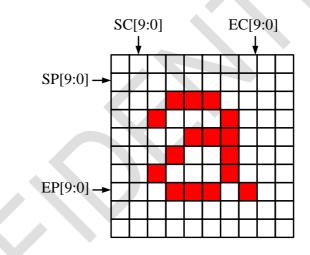


CASET(2A00h~2A03h): Set Column Start Address

						CAS	SET						
la et/De se	DAA	Ado	Iress	D45.0	D7	DC	5	D4	D2	D0	2	Do	1157
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			2A00h	х	-	-	1	1	1	1	SC9	SC8	00
CASET	W/R	2Ah	2A01h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
CASET	VV/K	ZAII	2A02h	х	-	-	-	-	-	-	EC9	EC8	01
			2A03h	х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.

This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Description

(1) SC[9:0] always must be equal to or less than EC[9:0].

(2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.

Register Availability

Restriction

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes



	Status	Default Value								
	Status	SC[9:0]	EC[9:0]							
Default	Power On Sequence	0000h	018Fh							
	SW Reset	0000h	018Fh							
	HW Reset	0000h	018Fh							
Flow Chart	CASET 1st & 2nd Param 3rd & 4th Param RASET 1st & 2nd Param 3rd & 4th Param RAMWR RAMWR D1[B:0],D2[B:0] Any Com	eter: SC[9:0] eter: EC[9:0] (2Bh) eter: SP[9:0] eter: EP[9:0] (2Ch) Data]Dn[B:0]	Legend Command Parameter Display Action Mode Sequential transfer							



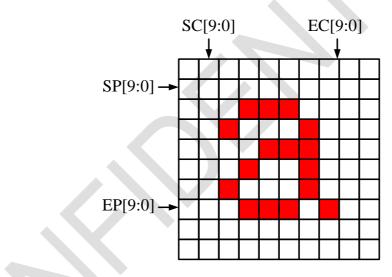
Description

RASET(2B00h~2B03h): Set Row Start Address

2B00H	RASET												
/2		Add	Iress	D15-8	D7	Б.	D5	D4	D3	D2	D1	D0	HEX
Inst/Para R/W	MIPI	Other	D6										
			2B00h	х	1	-	-	-		-	SP9	SP8	00
RASET V	W/R	2Bh	2B01h	х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
	VV/IX	IX ZDII	2B02h	х	1	-	-	-	1	1	EP9	EP8	01
					2B03h	х	EP7	EP6	EP5	EP4	EP3	EP2	EP1

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.

This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



(1) SP[9:0] always must be equal to or less than EP[9:0]

Restriction (2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes



			_						
	Status	Default Value							
	Status	SP[9:0]	EP[9:0]						
Default	Power On Sequence	0000h	018Fh						
	SW Reset	0000h	018Fh						
	HW Reset	0000h	018Fh						
Flow Chart	CASET (2Ah 1st & 2nd Parameter: 3rd & 4th Parameter: RASET (2Bh 1st & 2nd Parameter: 3rd & 4th Parameter: RAMWR (2C	SC[9:0] EC[9:0] SP[9:0] h) Dn[B:0]	Legend Command Parameter Display Action Mode Sequential transfer						



Availability

RAMWR (2C00h): Memory Write

2C00H	RAMWR												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	Da	D1	D0	ПΕΛ
	IX/VV	MIPI	Other	D15-8	יט	D0	Do	D4	DS	D2	D1	DO	HEX
RAMWR			2C00h	Х	0	0	1	0	1	1	0	0	2C
	R/W	2Ch	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D ₁ 4	D ₁ 3	D ₁ 2	D ₁ 1	D ₁ 0	
IVAIVIVVIX	17,44	2011	:	Х	:	:	:	:	:	:	1	:	
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0	
Description	memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is thei incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the En Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the Encolumn (EC) value or the host processor sends another command.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												
					Statu	S			A	/ailabili	ty		
			Normal I	Mode On	, Idle N	/lode C	ff, Sle	ep Out		Yes			
Dagiato:			Normal I	Mode On	, Idle N	/lode C	n, Slee	ep Out		Yes			
Register		Ī	D	4. 1. 0	1.11. 5		" 01.	. 0 .		Va -			

Partial Mode On, Idle Mode Off, Sleep Out

Partial Mode On, Idle Mode On, Sleep Out

Sleep In

Yes

Yes

Yes



Default	Status Power On Sequence SW Reset HW Reset	Default Value Contents of memory is set randomly Contents of memory is not cleared Contents of memory is not cleared
Flow chart	RAMWR (2Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer



RAMRD (2E00h): Memory Read

2E00H						RA	MRD						
Inst/Para	R/W	Ac MIPI	ldress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			2E00h	Х	0	0	1	0	1	1	1	0	2E
			1 st Pixel	Х	D ₁ 7	D ₁ 6	D₁5	D ₁ 4	D ₁ 3	D ₁ 2	D ₁ 1	D ₁ 0	
RAMRD	R/W	2Eh	:	Х	:	:	:	:	:	:	:	0 D ₁ 0 : D _N 0 or the hood RASET dege (SP) and the last	
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1		
Description	If MV(36 The colurespectivincremer Columnincremer Page (El If MV(36 The colurespectivincremer Page (El Pixels ar	ds. h-B5) mn an vely. P nted an (EC) v nted. F P) valu h-B5) mn an vely. P nted an P) valu e reac	d page re ixels are red pixels re la lue. The Pixels are le or the h	gisters a ead from ead from column read from ost proc gisters a ead from ead from ge regist	re researches the frame of the	et to the memorame mane mane mane mane mane mane mane m	e Start (Semory at (Semory at (Semory at (Semory at (Semory et to Semory et colur	Columnisc, SP, until the commisc, SP, until the pand to min reg	n (SC)). The e colur and the page and. n (SC)). The e page the colur the page the	and Si column mn reg e page e regist and Si page r e regist umn re	cart Pag n regist ister ec e regist cer equ cart Pag egister er equa gister i	ge (SP) er is th quals th er is als the ge (SP) is ther als the s incre	en ee End End , , n End mented
Restriction	There is	no res	triction on	length o	of parai	meters	•						
					Stat	tus			,	Availab	oility		
			Normal	Mode C	n, Idle	Mode	Off, Sle	еер Оц	ıt	Yes			
Register			Normal	Mode C	n, Idle	Mode	On, Sle	еер Ои	ıt	Yes	i		
Availability			Partial	Mode O	n, Idle	Mode	Off, Sle	eep Ou	t	Yes			
			Partial	Mode O	n, Idle	Mode (On, Sle	eep Ou	t	Yes			
					Slee		Yes						
			,						•				



Default	Status Power On Sequence SW Reset HW Reset	Default Value Contents of memory is set randomly Contents of memory is not cleared Contents of memory is not cleared	
Flow chart	Dummy Read Dummy Read Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer	



3000H					P	TLAR (Partial	Area)					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
			3000h	х	-	-	-	-	-	-	SR9	SR8	00
DTI AD	D 44/	201-	3001h	х	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
PTLAR	R/W	30h	3002h	х	-	-	1	1	1	-	ER9	ER8	01
			3003h	х	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	8F
	Row (I	ER), as	h this co illustrate Start Ro	d in the				olan KC	w (SK)	anu ini	e secoi	iu trie E	iliu
	Star	t Row	=							-			
	SR[9:0] -	→		_								
			#							-			
			\mp		-	-				- >	Partia Area		
	End	Row	\equiv										
		9:0] -	→ ±										
										-			
Description	I.C. E.	LD.	01.10										
	If End	x Row <	Start Ro	ow									
			_								>	Partial	
	ER	[9:0]	→_							\blacksquare	J	Area	
			_							 			
										\equiv			
			=										
			ξ=							\perp	_		
	SR	[9:0]	→ _								>	Partial Area	
											1		
			Start Ro										



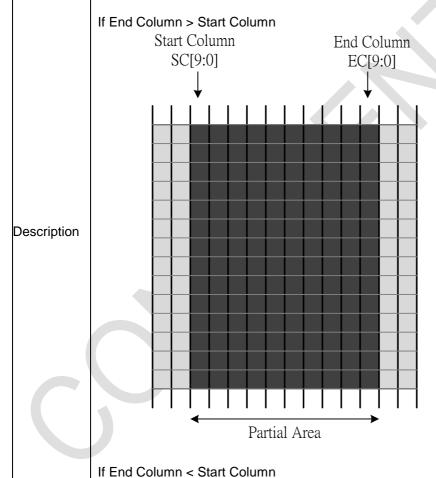
	Status		Availability
	Normal Mode	On, Idle Mode Off, Sleep Ou	t Yes
Register	Normal Mode	On, Idle Mode On, Sleep Ou	t Yes
Availability	Partial Mode (On, Idle Mode Off, Sleep Out	Yes
	Partial Mode (On, Idle Mode On, Sleep Out	Yes
	Sleep In		Yes
	Ctatus	Default Value	<i>/</i>
	Status	SR[9:0]	ER[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow chart	1. To Enter Partial Mo PTLAR (30h) 1st & 2nd Parameter: SR[9:0] 3rd & 4th Parameter: ER[9:0] PTLON (12h) Partial Mode	Partial Mode DISPOFF (28h NORON (13h) Partial Mode OF Image Data D1[B:0],D2[B:0]Dn[B:0] DISON (29h)	Optional to prevent tearing effect image display Legend Command Parameter Display Action



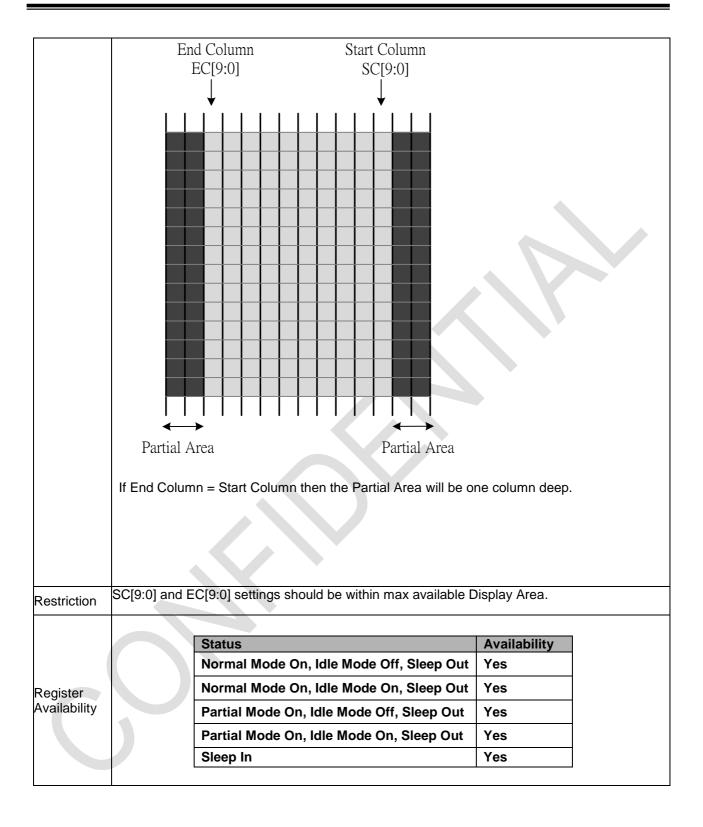
PTLAR (3100h): Vertical Partial Area

3000H		PTLAR (Partial Area)											
Inot/Doro	R/W	Add	ress	D15-8	D7	De	D5	D4	D3	D2	D1	D0	LIEV
Inst/Para R	I K/VV	MIPI	Other	15-6		D6			D3	DZ	D1	DU	HEX
			3100h	х	-	1	ı	-	ı	ı	ı	SC8	00
DTLAD	DAM	R/W 30h	3101h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
PTLAR	K/VV		3102h	Х	-	-	-	-	-	-	-	EC8	01
			3103h	х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure.









		Default Value	
	Status	SC[9:0]	EC[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow chart	1. To Enter Partial Mod PTLAR (30h) 1st & 2nd Parameter: SR[9:0] 3rd & 4th Parameter: ER[9:0] PTLON (12h) Partial Mode Note: B=23	Partial Mode DISPOFF (28 NORON (13h Partial Mode C Image Data D1[B:0],D2[B:CDn[B:0] DISON (29h	Optional to prevent tearing effect image display h) Legend Command Parameter Display Action Mode Sequential transfer



TEOFF (3400h): Tearing Effect Line OFF

3400H				TEC	OFF (T	earing	Effec	t Line	OFF)				
		Addr	ess										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	W	34h	3400h				No A	rgume	ent				
Description	This line.	comman	d turns o	ff the disp	olay mo	odule's	Tearir	ng Effe	ect out	put sig	nal on	the TE	signal
Restriction	This	comman	d has no	effect wh	en the	Tearir	ng Effe	ct outp	out is a	already	off.		
			_										
			Status	l Mada O	مالما م	Mada	0" 0	·leen (Availal	oility		
				Mode O			-	_		Yes			
Register Availability				Mode O Mode Or						Yes Yes			
				Mode Or						Yes			
			Sleep I		-,			201		Yes			
			•										
Default				Status Power (SW Res HW Res	set	quence		Defau OFF OFF OFF	lt Valu	e			
Flow Chart		TE	ne Output	h)							Com Para Dis	gend mand meter splay etion ode uential nsfer	



TEON (3500h): Tearing Effect Line ON

	TEON (Tearing Effect Line ON)											
DΛΛ	Address		D15 0	D7	De	DE	. D4	D3	D3	D1	D0	HEX
K/VV	MIPI	Other	ס-פוע	יט	DO	DJ	D4	D3	DZ	וטו	D0	HEA
R/W	35h	3500h	Х	0	0	0	0	0	0	TE_M	TELOM	00
	R/W R/W	R/W MIPI	R/W MIPI Other	R/W Address D15-8 D15-8	R/W Address D15-8 D7	R/W Address D15-8 D7 D6	R/W Address D15-8 D7 D6 D5	R/W Address D15-8 D7 D6 D5 D4	R/W Address D15-8 D7 D6 D5 D4 D3	R/W Address D15-8 D7 D6 D5 D4 D3 D2	R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1	R/W Address D15-8 D7 D6 D5 D4 D3 D2 D1 D0

Bit	Symbol	Description	Comment
D0	TELOM	Output mode of TE signal	0:only V-blanking 1:V-blanking +H-blanking
D1	TE_M	Output mode of TE signal set	1: Refresh frame active <note> TE output active at refresh frame to avoid tearing effect, command can be set: 1. 0x3500=00.or 2. 0x3500=02.</note>

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.

Description



If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.

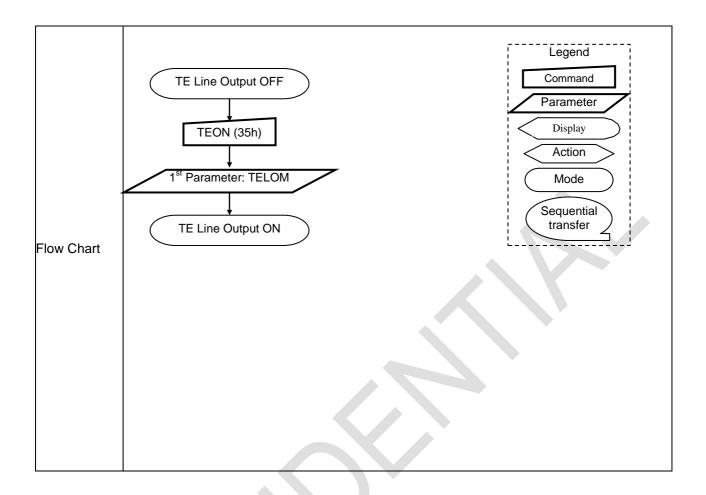


The Tearing Effect Output line shall be active low when the display module is in Sleep mode.



Restriction	This command has no effect when Tearing Effect output is alr	eady ON.
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Dogiotor	Partial Mode On, Idle Mode Off, Sleep Out	Yes
Register Availability	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Pefault	Status Power On Sequence OFF SW Reset HW Reset OFF	





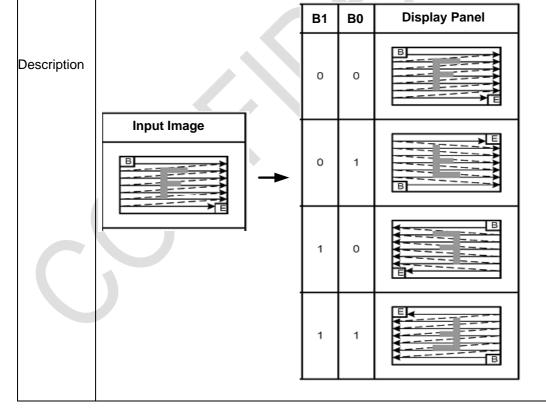


MADCTR (3600h): Scan Direction Control

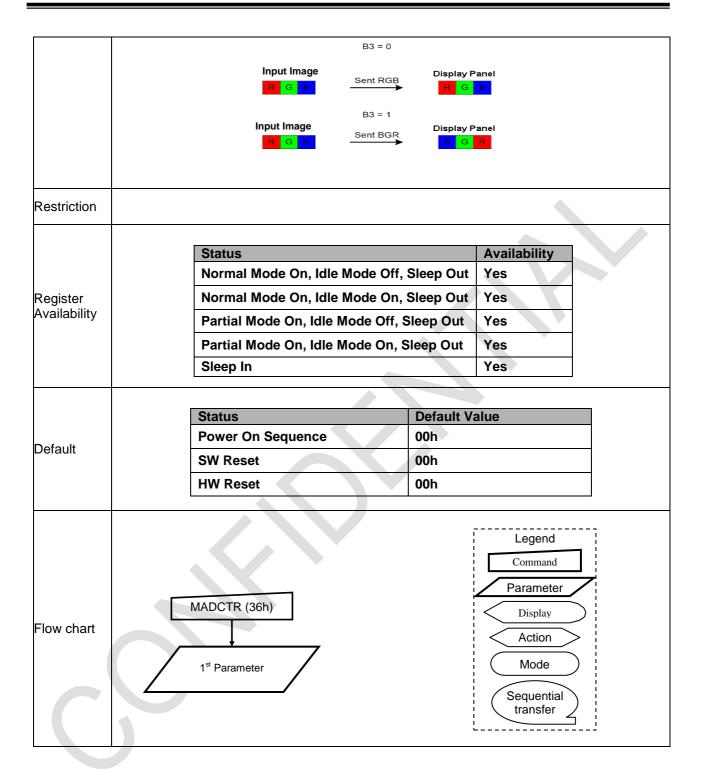
3600H		MADCTR (Scan Direction Control)											
Inst/Para	Inst/Para R/W Addr. MIPI	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Inst/Para		MIPI	Other	ס-פוע	<i>D1</i>	סט	D3	D4	DS	DZ			HEX
MADCTR	W	36h	3600h	х	D7	D6	D5	D4	D3	D2	D1	D0	00

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
D7	MY	Row Address Increment	0: Increasing in vertical
<i>D1</i>	IVII	Now Address increment	1: Decreasing in vertical
D6	MX	Column Address Increment	0: Increasing in horizontal
Ъ	IVIX	Column Address increment	1: Increasing in horizontal
D5	MV	Row/Column Order (MV)	0: Row/column exchange
DS	IVIV	Row/Column Order (IVIV)	1: Normal
D4	ML	Vertical Refresh Order	0: LCD Refresh Top to Bottom
D4	IVIL	Vertical Reflesh Order	1: LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
D2	Reserved		0
D1	RSMX	Horizontal Flip	'0' = Normal display
וטו	KOWA	Horizontal Flip	'1' = Flipped display
D0	RSMY	Vertical Flip	'0' = Normal display
טט	KOIVIT	Vertical Flip	'1' = Flipped display









IDMOFF (3800h): Idle Mode Off

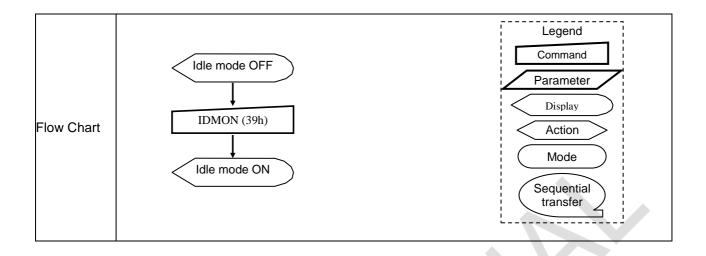
3800H		1010 111	<u> </u>	II	DMOF	F (Idle	Mode	Off)					
Inst/Para	R/W	Ac MIPI	Idress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	W	38h	3800h				No A	rgume	nt				
Description	This c	ommano	d causes th	e display ı	module	e to ex	it Idle r	mode.		•			
Restriction	This c	ommano	d has no eff	ect when	the dis	play m	nodule	is not	in Idle	mode.			
Register Availability			Status Normal M Normal M Partial M Partial M Sleep In	ode On, I	dle Mo	ode Oi de Off	n, Slee , Slee _l	ep Out	Yes		У		
Default				Status Power Or SW Rese HW Rese	t	ence	ldle ldle	fault V e Mode e Mode e Mode	Off Off				
Flow Chart	\ [\ \	IDMC	once ON OFF (38h) ode OFF							Par	egend mmand rameter Display Action Mode quentia ansfer		



IDMON (3900h): Enter_idle_mode

3900H			Enter_idle_mode										
		Add	Iress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		IVIIPI	Other										
IDMON	W	39h	3900h				No .	Argum	ent				
Description	In Idle N	lode, cole each of t	auses the or express he R, G a nput Imag	sion is re nd B col	duced	. Color	s are s	hown (on the	€	/ device		g the
	Color Black Blue Red Mager Green Cyan Yellow White	0XXX 0XXX 1XXX 1XXX 0XXX 0XXX	6 R5 R4 R3 XXXX XXXX XXXX XXXX XXXX XXXX XXXX	R2 R1 R0		G7 G6 G DXXXXX DXXXXX DXXXXX DXXXXX DXXXXX DXXXXX DXXXXX DXXXXX DXXXXX	XX XX XX XX XX XX	3 G2 G1	G0	B0			
Restriction	This cor	nmand h	as no effe	ct when	modul	e is alr	eady in	n idle o	n mod	e.			
			tatus							lability	/		
			ormal Mo					•	Yes				
Register Availability			ormal Mo				•	•	Yes				
			artial Mod				<u> </u>		Yes				
			leep In	ao		40 011	, 0.00	Jul	Yes				
Default			Po SV	atus wer On S V Reset V Reset	Seque	nce	ldle N	ult Valu Mode C Mode C Mode C	Off Off				







COLMOD (3A00h): Interface Pixel Format

<u> </u>	00 10	<i>,,</i> (0011)	,co.	1400 1	17011	minat			on): Intoriace i ixeri emiat												
3A0	ООН		COLMOD (Interface Pixel Format)																		
lnot/	Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
IIISU	raia	K/VV	MIPI	Other	D10-0 D7	D6	טט	D4	כם	DZ	וטו	00	I ILLX								
COL	MOD	W	3Ah	3A00h	х	0	1	1	1	0	IFPF[2]	IFPF[1]	IFPF[0]	77							
			command sets the pixel format for the RGB image data used by the interface. F[2:0]: MCU Pixel Format Definition.																		

If not used DPI interface, then the corresponding bits in the parameter are ignored.

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
SPI 3 bit/pixel (8 colors); SPI 1-1-1	0	0	1
SPI 8 bit/pixel (256 colors); SPI 3-3-2	0	1	0
SPI 8 bit/pixel (256 colors); SPI 256 Gray	0	1	1
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
24bit/pixel (16.7M colors)	1	1	1

SPI 1-1-1

RGB 1-1-1 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	D	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	x	x			B1[0]	R2[0]	G2[0]	B2[0]	1st pixel Data Write
2nd RAM Data Write	1	x	x	R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]	2nd pixel Data Writ
3rd RAM Data Write	1	х	x	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]	3rd pixel Data Write
So on										

Description

SPI 3-3-2

RGB 3-3-2 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[2]	R1[1]					ві[1]	B1[0]	1st pixel Data Write
2nd RAM Data Write	1	R2[2]			G2[2]		G2[0]	B2[1]	B2[0]	2nd pixel Data Writ
3rd RAM Data Write	1	R3[2]			G3[2]			B3[1]	B3[0]	3rd pixel Data Write
So on										

SPI 256 Gray

RGB 256 Gray	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	P1[7]								1st pixel Data Write
2nd RAM Data Write	1	P2[7]	P2[6]						P2[0]	2nd pixel Data Write
3rd RAM Data Write	1	P3[7]	P3[6]	P3[5]	P3[4]	P3[3]	P3[2]		P3[0]	3rd pixel Data Write
So on										

Restriction



	Status		Availability
	Normal Mode On, Idle Mod	e Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mod	e On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode	e Off, Sleep Out	Yes
	Partial Mode On, Idle Mode	On, Sleep Out	Yes
	Sleep In	,	Yes
	<u>-</u>		
	Status	Default Val	ue
	Power On Sequence	77h	
Default	SW Reset	77h	
	HW Reset	77h	
Exam	ple:		Legend
	16-bits/Pixel Mode		Command
			Parameter
	COLMOD (3Ah)		Display
Flow chart			
	1 st Parameter		Action
	(06h)		Mode
			Sequential
	18-bits/Pixel Mode		transfer



RAMWRC (3C00h): Memory Continuous Write

3C00H			RAMWRC											
Inst/Para	R/W	Ac	ldress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE	
mour ara	1000	MIPI	Other	2100	<i>-</i>				20	52	J.			
			3C00h	Х	0	0	1	1	1	1	0	0	3C	
RAMWR	R/W	3Ch	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D ₁ 4	D₁3	D₁2	D ₁ 1	D ₁ 0		
IXAIVIVIX	IX/VV	3011	:	Х	• •	:	:	:	:	:	:	:		
			N th Pixel	Х	D _N 7	D _N 6	D _N 5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0		
Description	write_n If MV(3 Data is RAMW written The co written host pr (EP - S If MV(3 Data is RAMW written registe frame r proces + 1) the Frame	Seh-B5 writte (R(2Ch to the lumn r to the ocesses SP + 186h-B5 writte (R(2Ch to the r is the memor sor sele extra	n continuin) or RAM frame me register is frame me or sends a the extra	mmand. ng from WRC(30 emory un another of a pixels a mg from WRC(30 emory un a SP and e column er comme e ignored s and Inte	the pix Ch). The cet to So till the pix Ch). The till the pix Ch). The the coregister and. If d.	el locat e colum column C and t coage re nd. If th ored. el locat e page eage re lumn re er equa the nul	ion after register en en uml ion after register en	er the wester is the regular of per the were the were the were the content of pixels were the content of pixels were the were the content of pixels were the content	rite ran hen inc s the E ter is in the Enc pixels e rrite ran n incre he End mentec umn (E exceed	ige of the rement nd Coloremer I Page xceeds age of the mented Page (d. Pixels C) values (EC)	ne preved and umn (E oted. Pi (EP) value (EC – ne preved and pi EP) value are we e or the e o	ious pixels C) va xels are alue or SC + 1 ious xels are lue. The ritten to e host 1) * (E	are lue. e tthe) * e e page	



	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Ou	t Yes
	Normal Mode On, Idle Mode On, Sleep Ou	t Yes
Register Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status Defa	ault Value
-		mory is set randomly
Default		emory is not cleared
		emory is not cleared
	TIW Neset Contents of the	emory is not cleared
Flow chart	RAMWRC (3Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command	Legend Command Parameter Display Action Mode Sequential transfer



RAMRDC (3E00h): Memory Continuous Read

3E00H						RA	MRDC						
Inst/Para	R/W	Ac	ldress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
movi ara	1,7,7,	MIPI	Other	2.00)		1	.			J .	20	,
			3E00h	Х	0	0	1	1	1	1	1	0	3E
RAMRDC	R/W	3Eh	1 st Pixel	Х	D ₁ 7	D₁6	D₁5	D ₁ 4	D₁3	D ₁ 2	D ₁ 1	D ₁ 0	
KAWIKDC	IX/VV	JLII	:	Х	:	:	:	:	:	:		:	
		his commar	N th Pixel	Х	D _N 7	D _N 6	D_N5	D _N 4	D _N 3	D _N 2	D _N 1	D _N 0	
Description	If MV(3 Data is RAMW written The co written host pr (EP – 3 If MV(3 Data is RAMW written registe frame proces + 1) the Frame When ignored	memor 36h-B5 s writte /R(2Ch to the socesse SP + 1 36h-B5 s writte /R(2Ch to the r is the memor sor ser e extra Memor the train	n continuin) or RAM frame me register is frame me or sends a the extra i) = 1: In continuin or RAM frame me en reset to ry until the nds anoth a pixels are ory Accessorsfer num	mmand. ng from WRC(30 emory un then resemory un another of a pixels a ng from WRC(30 emory un o SP and e column er comme e ignored s and Intel ber of da d follow a	the pix Ch). The cet to Solutil the pix Ch). The till the pix Ch). The till the pix the concepts	el locate column C and to cage rend. If the cage render e quaethe nuisetting eeds (E	ion aftern register en en uml ion after register en uml ion after reg	er the wester is the requals to ber of pure the were the were the were the were the were the column of pixels WEMO ET(2Bh	rrite ranchen incomplete incomple	age of the rement of Colorement Page (Page	ne prevented and umn (E nted. Pi (EP) value (EC – he prevented and pi EP) value or the - SC + exceedir	ious pixels C) va xels ar alue or SC + 1 ious xels ar lue. The ritten to e host 1) * (E	are lue. e the) * e pag o the P – S will b
Restriction	write lo	cation	rite should . Otherwis written to	se, data	written	with R							



	Status		Availability	
	Normal Mode On, Idle Mode	Off, Sleep Out	Yes	
Register	Normal Mode On, Idle Mode	On, Sleep Out	Yes	
Availability	Partial Mode On, Idle Mode (Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode (On, Sleep Out	Yes	
	Sleep In		Yes	
	Status	Default \	Value	
Default	Power On Sequence C	ontents of memory	y is set randomly	,
	SW Reset 0	Contents of memor	ry is not cleared	
	HW Reset C	Contents of memor	ry is not cleared	
Flow chart	RAMWRC (3Ch) Image Data D1[B:0],D2[B:0]Dn[B:0] Any Command		Par D A Sec	egend mmand ameter display action Mode quential ansfer



STESL(4400h): Set_Tear_Scanline

STESL(4400	11 <i>)</i> . 3	el_lea	ar_Sca	niine									
4400H					STESL	_(Set_	Γear_S	canlin	e)				
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISI/Faia	IX/VV	MIPI	Other	D13-0	D1	D0	D3	D4	D3	DZ	Di	D0	TILX
STESL	W	44h	4400h	Х	STS[15]	STS[14]	STS[13]	STS[12]	STS[11]	STS[10]	STS[9]	STS[8]	00
			4401h	Х	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00
Description	the dis B4. Th Line m	splay rea ne Tearii	aches lin ng Effect	n the disp e N. The Line On	TÉ sigr	nal is n	ot affec	ted by	changi cribes	ng set_	_addres	ss_mo	de bit utput
	The T	earing E	ffect Ou	tput line s	hall be	active	low wh	en the	display	/ modu	le is in	Sleep	mode.
Restriction													
		ĺ	Status						Av	ailabili	tv		
			Norma	Mode O	n, Idle	Mode	Off, SI	eep Ou					
Register			Norma	Mode O	n, Idle	Mode	On, SI	еер Оι	ıt Ye	s			
Availability			_	Mode Or		_							
				Mode Or	i, idle i	Mode (On, Sle	ep Out	Ye:				
			Sleep I	n					Te	5			
Default				Status Power Or SW Rese HW Rese	t	ence	STS STS	ault Val [15:0]= [15:0]= [15:0]=	:16'h00 :16'h00	000			
Flow Chart			Send 1st p	tear_scanlin	e [8]					Acti Mo	nand neter		



GSL (4500h): Get_Scanline

4500H					GSI	_(Get_	Scanli	ne)					
Inst/Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
mour ara	1,7,1,	MIPI	Other	2100				<u> </u>					
001	_	45h	4500h	Х	GTS[15]	GTS[14]	GTS[13]	GTS[12]	GTS[11]	GTS[10]	GTS[9]	GTS[8]	0x
GSL	R	45h	4501h	х	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	numbe first sc	er of sca an line i	n lines on s defined	current so a display as the firs e value re	device at line o	is def of V-Sy	ined as nc and	s VSYN I is den	V + V oted a	BP + \ s Line	/ACT +		
Restriction	-	Status Availability											
		Γ	Status						Ava	ailabili	ty		
			Normal I	Mode On	, Idle N	lode C	ff, Sle	ep Ou	Yes	•			
Register			Normal I	Mode On	, Idle N	lode C	n, Sle	ep Ou	Yes	5			
Availability			Partial M	lode On,	Idle M	ode O	ff, Slee	p Out	Yes	5			
		_		lode On,	ldle M	ode O	n, Slee	p Out	Yes	-			
			Sleep In						Yes	5			
Flow Chart		Send 1st	get_scanline Wait 3us ummy Read parameter GTS				Con Para	gend nmand ameter Display ction Mode equential transfer					



DSTBON (4F00h): Deep Standby Mode On

4F00H	0011).	Deep	Stariu				Stand	by Mod	la On)				
4F00H		l		Di		(Deeb	Stand	by woo	ie On)	I	I	I	
Inst/Para	R/W	Add MIPI	ress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSTBON	W	4Fh	4F00h	Х	0	0	0	0	0	0	0	DSTB	00
Description	DSTB: Notes: 1. To 2. Fo	="1", ent : o exit De or MIPI I	d is used ter deep ep Stan F, if deep -D1_P/N	standby dby Mod standb	mode de, inpu y mode	It low p	ulse mo	ore than se pull	HSSI_0	CLK_P		ζ.	
Restriction	-												
		[Status						Av	/ailabil	ity		
				l Mode	On, Idl	e Mode	Off, S	leep O					
Register			Norma	l Mode	On, Idl	e Mode	On, S	leep O	ut Ye	es			
Availability		-		Mode C									
			Partial Sleep I	Mode C	n, Idle	Mode	On, SI	eep Ou	it Ye				
			Sieepi						16	53			
			Status					Default	Value				
D - (- 1)			Power C	n Sequ	ence	7)0h	raido			1	
Default		3	SW Res	et			(00h					
		l	HW Res	et			(00h					
Flow chart		Parar	TBON (4F	B=1						P	Display Action Mode equentia		



WRDISBV (5100h): Write Display Brightness

5100H				, , , , , , , , , , , , , , , , , , ,	g		RDISB	V					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	W	51h	5100h	х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF
		ciple rela	is used to					st brigh	tness ar	nd FFh v	/alue me	eans the	highest
Description													
Restriction	The d	isplay s	upplier o	annot u	se this	comma	and for	tuning					
			Ctatura						Α.	انطماني	1:4		
			Status	l Mode	On Idl	e Mode	e Off S	Sleen C		vailabil	lity		
Register				I Mode									
Availability				Mode (
				Mode (
			Sleep						Y				
			Status					Defaul	t Value)			
Default			Power	On Seq	uence			FFh					
Deladit			SW Res	set				FFh					
			HW Re	set				FFh					
Flow chart		Para	RDISBV (5	/[7:0]						P	Legend Commander Parameter Display Action Mode Requenti transfer	d er	



RDDISBV (5200h): Read Display Brightness

5200H							DISBV						
L - 1/D	D 44/	Add	dress	D45.0	D.7	Do	De	D.4	Do	Do	D4	Do	LIEV
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	R	52h	5200h	Х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF
Description		ole relat		rightness v s that 00h v		eans the	e lowest	brightn	ess and	l FFh va	alue mea	ans the	highest
Restriction	-												
			_										
		-	Status	l Mode O	n Idla	Mode	Off SI	oon Oi		ailabili s	ty		
		=		l Mode O	*		-						
Register Availability		=		Mode Or				·					
		-		Mode Or									
		ļ	Sleep I	n					Ye	S			
		•	Status				D	efault	Value				
		ı	Power C	n Seque	nce		F	Fh					
Default			SW Res	et			F	Fh					
Doraun		ı	HW Res	et			F	Fh					
	RDD	DISBV (52hH)			Lege	end						
Flow Chart		nd param DBV[7:0	neter	Host Driver	(Param Disp Acti Moo	lay on de						



WRCTRLD (5300h): Write Display Control

5300H		,		, p. 1.1.			RDISB	V					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	W	53h	5300h	х	0	0	BCTRL	0	DD	0	0	0	28
Description			ness cont										
Restriction	The d	isplay s	upplier c	annot u	se this	comm	and for	tuning					
Register Availability Default			Norma Partial Partial Sleep Status	I Mode I Mode (Mode (Mode (In On Sequence)	On, Idle On, Idle On, Idle	e Mod	e On, S e Off, SI e On, SI	Bleep O	Out Yout Yout Yout Yout You	es es es	lity		
Flow chart		Para	RDISBV (5	/[7:0]							Legend Commander Paramete Display Action Mode Eequentiitransfer	d der	



RDCTRLD (5400h): Read Display Control

5400H			<u> </u>	,		RDI	DISBV						
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	R	54h	5400h	х	0	0	BCTRL	0	DD	0	0	0	28
Description				rol ,1=enab ntrol ,1=ena									
Restriction	-									1			
		ſ	Status		_	_	_	_	Δν	ailabili	tv		
				I Mode O	n, Idle	Mode	Off, SI	еер Оі			Ly		
Register				l Mode O	-								
Availability		-		Mode Or	<u> </u>			_					
			Sleep I	Mode Or n	i, idie i	wode (Jn, Sie	ep Ou	Ye Ye				
		L											
		;	Status				D	efault '	Value				
		l	Power C	n Seque	nce		28	3h					
Default			SW Res				28					_	
		L	HW Res	et			28	3h					
						Lege		-7					
	RDD	DISBV (52hH)	Host	Г	Comn							
		<u> </u>	7	Driver	_	Paran	neter						
	Se	nd param DBV[7:0	neter		<	Disp							
Flow Chart			_/			Mo	=						
						Seque							
						trans	ster						



RDCTRLD (5500h): RAD_ACL Control

5500H			_			RDE	DISBV						
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRADACL	W	55h	5500h	Х	0	0	0	0	0	0	RAD_A	CL[1:0]	00
Description	RAD_A	CL[1:0]	=11, Ena	o control R ble Raydiu able Raydiu	ım ACL	function	٦.	on for A	CL (Aut	o Curre	nt Limit))	
Restriction	-												
		ſ	Status						Av	ailabili	ity		
		-		Mode O									
Register Availability		-		Mode O				-					
rtvanability		-		Mode On Mode On	-	_							
		<u>-</u>	Sleep I		,				Ye				
		3	Status				D	efault '	Value				
		I	Power C	n Seque	nce		28	3h					
Default			SW Res	et			28	3h					
Delault		ı	HW Res	et			28	3h					
Flow Chart		od param DBV[7:0	eter	Host Driver	(Comm Param Disp Action Moc	neter lay on de						



IMGEHCCTR (5800h): Set_color_enhance

MGEHCCTR	(580	10h):	Set_cc	olor_	<u>enhar</u>	ice							
5800H					WI	RCE (se	et_colo	r_enha	nce)				
Inst/Para	R/W	Add MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCE	W	58h	5800h	х	0	0	0	0	0	SLR_EN	SLR_LEV EL1	SLR_LEV EL0	00
Description		R_EN	EL[1:0]	Sun Enh Sun	light Rea	adable nt Enal			'1': e	e disable; nable 2, low to h	nigh		
Restriction	-												
Register Availability			Norma Partia	al Mod I Mod I Mod	de On, e On, I	Idle Mo	ode On, de Off,	Sleep C Sleep C Sleep C	Out Out	Availa Yes Yes Yes Yes Yes	bility		
Flow Chart		Con Part	gend nmand Display Etion Mode equential transfer	7									



IMGEHCCTR (5900h): Read_color_enhance

MGEHCCIR	(390	UII) . F	reau_u	JOIOI_E	iiiiaii	Ce								
5900H					RDCI	E (set_	color_c	enhand	ce)					
Inct/Dave	DAA	Add	ress	D45.0	D-7	DC	Dr	D4	D0	D0	2	D C	ПСЛ	
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
RDCE	R	59h	5900h	Х	0	0	0	0	0	SLR_EN	SLR_LEV EL1	SLR_LE VEL0	00	
	D:			D-	! !! -				\/=l					
	Bit	R_EN		Sui	scriptio nlight Re	eadable			Value '0' : dis	sable;				
	SLI	X_EIN				ent Ena	able		'1': en	able				
	SLI	R_LEVE	L[1:0]			eadable ent Lev	⁄el		0~2,	low to hi	igh			
Description														
Restriction	-													
Register Availability			Norma Partial Partial		On, Idle	e Mode Mode	On, S Off, SI	leep O eep Ou	ut ut ut it		oility			
Flow Chart		Partial Mode On, Idle Mode On, Sleep Out Sleep In Legend Command Parameter Display Action Mode Sequential transfer												



CESLRCTR (5A00h): Set_color_enhance1

CESLRCTR (JAUL	/n) : 8	et_co	ior_e	ennanc	e i							
5A00H					CESL	RCTR (set_co	lor_enh	nance1)				
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8		D6	D5	D4	D3	D2	D1	D0	HEX
CESLRCTR	W/R	5Ah	5A00h	Χ	SLR_AM BI_IN7	SLR_AM BI_IN6	SLR_AM BI_IN5	SLR_AM BI_IN4-	SLR_AM BI_IN3	SLR_AM BI_IN2	SLR_AM BI_IN1	SLR_AM BI_IN0	00
						41			1,,,				
	Bit				Descrip				Value	9			
	SL	R_AMB	SI_IN[7:0]		Low byt	e of amb	ient ligh	t value	00h				
Description													
Restriction													
Register Availability			Norm Partia	al Mo al Mo al Mod	de On, de On, de On, le de On, le	Idle Mo	de On, de Off,	Sleep C	Out Out	Availa Yes Yes Yes Yes	bility		
Flow Chart		Com Para C Ac Se	mand meter Display Etion Mode equential transfer	>									



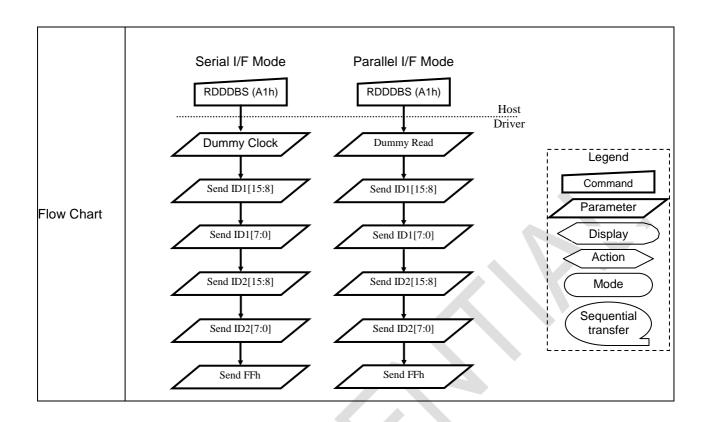
CESLRCTR (5B00h): set_color_enhance1

5B00H	(5B00n) : set_color_ennance1 CESLRCTR (set_color_enhance1)												
	A		ress									'	
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CESLRCTR	W/R	5Bh	5B00h		SLR_AM BI_IN15	SLR_AM BI_IN14	SLR_AM BI_IN13	SLR_AM BI_IN12-	SLR_AM BI_IN11	SLR_AM BI_IN10	SLR_AM BI_IN9	SLR_AM BI_IN8	00
	Bit			Value									
	SLR_AMBI_IN[15:8]				escription igh byte c		nt light v	00h					
Description													
Restriction	-												
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In										oility		
Flow Chart	Legend Command Parameter Display Action Mode Sequential transfer												



RDDDBS(A100h): Read_DDB_Start

A100H	RDDDBS(Read_DDB_Start)													
Inst/Para	R/W	Address MIPI Other		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
RDDDBS	R	A1h	A100h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0	
			A101h	х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01	
			A102h	х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80	
			A103h	х	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90	
			A104h	х	1	1	1	1	1	1	1	1	FF	
Description	1st parameter: Supplier ID code 2nd parameter: Supplier ID code 3rd parameter: Module ID 4th parameter: Module ID 5th Exit code (FFh).													
Restriction														
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default														
		Statu	s	Default Value										
							After MTP Before			MTP				
		Powe	r On Se	equence		MTP	MTP Value 01h, D			00h, 90h, 60h, FFh				
		SW R	W Reset				Value	01h, D0h, 90h, 60h, FFh			h			
		HW F	Reset			MTP	TP Value 01h, D0h, 90h, 60h, FF				h			

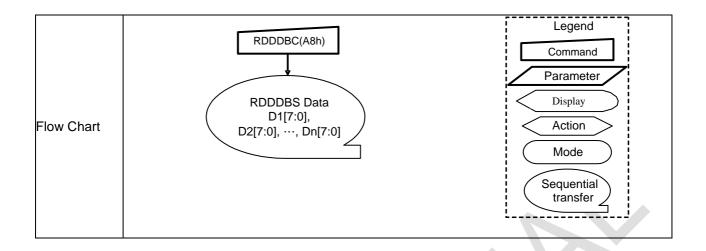




RDDDBC(A800h): Read DDB Continous

A800H				B Con		F	RDDDB	С					
		Ado	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			A800h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0
			A801h	х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01
RDDDBC	R	A8h	A802h	Х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80
			A803h	х	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90
			A804h	х	1	1	1	1	1	1	1	1	FF
Description	point Note: block Note: 1. Se 2. Re	te: For use example, Set maximum return packet size=3 Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]											
	A Rea	Read 0xA8, return 2 bytes MID[15:8], RID[7:0], RID[15:8] and 0xFF Read DDB Start command (RDDDBS) should be executed at least once before a Read DB Continue mmand (RDDDBC) to define the read location. Otherwise, data read with a Read DDB ontinue c ommnd is undefined.											
Restriction	DDB comn	Contin nand (F	ue RDDDB	C) to de	fine the								
Restriction	DDB comn	Contin nand (F	ue RDDDB	C) to de is undef	fine the				ise, dat		with a R		
Restriction	DDB comn	Contin nand (F	e RDDDB ommnd	C) to de is undef	fine the ined.	read lo	cation.	Otherw	ise, dat	a read v	with a R		
Register	DDB comn	Contin nand (F	Stat	C) to de is undef us	fine the ined.	read lo	de Off,	Otherw Sleep	A Dut	a read v	with a R		
Register	DDB comn	Contin nand (F	Stat Norr	C) to de is undef	fine the fined. de On, l	read lo	de Off,	Otherw Sleep	A Dut Y	a read v	with a R		
Register	DDB comn	Contin nand (F	Stat Norr Part	C) to de is undef us mal Mod ial Mod	de On, lee On, lee On, lee On, lee	read lo	de Off, de On,	Sleep (Sleep C	Out YOut YOut YOut Y	a read v	with a R		
Register	DDB comn	Contin nand (F	Stat Norr Part	C) to de is undef us mal Mod ial Mod	de On, lee On, lee On, lee On, lee	read lo	de Off, de On,	Sleep (Sleep C	Out YOut YOut YOut Y	vailabi es es	with a R		
Register	DDB comn	Contin nand (F	Stat Norr Part	C) to de is undef us mal Mod ial Mod	de On, lee On, lee On, lee On, lee	read lo	de Off, de On,	Sleep (Sleep C	Out YOut YOut YOut Y	a read v	with a R		
Register	DDB comn	Continnand (I	Stat Norr Part Slee	C) to de is undef us mal Mod ial Mod	de On, le e On, le	read lo	de Off, de On, le On,	Sleep (Sleep C	Out YOut YOut YOut Y	a read v	with a R		
Register	DDB comn	Contin nand (F	Stat Norr Part Slee	C) to de is undef us mal Mod ial Mod	de On, le e On, le	Idle Mo	de Off, de On, de On, Value	Sleep (Sleep C	Out YOut YOut YOUT	a read v	with a R		
Register Availability	DDB comn	Continnand (Finue co	Stat Norr Part Slee	C) to de is undef us mal Mod ial Mod	de On, le On, le	dle Modelle Mo	de Off, de On, see On,	Sleep (Sleep C	Dut Y Dut Y Out Y Out Y	vailabi es es es es	lity		
Restriction Register Availability Default	DDB comn	Continuand (Innue continue con	Stat Norr Part Slee	C) to de is undef us mal Mod ial Mod ep In	de On, le On, le On, le	read lo	de Off, de On, de Off, see On,	Sleep C Sleep C Sleep C	ADut Y Dut Y Dut Y Out Y Out Y Out Y	vailabi es es es es es	lity		







RDFCS(AA00h): Read First Checksum

AA00H							RDFCS	3					
Inst/Para	R/W	Add	Iress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
111301 414	17,44	MIPI	Other	סום	זט	D0	D3	DŦ	D3	DZ	Di	D0	TILX
RDFCS	R	AAh	AA00h	х	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	Set" a regist acces	area ters (no ss to th	ot includ ose	rns the f le "Manu me mem	ıfacture	Comm	and Se						
Restriction	area			to wait 1 re can re					rite acc	ess on	"User C	ommar	nd Set'
		Status							Avai	ilability	<u> </u>		
				On, Idl	e Mode	Off, SI	leep Οι	ıt	Yes	liability			
Register		Norma	al Mode	On, Idl	e Mode	On, SI	eep Ou	ıt	Yes				
Availability		Partia	Mode	On, Idle	Mode	Off, Sle	ep Out		Yes				
		Partia	Mode	On, Idle	Mode	On, Sle	ep Out		Yes				
		Sleep	In						Yes				
Default		Status Powe S/W F H/W F	r On Se Reset	quence		C	Default V OOh OOh OOh	√alue					
Flow Chart			[RDFCS Send Pa FCS[rameter					P. Se	Legend Command aramete Display Action Mode equentia transfer		



RDCCS(AF00h): Read Continue Checksum

AF00H							RDCCS	5					
Inst/Para	R/W	Add MIPI	lress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCCS	R	AFh	AF00h	х	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	the fir	rst ksum h	as calc	rns the outline the control of the c	om "Us	er Com	mand S	et" area	a registe	ers and	the frar	•	
Restriction				to wait 3 e there								Commar	nd Set"
		01-1-							A	1.1114	<u> </u>		
		Statu		de On, lo	dlo Mod	40 Off	Sloop C) i i t	Yes	ability			
Register				de On, lo					Yes				
Availability		Parti	al Mod	e On, Id	le Mod	e Off, S	leep O	ut	Yes				
		Parti	al Mod	e On, Id	le Mod	e On, S	leep O	ut	Yes				
		Slee	p In						Yes				
Default		Status Power S/W F	r On Se Reset	quence				Defa 00h 00h 00h	ault Valu	Je			
Flow Chart				Send Pa CCS	rameter					P	Legend Command aramete Display Action Mode equentia transfer		



SetHBMMode (B000h): Set_HBM Mode

<u>SetHBMMod</u>	e (Ro	<u>(00h</u>	: Set_F	IBM	<u>Mode</u>								
В000Н						Se	tHBMM	ode					
In at/Dara	DAM	Add	dress	245.0	D7	DC	DE	C /	, D2	Do	D4	Do	HEX
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	1 D3	D2	D1	D0	
SetHBMMode	W/R	B0h	B000h	х	0	0	0	0	0	1	HBM_E N	0	04
	Е	Bit		Des	cription				Value				
	F	IBM_E	N	High	n brightn	ess mod	le selecti	on	HBM_EN=	:1: Seled	ct HBM m	node	
Description													
Restriction							V						
			Status	5						Availa	bility		
			Norma	al Mod	de On,	ldle Mo	de Off,	Slee	ep Out	Yes			
Register							de On,		_	Yes			
Availability							de Off,			Yes			
					e On, l	dle Mod	de On,	Slee	o Out	Yes			
			Sleep	ln						Yes			
Flow Chart	2	Com Pars	gend Inmand Inma										



SetDSIMode (C200h): set_DSI Mode

C200H	(020	<u> </u>	<u> </u>	11110		Se	etDSIMe	ode					
Inst/Para	R/W			015-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SetDSIMode	W/R	MIPI C2h	Other C200h		0	0	0	0	0	0	DM1	DM0	00
SelDSilviode	VV/IX	CZII	C20011	Х	U	U	U	0	0	U	DIVIT	DIVIO	00
Description		Bit DM[1:0]			cription	ng mode	selection	n	Value 2'b00: inte 2'b01: rese 2'b10: VS\ 2'b11: exte HSYNC al	erved YNC alig ernal timi	n mode ing (VSY	NC+	
Restriction	Note: (1) If	video	mode, ne	eed to	set DN	M[1:0] =	2'b11.						
			Status		do On	Idlo Ma	de Off	Clas	n Out	Availa	bility		
Dogistor					-	Idle Mo			-	Yes Yes			
Register Availability						dle Mod			-	Yes			
						dle Mod				Yes			
			Sleep		,		,			Yes			
Flow Chart		Com Pars L Ad	gend mand meter Display Ction Mode equential transfer										

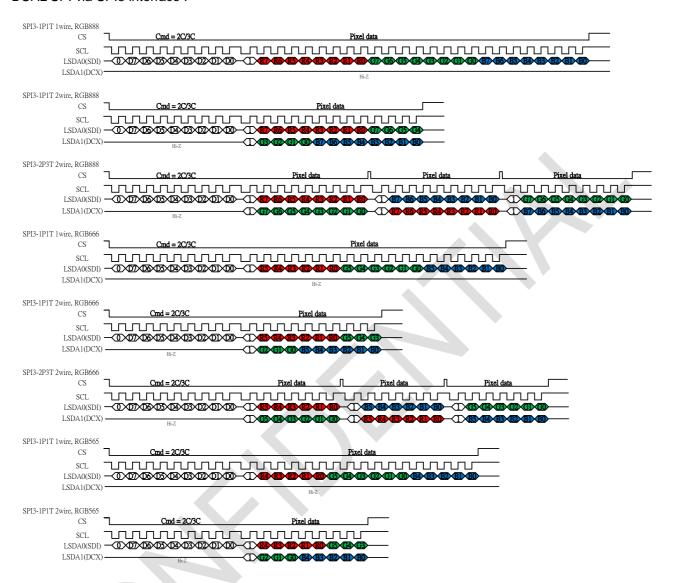


SetDSPIMode (C400h): set_DSPI Mode

C400H	C (O-	10011)	. 301_2	, <u> </u>	Mode	Set	: DSPI r	node	е					
Inst/Para	R/W	MIPI	Other	015-8	D7	D6	D5	D.		D3	D2	D1	D0	HEX
SetDSPIMode	W/R	C2h	C200h	Х	ĀM	-	FG1	FG			-	-	N	00
	E	Bit		Des	cription					lue				
	С	SPI_EN	I	DAU	JL SPI N	ODE E	nable		1:	disable enable				
Description	С	SPI_CF	⁻ G[1:0]		JL SPI W				10 11	: 1P1T f	or 1 wire or 2 wire or 2 wire ed)		
Description	S	SPI_WRA	AM	SPI/ Mak befo	command SPINK into ing sure to re host wi SPINK into	terfaces. o set SPI rites SR <i>A</i>	_WRAM=	:1		disable SPI inte	rface wr	ite RAM	l enable	
	Note	: detail	ed DAUL	SPI	formats	are des	scribed	at ne	ext p	page.				
Restriction														
			Status				$\underline{}$				Availa	hility		
					de On,	Idle Mo	ode Off,	Sle	ep (Out	Yes	Dinity .		
Register			Norma	al Mo	de On,	Idle Mo	de On,	Sle	ер (Out	Yes			
Availability			Partia	Mod	le On, le	dle Mo	de Off,	Slee	рΟ	ut	Yes			
			Partia	Mod	le On, le	dle Mo	de On,	Slee	рO	ut	Yes			
			Sleep	In							Yes			
Flow Chart		Com Pars L A Si	gend Immand Display Edion Mode equential transfer	7										

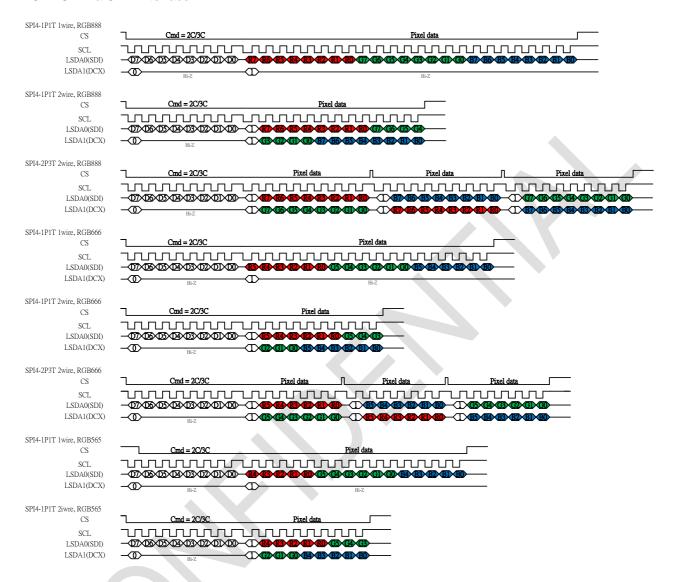


DUAL SPI via SPI3 interface:





DUAL SPI via SPI4 interface:





RDID1 (DA00h): ID1 Code

0XDA00h						WI	RDID								
lu atrivati a n	D/M	Ad	dress					Paran	neter						
Instruction	R/W	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
WRDID	R	0xDAh	0XDA00h	00h				ID1	[7:0]				0x00h		
	This	comma	ind is for N	Module Ma	anufac	cture N	lumbe	r					•		
Description		E	Bit		Desc	ription				Dat	а				
Description		ID1	[7:0]	Module	dule Manufactor Number										
	,			1											
Restriction															
				Status					A	vailabil	ity				
		Norma	al Mode O	n, Idle Mo	de Of	f, Slee	p Out			Yes					
Register		Norma	al Mode O	n, Idle Mo	de Or	, Slee	p Out			Yes					
Availability		Partia	l Mode Or	n, Idle Mo	de Off	, Slee	Out			Yes					
		Partia	l Mode Or	n, Idle Mo	de On	, Slee	o Out			Yes					
				Sleep In						Yes					
													=		
			Status					Defau	lt Value	е					
			Status				0x	DAh /	0XDA	00h					
Default		Pow	er On Sec	quence				0x	00h						
			S/W Res	et				0x	00h						
			H/W Res	et				0x	00h						
													=		



RDID2 (DB00h): ID2 Code

0XDB00h						WI	RDID						
lu atmustis a	DAM	Ad	dress					Paran	neter				
Instruction	R/W	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDID	R	0xDBh	0XDB00h	00h				ID2	[7:0]				0x80h
	This	s comm	and is for	Module/E	Priver '	Versio	n Num	ber					
Description		i	Bit		Desc	ription				Dat	a		
Description		ID2[7:0] Module/Driver Version Number											
Restriction													
		Otation Availability											
				Status					A۱	/ailabil	ity		
		Norma	al Mode O	n, Idle Mo	de Of	f, Slee	p Out			Yes			
Register		Norma	al Mode O	n, Idle Mc	de Or	n, Slee	p Out			Yes			
Availability		Partia	l Mode Or	n, Idle Mo	de Off	, Slee	Out			Yes			
		Partia	I Mode Or	n, Idle Mo	de On	, Slee	Out			Yes			
				Sleep In						Yes			
													-
			Otatus					Defau	lt Value	Э			
			Status		*		0x	DBh /	0XDB(00h			
Default		Pow	er On Sec	quence				0x	80h				
			S/W Res	et				0x	80h				
			H/W Res	et				0x	80h				
													4



RDID3 (DC00h): ID3 Code

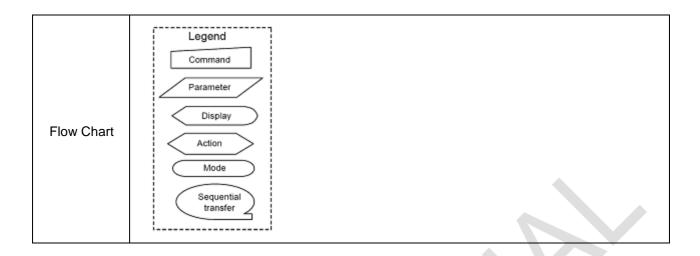
0XDC00h						WI	RDID						
lu atrivati a n	D/M	Add	dress					Paran	neter				
Instruction	R/W	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDID	R	0xDCh	0xDC00h	00h				ID3	[7:0]				0x00h
	This	comma	nd is for I	Module / [Driver	ID							
Description		Bit Description Data											
Description		ID3[7:0] Module /Driver ID											
	'												
Restriction													
													1
				Status					A۱	vailabil	ity		ł
			l Mode O	-			•			Yes			4
Register		Norma	l Mode O	n, Idle Mo	de Or	n, Slee	p Out			Yes			
Availability		Partia	l Mode Oı	n, Idle Mo	de Off	, Slee	o Out			Yes			
		Partia	l Mode Oı	n, Idle Mo	de On	, Slee _l	o Out			Yes			
				Sleep Ir						Yes			
	,												
			4										=
			Chatria					Defau	lt Value	е			
		Status 0xDCh / 0xDC00h											
Default		Pow	er On Sed	quence				0x	00h				
			S/W Res	et				0x	00h				
			H/W Res	et				0x	00h				
				_			_		_	_	_		=



(FE00h): CMD Mode Switch

FEOUN): CIVID	Mod	ode Switch											
FE00H			N	MAUCCT	R (Man	ufactu	re Cor	nmand	Set C	ontrol)		
Instruction	R/W	Add	dress		Т	Т		Param	eter	1	T	ı	T
	17/44	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CMD Mode Switch	W	FEh	FE00h	00h	СМІ	D_REA	DKEY	[3:0]	C	CMD_P	age[3:0	0]	00
	CME This	REA	.DKEY[3	sed to read to read to sw								er	
	CI	CMD_Page[3:0] Hex Value Description											
Description		0000 00h (default) User Command Set (UCS = CMD1)											
		0001 01h Manufacture Command Set Page0 (CMD2 P0)											
		001	0	0	2h	Ma	nufactu	ire Com	mand S	Set Page	e1 (CM	D2 P1)	
		010	00	0-	4h	Ma	nufactu	ire Com	mand S	Set Page	e3 (CM	D2 P3)	
		010)1	0	5h	Ma	nufactu	ire Com	mand S	Set Page	e4 (CM	D2 P4)	
Restriction	-												
				Sta	itus					Availal	oility		
		Nori	mal Mod	le On, Idle	Mode	Off, SI	еер О	ut		Yes	3		
Register		Nori	mal Mod	le On, Idle	Mode	On, SI	еер О	ut		Yes	6		
Availability		Par	tial Mode	e On, Idle	Mode	Off, Sl	еер Оц	ıt		Yes	6		
		Par	tial Mod	e On, Idle	Mode	On, Sl	еер Оц	ıt		Yes	3		
				Slee	p In					Yes	8		
		S	tatus					Defa	ult Valı	ue			
								FEh	/ FE00)h			
Default	Po	wer O	n Seque	ence					00h				
		S/M	/ Reset						00h				
		H/W	/ Reset						00h				
		H/W	/ Reset						00h				



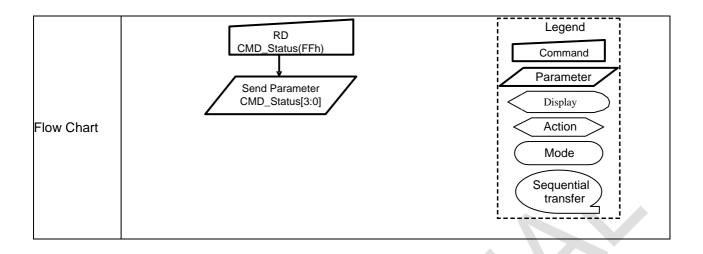




(FF00h): Read CMD Status

(FF00h): Read	CIVIL												
FF00H				MAUCCTI	R (Mar	ufactu	ure Cor	nmand	Set C	ontrol)		
Instruction	R/W	Add	dress		I	I	1	Param	eter	I	I		I
		MIPI	Others		D7	D6	D5	D4	D3	D2	D1	D0	HEX
RD CMD Status	R	FFh	FF00h	00h	0	0	0	0		MD_St			00
				sed to sw	itch the	e Manu	ufacture	Comn	nand P	ages a	nd Use	er	
	Com	mands	s sets.										
	СМ	D_Stat	_Status[3:0] Hex Value Description										
		0000 00h (default) User Command Set (UCS = CMD1)											
Description		0001 01h Manufacture Command Set Page0 (CMD2 P0))		
Docompaion		0010 02h Manufacture Command Set Page1 (CMD2 P1))	
		001	11		03h	N	/lanufact	ture Cor	mmand	Set Pag	ge2(CN	MD2 P2)
		010	00		04h	N	/lanufact	ture Cor	nmand	Set Pag	ge3(CN	MD2 P3)
		010	01	1	05h	Ŋ	/lanufact	ture Cor	mmand	Set Pag	ge4(CI	MD2 P4)
				l									
Restriction	-												
				Sta	itus					Availal	oility		
		Norr	mal Mod	e On, Idle	e Mode	Off, S	leep Ou	ut		Yes	6		
Register		Norr	mal Mod	e On, Idle	Mode	On, S	leep O	ut		Yes	5		
Availability		Par	tial Mod	e On, Idle	Mode	Off, SI	leep Ou	ıt		Yes	5		
		Par	tial Mod	e On, Idle	Mode	On, SI	leep Ou	ıt		Yes	6		
				Slee	ep In					Yes	3		
		Status Default Value											
		FFh / FF00h											
Default	Po	Power On Sequence 00h											
		S/W	/ Reset						00h				
		H/W	/ Reset						00h				







7. Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM67162 is used out of the absolute maximum ratings, the RM67162 may be permanently damaged. To use the RM67162 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM67162 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 5.5	V
Power supply voltage	VDD (VDDA, VDDB, VDDR)	-0.3 ~ + 5.5	V
Cumply valte as (MAV)	AVDD-AVSS	-0.3 ~ + 6.6	V
Supply voltage (MV)	VCL-AVSS	-0.3 ~ + 6.6	V
Supply voltage (HV)	VGH - VGLX	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C
	·		

Notes:

If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	Pass 3KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass 300V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.



7.4 DC Characteristics

7.4.1 Basic Characteristics	Symbol	Condition	Min.	Тур.	Max.	Unit	Related Pins
Parameter							
Analog Power Supply Voltage	VDD	Operation Voltage	2.7	2.8	3.6	V	Note 1
1/0 : 5	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1,2
/O pin Power Supply Voltage							
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 3
Logic High level Output voltage	VOH	lout = -1 mA	0.8* VDDI	-	VDDI	V	Note 3
Logic Low level Output voltage	VOL	lout = +1 mA	0.0	-	0.2* VDDI	V	Note 3
Logic High level input current (Except MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (Except MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
Logic High level input current (MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
AVDD booster voltage	AVDD		4.5		6.5	V	Note 3
VCL booster voltage	VCL		-3.5		-5	V	Note 3
VGH booster voltage	VGH		AVDD		2AVDD	V	Note 3
VGL booster voltage	VGL		VCL		VCL -AVDD	V	Note 3
Voltage difference between VGH and VGL	VGHL	VGH-VGL			30	V	Note 3
Gamma reference voltage	VGMP		2.0		6.0	V	Note 3,4
Gamma reference voltage	VGSP		0.0		4.5	V	Note 3
OSC	Face		20.24	22	23.76	MHz	
USU	Fosc	0.015 AVDD 4.01/	20.24	22	23.70	IVITIZ	TDD
Channel deviation voltage	V_{DEV}	Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V				mV	TBD
Channel deviation voltage	V_{DEV}	1.0V < Sout < AVDD-1.0V				mV	TBD

Notes:

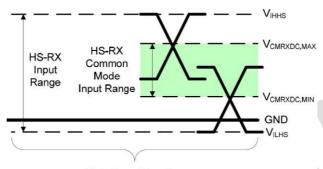
- 1. VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
- 2. Recommend VDDI=1.8V for power saving.
- 3. Ta(ambient temperature) ranges from -30° C to 85 $^{\circ}$ C.
- 4. $VGMP \le AVDD 0.2V$



7.5 MIPI Characteristics

7.5.1 High-Speed Receiver Specification

DC Specifications



High Speed Receiver

Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

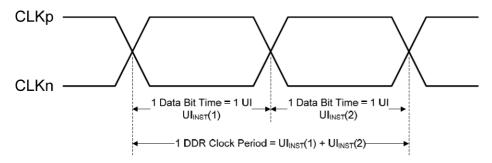
Notes:

- 1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
- 2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz



7.5.2 Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Тур	Max	Units	Notes
UI instantaneous	UI _{INST}	2		12.5	ns	1,2

Notes:

- 1. This value corresponds to a minimum 80 Mbps data rate.
- 2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

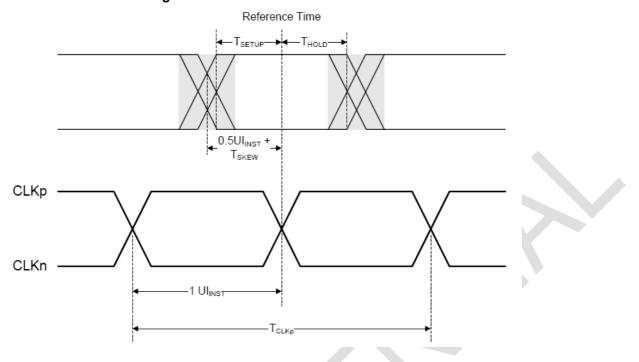
		Min	Тур	Max	Units	Notes
Data to Clock Skew [measured at transmitter]		-0.15		0.15	UI _{INST}	1
Data to Clock Setup Time [receiver]	T _{SETUP[RX]}	0.15			UI _{INST}	2
Clock to Data Hold Time [receiver]	T _{HOLD[RX]}	0.15			UI _{INST}	2

Notes:

- 1. Total silicon and package delay budget of 0.3*Ul_{INST}
- 2. Total setup and hold window for receiver of 0.3*UIINST



7.5.3 Data to Clock Timing Definitions





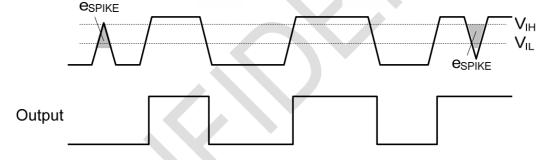
7.5.4 Low power transceiver specifications

Parameters	Symbol	Condition	Min	Тур	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE ^(1.2.3)	Fig. 2	Input pulse rejection			300	V.ps

Notes:

Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State. An impulse less than this will not change the receiver state.

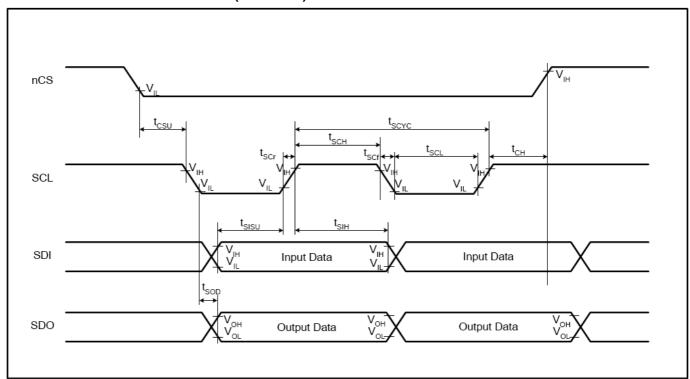
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers. Input Glitch Rejection of Low Power Receivers as follow.





7.6 AC Characteristics

7.6.1 Serial Interface Characteristics (3-wire SPI)



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	T_{SCYC}	Clock cycle (Write)	20		ns	
	T _{SCYC}	Clock cycle (Read)	300		ns	
	T _{SCH}	Clock "H" pulse width (Write)	9		ns	
SCL	T _{SCH}	Clock "H" pulse width (Read)	140		ns	
SCL	T _{SCL}	Clock "L" pulse width (Write)	9		ns	_
	T _{SCL}	Clock "L" pulse width (Read)	140		ns	
	T _{SCr} Clock rise time			2	ns	
	T_{SCf}	Clock fall time		2	ns	
nCS	T_{CSU}	Chip select setup time	10		ns	
1103	T _{CH}	Chip select hold time	10		ns	-
SDI (SDA)	T _{SISU}	Data input setup time	5		ns	
SDI (SDA)	T _{SIH}	Data input hold time	5		ns	-
SDO (SDA)	T_{SOD}	Data output setup time		120	ns	
300 (30A)	T _{SOH}	Data output hold time	5		ns	-

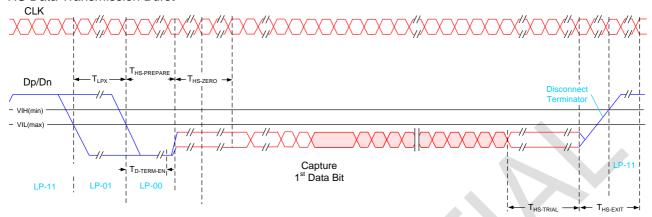
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, GND=0V

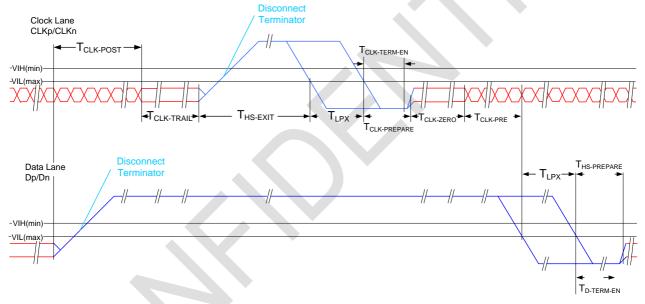


7.6.2 DSI Timing Characteristics

HS Data Transmission Burst



HS clock transmission

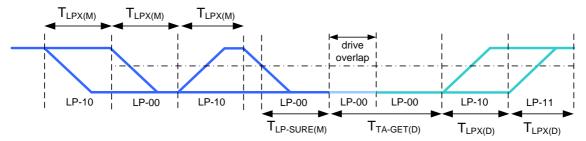




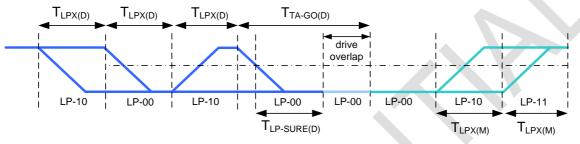
Timing Parameters:

Parameter	Description	Min	Тур	Max	Unit
T _{CLK-POST}	Time that the transmitter continues to send	60ns + 52*UI	. , , ,	Max	ns
· CLK-POST	HS clock after the last associated Data	000 1 02 01			1.0
	Lane has transitioned to LP Mode. Interval				
	is defined as the period from the end of				
	T _{HS-TRAIL} to the beginning of T _{CLK-TRAIL} .				
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0	60			ns
	state after the last payload clock bit of a HS				
	transmission burst.				
T _{HS-EXIT}	Time that the transmitter drives LP-11	300			ns
	following a HS burst.				
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable	Time for Dn to		38	ns
	the HS line termination, starting from the	reach V _{TERM-EN}			
	time point when Dn crosses V _{IL,MAX} .				
T _{CLK-PREPARE}	Time that the transmitter drives the Clock	38		95	ns
	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
	transmission.				
T _{CLK-PRE}	Time that the HS clock shall be driven by	8			UI
	the transmitter prior to any associated Data				
	Lane beginning the transition from LP to				
	HS mode.				
T _{CLK-PREPARE}	T _{CLK-PREPARE} + time that the transmitter	300			ns
+ T _{CLK-ZERO}	drives the HS-0 state prior to starting the				
	Clock.				
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable	Time for Dn to		35 ns +4*UI	
	the HS line termination, starting from the	reach V _{TERM-EN}			
	time point when Dn crosses V _{IL,MAX} .				
T _{HS-PREPARE}	Time that the transmitter drives the Data	40ns + 4*UI		85 ns + 6*UI	ns
	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
	transmission				
T _{HS-PREPARE}	T _{HS-PREPARE} + time that the transmitter	145ns + 10*UI			ns
+ T _{HS-ZERO}	drives the HS-0 state prior to				
	transmitting the Sync sequence.				
T _{HS-TRAIL}	Time that the transmitter drives the flipped	60ns + 4*UI			ns
	differential state after last payload data bit				
	of a HS transmission burst				

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode:

Parameter	Description	Min	Тур	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(M)}		2*T _{LPX(M)}	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA\text{-}GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*T _{LPX(D)}		ns	2
$T_{TA\text{-}GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*T _{LPX(D)}		ns	2
T _{TA-SURE(D)}	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{LPX(D)}		2*T _{LPX(D)}	ns	2

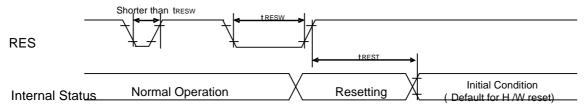
NOTE:

2. Transmitter-specific parameter

^{1.} T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.



7.6.3 Reset Timing



Reset input timing:

VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

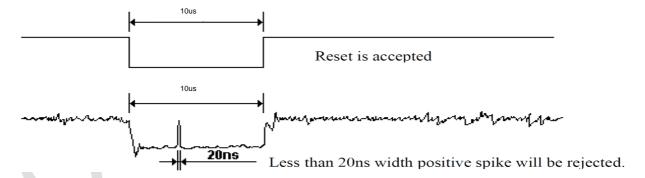
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t _{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μS
4	*2) Poset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
t _{REST}	*2) Reset complete time	-		-	120	When reset applied during Sleep out mode	ms

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10μs	Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX. Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

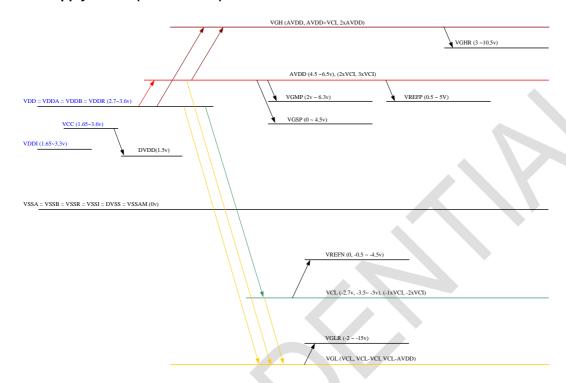


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



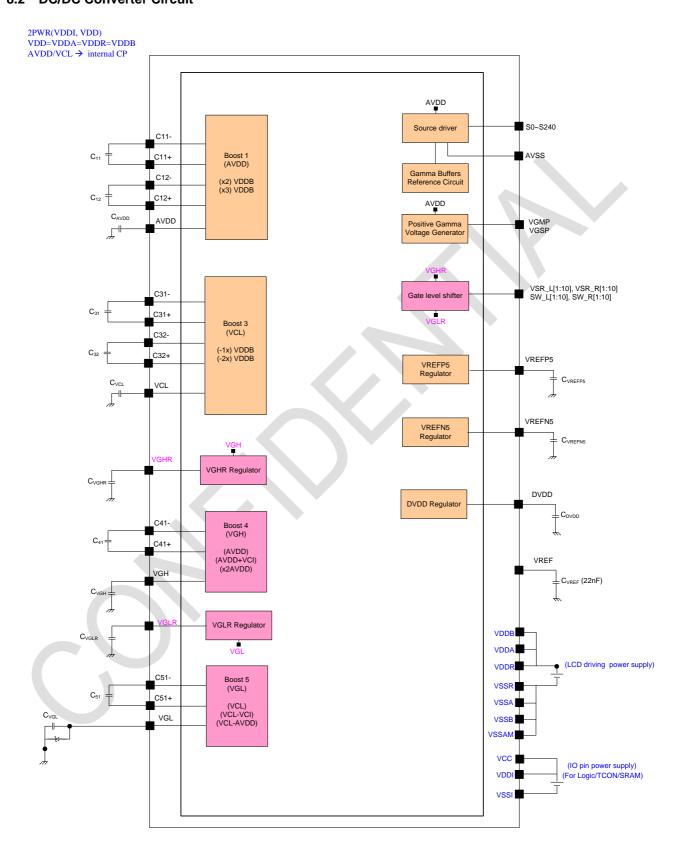
8. Power Generation

8.1 2 Supply Power (VDDI/VDD)





8.2 DC/DC Converter Circuit





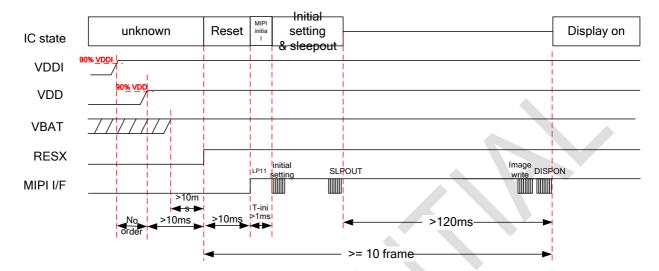
8.3 External Components

No.	Signal name	Values	Max ability
1	VDDA, VDDR, VDDB	Cap , 2.2uF	6.3V
2	VDDI, VCC	Cap , 2.2uF	6.3V
3	VREF	Cap , 22nF	6.3V
4	DVDD	Cap , 1.0uF	6.3V
5	VREFN5/VREFP5	Cap , 1.0uF	6.3V
6	VGHR	Cap , 1.0uF	16V
7	VGLR	Cap , 1.0uF	16V
8	BVP3D	Cap , 2.2uF	10V
9	BVN3D	Cap , 2.2uF	10V
10	C11P/C11N	Cap , 1.0uF	6.3V
11	C12P/C12N	Cap , 1.0uF	6.3V
12	AVDD	Cap , 2.2uF	10V
13	C31P/C31N	Cap , 1.0uF	6.3V
14	C32P/C32N	Cap , 1.0uF	6.3V
15	VCL	Cap , 2.2uF	6.3V
16	C41P/C41N	Cap , 1.0uF	16V
17	VGH	Cap , 2.2uF	25V
18	C51P/C51N	Cap , 1.0uF	16V
19	VGL	Cap , 2.2uF	25V
20	VGL (VGL-GND)	Schottky Diode	

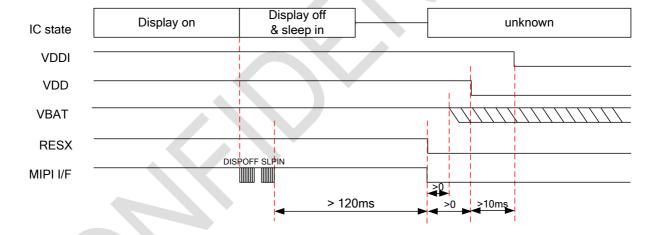


8.4 Power on/off sequence and timing

Power On sequence



Power Off sequence





8.5 Power Level Modes

Normal display mode on = NORON
Partial mode on = PTLON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN
Deep standby mode = DSTBON

Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

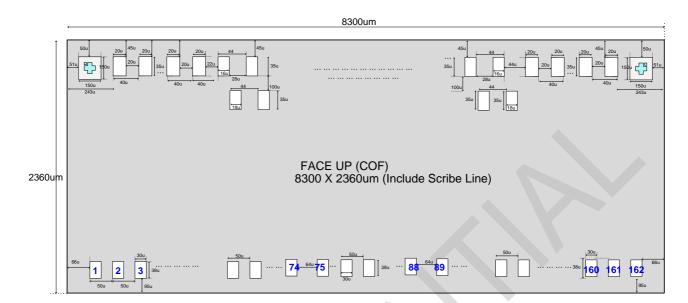
7. Power Off Mode

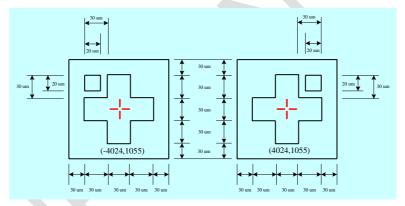
In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.



9. Pad Diagram and Coordination





Chip size: 8300 um x 2360um (Include sealing and scribe line)

Chip thickness: 200/300 um
 PAD coordinates: PAD center
 PAD coordinates origin: Chip center

Au bump size

17um x 35um: Source:S0~S240
 20um x 35um: gate control signal

3. 30um x 38um: Input Pads

Au bump pitch: See PAD coordinates table

■ Au bump height: 12±2 um (typ.)

■ No. in the figure corresponds to No. in the PAD coordinates table

Alignment mark

Alignment mark shape	Х	Υ
left	4024	1055
right	-4024	1055



■ Pad Coordinate (Unit: um)

NO.	PAD NAME
1	ANALOG_TEST1
2	VGLR
3	VGLR
4	VGHR
5	VGHR
6	VREFP5
7	VREFP5
8	VREFP5
9	VREFN5
10	VREFN5
11	VREFN5
12	BVP3D
13	BVP3D
14	BVN3D
15	BVN3D
16	VCL
17	VCL
18	AVDD
19	AVDD
20	VREF
21	VGSP
22	VGMP
23	DUMMY
24	ANALOG_TEST2
25	VDDR
26	VDDR
27	VDDA
28	VDDA
29	AVSS
30	AVSS
31	AVSS
32	VSSR
33	VSSR
34	VSSR
35	TE1
36	SWIRE
37	OLED_EN
38	TE
39	RESX
40	SDO
41	VSSI
42	SDI_RDX
43	DCX
44	WRX_SCL
45	CSX
46	D[0]
47	VSSI
48	D[1]
49	D[2]
50	D[3]
	_ rol

51 D[4] 52 D[5] 53 VSSI 54 D[6] 55 D[7] 56 TEST1 57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_DO_N 84 VSSAM 85 HSSI_DO_N 89 VSSR		5.41
53 VSSI 54 D[6] 55 D[7] 56 TEST1 57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 82 HSSI_DO_P 86 HSSI_DO_N 87 HSSI_DO_N 88 HSSI_DO_N 89 VSSR 90 VSS		
54 D[6] 55 D[7] 56 TEST1 57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_DO_P 86 HSSI_DO_N 87 HSSI_DO_N 88 HSSI_DO_N 89 VSSR 90 VSSR 91 VSS		
55 D[7] 56 TEST1 57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_DO_P 84 VSSAM 85 HSSI_DO_N 88 HSSI_DO_N 89 VSSR 90 VSSR 91 VS		
56 TEST1 57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_DO_P 84 VSSAM 85 HSSI_DO_N 86 HSSI_DO_N 87 HSSI_DO_N 88 HSSI_DO_N 89 VSSR 90		
57 EXTCLK 58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 82 HSSI_DO_P 84 VSSAM 85 HSSI_DO_N 84 VSSA 90 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS <td></td> <td></td>		
58 TEST2 59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 82 HSSI_CLK_N 83 HSSI_DO_P 86 HSSI_DO_N 87 HSSI_DO_N 88 HSSI_DO_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93		
59 VSSI 60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_N 87 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94		
60 TEST3 61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
61 IM1 62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
62 IM0 63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
63 DSWAP 64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
64 TESTEN 65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
65 PSWAP 66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
66 BSTM 67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
67 VDDI 68 VDDI 69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 81 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
68 VDDI 69 VCC 70 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
69 VCC 70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_N 82 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P	67	
70 VCC 71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_CLK_P 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
71 DVDD 72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
72 DVDD 73 DVSS 74 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P	70	
73 DVSS 74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_P 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
74 DVSS 75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
75 HSSI_D1_P 76 HSSI_D1_P 77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
76		
77 HSSI_D1_N 78 HSSI_D1_N 79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P	75	
78		
79 VSSAM 80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 90 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
80 HSSI_CLK_P 81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
81 HSSI_CLK_P 82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
82 HSSI_CLK_N 83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
83 HSSI_CLK_N 84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
84 VSSAM 85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
85 HSSI_D0_P 86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P		
86 HSSI_D0_P 87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
87 HSSI_D0_N 88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		HSSI_D0_P
88 HSSI_D0_N 89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
89 VSSR 90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
90 VSSR 91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P	88	
91 VSSA 92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
92 VSSA 93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
93 AVSS 94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
94 AVSS 95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
95 VSSB 96 VSSB 97 VSSB 98 C11P 99 C11P		
96 VSSB 97 VSSB 98 C11P 99 C11P		
97 VSSB 98 C11P 99 C11P	95	
98 C11P 99 C11P	96	
99 C11P	97	
	98	
100 C11P	99	
	100	C11P

101 102 103 104 105 106 107 108	C11N C11N C11N C12P C12P C12P
103 104 105 106 107 108	C11N C12P C12P
104 105 106 107 108	C12P C12P
105 106 107 108	C12P
106 107 108	
107 108	C12P
108	0121
	C12N
109	C12N
	C12N
110	VDDB
111	VDDB
112	VDDB
113	VDDR
114	VDDR
115	VDDR
116	AVDD
117	AVDD
118	AVDD
119	C31P
120	C31P
121	C31P
122	C31N
123	C31N
124	C31N
125	VCL
126	VCL
127	VCL
128	C32P
129	C32P
130	C32P
131	C32N
132	C32N
133	
134	C32N C41P
	C41P
135	
136	C41N
137	C41N
138	C51N
139	C51N
140	C51P
141	C51P
142	VGH
143	VGH
144	VGHR
145	VGHR
146	VGHR
147	VGHR
148	VGHR
149	VGLR
150	VGLR

151 VGL 152 VGL 153 AVSS 154 AVSS 155 AVSS 156 MTP_PWR 157 MTP_PWR 158 MTP_PWR 159 MTP_PWR 160 MTP_PWR 161 MTP_PWR 162 DUMMY 163 VGLR 164 VGHR 165 VREFN5 166 VREFN5 167 VSR_L[10] 168 VSR_L[9] 169 VSR_L[1] 170 VSR_L[6] 172 VSR_L[6] 173 VSR_L[1] 174 VSR_L[3] 175 VSR_L[2] 176 VSR_L[1] 177 SW_L[2] 179 SW_L[3] 180 SW_L[4] 181 SW_L[5] 182 SW_L[6] 183 SW_L[10] 186 SW_		
153 AVSS 154 AVSS 155 AVSS 156 MTP_PWR 157 MTP_PWR 158 MTP_PWR 159 MTP_PWR 160 MTP_PWR 161 MTP_PWR 162 DUMMY 163 VGLR 164 VGHR 165 VREFN5 166 VREFN5 167 VSR_L[10] 168 VSR_L[9] 169 VSR_L[8] 170 VSR_L[7] 171 VSR_L[6] 172 VSR_L[6] 173 VSR_L[2] 176 VSR_L[2] 176 VSR_L[2] 177 SW_L[3] 180 SW_L[4] 181 SW_L[6] 182 SW_L[6] 183 SW_L[7] 184 SW_L[8] 185 SW_L[9] 186 SW_L[10] 187	151	VGL
154 AVSS 155 AVSS 156 MTP_PWR 157 MTP_PWR 158 MTP_PWR 159 MTP_PWR 160 MTP_PWR 161 MTP_PWR 162 DUMMY 163 VGLR 164 VGHR 165 VREFP5 166 VREFN5 167 VSR_L[10] 168 VSR_L[9] 169 VSR_L[8] 170 VSR_L[6] 172 VSR_L[6] 173 VSR_L[6] 174 VSR_L[1] 175 VSR_L[2] 176 VSR_L[1] 177 SW_L[3] 180 SW_L[4] 181 SW_L[5] 182 SW_L[6] 183 SW_L[7] 184 SW_L[8] 185 SW_L[9] 186 SW_L[10] 187 SDMY 188	152	VGL
155 AVSS 156 MTP_PWR 157 MTP_PWR 158 MTP_PWR 159 MTP_PWR 160 MTP_PWR 161 MTP_PWR 162 DUMMY 163 VGLR 164 VGHR 165 VREFP5 166 VREFN5 167 VSR_L[10] 168 VSR_L[9] 169 VSR_L[8] 170 VSR_L[6] 172 VSR_L[6] 173 VSR_L[6] 174 VSR_L[2] 175 VSR_L[1] 176 VSR_L[1] 177 SW_L[1] 178 SW_L[2] 179 SW_L[3] 180 SW_L[4] 181 SW_L[5] 182 SW_L[6] 183 SW_L[7] 184 SW_L[8] 185 SW_L[9] 186 SW_L[10] 187	153	AVSS
156 MTP_PWR 157 MTP_PWR 158 MTP_PWR 159 MTP_PWR 160 MTP_PWR 161 MTP_PWR 162 DUMMY 163 VGLR 164 VGHR 165 VREFP5 166 VREFN5 167 VSR_L[10] 168 VSR_L[8] 170 VSR_L[8] 170 VSR_L[6] 172 VSR_L[6] 173 VSR_L[6] 174 VSR_L[3] 175 VSR_L[1] 176 VSR_L[1] 177 SW_L[1] 178 SW_L[2] 179 SW_L[3] 180 SW_L[4] 181 SW_L[5] 182 SW_L[6] 183 SW_L[7] 184 SW_L[8] 185 SW_L[10] 186 SW_L[10] 187 SDMY 188	154	AVSS
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