
STM32
CubeMX

1. Description

1.1. Project

Project Name	virtlab-user
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	10/27/2021

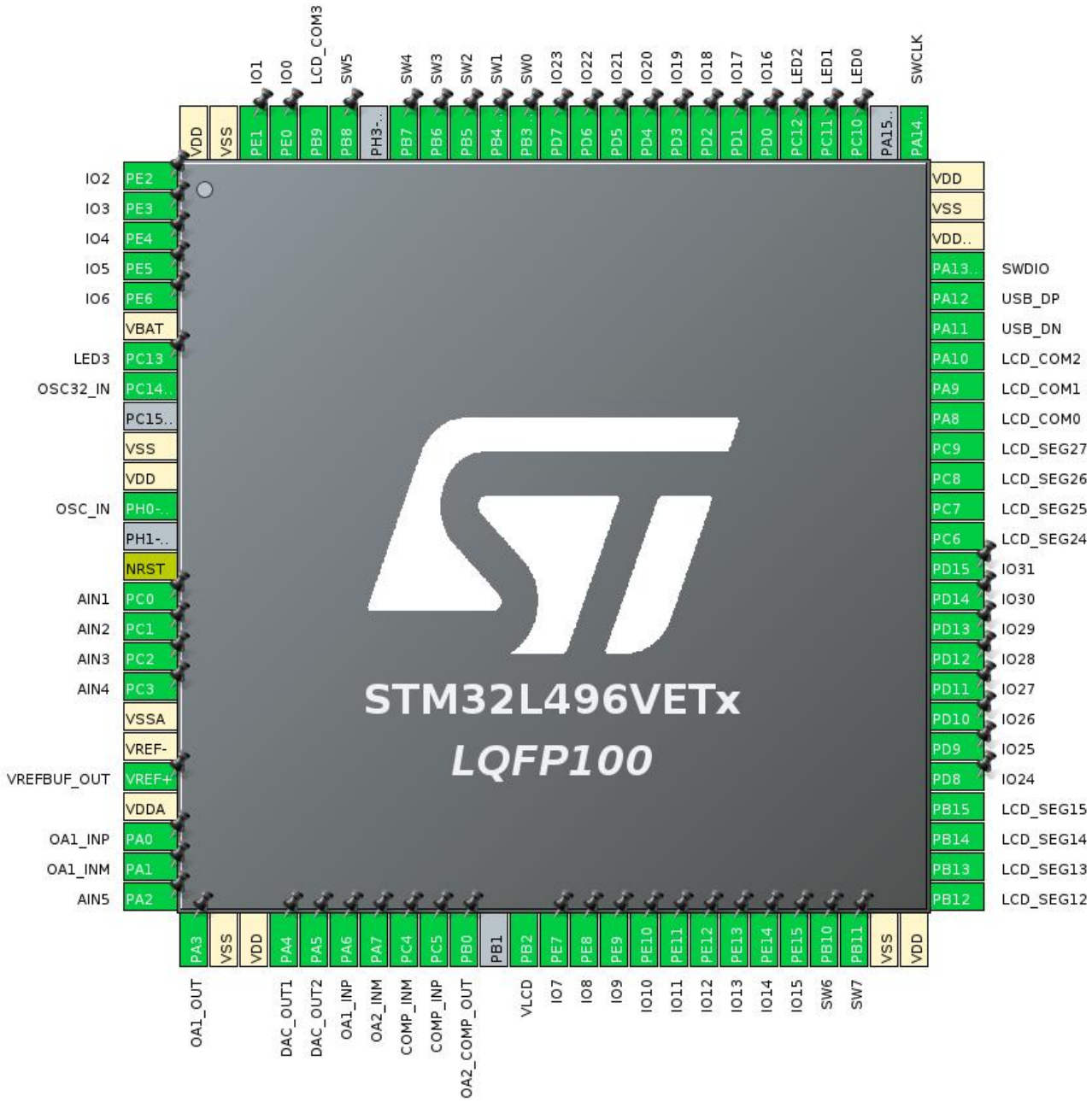
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

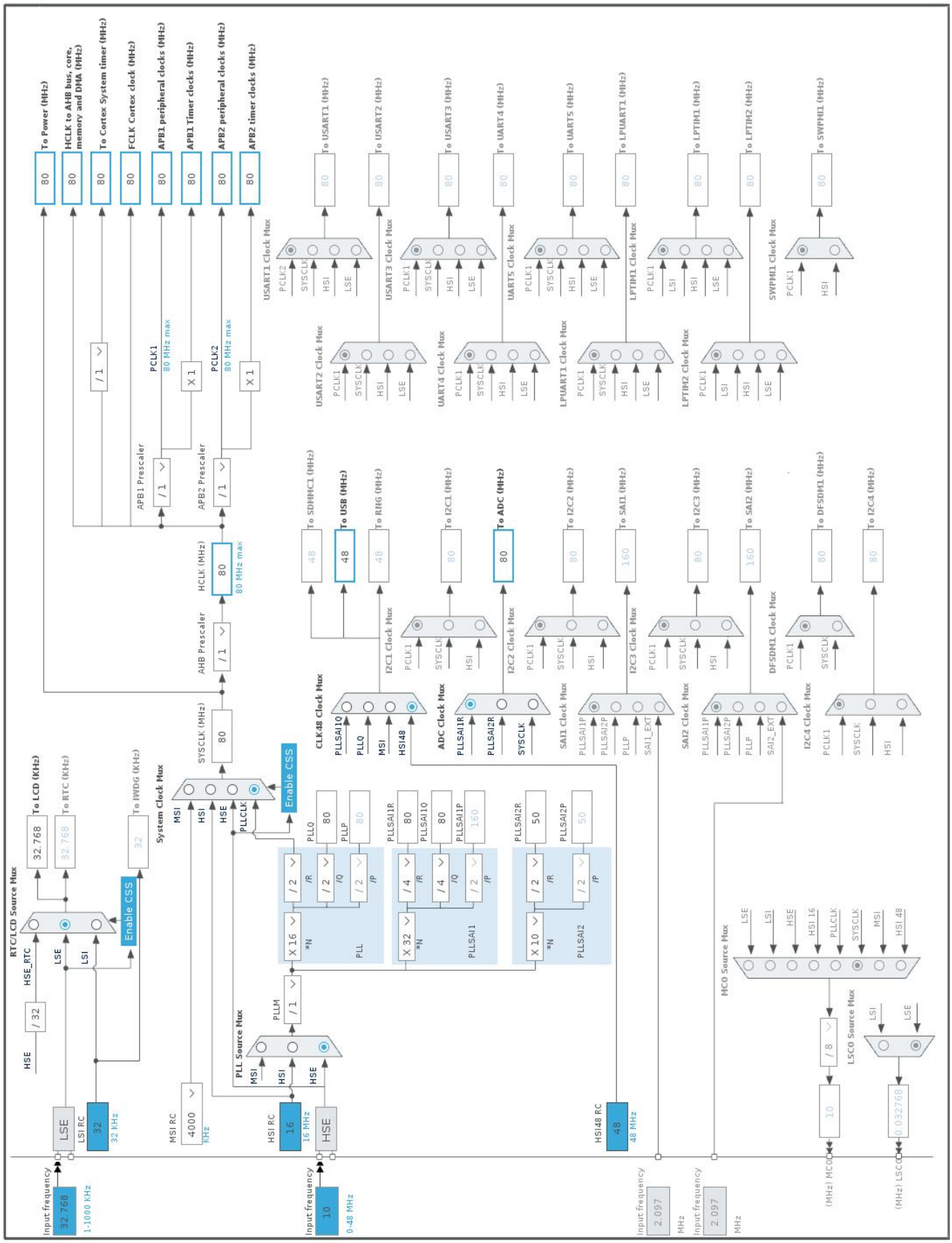
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	IO2
2	PE3 *	I/O	GPIO_Input	IO3
3	PE4 *	I/O	GPIO_Input	IO4
4	PE5 *	I/O	GPIO_Input	IO5
5	PE6 *	I/O	GPIO_Input	IO6
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	LED3
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	OSC32_IN
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	OSC_IN
14	NRST	Reset		
15	PC0	I/O	ADC1_IN1	AIN1
16	PC1	I/O	ADC1_IN2	AIN2
17	PC2	I/O	ADC1_IN3	AIN3
18	PC3	I/O	ADC1_IN4	AIN4
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	MonoIO	VREFBUF_OUT	
22	VDDA	Power		
23	PA0	I/O	OPAMP1_VINP	OA1_INP
24	PA1	I/O	OPAMP1_VINM	OA1_INM
25	PA2	I/O	ADC1_IN7	AIN5
26	PA3	I/O	OPAMP1_VOUT	OA1_OUT
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DAC1_OUT1	DAC_OUT1
30	PA5	I/O	DAC1_OUT2	DAC_OUT2
31	PA6	I/O	OPAMP2_VINP	OA1_INP
32	PA7	I/O	OPAMP2_VINM	OA2_INM
33	PC4	I/O	COMP1_INM	COMP_INM
34	PC5	I/O	COMP1_INP	COMP_INP
35	PB0	I/O	OPAMP2_VOUT	OA2_COMP_OUT
37	PB2	I/O	LCD_VLCD	VLCD
38	PE7 *	I/O	GPIO_Input	IO7
39	PE8 *	I/O	GPIO_Input	IO8

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PE9 *	I/O	GPIO_Input	IO9
41	PE10 *	I/O	GPIO_Input	IO10
42	PE11 *	I/O	GPIO_Input	IO11
43	PE12 *	I/O	GPIO_Input	IO12
44	PE13 *	I/O	GPIO_Input	IO13
45	PE14 *	I/O	GPIO_Input	IO14
46	PE15 *	I/O	GPIO_Input	IO15
47	PB10 *	I/O	GPIO_Input	SW6
48	PB11 *	I/O	GPIO_Input	SW7
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	LCD_SEG12	
52	PB13	I/O	LCD_SEG13	
53	PB14	I/O	LCD_SEG14	
54	PB15	I/O	LCD_SEG15	
55	PD8 *	I/O	GPIO_Input	IO24
56	PD9 *	I/O	GPIO_Input	IO25
57	PD10 *	I/O	GPIO_Input	IO26
58	PD11 *	I/O	GPIO_Input	IO27
59	PD12 *	I/O	GPIO_Input	IO28
60	PD13 *	I/O	GPIO_Input	IO29
61	PD14 *	I/O	GPIO_Input	IO30
62	PD15 *	I/O	GPIO_Input	IO31
63	PC6	I/O	LCD_SEG24	
64	PC7	I/O	LCD_SEG25	
65	PC8	I/O	LCD_SEG26	
66	PC9	I/O	LCD_SEG27	
67	PA8	I/O	LCD_COM0	
68	PA9	I/O	LCD_COM1	
69	PA10	I/O	LCD_COM2	
70	PA11	I/O	USB_OTG_FS_DM	USB_DN
71	PA12	I/O	USB_OTG_FS_DP	USB_DP
72	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	SWDIO
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	SWCLK
78	PC10 *	I/O	GPIO_Output	LED0
79	PC11 *	I/O	GPIO_Output	LED1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
80	PC12 *	I/O	GPIO_Output	LED2
81	PD0 *	I/O	GPIO_Input	IO16
82	PD1 *	I/O	GPIO_Input	IO17
83	PD2 *	I/O	GPIO_Input	IO18
84	PD3 *	I/O	GPIO_Input	IO19
85	PD4 *	I/O	GPIO_Input	IO20
86	PD5 *	I/O	GPIO_Input	IO21
87	PD6 *	I/O	GPIO_Input	IO22
88	PD7 *	I/O	GPIO_Input	IO23
89	PB3 (JTDO/TRACESWO) *	I/O	GPIO_Input	SW0
90	PB4 (NJTRST) *	I/O	GPIO_Input	SW1
91	PB5 *	I/O	GPIO_Input	SW2
92	PB6 *	I/O	GPIO_Input	SW3
93	PB7 *	I/O	GPIO_Input	SW4
95	PB8 *	I/O	GPIO_Input	SW5
96	PB9	I/O	LCD_COM3	
97	PE0 *	I/O	GPIO_Input	IO0
98	PE1 *	I/O	GPIO_Input	IO1
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	virtlab-user
Project Folder	/home/max/STM32CubeIDE/workspace_1.6.1/virtlab-user
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Basic
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DAC1_Init	DAC1
4	MX_OPAMP1_Init	OPAMP1
5	MX_OPAMP2_Init	OPAMP2
6	MX_ADC1_Init	ADC1
7	MX_ADC3_Init	ADC3
8	MX_COMP1_Init	COMP1
9	MX_LCD_Init	LCD
10	MX_USB_DEVICE_Init	USB_DEVICE

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496VETx
Datasheet	DS11585_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

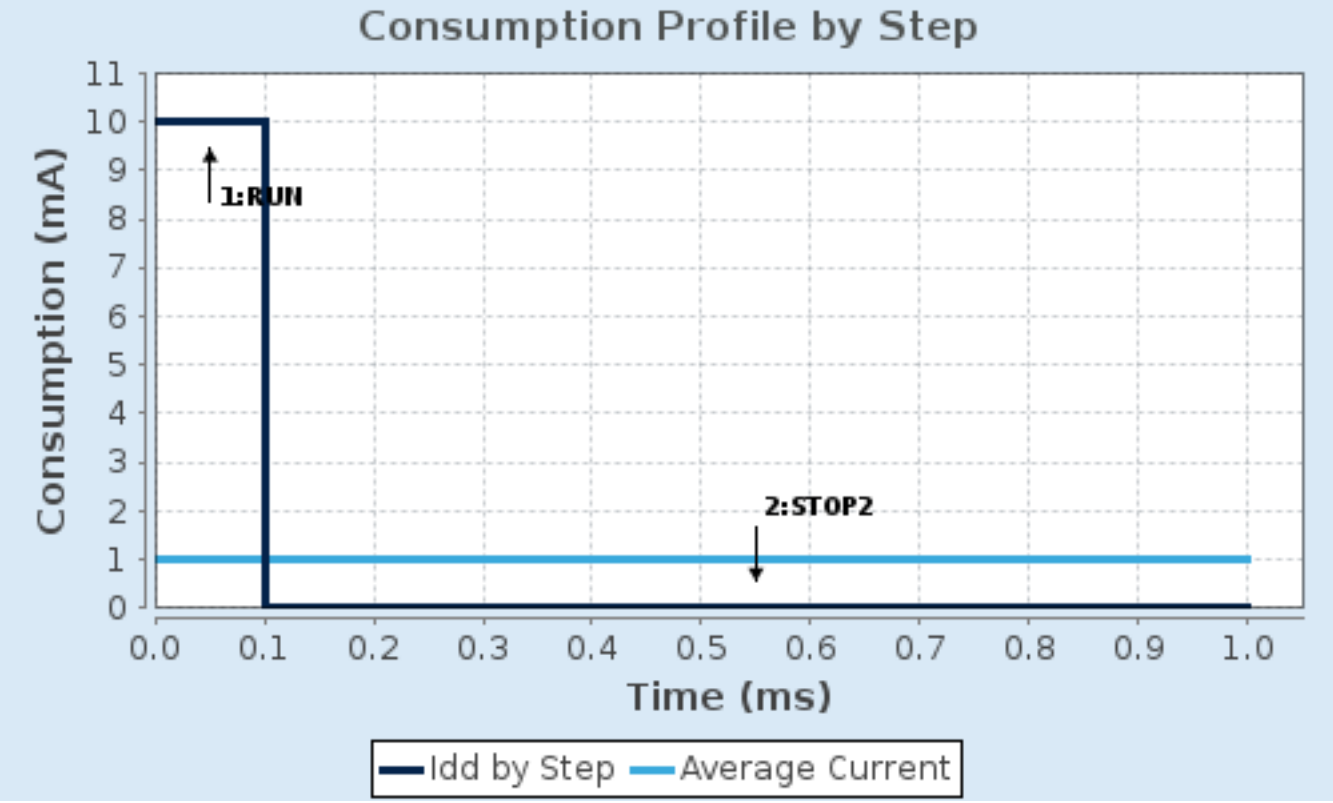
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10 mA	2.69 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.74	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1 mA
Battery Life	4 months, 19 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
11
10
9
8
7
6
5
4
3
2
1
0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN7: IN7 Single-ended

IN8: OPAMP1 Output Single-ended

IN15: OPAMP2 Output Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC3
mode: VDAC1_OUT1 Channel
mode: VDAC1_OUT2 Channel

7.2.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel DAC1_OUT1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. COMP1

mode: Input [+]

Input [-]: INM

7.3.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed
Trigger Mode	None
Hysteresis Level	None

Output Configuration:

Blanking Source	None
Output Pol	COMP output on GPIO isn't inverted

7.4. DAC1

OUT1 mode: Connected to external pin and to on chip-peripherals

OUT2 mode: Connected to external pin and to on chip-peripherals

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.5. LCD

Mode: 1/4 Duty Cycle

mode: SEG12

mode: SEG13

mode: SEG14
mode: SEG15
mode: SEG24
mode: SEG25
mode: SEG26
mode: SEG27

7.5.1. Parameter Settings:

Clock Parameters:

Clock Prescaler	1
Clock Divider	16

Basic Parameters:

Duty Selection	1/4
Bias Selector	1/4
Multiplex mode	Disable

Advanced Parameters:

Voltage Source Selection	Internal
Contrast Control	2.60V
Dead Time Duration	No dead Time
High Drive	Disable
Pulse ON Duration	0 pulse
Blink Mode	Disabled
Blink Frequency	fLCD/8

7.6. OPAMP1

Mode: PGA Connected

7.6.1. Parameter Settings:

Basic Parameters:

Power Supply Range	Power Supply Range Low
Power Mode	Normal
PGA Gain	2
User Trimming	Disable

7.7. OPAMP2

Mode: PGA Connected

7.7.1. Parameter Settings:

Basic Parameters:

Power Supply Range	Power Supply Range Low
Power Mode	Normal
PGA Gain	2
User Trimming	Disable

7.8. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : BYPASS Clock Source

7.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.9. SYS

Debug: Serial Wire

VREFBUF Mode: Internal voltage reference

Timebase Source: TIM16

7.9.1. Parameter Settings:

Voltage_Reference_Buffer_Settings:

Trimming Mode	Factory Trimming
Internal Voltage reference scale	SCALE 0: around 2.048 V

7.10. USB_OTG_FS

Mode: Device_Only

7.10.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.11. FREERTOS

Interface: CMSIS_V2

7.11.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled

USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	3000
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.11.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled

uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.11.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.12. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.12.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	**Disabled ***
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.12.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	AIN1
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	AIN2
	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	AIN3
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	AIN4
	PA2	ADC1_IN7	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	AIN5
COMP1	PC4	COMP1_INM	Analog mode	No pull-up and no pull-down	n/a	COMP_INM
	PC5	COMP1_INP	Analog mode	No pull-up and no pull-down	n/a	COMP_INP
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	DAC_OUT1
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	DAC_OUT2
LCD	PB2	LCD_VLCD	Alternate Function Push Pull	No pull-up and no pull-down	Low	VLCD
	PB12	LCD_SEG12	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	LCD_SEG13	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	LCD_SEG14	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	LCD_SEG15	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LCD_SEG24	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LCD_SEG25	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	LCD_SEG26	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	LCD_SEG27	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	LCD_COM0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	LCD_COM1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	LCD_COM2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LCD_COM3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
OPAMP1	PA0	OPAMP1_VINP	Analog mode	No pull-up and no pull-down	n/a	OA1_INP
	PA1	OPAMP1_VINM	n/a	n/a	n/a	OA1_INM
	PA3	OPAMP1_VOUT	Analog mode	No pull-up and no pull-down	n/a	OA1_OUT
OPAMP2	PA6	OPAMP2_VINP	Analog mode	No pull-up and no pull-down	n/a	OA1_INP
	PA7	OPAMP2_VINM	n/a	n/a	n/a	OA2_INM
	PB0	OPAMP2_VOUT	Analog mode	No pull-up and no pull-down	n/a	OA2_COMP_OUT
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	OSC32_IN
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_IN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	(PH0)					
SYS	VREF+	VREFBUF_OUT	n/a	n/a	n/a	
	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DN
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO2
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO3
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO4
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO5
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO6
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO7
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO8
	PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO9
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO10
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO11
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO12
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO13
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO14
	PE15	GPIO_Input	Input mode	**Pull-up ***	n/a	IO15
	PB10	GPIO_Input	Input mode	**Pull-down ***	n/a	SW6
	PB11	GPIO_Input	Input mode	**Pull-down ***	n/a	SW7
	PD8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO24
	PD9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO25
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO26
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO27
	PD12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO28
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO29
	PD14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO30
	PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO31
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO16
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO17
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO18
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO19
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO20
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO21
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO22
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO23
	PB3 (JTDO/TRACESWO)	GPIO_Input	Input mode	**Pull-down ***	n/a	SW0
	PB4 (NJTRST)	GPIO_Input	Input mode	**Pull-down ***	n/a	SW1
	PB5	GPIO_Input	Input mode	**Pull-down ***	n/a	SW2
	PB6	GPIO_Input	Input mode	**Pull-down ***	n/a	SW3
	PB7	GPIO_Input	Input mode	**Pull-down ***	n/a	SW4
	PB8	GPIO_Input	Input mode	**Pull-down ***	n/a	SW5
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO0
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IO1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
USB OTG FS global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
ADC3 global interrupt	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
COMP1 and COMP2 interrupts through EXTI lines 21 and 22	unused		
LCD global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM1 update interrupt and TIM16 global	false	true	true

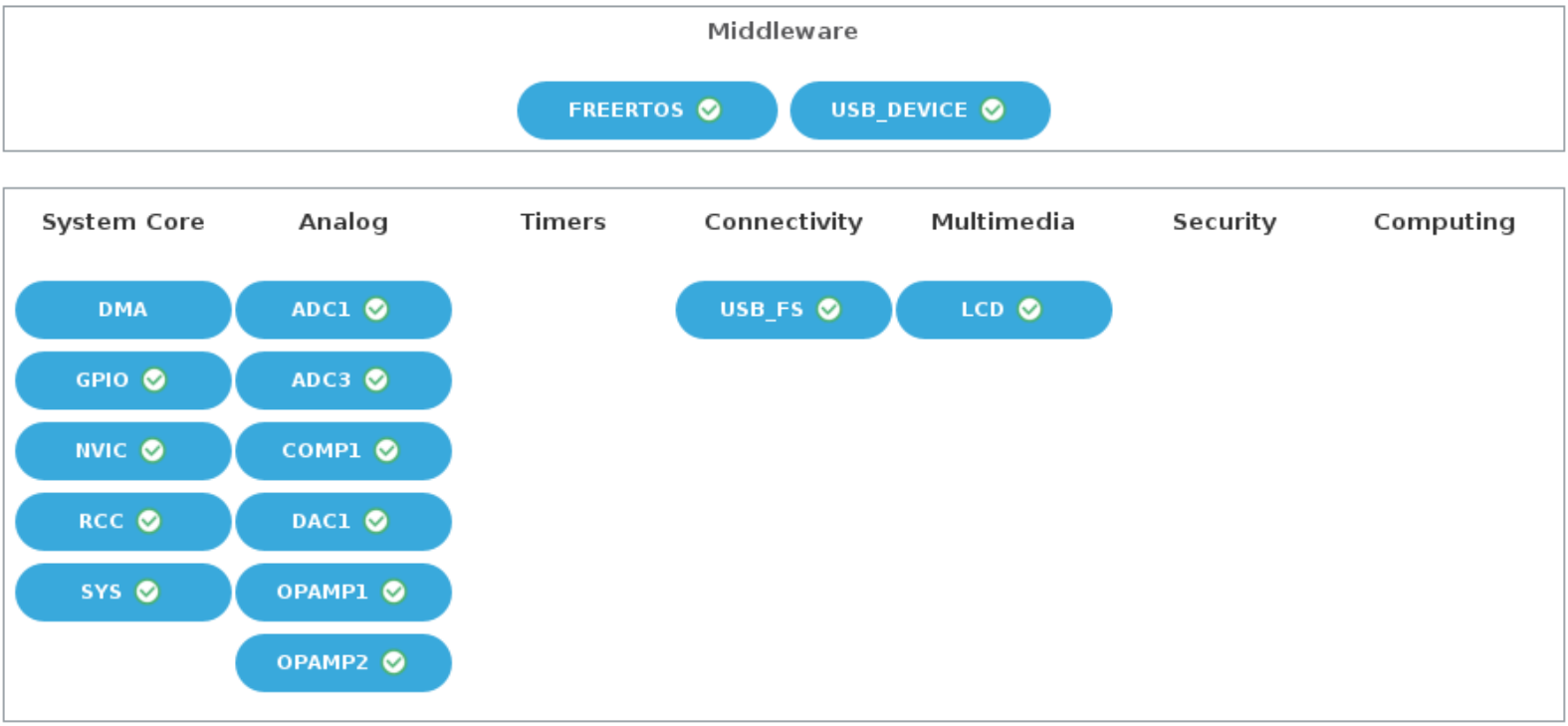
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
interrupt			
USB OTG FS global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00284211.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00083560.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00264473.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209748.pdf

Application note	http://www.st.com/resource/en/application_note/DM00125306.pdf
Application note	http://www.st.com/resource/en/application_note/DM00141025.pdf
Application note	http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note	http://www.st.com/resource/en/application_note/DM00148033.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209768.pdf
Application note	http://www.st.com/resource/en/application_note/DM00216518.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269143.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00260952.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00338361.pdf
Application note	http://www.st.com/resource/en/application_note/DM00264868.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00367673.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note	http://www.st.com/resource/en/application_note/DM00476869.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660597.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf