ADVANCE INFORMATION

MX26C4000B

4M-BIT [512K x 8] CMOS MULTIPLE-TIME-PROGRAMMABLE-EPROM

FEATURES

- 512Kx 8 organization
- Single +5V power supply
- +12V programming voltage
- Fast access time:70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current:30mA
- Standby current: 100uA
- Chip erase time: 2s (typ.)
- Chip program time: 25s (typ.)
- 100 minimum erase/program cycles
- Typical fast programming cycle duration 100us/byte
- Package type:
  - 32 pin plastic DIP
  - 32 pin PLCC
  - 32 pin TSOP
  - 32 pin SOP

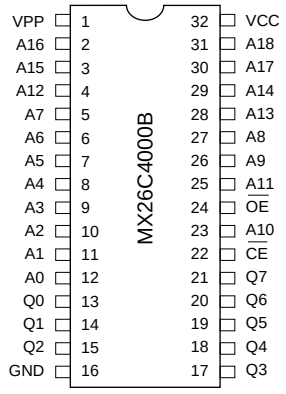
GENERAL DESCRIPTION

The MX26C4000B is a 5V only, 4M-bit, MTP EPROM™ (Multiple Time Programmable Read Only Memory). It is organized as 512K words by 8 bits per word, operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. It is design to be programmed and erased by an EPROM programmer or on-board. The MX26C4000B supports a intelligent fast programming algorithm which can result in programming time of less than one minute.

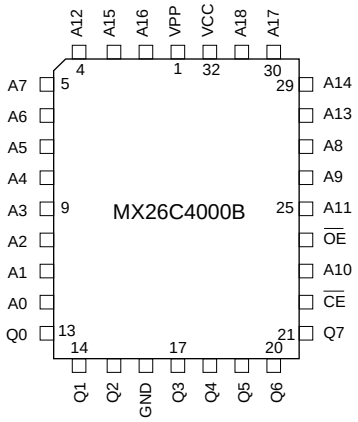
This MTP EPROM™ is packaged in industry standard 32 pin dual-in-line packages, 32 lead PLCC, 32 lead SOP and 32 lead TSOP packages.

PIN CONFIGURATIONS

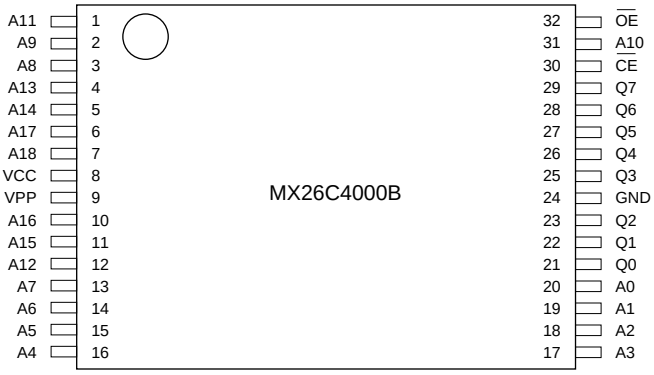
32 PDIP/SOP



32 PLCC



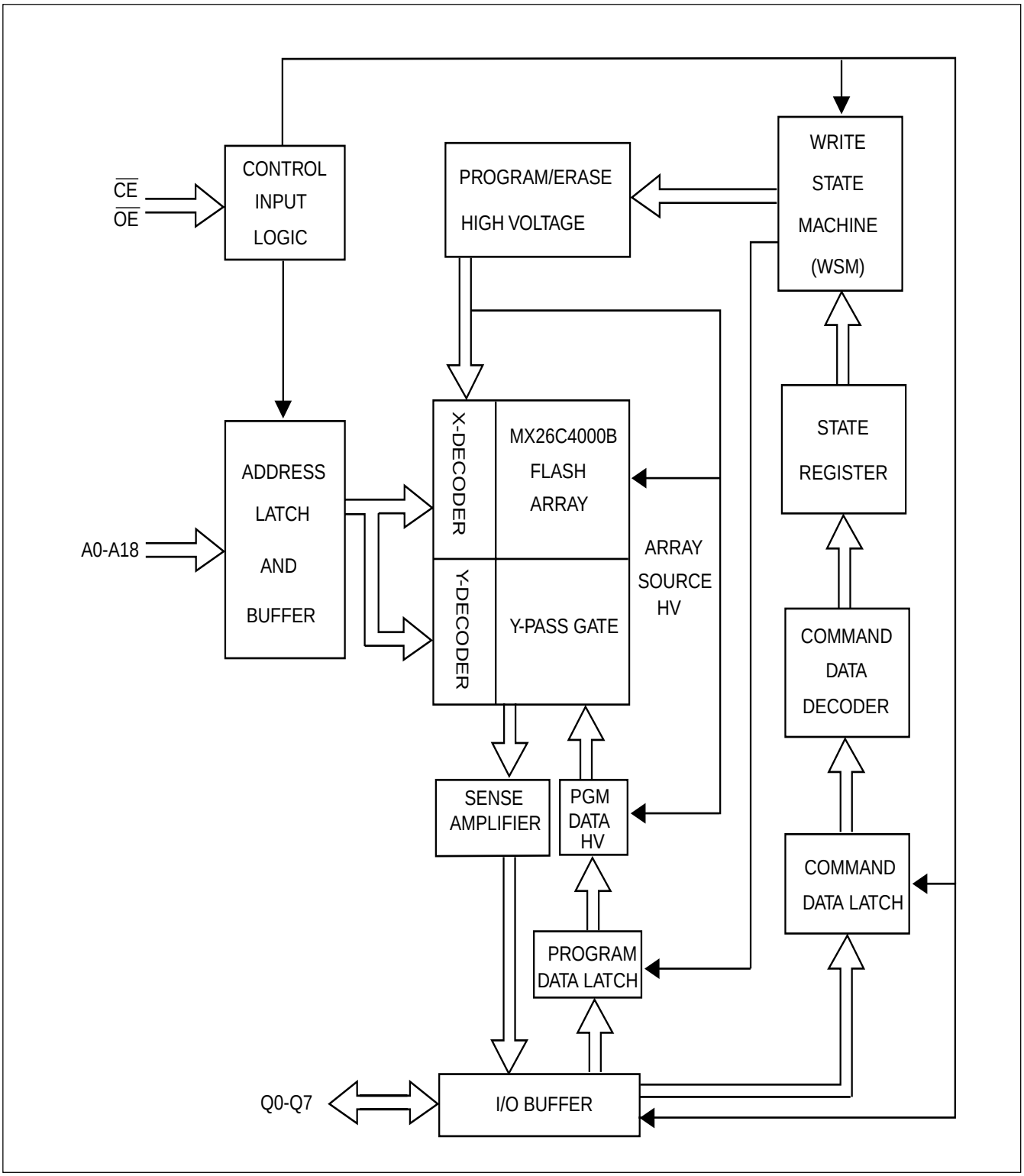
32 TSOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

When the MX26C4000B is delivered, or it is erased, the chip has all 4M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX26C4000B through the procedure of programming.

ERASE ALGORITHM

The MX26C4000B do not required preprogramming before an erase operation. The erase algorithm is a close loop flow to simultaneously erase all bits in the entire array. Erase operation starts with the initial erase operation. Erase verification begins at address 0000H by reading data FFH from each byte. If any byte fails to erase. the entire chip is reerased. to a maximum for 10 pulse counts of 500ms duration for each pulse. The maximum cumulative erase time is 3s. However. the device is usually erased in no more than 3 pulses. Erase verification time can be reduced by storing the address of the last byte that failed. Following the next erase operation verification may start at the stored address location. JEDEC standard erase algorithm can also be used. But erase time will increase by performing the unnecessary preprogramming.

PROGRAM ALGORITHM

The device is programmed byte by byte. A maximum of 25 pulses. each of 100us duration is allowed for each byte being programmed. The byte may be programmed sequentially or by random. After each program pulse, a program verify is done to determine if the byte has been successfully programmed.

Programming then proceeds to the next desired byte location. JEDEC standard program algorithms can be used.

DATA WRITE PROTECTION

The design of the device protects against accidental erasure or programming. The internal state machine is automatically reset to the read mode on power-up. Using control register architecture, alteration of memory can only occur after completion of proper command sequences. The command register is only active when V_{PP} is at high voltage. when $V_{PP} = V_{PPL}$, the device defaults to the Read Mode. Robust design features prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise. To avoid initiation of write cycle during V_{CC} power-up, a write cycle is locked out for V_{CC} less than 4V. The two- command program and erase write sequence to the command register provide additional software protection against spurious data changes.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. Verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, and VPP at its programming voltage.

ERASE VERIFY MODE

Verification should be performed on the erased chip to determine that the whole chip(all bits) was correctly erased. Verification should be performed with $\overline{OE}$ and $\overline{CE}$ at VIL, and VCC = 5V, VPP = 12.5V

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from MTP EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25℃ ±5℃ ambient temperature range that is required when programming the MX26C4000B.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX26C4000B, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX26C4000B has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX26C4000B has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX26C4000B also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each of the eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

OUTPUT DISABLE

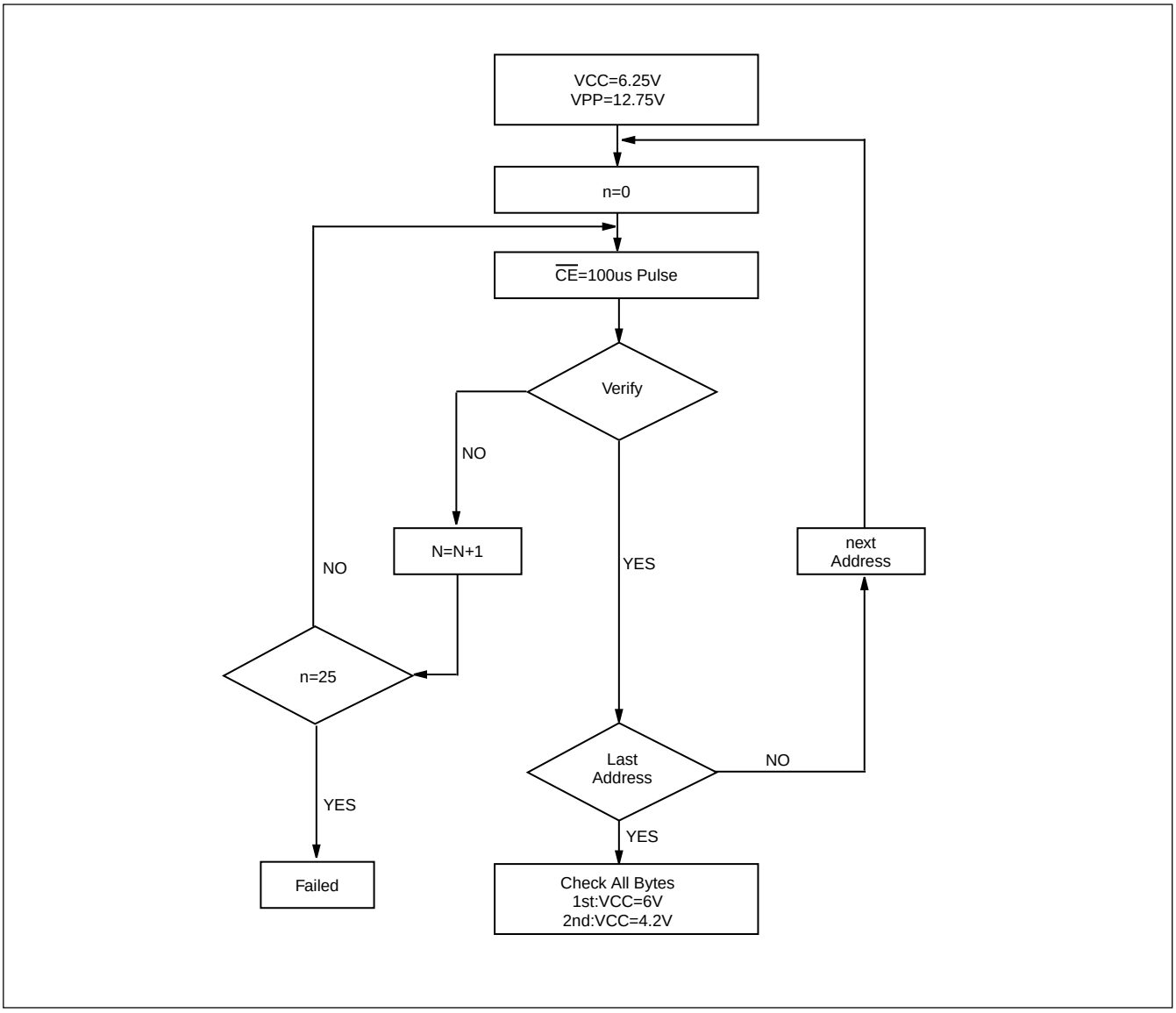
Output is disabled when $\overline{OE}$ is at logre high. When in output disabled all circuitry is enabled. Except the output pins are in a high impedance state(Hi-Z).

Table 1: BUS OPERATIONS

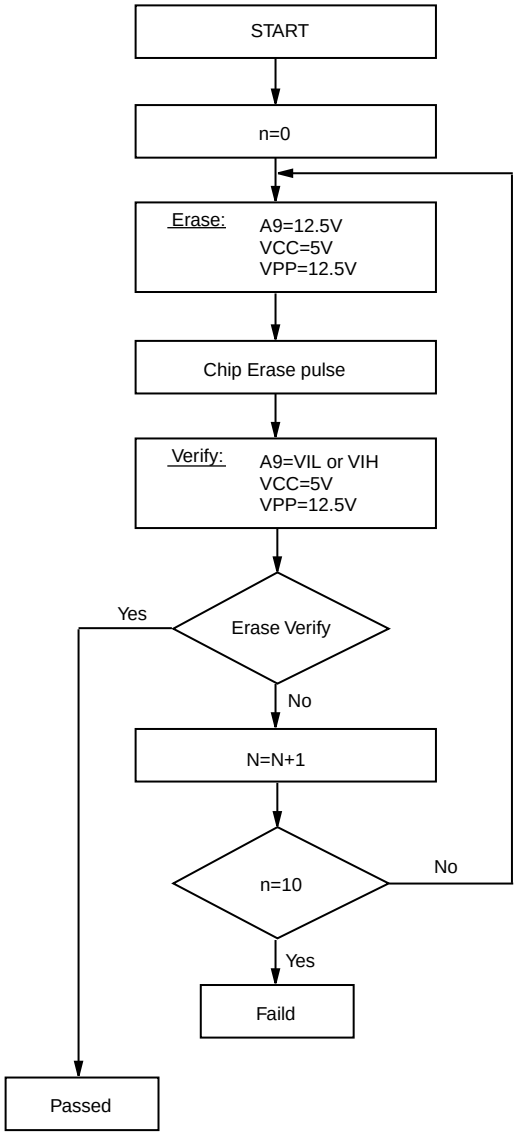
Mode	VPP(1)	A0	A9	$\overline{CE}$	$\overline{OE}$	Q0~Q7
Read	VPPL	A0	A9	VIL	VIL	Data Out
Output Disable	VPPL	X	X	VIL	VIH	Hi-Z
Standby	VPPL	X	X	VIH	X	Hi-Z
Manufacturer Identification	VPPL	VIL	VID(2)	VIL	VIL	Data=C2H
Device Identification	VPPL	VIH	VID(2)	VIL	VIL	Data=C0H
Program	VPPH	A0	X	VIL	VIH	Data In
Verify	VPPH	A0	X	VIH	VIL	Data Out
Program Inhibit	VPPH	X	X	VIH	VIH	Hi-Z

Note:
1. Refer to DC Characteristics. When VPP=VPPL memory contents can be read but not written or erased.
2. VID is the intelligent identifier high voltage. Refer to DC Characteristics.
3. Read operations with VPP=VPPH may access array data or the intelligent identifier codes.
4. With VPP at high voltage the standby current equals ICC+IPP(standby).
5. Refer to Table 2 for vaild data-in during a write operation.
6. X can be VIL or VIH.

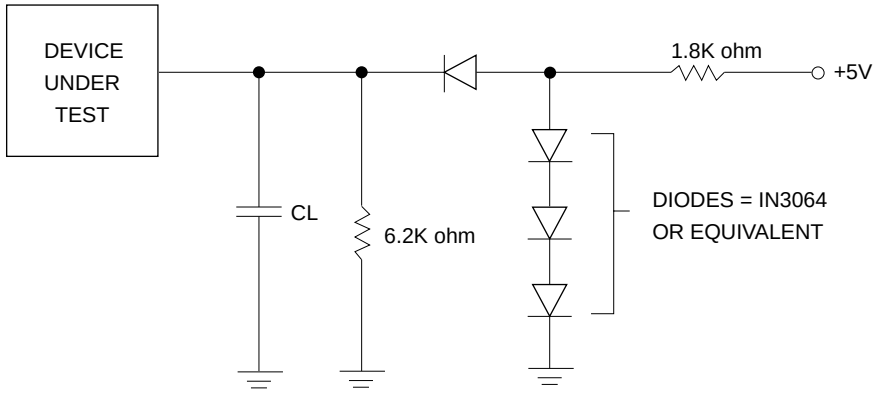
PROGRAMMING ALGORITHM FLOW CHART



ERASE ALGORITHM FLOW CHART

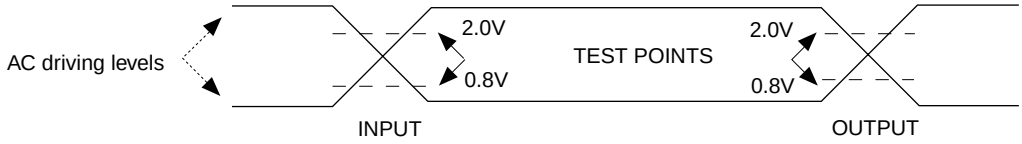


SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V for commercial grade.
Input pulse rise and fall times are equal to or less than 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC OPERATING CONDITION FOR READ OPERATION

		MX26C4000B			
		-90	**-100**	**-120**	-150
Operating Temperature	Industrial	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance		6	pF	VIN = 0V
COUT	Output Capacitance		12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

DC CHARACTERISTICS TA = -45℃ ~ 85℃, VCC=5V±10%

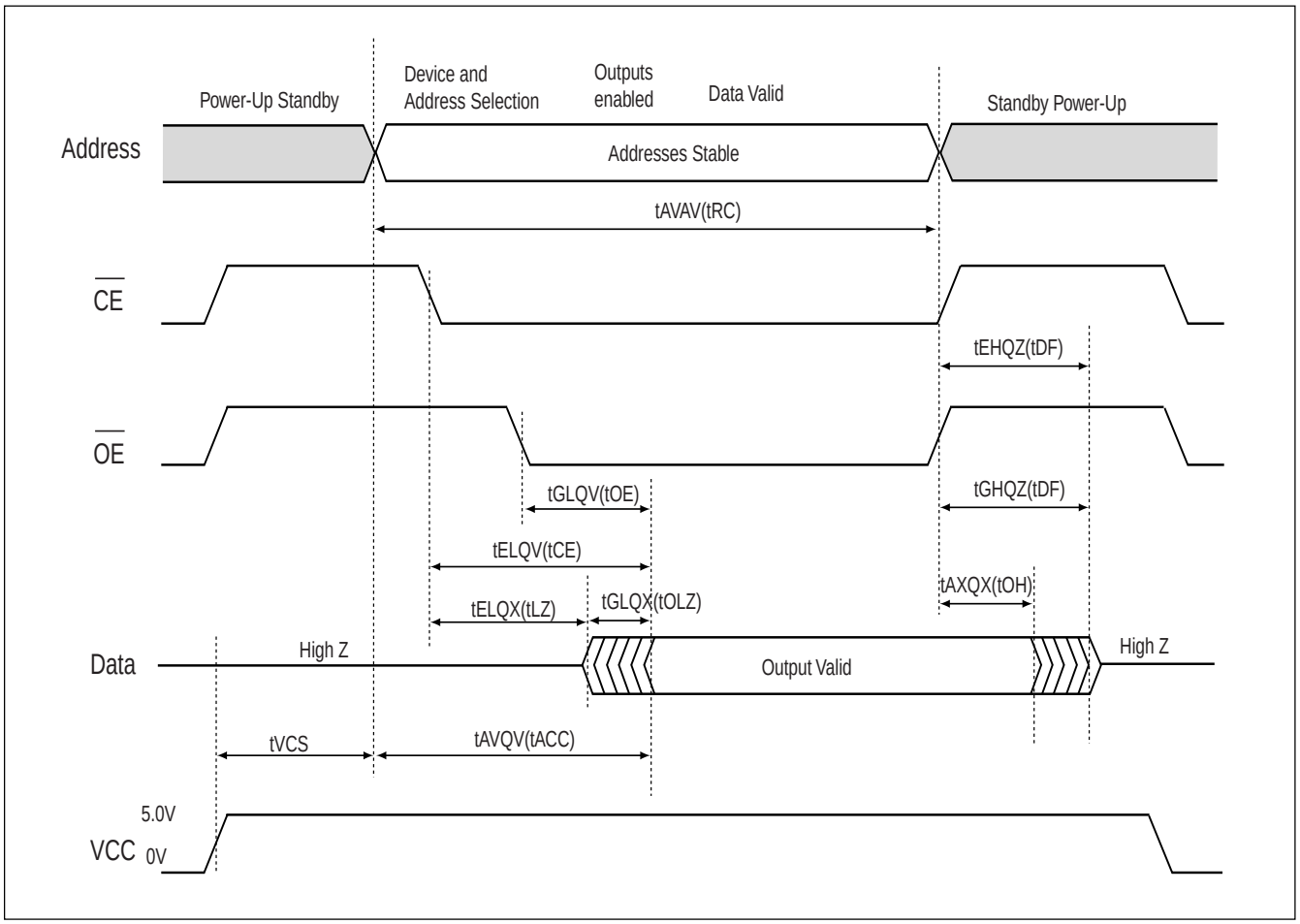
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.0	VCC + 1	V	
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA, VCC=VCC MIN
VOH	Output High Voltage (TTL)	2.4		V	IOH = -0.4mA
VOH	Output High Voltage (CMOS)	VCC-0.7V		V	IOH = -0.1mA
ICC1	VCC Active Current		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$=VIH, f=5MHz
ISB	VCC Standby Current (CMOS)		100	uA	$\overline{CE}$=VCC+0.2V, VCC=VCC MAX
ISB	VCC Standby Current (TTL)		1	mA	$\overline{CE}$=VIH, VCC=VCC MAX
IPP	VPP Supply Current (Program)		10	uA	$\overline{CE}$=$\overline{WE}$=VIL, $\overline{OE}$=VIH
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
VCC1	Fast Programming Supply Voltage	6.0	6.5	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

AC RAED CHARACTERISTICS OVER OPERATING RANGE WITH VPP=VCC

Symbol		Parameter	70		90		100		120		150		Unit
Jeded	STD		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tAVAV	TRC	Read Cycle Time	70		90		100		120		150		ns
tELQV	TCE	$\overline{CE}$ Access Time	0	70	0	90	0	100	0	120	0	150	ns
tAVQV	TACC	Address Access Time	0	70	0	90	0	100	0	120	0	150	ns
tGLQV	TOE	$\overline{OE}$ Access Time	0	35	0	40	0	45	0	50	0	65	ns
tELQX	TLZ	$\overline{CE}$ to Output in Low Z(Note 1)	0		0		0		0		0		ns
tEHQZ	TDF	Chip Disable to Output in High Z (Note 2)	0	30	0	30	0	35	0	35	0	50	ns
tGLQX	TOLZ	$\overline{OE}$ to Output in Low Z (Note 1)	0		0		0		0		0		ns
tGHQZ	TDF	Output Disable to Output in High Z (Note 1)	0	30	0	30	0	35	0	35	0	50	ns
tAXQX	TOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, change		0		0		0		0		0	ns
tVCS	TVCS	VCC Setup Time to Valid Read (Note 2)		50		50		50		50		50	us

Note:
1. Sampled: not 100% tested.
2. Guaranteed by design. not tested.

AC WAVEFORMS FOR READ OPERATIONS



AC WAVEFORMS FOR ERASE OPERATIONS

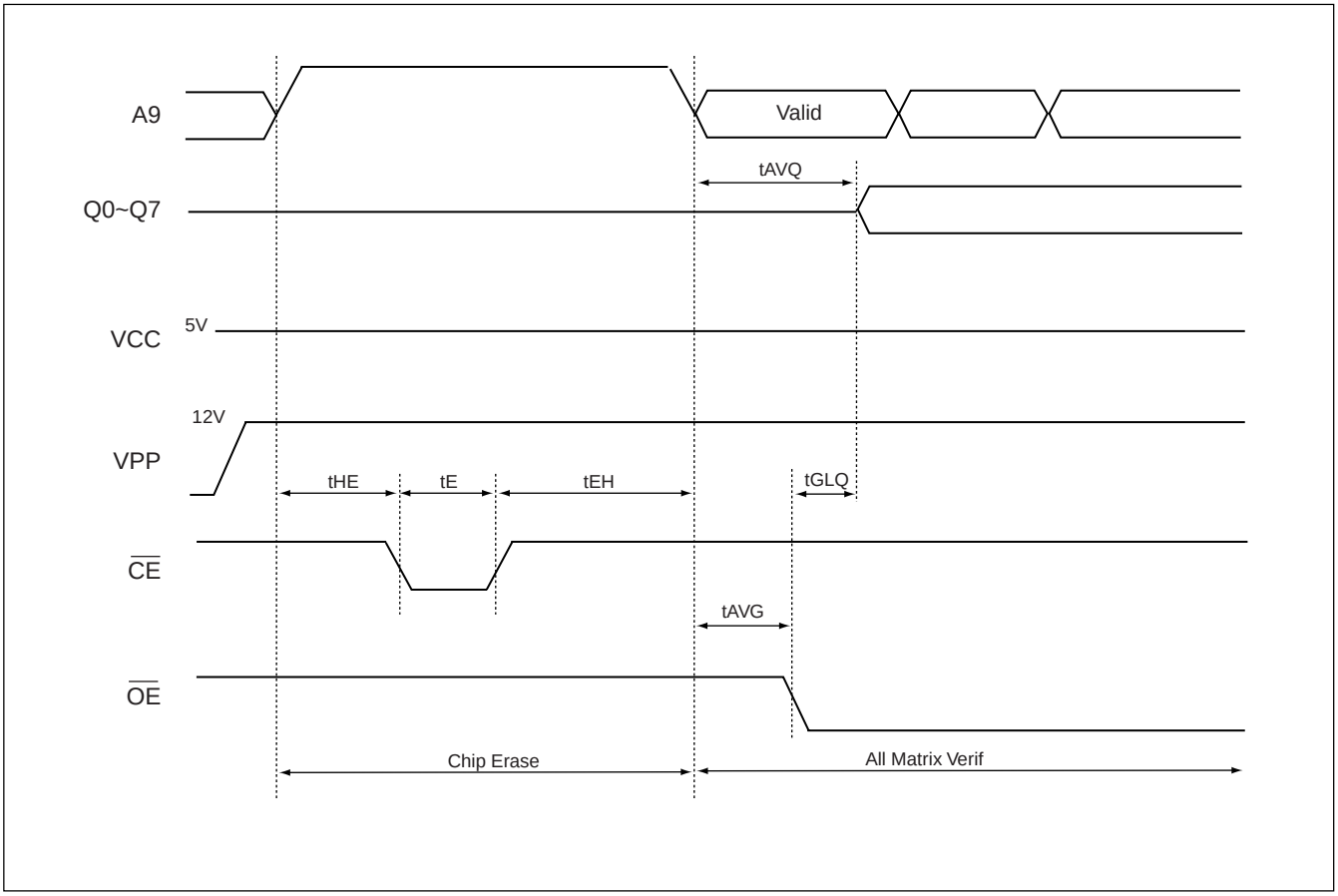


Table 2. Erasing Mode AC Characteristics (1) (TA=25℃; VCC=5V±0.25V; VPP=12.5V±0.25V)

Symbol	Parameter	Min	Max	Unit
tA9HEL	A9 High to Chip Enable Low	2		us
tAVGL	Address Valid to Output Enable Low	2		us
tAVQV	Address Valid to Data Valid		100	ns
tEHA9L	Chip Enable High to A9 Low	2		us
tER	First Erase Time	500		ms
tGLQV	Output Enable Low to Data Valid		30	ns

(1) VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

AC WAVEFORMS FOR PROGRAMMING OPERATIONS

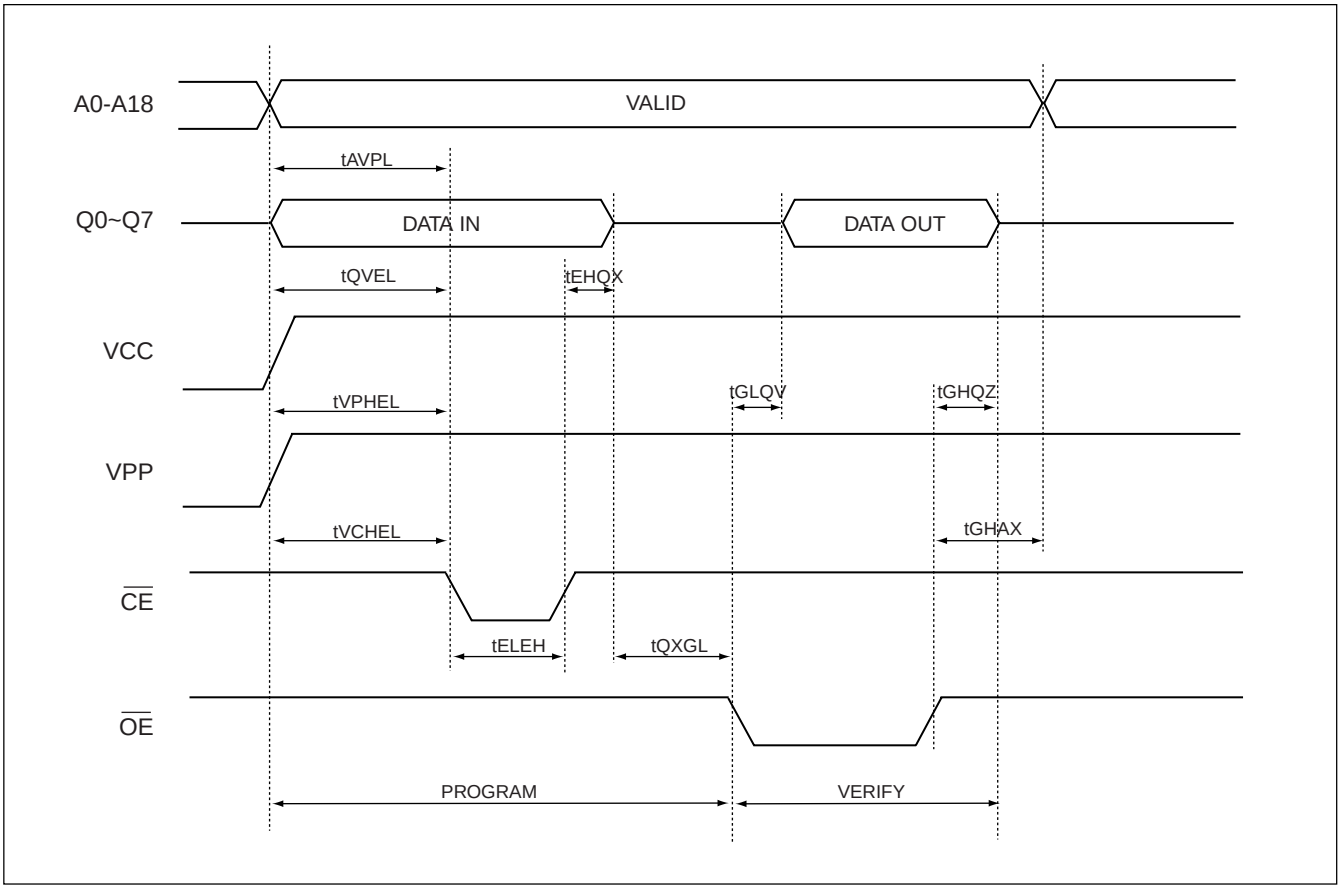


Table 3. Programming Mode AC Characteristics (1)
(TA=25℃; VCC=6.25V±0.25V; VPP=12.5V±0.25V)

Symbol	Alt	Parameter	Min	Max	Unit
tAVPL	tAS	Address Valid to Chip Enable Low	2		us
TQVEL	tDS	Input Valid to Chip Enable Low	2		us
TVPHEL	tVPS	VPP High to Chip Enable Low	2		us
TVCHEL	tVCS	VCC High to Chip Enable Low	2		us
TELEH	tPW	Chip Enable Program Pulse Wodth	95	105	us
TEHQX	tDH	Chip Enable High to Input Transition	2		us
TQXGL	tOES	Input Transition to Output Enable Low	2		us
TGLQV	tOE	Output Enable Low to Output Valid		100	ns
TGHQZ	tDFP	Output Enable High to Output Hi-Z	0	130	ns
TGHAX	tAH	Output Enable High to Address Transition	0		ns

(1) VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.
(2) Sampled only, not 100% tested.

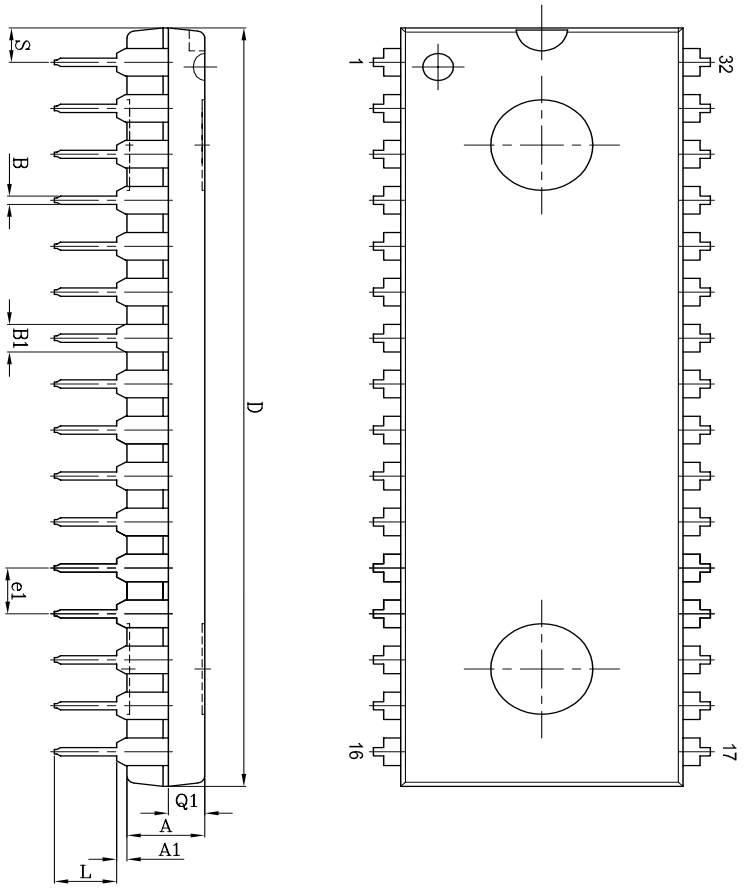
ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING Current MAX.(mA)	STANDBY Current MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX26C4000BPC-90	90	30	100	0℃ to 70℃	32 Pin DIP
MX26C4000BQC-90	90	30	100	0℃ to 70℃	32 Pin PLCC
MX26C4000BMC-90	90	30	100	0℃ to 70℃	32 Pin SOP
MX26C4000BTC-90	90	30	100	0℃ to 70℃	32 Pin TSOP
MX26C4000BPC-10	100	30	100	0℃ to 70℃	32 Pin DIP
MX26C4000BQC-10	100	30	100	0℃ to 70℃	32 Pin PLCC
MX26C4000BMC-10	100	30	100	0℃ to 70℃	32 Pin SOP
MX26C4000BTC-10	100	30	100	0℃ to 70℃	32 Pin TSOP
MX26C4000BPC-12	120	30	100	0℃ to 70℃	32 Pin DIP
MX26C4000BQC-12	120	30	100	0℃ to 70℃	32 Pin PLCC
MX26C4000BMC-12	120	30	100	0℃ to 70℃	32 Pin SOP
MX26C4000BTC-12	120	30	100	0℃ to 70℃	32 Pin TSOP
MX26C4000BPC-15	150	30	100	0℃ to 70℃	32 Pin DIP
MX26C4000BQC-15	150	30	100	0℃ to 70℃	32 Pin PLCC
MX26C4000BMC-15	150	30	100	0℃ to 70℃	32 Pin SOP
MX26C4000BTC-15	150	30	100	0℃ to 70℃	32 Pin TSOP
MX26C4000BPI-90	90	30	100	-40℃ to 85℃	32 Pin DIP
MX26C4000BQI-90	90	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C4000BMI-90	90	30	100	-40℃ to 85℃	32 Pin SOP
MX26C4000BTI-90	90	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C4000BPI-10	100	30	100	-40℃ to 85℃	32 Pin DIP
MX26C4000BQI-10	100	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C4000BMI-10	100	30	100	-40℃ to 85℃	32 Pin SOP
MX26C4000BTI-10	100	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C4000BPI-12	120	30	100	-40℃ to 85℃	32 Pin DIP
MX26C4000BQI-12	120	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C4000BMI-12	120	30	100	-40℃ to 85℃	32 Pin SOP
MX26C4000BTI-12	120	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C4000BPI-15	150	30	100	-40℃ to 85℃	32 Pin DIP
MX26C4000BQI-15	150	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C4000BMI-15	150	30	100	-40℃ to 85℃	32 Pin SOP
MX26C4000BTI-15	150	30	100	-40℃ to 85℃	32 Pin TSOP

PACKAGE INFORMATION

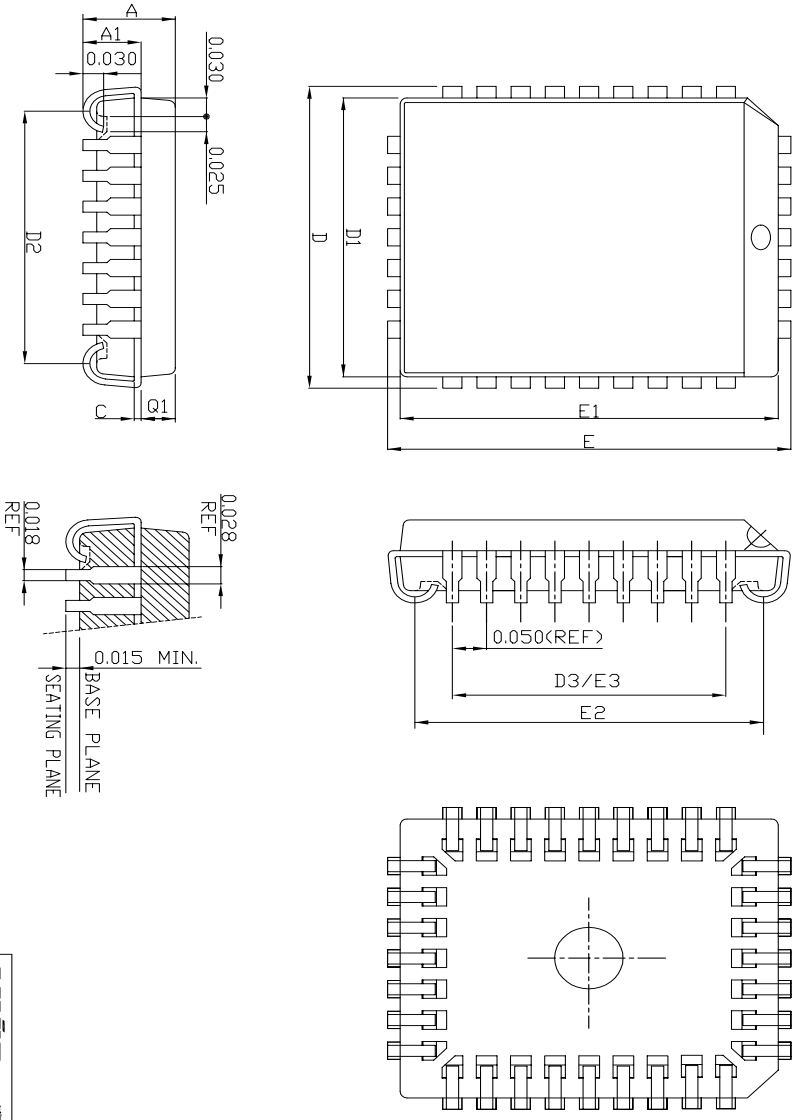
32-PIN PLASTIC DIP(600 mil)



SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	1.65±0.005	41.91±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.075±0.005	1.905±0.127

MIC 旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO.
				6110-0202.2
TITLE: PACKAGE OUTLINE FOR PDIP 32L (600 MIL)				TOLERANCE: .X ± ANGLE; .XX ±.01; .XXX±.002
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Leo Lee	05-02-01		4

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

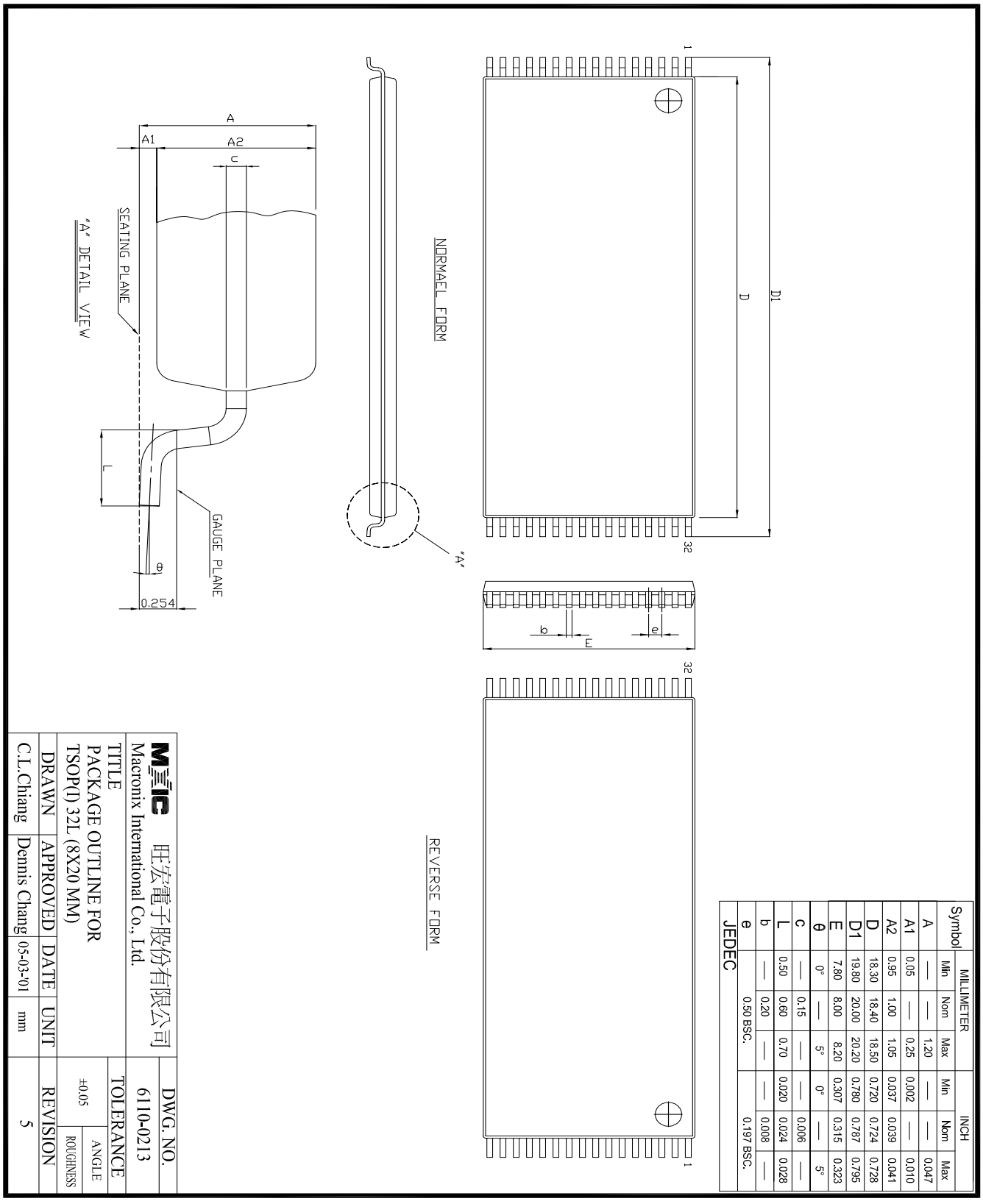


Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A			0.140			3.56
A1	0.080	0.085	0.090	2.03	2.16	2.29
Q1	0.048	0.050	0.052	1.22	1.27	1.32
c		0.010(REF)			0.25(REF)	
D	0.485	0.490	0.495	12.32	12.45	12.57
D1	0.450	0.453	0.456	11.43	11.51	11.58
D2	0.400	0.410	0.420	10.16	10.41	10.67
D3		0.300(REF)			7.62(REF)	
E	0.585	0.590	0.595	14.86	14.99	15.11
E1	0.550	0.553	0.556	13.97	14.05	14.12
E2	0.500	0.510	0.520	12.70	12.95	13.21
E3		0.400(REF)			10.16(REF)	

REFERENCE DOCUMENT : JEDEC SPEC - MS-016a

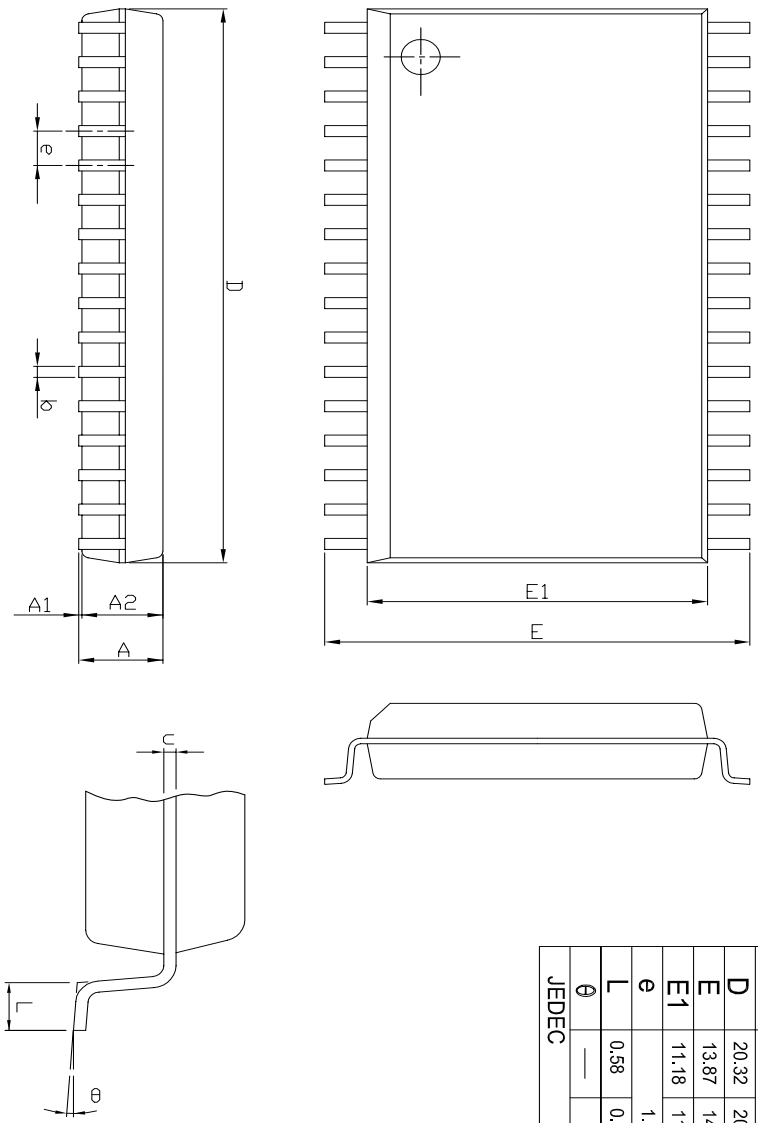
MIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0209.1
TITLE			TOLERANCE
PACKAGE OUTLINE FOR PLCC 32L			.X ± .XX ±01 .XXX±.002 ANGLE ±2°
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-03-'01	inch
			REVISION 2

32-PIN PLASTIC TSOP



Symbol	MILLIMETER			INCH		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.25	0.002	—	0.010
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.30	18.40	18.50	0.720	0.724	0.728
D1	19.80	20.00	20.20	0.780	0.787	0.795
E	7.80	8.00	8.20	0.307	0.315	0.323
θ	0°	—	5°	0°	—	5°
c	—	0.15	—	—	0.006	—
L	0.50	0.60	0.70	0.020	0.024	0.028
b	—	0.20	—	—	0.008	—
e		0.50 BSC.			0.197 BSC.	
JEDEC						

32-PIN PLASTIC SOP (450 mil)



Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b		0.41REF			0.016 REF	
c		0.20 REF			0.008 REF	
D	20.32	20.45	20.57	0.800	0.805	0.810
E	13.87	14.12	14.38	0.546	0.556	0.566
E1	11.18	11.30	11.43	0.440	0.445	0.450
e		1.27 REF			0.050 REF	
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	5°		—
JEDEC						

旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0206
TITLE	PACKAGE OUTLINE FOR SOP 32L (450 MIL)		TOLERANCE
			X ± ANGLE
			.XX ±.01
			.XXX±.002 ROUGHNESS
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-03-01	INCH
			REVISION
			2

REVISION HISTORY

Revision No.	Description	Page	Date
0.1	To add erase/program cycle	P1	DEC/18/2000
	Change title from MX26C4000A to MX26C4000B	All	
0.2	To added 32SOP/TSOP types package and access time 150ns	P1,10,11,16,18	MAR/27/2001
	Modify device ID old 32H-->New C0H	P5	
	Modify read ID method	P4,5,6,12	
	Modify erase/program cycle from 100 to 50	P1	
	Modify VCC Standby Current(TTL) from 1mA to 1.5mA	P10	
0.3	To added VCC1 & VPP1 to DC Characteristics Table	P10	APR/23/2001
	Modify Package Information	P17~20	
0.4	To added chip erase time / chip program time	P1	JUL/04/2001
	Modify Package Information	P17~20	
0.5	Modify the Programming Operations Timing Waveforms	P15	OCT/04/2001
0.6	1.Cancel the command mode	P12	JAN/14/2002
	2.Modify the cycle time from 50-->100	P1	
	3.Modify the erase/program operation timing waveform and flowchart	P6,7,12,13	

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