MAIN FPGA UNIT

Resistor Array

ZIF-PLCC cocket

Willem.schdoc

p_[48..1]

p_[48..1]
R_[48..1]

R_[48..1]

VCC

3V

R_48.SchDoc

DIP48_PLCC_R

TXD
RXD
5V
3V_PLUS
clk_16
UART_to_FPGA
Data_From_PGA
UART_to_MEGA
Reset
Reset_FW
FW_data
FW_clk
PWR_ERROR
VDDy

MEGA-88

PWR_ERROR
FW_clk
FW_data
Reset_FW
Reset
UART_to_MEGA
Data_From_PGA
UART_to_FPGA
clk_16
3V_PLUS
5V

RXD
TXD
VDDy

PWM_0A
PWM_0B

ADC_5
ADC_12
ADC_CONTROL_3
ADC_CONTROL_5
VCC_ON
VPP_ON

DC-DC converters

3V
PWM_0A
PWM_0B

ADC_5
ADC_12
ADC_CONTROL_3
ADC_CONTROL_5
VCC_ON
VPP_ON

5V

VCC

ATMEGA.SchDoc

DC_DC.SchDoc

USB_COM

5V
RXD
TXD

VDDy

Willem_USB v1.5

J3   USB_CON

1
2
3
4
5
6

5V_CP
U-
U+

C9

0.01

5V_CP
U-
U+

GND

USB_COM.SchDoc

ATMEGA88_DIP28

D12
10BQ040

C12 100*6V

C10 0.1

GND

R3

VDDy

C11 1.0

1K

GND

U2

VCC	
	AVCC 20
	AREF 21
	GND 22

14 PB0 (ICP)
15 PB1 (OC1A)
16 PB2 (SS/OC1B)
17 PB3 (MOSI/OC2)
18 PB4 (MISO)
19 PB5 (SCK)
9 PB6 (XTAL1/TOSC1)
10 PB7 (XTAL2/TOSC2)

clk_16
Reset_FW
Reset
FW_data
Data_From_PGA
FW_clk

XTAL_1
XTAL_2

2 PD0 (RXD)
3 PD1 (TXD)
4 PD2 (INT0)
5 PD3 (INT1)
6 PD4 (XCK/T0)
11 PD5 (T1)
12 PD6 (AIN0)
13 PD7 (AIN1)

(ADC0) PC0 23
(ADC1) PC1 24
(ADC2) PC2 25
(ADC3) PC3 26
(ADC4/SDA) PC4 27
(ADC5/SCL) PC5 28
(RESET) PC6 1

TXD
RXD
UART_to_MEGA
UART_to_FPGA
PWM_0B
PWM_0A
PWR_ERROR

ADC_5
ADC_12
ADC_CONTROL_5
ADC_CONTROL_3
VPP_ON
VCC_ON
3V_PLUS

GND

5V

5V

R26 1K

D4

ACTIVE

GND

J4

3
2
1

CON3

XTAL_1

XTAL_2

ATMega-88

VPP-VCC Generators

VDDy

R18
330

PWR_ON
D10

C28
4.7

USB-COM converter

GND

14	nc	U3	nc	15
13	nc		nc	16
12	SUSPEND		nc	17
11	/SUSPEND		nc	18
10	nc		nc	19
9	/RST		nc	20
8	VBUS		nc	21
7	VREGIN		nc	22
6	VDD		CTS	23
5	D-		RTS	24
4	D+		RXD	25
3	GND		TXD	26
2	RI	CP2102	DSR	27
1	DCD		DTR	28

U-
U+

RXD
TXD

5V_CP

U+
U+

1.0
C29

GND

R19
1

C30
30*6V

C31
0.1
C32

0.22
C33

470*6.3V

U-
U-

5V

P_5
P_4
P_3
P_2
P_1

P_6
P_7
FW_DATA

VDDy

GND

C1 0.1   C3 0.22   C39 1.0

3V

VR1

5V

3V

D1   2_5V
Diode   C5 C6
4.7 0.1

Vin Vout
GND

GND   Volt Reg   R1   GND
DIODE   1K   Q5
D2   2N7002

3V_PLUS

R22 1K

C_D   R22 1K
STATUS   R23 1K
RESET_FW   R24 1K

3V   73   TDI
100   TCK
24   TMS
3   TDO

84 82 81 80 79 78 77 76   DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0

83 67 44 17 4   VCCIO VCCIO VCCIO VCCIO VCCIO

92 72 60 52 35 12 37   VCCINT VCCINT VCCINT VCCINT VCCINT VCCINT VCC_CKLK

U1

EP1K10TC100-3

GND P_9

FW_CLK   90   CLK
CLK_16   39   CLK/GCLK1

P_8   29   LOCK
RXD   97   nWS
UART_TO_MEGA   96   nRS
DATA_FROM_PGA 99   nCS
TXD   98   CS
F_1   87   DEV_CLRn
F_2   93   DEV_OE

F_3   10   INIT_DONE
F_4   8   RDYnBUSY
F_8   5   DCLK
FW_CLK   75   DCLK

C_D   74   nCE
1   CONF_DONE
STATUS   25   nSTATUS
RESET_FW   51   nCONFIG
54   MSEL0
53   MSEL1
2   nCEO
GND

RESET   38   INPUT
UART_TO_FPGA   40   INPUT
F_6   89   INPUT
PWR_ERROR   91   INPUT

I/O   6   P_10
I/O   7   P_11
I/O   9   P_12
I/O   13   P_13
I/O   14   P_14
I/O   15   P_15
I/O   16   P_16
I/O   19

I/O   20   P_17
I/O   21   P_18
I/O   22   P_19
I/O   23   P_20
I/O   26   P_21
I/O   27   P_22
I/O   28   P_23
I/O   30   P_24

I/O   31   P_25
I/O   32   P_26
I/O   33   P_27
I/O   34   P_28
I/O   43   P_29
I/O   45   P_30
I/O   46   P_31
I/O   47   P_32

I/O   48   P_33
I/O   49   P_34
I/O   50   P_35
I/O   55   P_36

GND_CKLK GNDINT GNDINT GNDINT GNDINT GNDINT GNDINT GNDINT GNDINT
41 11 18 36 42 59 66 88 95

94 86 85   71 70 69 68 65 64 63 62   61 58 57 56

I/O I/O I/O   I/O I/O I/O I/O I/O I/O I/O I/O   I/O I/O I/O I/O

FW_clk   FW_CLK
FW_data   FW_DATA
UART_to_FPGA   UART_TO_FPGA
UART_to_MEGA   UART_TO_MEGA
Data_From_PGA   DATA_FROM_PGA
Reset_FW   RESET_FW
Reset   RESET
clk_16   CLK_16
PWR_ERROR   PWR_ERROR
5V   5V
3V   3V
TXD   TXD
RXD   RXD

J13
CON10
1
2
3
4
5
6
7
8
9
10

GND
5V
3V
F_1
F_2   R4 150
F_3   R6 150
F_4   R7 150
F_5   R10 150
F_6   R12 150
R25 150

P_37
P_38
P_39
P_40
P_41
P_42
P_43
P_44
P_45

F_5
F_7
FW_DATA
P_48
P_47
P_46

J16   VCC
1   Pull-up

J17
1
2
3
4
5
6
7
8
9
10

P_41
P_42
P_44
P_46
P_47
P_38

C_D   D11
FW_LOAD   D3   GND
ERROR

C7 0.1   C8 10.0   R2 270
3V   PWR_ERROR

FPGA module

p [48..1]

p_[48..1]

ResArray 5.6K