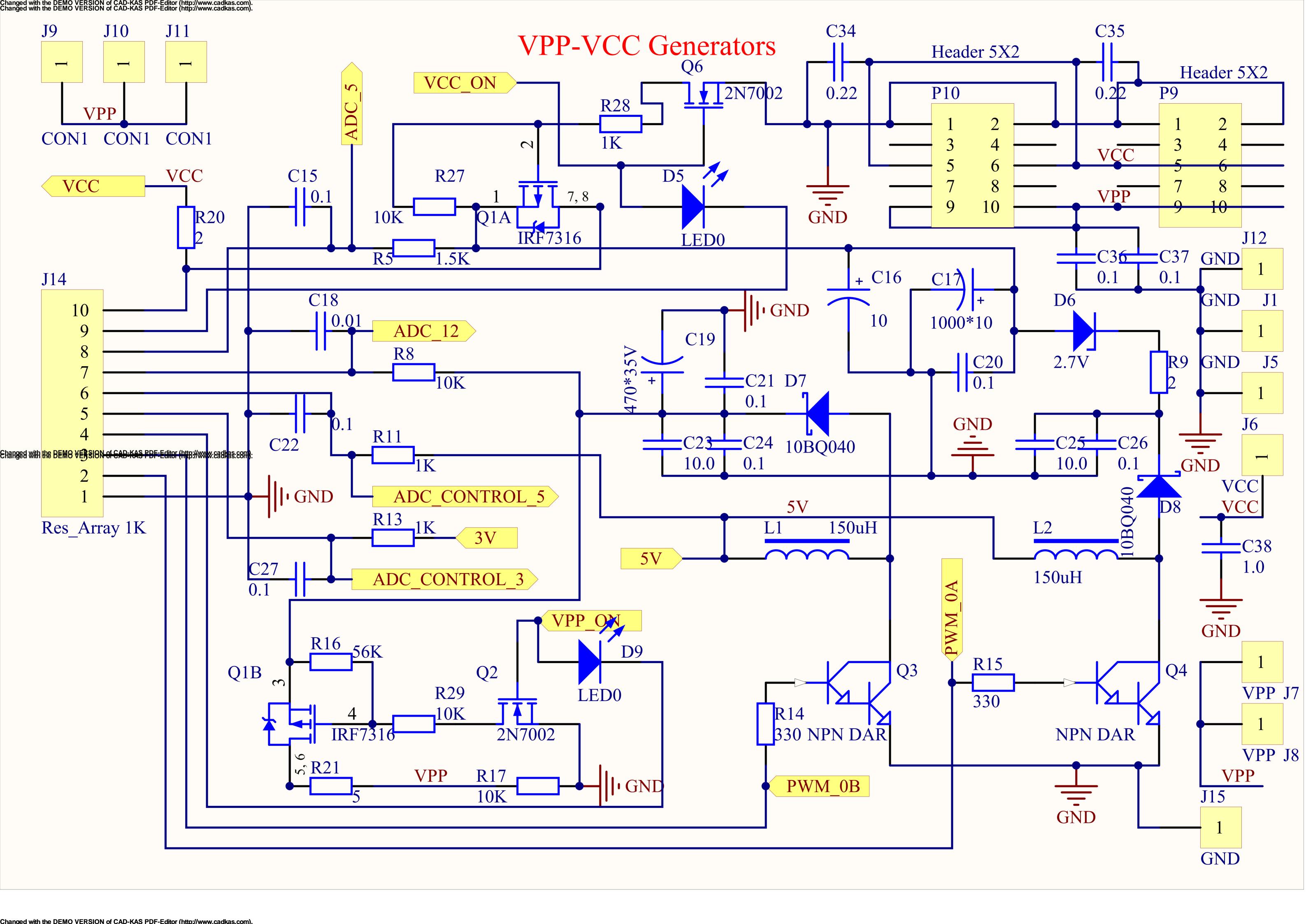
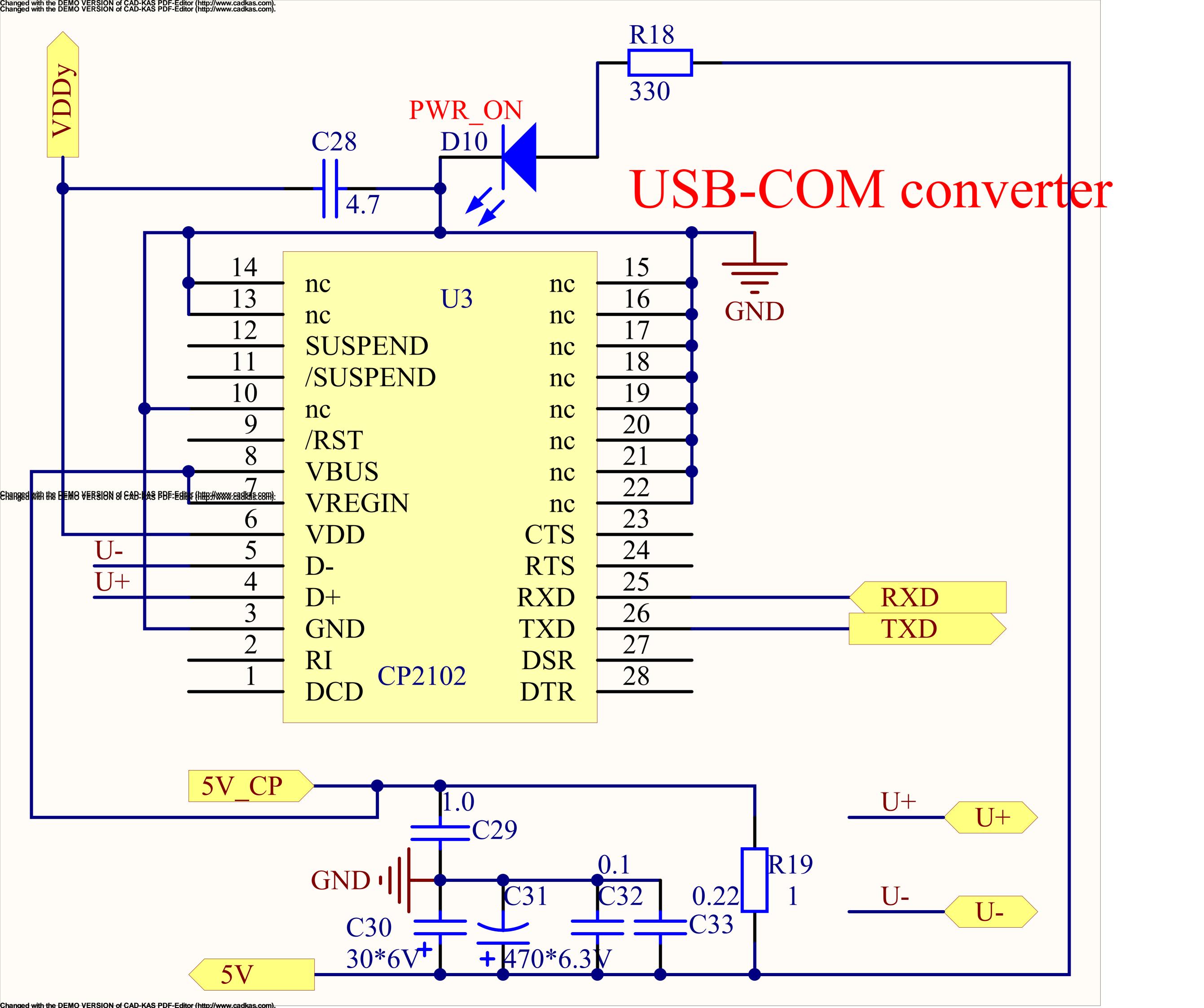
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DEV\_CC FW DATA P 19 FW data UART TO FPGA P 20 DEV\_OE UART\_to\_FPGA UART\_TO\_MEGA UART to MEGA DATA FROM PGA INIT\_DONE Data From PGA RESET FW RDYnBUSY Reset FW P 24 RESET Changed with the DEMO VERSION of CAD-KAS PDF-Editor (http://www.lalkale.com). Reset CLK 16 DCLK clk 16 PWR ERROR P 25 PWR\_ERROR P 26 CDCONF\_DONE TXD **STATUS** nSTATUS TXD RXD RESET FW RXD nCONFIG J13 P 30 MSEL0 P 31 GND MSEL1 P 32 CON<sub>10</sub> nCEO 38 40 89 RESET P 33 **INPUT** UART TO FPGA P 34 **INPUT** P 35 150 **INPUT** PWR ERROR P 36 **INPUT** 150 150 P 37 P 38 J17 J16 VCC D11 P 39  $C_D$ Pull-up P 40 GND <del>-</del> FW DATA FW LOAD P 42 P 43 **ERROR** P 45 P 38 PWR\_ERROR p [48..1] p\_[48..1] ResArray 5.6K

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