PINCM	TI IOMUX #DEFINE	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7	MODE 8	MODE 9
0	**1**	PA0	UART0_TX	I2C0_SDA	TIMA0_C0	TIMA_FAL1	TIMG8_C1	FCC_IN		
1	**2**	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMA_FAL2	TIMG8_IDX	TIMG8_C0		
6	**7**	PA2	TIMG8_C1	SPI0_CS0	TIMG7_C1	SPI1_CS0				
7	**8**	PA3	TIMG8_C0	SPI0_CS1	UART2_CTS	TIMA0_C2	COMP1_OUT	TIMG7_C0	TIMA0_C1	I2C1_SDA
8	**9**	PA4	TIMG8_C1	SPI0_POCI	UART2_RTS	TIMA0_C3	LFCLK_IN	TIMG7_C1	TIMA0_C1N	I2C1_SCL
9	**10**	PA5	TIMG8_C0	SPI0_PICO	TIMA_FAL1	TIMG0_C0	TIMG6_C0	FCC_IN		
10	**11**	PA6	TTIMG8_C1	SPI0_SCK	TIMA_FAL0	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N	
13	**14**	PA7	COMP0_OUT	CLK_OUT	TIMG8_C0	TIMA0_C2	TIMG8_IDX	TIMG7_C1	TIMA0_C1	
18	**19**	PA8	UART1_TX	SPI0_CS0	UART0_RTS	TIMA0_C0	TIMA1_C0N			
19	**20**	PA9	UART1_RX	SPI0_PICO	UART0_CTS	TIMA0_C1	RTC_OUT	TIMA0_C0N	TIMA1_C1N	CLK_OUT
20	**21**	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA1_C0	TIMG12_C0	TIMA0_C2	I2C1_SDA	CLK_OUT
21	**22**	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA1_C1	COMP0_OUT	TIMA0_C2N	I2C1_SCL	
33	**34**	PA12	UART3_CTS	SPI0_SCK	TIMG0_C0	CAN_TX	TIMA0_C3	FCC_IN		
34	**35**	PA13	UART3_RTS	SPI0_POCI	UART3_RX	TIMG0_C1	CAN_RX	TIMA0_C3N		
35	**36**	PA14	UART0_CTS	SPI0_PICO	UART3_TX	TIMG12_C0	CLK_OUT			
36	**37**	PA15	UART0_RTS	SPI1_CS2	I2C1_SCL	TIMA1_C0	TIMG8_IDX	TIMA1_C0N	TIMA0_C2	
37	**38**	PA16	COMP2_OUT	SPI1_POCI	I2C1_SDA	TIMA1_C1	TIMA1_C1N	TIMA0_C2N	FCC_IN	
38	**39**	PA17	UART1_TX	SPI1_SCK	I2C1_SCL	TIMA0_C3	TIMG7_C0	TIMA1_C0		
39	**40**	PA18	UART1_RX	SPI1_PICO	I2C1_SDA	TIMA0_C3N	TIMG7_C1	TIMA1_C1		
40	**41**	PA19	SWDIO							
41	**42**	PA20	SWCLK							
45	**46**	PA21	UART2_TX	TIMG8_C0	UART1_CTS	TIMA0_C0	TIMG6_C0			
46	**47**	PA22	UART2_RX	TIMG8_C1	UART1_RTS	TIMA0_C1	CLK_OUT	TIMA0_C0N	TIMG6_C1	
52	**53**	PA23	UART2_TX	SPI0_CS3	TIMA0_C3	TIMG0_C0	UART3_CTS	TIMG7_C0	TIMG8_C0	
53	**54**	PA24	UART2_RX	SPI0_CS2	TIMA0_C3N	TIMG0_C1	UART3_RTS	TIMG7_C1	TIMA1_C1	
54	**55**	PA25	UART3_RX	SPI1_CS3	TIMG12_C1	TIMA0_C3	TIMA0_C1N			
58	**59**	PA26	UART3_TX	SPI1_CS0	TIMG8_C0	TIMA_FAL0	CAN_TX	TIMG7_C0		
59	**60**	PA27	RTC_OUT	SPI1_CS1	TIMG8_C1	TIMA_FAL2	CAN_RX	TIMG7_C1		
2	**3**	PA28	UART0_TX	I2C0_SDA	TIMA0_C3	TIMA_FAL0	TIMG7_C0	TIMA1_C0		
3	**4**	PA29	I2C1_SCL	UART2_RTS	TIMG8_C0	TIMG6_C0				
4	**5**	PA30	I2C1_SDA	UART2_CTS	TIMG8_C1	TIMG6_C1				
5	**6**	PA31	UART0_RX	I2C0_SCL	TIMA0_C3N	TIMG12_C1	CLK_OUT	TIMG7_C1	TIMA1_C1	
11	**12**	PB0	UART0_TX	SPI1_CS2	TIMA1_C0	TIMA0_C2				
12	**13**	PB1	UART0_RX	SPI1_CS3	TIMA1_C1	TIMA0_C2N				
14	**15**	PB2	UART3_TX	UART2_CTS	I2C1_SCL	TIMA0_C3	UART1_CTS	TIMG6_C0	TIMA1_C0	
15	**16**	PB3	UART3_RX	UART2_RTS	I2C1_SDA	TIMA0_C3N	UART1_RTS	TIMG6_C1	TIMA1_C1	
16	**17**	PB4	UART1_TX	UART3_CTS	TIMA1_C0	TIMA0_C2	TIMA1_C0N			
17	**18**	PB5	UART1_RX	UART3_RTS	TIMA1_C1	TIMA0_C2N	TIMA1_C1N			
22	**23**	PB6	UART1_TX	SPI1_CS0	SPI0_CS1	TIMG8_C0	UART2_CTS	TIMG6_C0	TIMA1_C0N	
23	**24**	PB7	UART1_RX	SPI1_POCI	SPI0_CS2	TIMG8_C1	UART2_RTS	TIMG6_C1	TIMA1_C1N	
24	**25**	PB8	UART1_CTS	SPI1_PICO	TIMA0_C0	COMP1_OUT				
25	**26**	PB9	UART1_RTS	SPI1_SCK	TIMA0_C1	TIMA0_C0N				
26	**27**	PB10	TIMG0_C0	TIMG8_C0	COMP1_OUT	TIMG6_C0				
27	**28**	PB11	TIMG0_C1	TIMG8_C1	CLK_OUT	TIMG6_C1				
28	**29**	PB12	UART3_TX	TIMA0_C2	TIMA_FAL1	TIMA0_C1				
29	**30**	PB13	UART3_RX	TIMA0_C3	TIMG12_C0	TIMA0_C1N				
30	**31**	PB14	SPI1_CS3	SPI1_POCI	SPI0_CS3	TIMG12_C1	TIMG8_IDX	TIMA0_C0		
31	**32**	PB15	UART2_TX	SPI1_PICO	UART3_CTS	TIMG8_C0	TIMG7_C0			
32	**33**	PB16	UART2_RX	SPI1_SCK	UART3_RTS	TIMG8_C1	TIMG7_C1			
42	**43**	PB17	UART2_TX	SPI0_PICO	SPI1_CS1	TIMA1_C0	TIMA0_C2			
43	**44**	PB18	UART2_RX	SPI0_SCK	SPI1_CS2	TIMA1_C1	TIMA0_C2N			
44	**45**	PB19	COMP2_OUT	SPI0_POCI	TIMG8_C1	UART0_CTS	TIMG7_C1			
47	**48**	PB20	SPI0_CS2	SPI1_CS0	TIMA0_C2	TIMG12_C0	TIMA_FAL1	TIMA0_C1	TIMA1_C1N	
48	**49**	PB21	SPI1_POCI	TIMG8_C0						
49	**50**	PB22	SPI1_PICO	TIMG8_C1						
50	**51**	PB23	SPI1_SCK	COMP0_OUT	TIMA_FAL0					
51	**52**	PB24	SPI0_CS3	SPI0_CS1	TIMA0_C3	TIMG12_C1	TIMA0_C1N	TIMA1_C0N		
55	**56**	PB25	UART0_CTS	SPI0_CS0	TIMA_FAL2					
56	**57**	PB26	UART0_RTS	SPI0_CS1	TIMA0_C3	TIMG6_C0	TIMA1_C0			
57	**58**	PB27	COMP2_OUT	SPI1_CS1	TIMA0_C3N	TIMG6_C1	TIMA1_C1			