AN930.2: EFR32 Series 2 2.4 GHz Matching Guide

The EFR32 Series 2 devices include chip variants that provide 2.4 GHz-only operation. In addition, the EFR32xG21 chips are only available in a 4x4 mm 32-pin QFN package while the EFR32xG22 parts have both 32- and 40-pin package variants available (QFN32, TQFN32, QFN40). This application note describes the matching techniques applied to the EFR32 Series 2 Wireless Gecko Portfolio in the 2.4 GHz band.

For information on PCB layout requirements for proper 2.4 GHz operation, refer to application note, AN928.2: EFR32 Series 2 Layout Design Guide.

KEY POINTS

- Description of the applied 2.4 GHz matching networks and techniques for the EFR32 Series 2 devices
- Detailed discussion of the design steps and design examples
- Measured TX fundamental and harmonic performance
- Measured receive sensitivity values

1. Device Compatibility

This application note supports the following devices:

EFR32 Wireless Gecko Series 2:

- EFR32MG21
- EFR32MG22
- EFR32BG21
- EFR32BG22
- EFR32FG22

2. Introduction

This application note is intended to help users achieve the best 2.4 GHz RF match for targeted applications. It describes the details of matching network design procedures and presents additional test results.

Thorough derivations of four different matching options are presented for EFR32xG21:

- 4-element discrete LC match for up to 0 dBm power levels
- 3-element discrete LC match for up to +10 dBm power levels
- 5-element discrete LC match for up to +20 dBm power levels
- 4-element combined discrete LC match for both +10 and 0 dBm power levels

A 4-element discrete LC match for up to +6 dBm power levels is also presented for EFR32xG22.

The 4x4 mm, 32-pin 2.4 GHz-only version's package pinouts are shown in the figures below for each EFR32xG21 and EFR32xG22 part. The 2.4 GHz RF IO pins are highlighted with a red box.

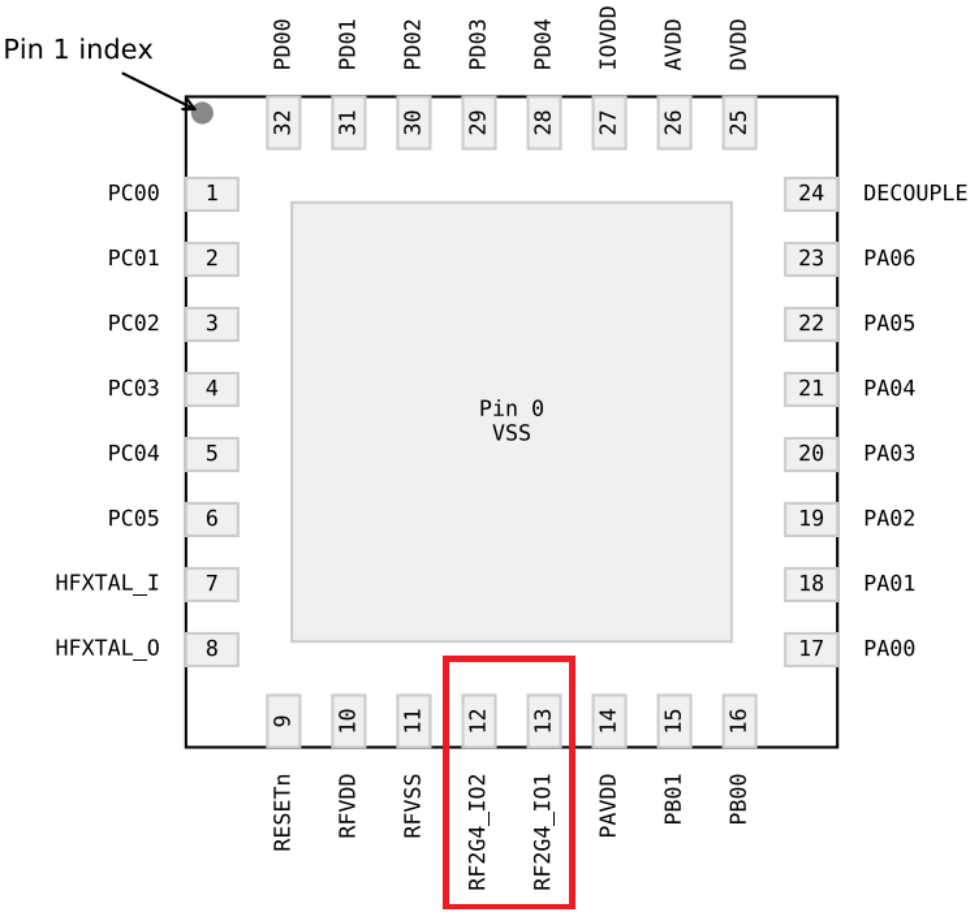


Figure 2.1. EFR32xG21 2.4 GHz RF IO Pins

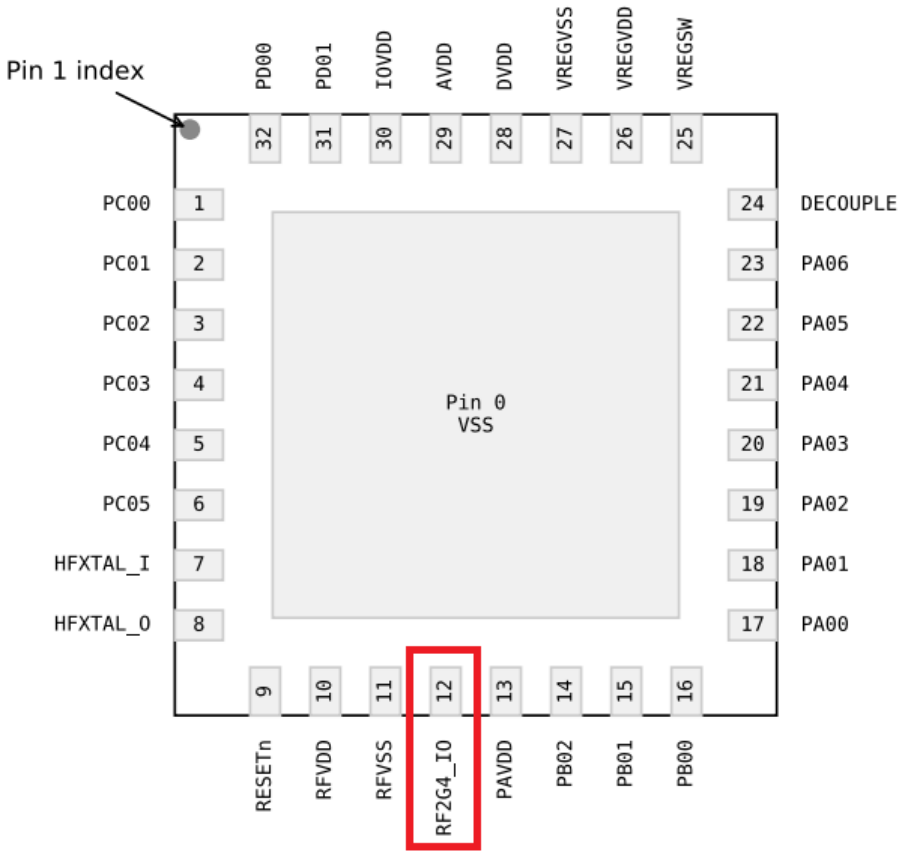


Figure 2.2. EFR32xG22 2.4 GHz RF IO Pin

2.1 Related Literature

Related documentation includes:

- AN928.2: EFR32 Series 2 Layout Design Guide
- AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations

3. RF Architecture Overview

3.1 EFR32xG21 RF Front-End Overview

The EFR32 Series 2 xG21 chip family has 2.4 GHz RF front ends only. The 2.4 GHz RF front-end architecture is shown in the figure below. The 2.4 GHz antenna interface consists of two pins (RF2G4_IO1 and RF2G4_IO2) that interface directly to the on-chip BALUN.

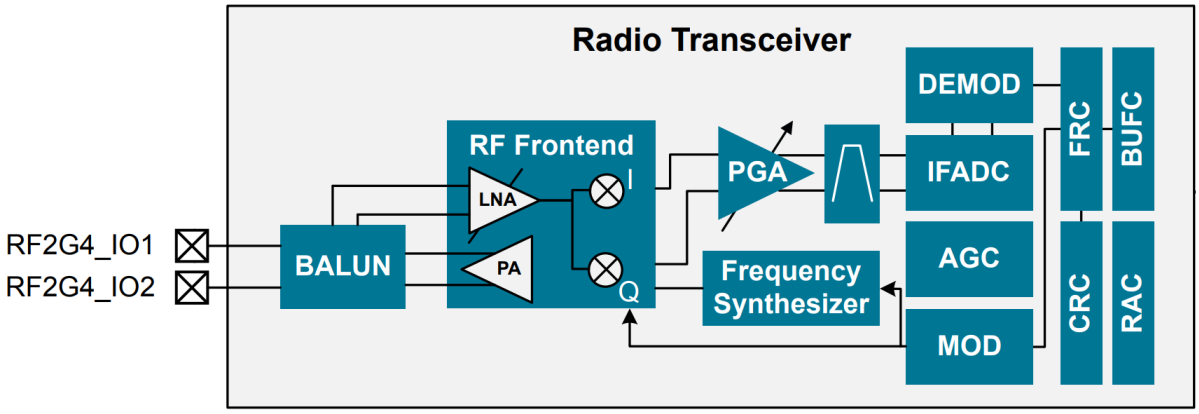


Figure 3.1. 2.4 GHz RF Front-end Configuration

Several changes compared to the EFR32 Series 1 chip variants are highlighted below:

- New RF front-end topology: Three PAs included that require an optimal load impedance for each TX power level, i.e., different matches are required per max TX power.
- Power supply scheme: There is no on-chip DCDC converter available. Optimized for mains-power applications.
- Pre-Regulator for the Power Amplifiers: Linear regulator with an input of PAVDD and output of PA blocks. Regulates to a target voltage when PAVDD > Vtarget. Follows supply with a ~30 mV offset when PAVDD ≤ Vtarget (and PA power will trail off also).
  - For +10 and 0 dBm PA modes: Vtarget = 1.8 V.
  - For +20 dBm PA mode: Vtarget = 3.3 V.
- RFSENSE removed, instead a wide-band power sensing block introduced for better out-of-band blocker detection and coexistence performance.

The on-chip part of the front-end comprises three PA structures optimized for the TX power levels of 0, 10, and 20 dBm, two differential LNAs, and an integrated balun. Each PA is biased through the PAVDD pin. Externally, a single-ended matching network and harmonic filtering are required.

- Differential Class-AB mode PA and an internal balun for TX power of +20 dBm
- Single-ended Class-D mode PA for TX power of +10 dBm
- Single-ended Class-D mode PA for TX power of 0 dBm
- Two LNAs
- Two RF IO ports available: Internal switches ground one of the two sides to create single-ended inputs / outputs on either RFIO pin. This also allows a switchless diversity solution, for instance.

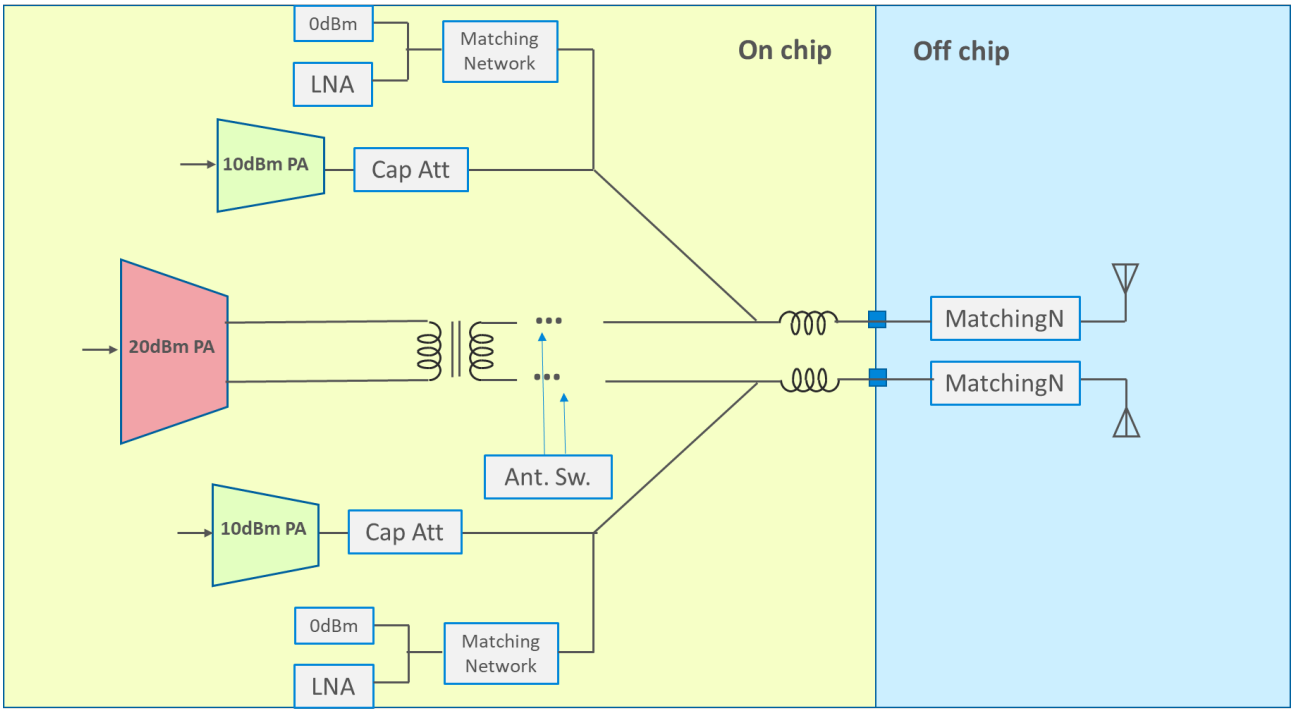


Figure 3.2. 2.4 GHz RF Front-end Block Diagram

3.2 EFR32xG22 RF Front-End Overview

The EFR32 Series 2 xG22 chip family has 2.4 GHz RF front ends only. The radio subsystem is shown in the figure below. The RF front-end consists of an integrated LNA and two separate PAs with an internal switch to select between them, while one RF IO port is available (RF2G4_IO) at a chip pin.

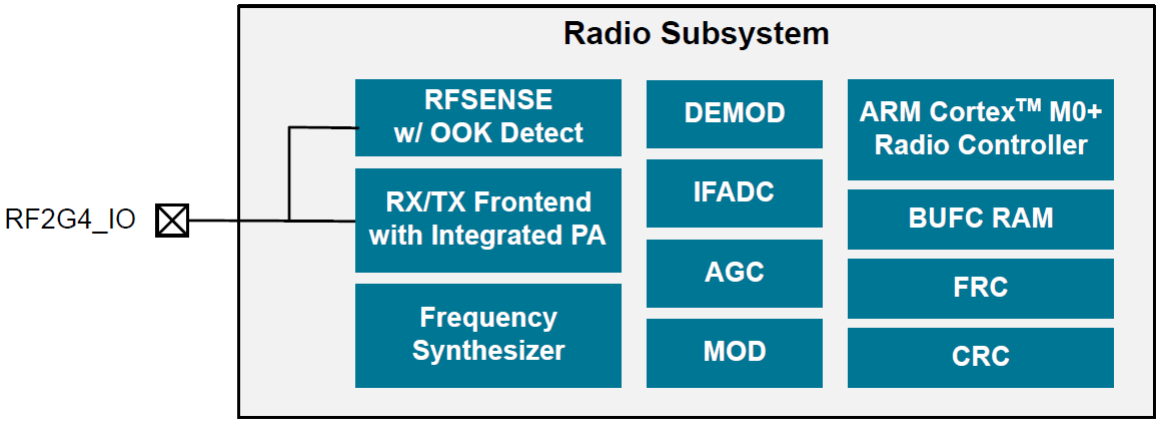


Figure 3.3. EFR32xG22 Radio Subsystem

A few highlights on the RF front-end blocks:

- Two separate Class-D PAs, optimized for maximum TX power levels of 0 and +6 dBm.
  - Each PA is biased through the PAVDD pin
  - Externally, a single-ended matching network and harmonic filtering are required
- Power supply scheme: An on-chip, dc-dc converter is available, so this chip variant is optimized for low-power applications with high efficiency.

4. 2.4 GHz RF Matching Design Steps

2.4 GHz RF matching design for EFR32 chips consists of the following steps:

1. Determine the optimum termination impedance for the PA. Note that different matching topologies are recommended for different TX power levels as shown in the Introduction section.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the pcb have a major effect, so tuning/optimization of the design is required. Here an optional EM simulation can be done, but simulations with well-estimated pcb parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

4.1 Determining the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the RF2G4_IO1/2 pin if 50 Ω termination is applied at the antenna port.

The RF2G4_IO1/2 RF port termination determines the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX mode. In addition, proper harmonic suppression and good RX sensitivity in reception mode are required.

4.1.1 EFR32xG21 Optimum PA Load Impedance

The design target of optimum load impedance looking from the PA to the antenna is 14 + j5 Ω at the PA. However, the optimum termination impedance for both delivering the desired power and achieving the best PA efficiency in TX mode is determined by load-pull testing. The optimum termination impedance at the chip pin is determined for each PA of the EFR32xG21 parts and it slightly differs for the different power levels, i.e., for the +20, +10, and 0 dBm PAs, and also differs from the design target at the PA due to bonding wire inductances and parasitics. This termination impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load. The optimum termination impedance at chip RF2G4_IO pin is the following:

- For the **+20 dBm** PA: Zload_opt = **12.6 - j11 Ω**
- For the **+10 dBm** PA: Zload_opt = **12.2 - j8.3 Ω**
- For the **0 dBm** PA: Zload_opt = **17.4 + j3.9 Ω**

The load-pull curves for each PA are shown in 6. Appendix 1 PA Optimum Termination Impedance on EFR32xG21.

Applications with one antenna, e.g., non-diversity applications, typically require using only one of the RF IO ports available on the EFR32xG21 parts, in which case the recommended active RF IO port is **RF2G4_IO2**. Because this pin has a shorter on-chip, internal connection to the PA blocks so slightly lower parasitics appear on this pin.

The proper impedance at one of the single-ended RF2G4_IO pins also depends on the loading of the other RF2G4_IO pin. To keep its effect negligible, for applications with one antenna with both +10 and +20 dBm PAs, it is recommended to directly tie the un-used RF2G4_IO pin back to the center GND pad of the chip. However, the 0 dBm PA requires to be DC blocked externally so the method described for the +10 and +20 dBm PAs doesn't work. The 0 dBm PA recommended match includes a series capacitor in the RF path but for proper operation a DC-blocking 0.5pF capacitor to GND needs to also be used on the unused RF port. Silicon Labs' reference radio boards are suitable and optimized to be used with the +10 and +20 dBm PAs because of the short between the chip pin and center GND pad under the chip. More detailed information about proper layout design can be found in application note, "AN928.2: EFR32 Series 2 Layout Design Guide".

In real radio links, the TX power and the receiver sensitivity together (i.e., the link budget) determine the range. So, with the applied TX termination impedance, the impedance match in RX mode should also be acceptable. Fortunately, the RX sensitivity is quite immune to impedance variations. The sensitivity variation is less than 0.5 dB if the termination changes from 50 Ω to the PA optimum impedance (Zload_opt) given above.

4.1.2 EFR32xG22 Optimum PA Load Impedance

The design target of optimum load impedance looking from the PA to the antenna is 50 Ω at the PA for both 0 and +6 dBm PA. However, the optimum termination impedance at the chip pin determined for each PA of the EFR32xG22 parts differs from the design target at the PA due to bonding wire inductances and parasitics. Also, the output match plus low-pass filter (LPF) section is designed to enhance the suppression of the 2nd- and 3rd-order harmonics. Thus, the optimum termination impedance at the chip pin is about **37 + j5 Ω** for both 0 and +6 dBm PA and this impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load.

Because the optimum termination impedance is the same for both 0 and +6 dBm PA, the matching network is also identical for these different power levels. Silicon Labs provides radio boards with one matching network applied, however, the series dc-blocking capacitor in the match plus LPF section must be needed only when the 0 dBm PA is being utilized.

4.2 Choosing the RF Matching Topology

The second step of the matching design procedure is to choose the appropriate RF matching topology.

In addition to creating an optimum termination impedance on the IC side, the matching solution must exhibit sufficiently robust harmonic filtering characteristics to comply with emissions standards. There are many different types of RF matching topologies. Separate matching and harmonic filtering sections can be utilized, or they can be combined in one circuit. To minimize the number of elements, all matches presented here are of the combined type, with low-pass circuits employed for their inherent harmonic suppression characteristics.

Four 2.4 GHz matching topologies for EFR32xG21 are presented here:

- 4-element discrete LC match for the 0 dBm PA, i.e., for power levels equal or below 0 dBm
- 4-element combined discrete LC match for both 0 and +10 dBm PA, i.e., for power levels equal or below +10 dBm
- 3-element discrete LC match for the +10 dBm PA, i.e., for power levels equal or below +10 dBm, but not suitable to operate with the 0 dBm PA (i.e., equal or below 0 dBm the required PA to be used is still the +10 dBm PA which has less power efficiency at that lower power range)
- 5-element discrete LC match for the +20dBm PA, i.e., for power levels equal or below +20 dBm (not suitable to operate with the 0 dBm PA)

For EFR32xG22, a single 4-element discrete LC match is provided that is optimized for both 0 and +6 dBm PA, i.e., for any power level available with this part.

4.3 Initial Design with Ideal, Loss-Free Elements

After choosing the appropriate topology for the application based on the TX power level requirements, the third step of the matching design procedure is to generate a lumped element schematic of the match with ideal loss-free elements and without PCB parasitics.

The matching circuit should show an input impedance of *Zload_opt* at the RF IO port of the chip while it is terminated by 50 Ω load at its output (ANT port). The impedance procedure is shown in the next sections, where, for simplification, the matching design is started from a termination impedance (*ZL*) which is the complex conjugate of the *Zload_opt* impedance. The reason is that the matching network will show the required *Zload_opt* impedance at its RF port only if it is perfectly matched there to a termination impedance which is the complex conjugate of the *Zload_opt* impedance.

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free ideal capacitors and inductors are used, and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization.

4.4 Design with Parasitics and Losses

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the used SMD components and also the PCB parasitic effects need to be taken into account during the matching network design. The SMD components at these high-frequency ranges behave as a resonator. A capacitor can be realized by a series RLC resonant circuit, meanwhile an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L-C components, and can have considerable series parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. For more details on the SMD parasitic descriptions and the rough estimation of PCB parasitics, refer to the application note, AN930.1: EFR32 Series 1 2.4 GHz Matching Guide, and the SMD manufacturer website at www.murata.com, in regards to the appropriate SMD equivalent circuits.

The SMD components with different sizes have different parasitics, so it is also important to calculate with the appropriate values. Silicon Labs reference designs use **SMD 0201** components.

The PCB parasitics also have effects on the RF performance versus tuned component values of the matching network. Silicon Labs reference design matching network component values are typically given with a 4-layer PCB with a separation of about 300 µm between the top (component-side) and first inner layer. This distance mostly determines the parasitics capacitance and via inductance, which influences the return-path impedance between the matching network and chip GND (especially at the harmonics). Also, the series trace placed between the chip pin and matching network is part of the match, the dimensions of which should be followed carefully from Silicon Labs reference designs. Refer to AN928.2: EFR32 Series 2 Layout Design Guide for more layout details.

In the case of using different PCB stack-up (e.g. 2-layer PCB with board thickness > 300 um), the matching network component values need tuning to keep the RF performance values, especially the harmonic suppressions.

The recommended matching network for the RF port(s) of each part is shown in the section Recommended Matching Networks. The circuit provides the optimum impedance load for the EFR32xG2x part while ensuring sufficient harmonic suppression. Some of the shunt capacitors are tuned to have self-resonances at the frequency ranges falling close to TX harmonics and therefore, they provide enhanced attenuation at specific harmonics. The impedance transformation procedure for each PA of EFR32xG21 is shown in the Smith Chart figures below. The impedance transformation procedure for the PAs of EFR32xG22 is not separately shown here on the Smith Chart because the matching network is basically a tuned LPF between 50 Ω loads.

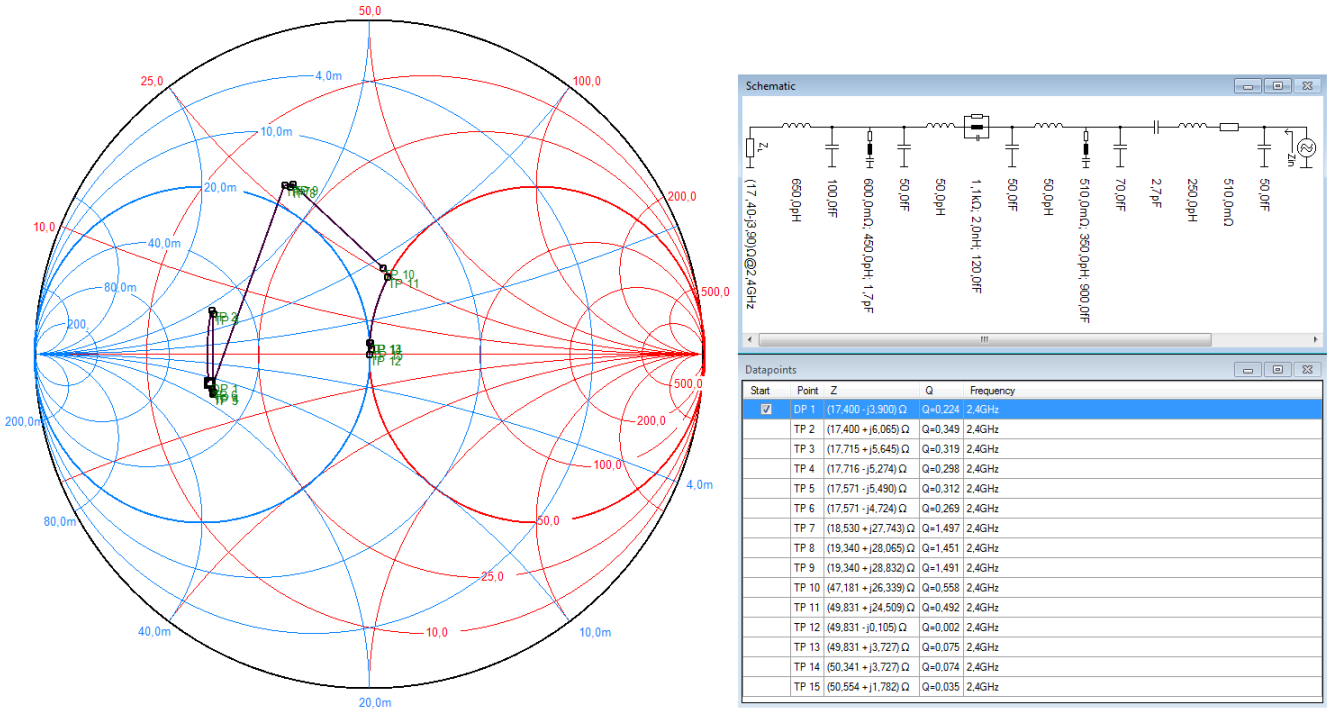
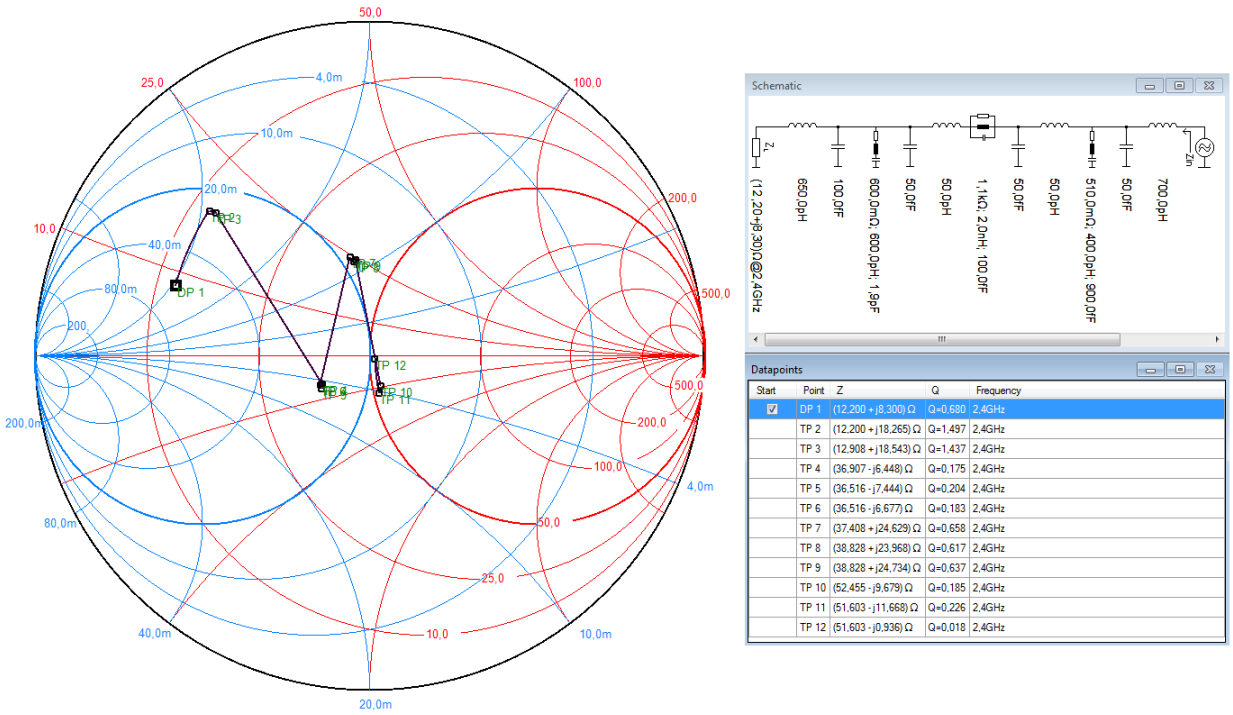
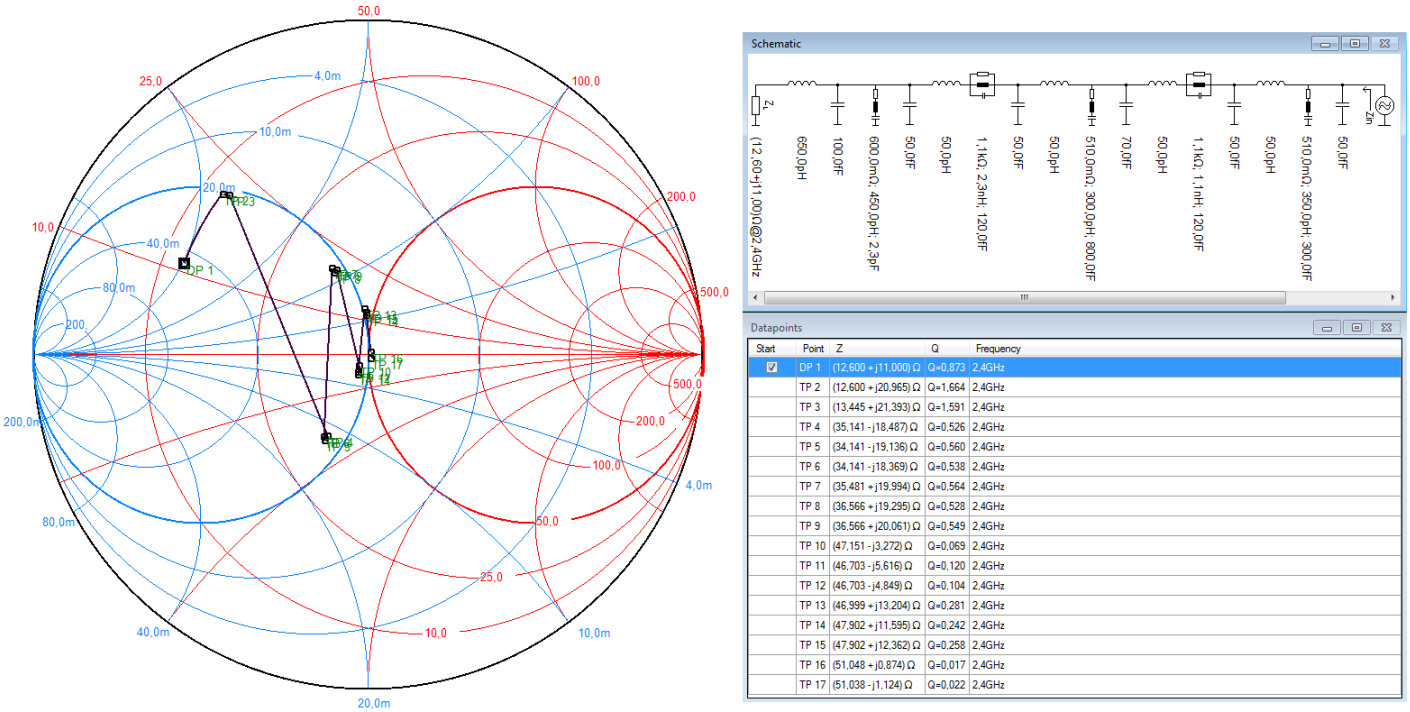


Figure 4.1. EFR32xG21 4-element Match with SMD and PCB Layout Parasitics Tuned for the 0 dBm Power Level Optimum



Start	Point	Z	Q	Frequency
☑	DP 1	(12,200 + j8,300) Ω	Q=0,680	2,4GHz
	TP 2	(12,200 + j18,265) Ω	Q=1,497	2,4GHz
	TP 3	(12,908 + j18,543) Ω	Q=1,437	2,4GHz
	TP 4	(36,907 - j6,448) Ω	Q=0,175	2,4GHz
	TP 5	(36,516 - j7,444) Ω	Q=0,204	2,4GHz
	TP 6	(36,516 - j6,677) Ω	Q=0,183	2,4GHz
	TP 7	(37,408 + j24,629) Ω	Q=0,658	2,4GHz
	TP 8	(38,828 + j23,968) Ω	Q=0,617	2,4GHz
	TP 9	(38,828 + j24,734) Ω	Q=0,637	2,4GHz
	TP 10	(52,455 - j9,679) Ω	Q=0,185	2,4GHz
	TP 11	(51,603 - j11,668) Ω	Q=0,226	2,4GHz
	TP 12	(51,603 - j0,936) Ω	Q=0,018	2,4GHz

Figure 4.2. EFR32xG21 3-element Match with SMD and PCB Layout Parasitics Tuned for the 10 dBm Power Level Optimum



Start	Point	Z	Q	Frequency
☑	DP 1	(12,600 + j11,000) Ω	Q=0,873	2,4GHz
	TP 2	(12,600 + j20,965) Ω	Q=1,664	2,4GHz
	TP 3	(13,445 + j21,393) Ω	Q=1,591	2,4GHz
	TP 4	(35,141 - j18,487) Ω	Q=0,526	2,4GHz
	TP 5	(34,141 - j19,136) Ω	Q=0,560	2,4GHz
	TP 6	(34,141 - j18,369) Ω	Q=0,538	2,4GHz
	TP 7	(35,481 + j19,994) Ω	Q=0,564	2,4GHz
	TP 8	(36,566 + j19,295) Ω	Q=0,528	2,4GHz
	TP 9	(36,566 + j20,061) Ω	Q=0,549	2,4GHz
	TP 10	(47,151 - j3,272) Ω	Q=0,069	2,4GHz
	TP 11	(46,703 - j5,616) Ω	Q=0,120	2,4GHz
	TP 12	(46,703 - j4,849) Ω	Q=0,104	2,4GHz
	TP 13	(46,999 + j13,204) Ω	Q=0,281	2,4GHz
	TP 14	(47,902 + j11,595) Ω	Q=0,242	2,4GHz
	TP 15	(47,902 + j12,362) Ω	Q=0,258	2,4GHz
	TP 16	(51,048 + j0,874) Ω	Q=0,017	2,4GHz
	TP 17	(51,038 - j1,124) Ω	Q=0,022	2,4GHz

Figure 4.3. EFR32xG21 5-element Match with SMD and PCB Layout Parasitics Tuned for the 20 dBm Power Level Optimum

4.5 Simulation Example on the 5-element Match for +20 dBm Power Level on EFR32xG21

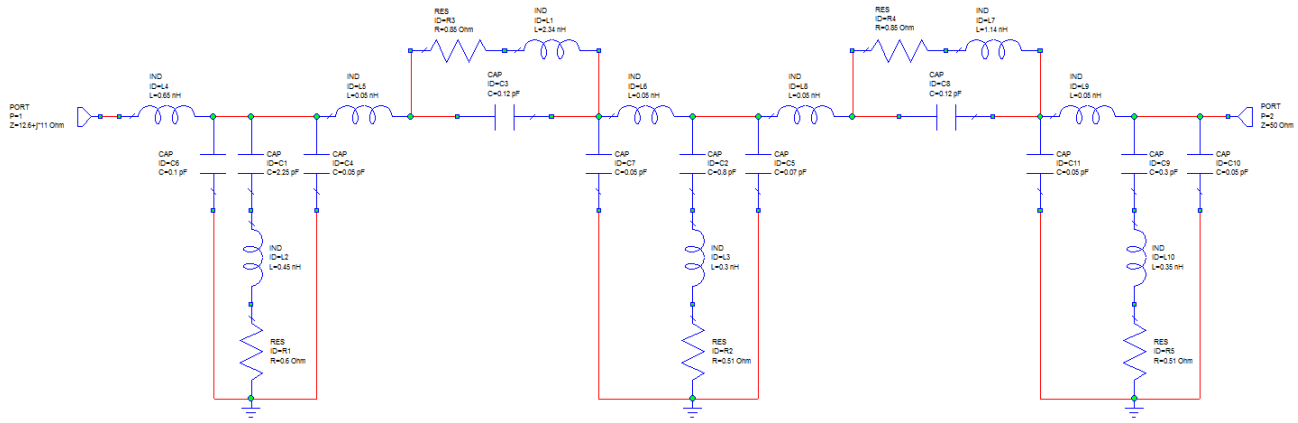


Figure 4.4. Discrete Schematic Model of 5-element Match with SMD and PCB Layout Parasitics

Port 1 (left-hand side-end) is the RF2G4_IO chip port/pin where the port impedance (*ZL*) should be set for the complex conjugate of optimum load impedance (*ZL=Zload_opt**), while the Port 2 (right end) is the 50-ohm antenna port.

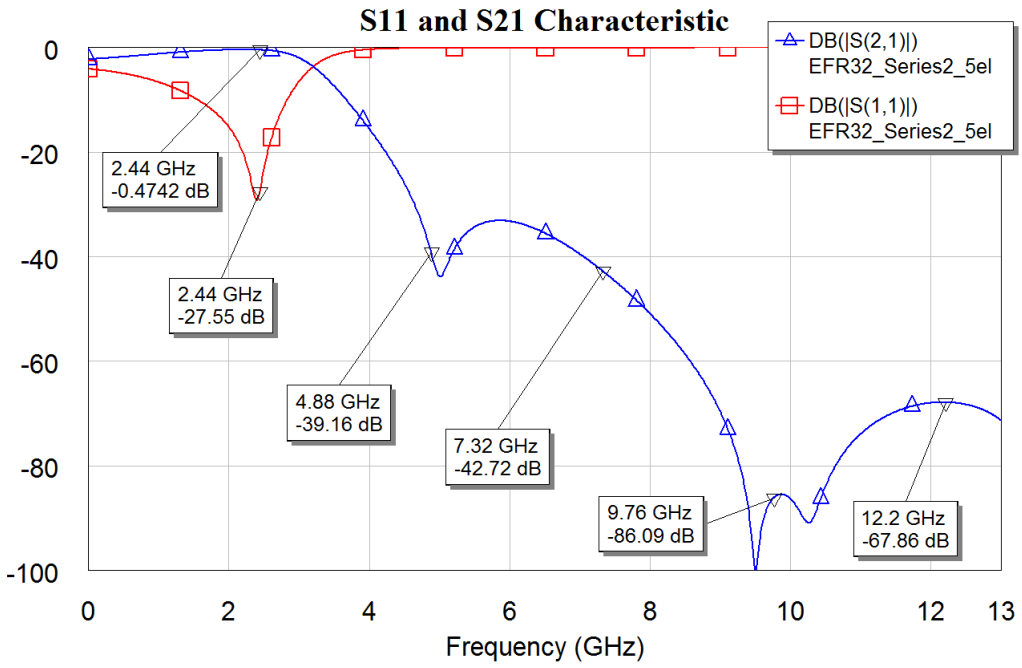


Figure 4.5. S11 and S21 Characteristics of 5-element Match for 20 dBm Power Level Optimum

5. Recommended Matching Networks

5.1 EFR32xG21 Matching Networks

5.1.1 Recommended Matching Network for the 0 dBm PA

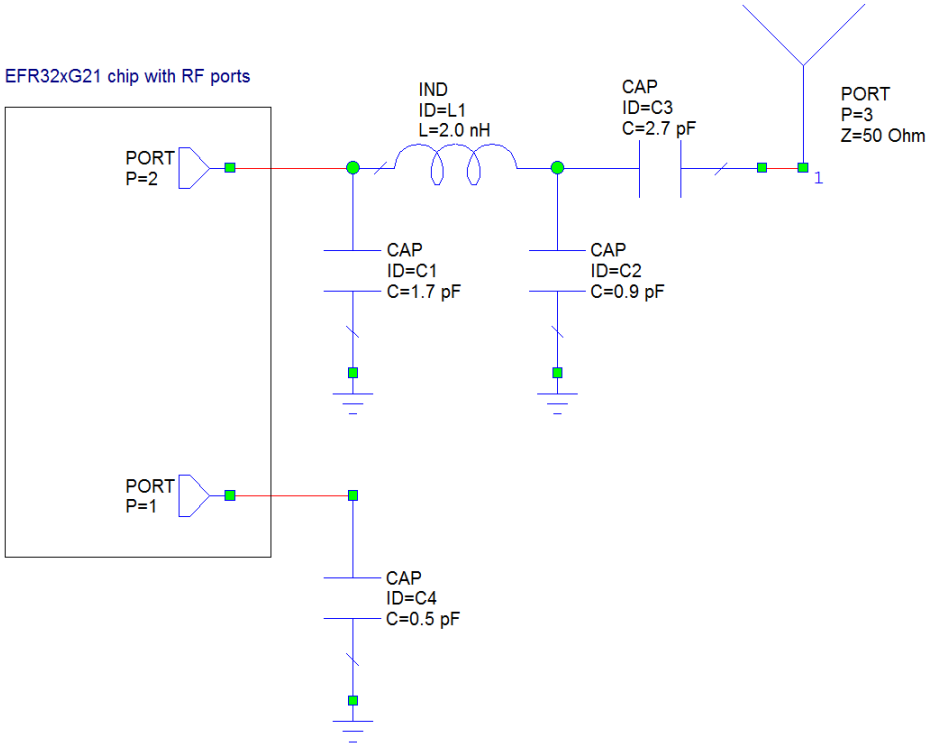


Figure 5.1. Matching Network Schematic for the 0 dBm PA

It is recommended to use this matching network shown above when the maximum transmitting power requirement is 0 dBm (TX power ≤ 0 dBm), i.e., the application utilizes the 0 dBm PA to achieve the possible best efficiency at that low power regions. Due to the highly optimized power efficiency, the need of 4-element matching network here is mostly driven by the harmonic suppression requirements. The unused RF2G4_IO pin needs to be grounded via an (DC-blocking) 0.5 pF capacitor.

Table 5.1. Final SMD Values for the 0 dBm PA (4-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.7 pF	± 0.5 %	GRM0335C1H1R7WA01D	Murata
L1	2.0 nH	± 0.1 nH	LQP03HQ2N0B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata
C3	2.7 pF	± 0.5 %	GRM0335C1H2R7WA01D	Murata
C4	0.5 pF	± 0.05 pF	GRM0335C1HR50WA01D	Murata

5.1.2 Recommended Matching Network for the +10 dBm PA

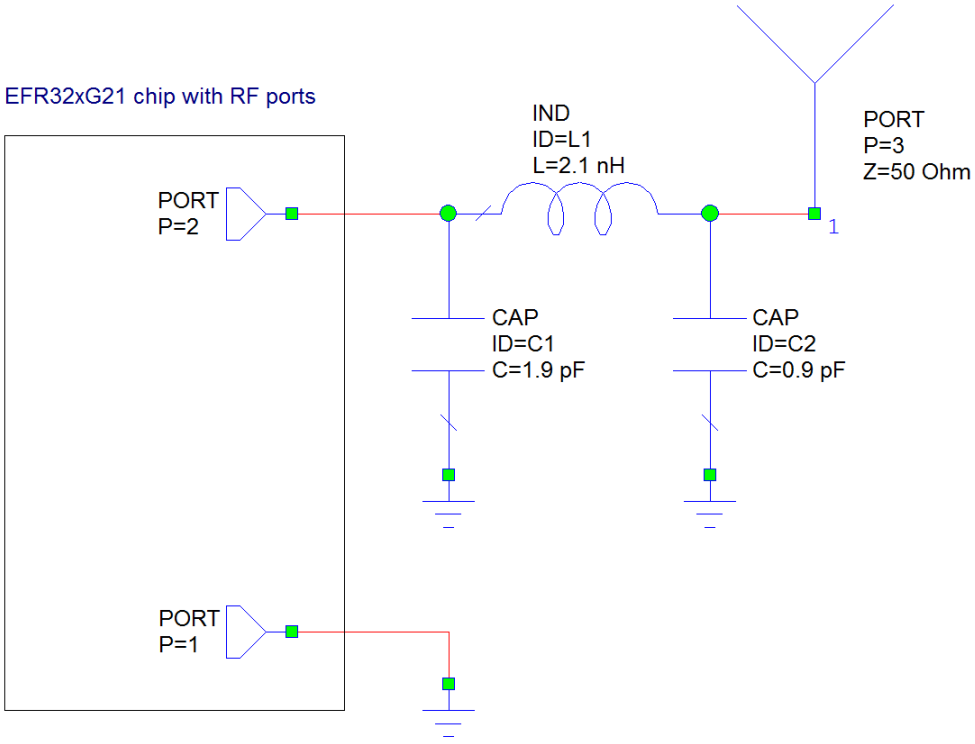


Figure 5.2. Matching Network Schematic for the +10 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +10 dBm (0 dBm < TX power ≤ +10 dBm), i.e., the application utilizes the +10 dBm PA to achieve the possible best efficiency at that power level state. The unused RF2G4_IO pin can be grounded directly. Make a short from the pin back to the center exposed pad of the part under the chip.

Table 5.2. Final SMD Values for the +10 dBm PA (3-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.5 %	GRM0335C1H1R9WA01D	Murata
L1	2.1 nH	± 0.1 nH	LQP03HQ2N1B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata

5.1.3 Recommended Combined Matching Network for Both 0/10 dBm PA

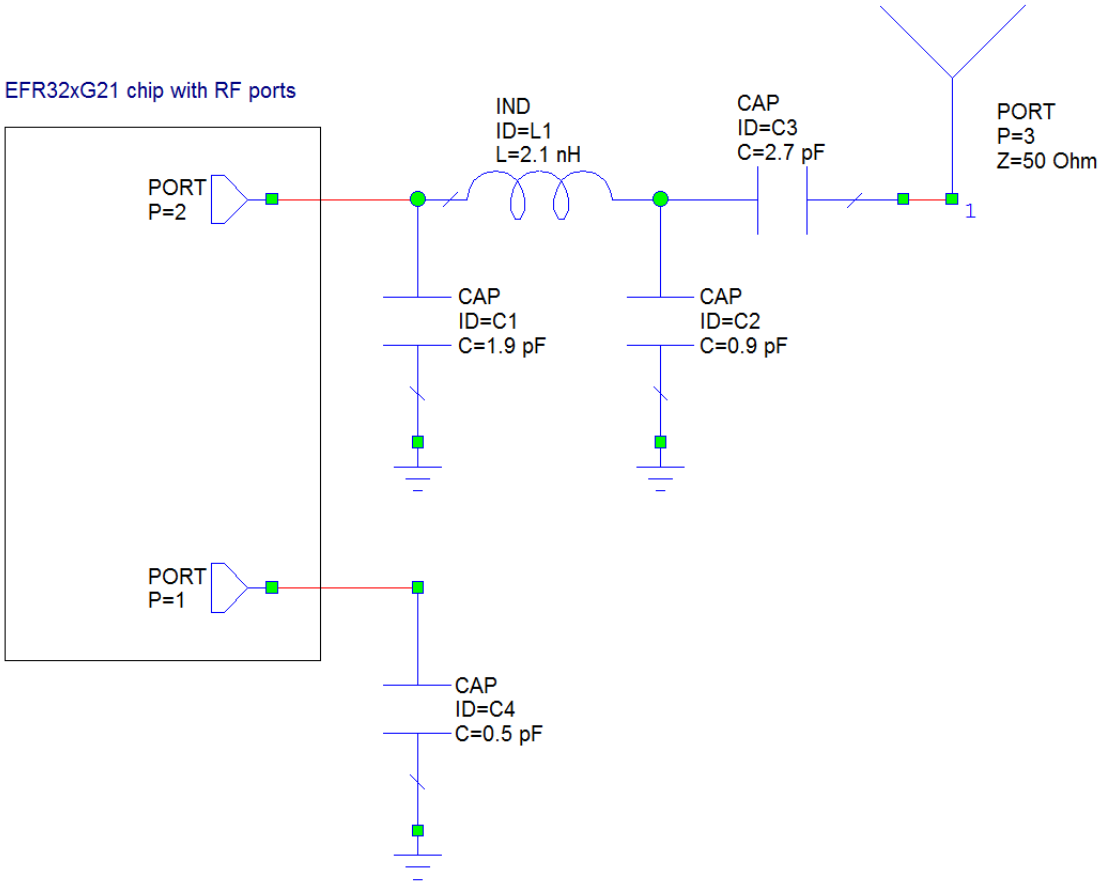


Figure 5.3. Combined Matching Network Schematic for both 0 and +10 dBm PA

Use the matching network shown above when the maximum transmitting power requirement is +10 dBm (TX power ≤ +10 dBm). Use 0 dBm PA for the best power efficiency equal or below 0 dBm. Ground the unused RF2G4_IO pin via an (DC-blocking) 0.5 pF capacitor.

Table 5.3. Final SMD Values for the 0/10 dBm PA Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.5 %	GRM0335C1H1R9WA01D	Murata
L1	2.1 nH	± 0.1 nH	LQP03HQ2N1B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata
C3	2.7 pF	± 0.5 %	GRM0335C1H2R7WA01D	Murata
C4	0.5 pF	± 0.05 pF	GRM0335C1HR50WA01D	Murata

5.1.4 Recommended Matching Network for the +20 dBm PA

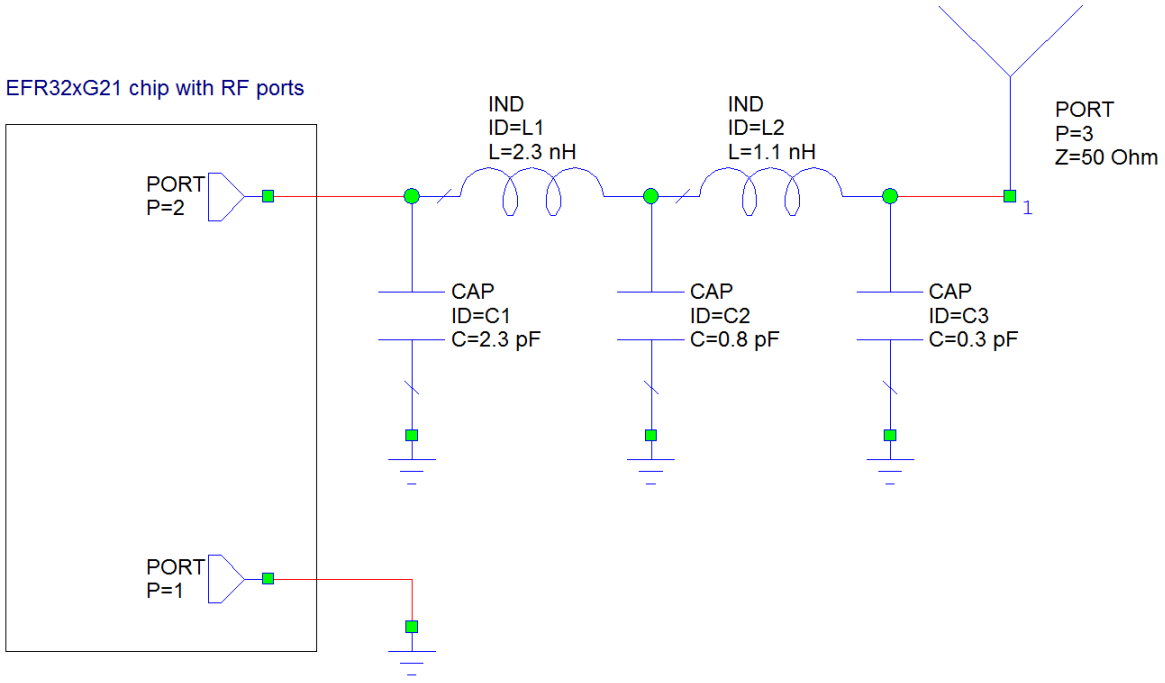


Figure 5.4. Matching Network Schematic for the +20 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +20 dBm (+10 dBm < TX power ≤ +20 dBm), i.e., the application utilizes the +20 dBm PA to achieve the possible highest TX power level available. Due to the optimized power efficiency, the need for 5-element matching network here is mostly driven by the harmonic suppression requirements. The unused RF2G4_IO pin can be grounded directly. Make a short from the pin back to the center exposed pad of the part under the chip.

Table 5.4. Final SMD Values for the +20 dBm PA (5-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01D	Murata
L1	2.3 nH	± 0.1 nH	LQP03HQ2N3B02D	Murata
C2	0.8 pF	± 0.05 pF	GRM0335C1HR80WA01D	Murata
L2	1.1 nH	± 0.05 nH	LQP03HQ1N1W02D	Murata
C3	0.3 pF	± 0.05 pF	GRM0335C1HR30WA01D	Murata

5.1.5 Measurement Results

Table 5.5. Measurement Results for Each Power Level (PA), Avg., Conducted

Match	PA	RX Sensitivity [dBm]	TX Power [dBm]	PA Current [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
0 dBm	0 dBm	-96.4	-0.3	4.3	-60.1	-64.2	-67.9	-60.9
+10 dBm	+10 dBm	-96.5	10.6	29.9	-47.7	-48.8	-48.0	-48.0
0 / 10 dBm	0 dBm	-96.4	-0.4	4.3	-62.1	-68.8	-68.8	-68.8
0 / 10 dBm	+10 dBm	-96.4	10.4	29.9	-62.1	-49.5	-68.1	-45.5
+20 dBm	+20 dBm	-96.3	20.2	178.1	-55.4	-51.5	-52.1	-52.1

RX Sensitivity test conditions: 1Mbps BLE PHY (MSK), BER < 0.1%.

5.2 EFR32xG22 Matching Networks

5.2.1 Recommended Combined Matching Network for Both 0/6 dBm PA on a 4-layer PCB

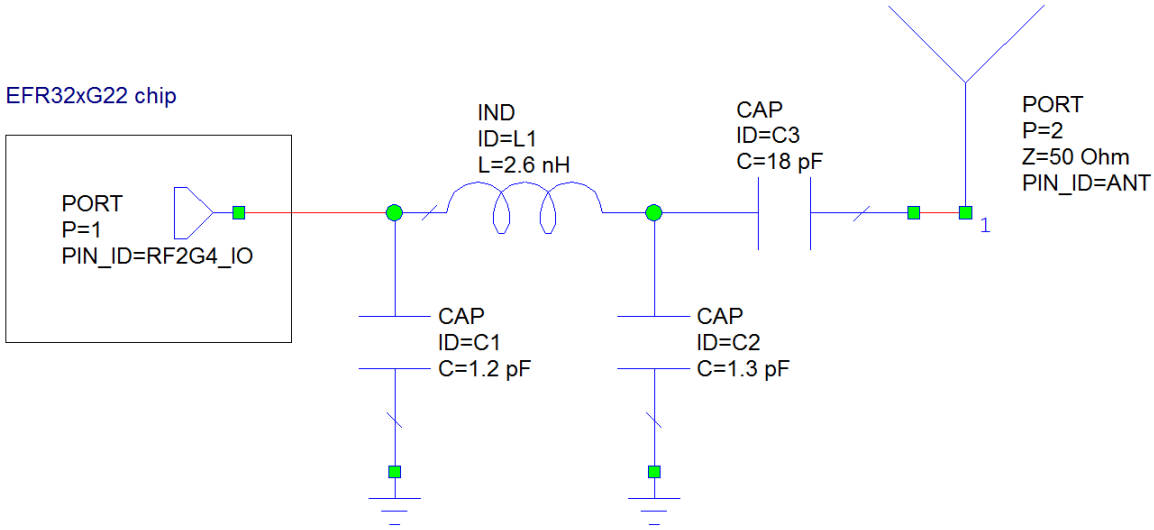


Figure 5.5. Combined Matching Network Schematic for Both 0 and +6 dBm PA on a 4-layer PCB

Use the matching network shown above with EFR32xG22 for any achievable power level. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm, i.e., simultaneously optimized with the 0 and +6 dBm PA as well.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

Furthermore, the EFR32xG22 part is also capable of transmitting at the output power level up to +8 dBm. However, higher than +6 dBm TX power output will result in higher current consumption and harmonic levels, and the +8 dBm TXP is not guaranteed over temperature and process variations. The power code for +8 dBm TXP needs to be maximized in rail using the matching network shown above with the PCB stack-up mentioned. The recommended raw power setting in rail is 127. For different PCB stack-up configurations the match might need tuning, and the slight tuning of the C1 component is the most effective to achieve different max power levels.

Table 5.6. Final SMD Values for the 0/6 dBm PA Match on a 4-layer PCB

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.2 pF	± 0.05 pF	GRM0335C1H1R2WA01D	Murata
L1	2.6 nH	± 0.1 nH	LQP03HQ2N6B02	Murata
C2	1.3 pF	± 0.1 pF	GRM0335C1H1R3BA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.2 Recommended Combined Matching Network for Both 0/6 dBm PA on a 4-layer Thin PCB

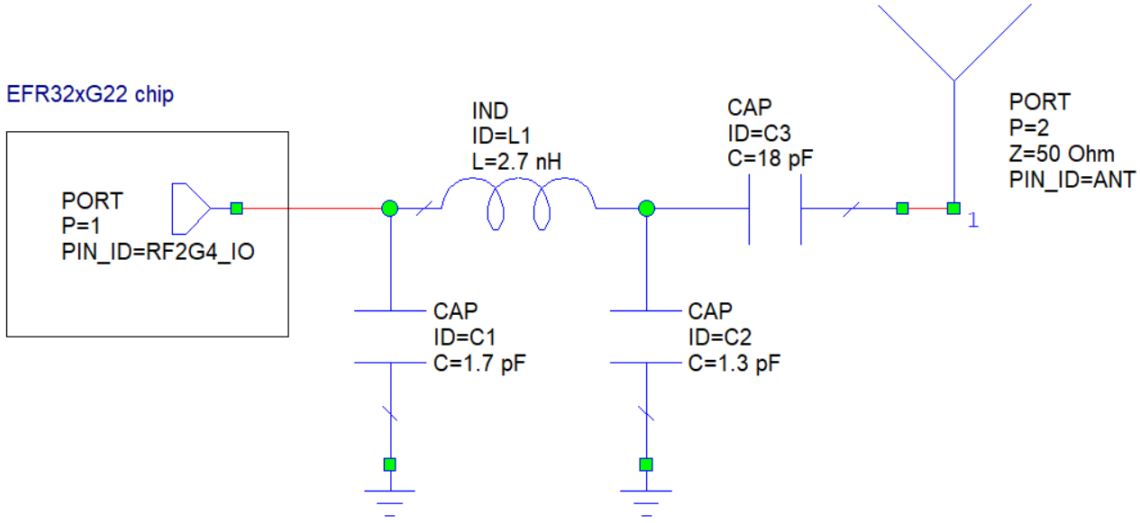


Figure 5.6. Combined Matching Network Schematic for both 0 and +6 dBm PA on a 4-layer Thin PCB

Use the matching network shown above with EFR32xG22 for any achievable power level on a 4- or more-layer PCB where the gap between the top and first inner layer is around only 70 µm. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm. The matching network is simultaneously optimized for both the 0 and +6 dBm PA.

Furthermore, the EFR32xG22 part is also capable of transmitting at the output power level up to +8 dBm. However, higher than +6 dBm TX power output will result in higher current consumption and harmonic levels, and the +8 dBm TXP is not guaranteed over temperature and process variations. The power code for +8 dBm TXP needs to be set close to the maximum in rail using the matching network shown above with the PCB stack-up described above. The recommended raw power setting in rail is 95.

The matching network component values are optimized for a 4-layer PCB with a separation of 70 µm between the top and first inner layer, while the total board thickness is 0.8 mm.

Table 5.7. Final SMD Values for the 0 / 6 dBm PA Match on a 4-layer Thin PCB

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.7 pF	± 0.1 pF	GRM0335C1H1R7BA01D	Murata
L1	2.7 nH	± 0.1 nH	LQP03TN2N7B02D	Murata
C2	1.3 pF	± 0.1 pF	GRM0335C1H1R3BA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.3 Recommended Matching Network for the 0 dBm PA on a 2-layer PCB

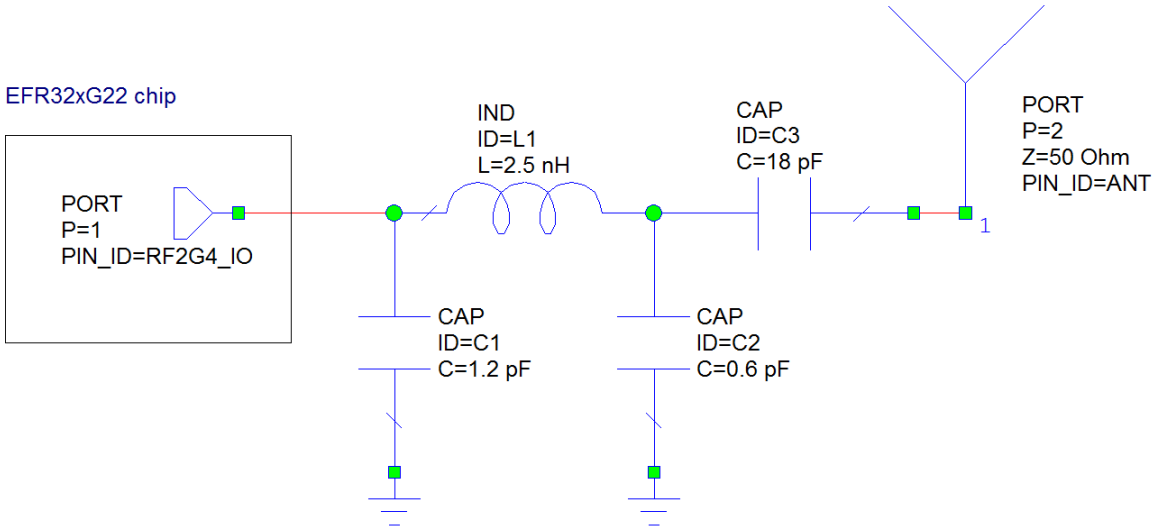


Figure 5.7. Matching Network Schematic for the 0 dBm PA on a 2-layer PCB

Use the matching network shown above with EFR32xG22 with the 0 dBm PA. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA.

The matching network component values are optimized for a 2-layer PCB with a separation of 800 µm between the top and bottom layer. Due to this increased separation (between the matching components and GND reference plane) the matching element values need tuning to keep the low-impedance resonance between the RF port and chip GND pad at the harmonics. Typically, the capacitor values have to be decreased because of the increased via inductance on a thicker PCB, while the series inductor also must be tuned to keep the optimum impedance at the fundamental.

For a low-cost 2-layer PCB design, the PA primarily recommended is the 0 dBm PA, which provides low harmonic content. Also, the suggested board thickness is (max) 0.8 mm.

Table 5.8. Final SMD Values for the 0/6 dBm PA Match on a 2-layer PCB

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.2 pF	± 0.05 pF	GRM0335C1H1R2WA01D	Murata
L1	2.5 nH	± 0.1 nH	LQP03HQ2N5B02	Murata
C2	0.6 pF	± 0.05 pF	GRM0335C1HR60WA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.4 Measurement Results

Table 5.9. Measurement Results for Each Power Level (PA), Avg., Conducted

Match	PA	PCB	RX Sensitivity [dBm] [1]	TX Power [dBm]	Current Cons. [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
0 / 6 dBm	0 dBm	4-layer	-98.4	0.2	4.6	-57.1	-62.7	-70 [2]	-70 [2]
0 / 6 dBm	+6 dBm	4-layer	-98.4	6.0 [3]	8.7	-52.0	-46.1	-66.5	-64.8
0 dBm	0 dBm	2-layer	-98.3	-0.5	4.7	-53.2	-58.5	-70 [2]	-70 [2]
0 / 6 dBm	+6 dBm	4-layer Thin	-99.0	8.2 [4]	10.8	-49.0	-49.3	-70 [2]	-59.1

Note:

1. Test conditions: 1 Mbps BLE PHY (MSK), BER < 0.1%.
2. Under SA noise floor.
3. Tested at +6 dBm power level.
4. Tested at raw power level setting of 95.

6. Appendix 1 PA Optimum Termination Impedance on EFR32xG21

The matching network should present an optimum impedance for the PA at the RF2G4_IO pin for the best RF performance if a 50 Ω termination is applied at the antenna port. The optimum impedance depends on the power level and is also different depending on which internal PA is actively used. The optimum impedances are determined empirically by load-pull methods. The load-pull curves for each PA are shown in the following figures below.

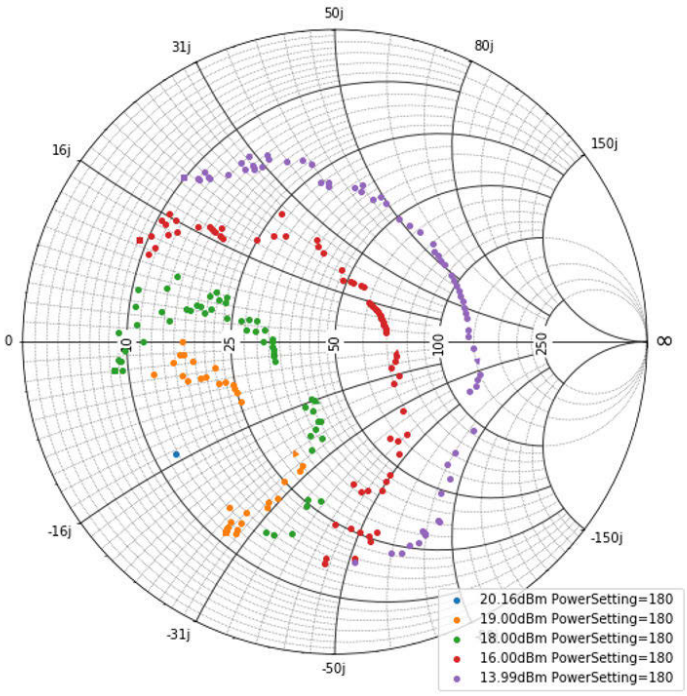


Figure 6.1. Load-pull curves for the 20 dBm PA

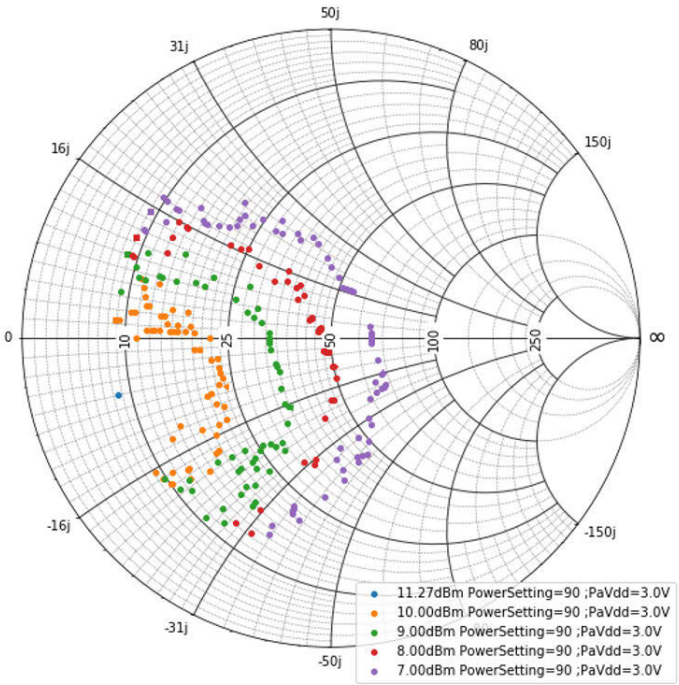


Figure 6.2. Load-pull curves for the 10 dBm PA

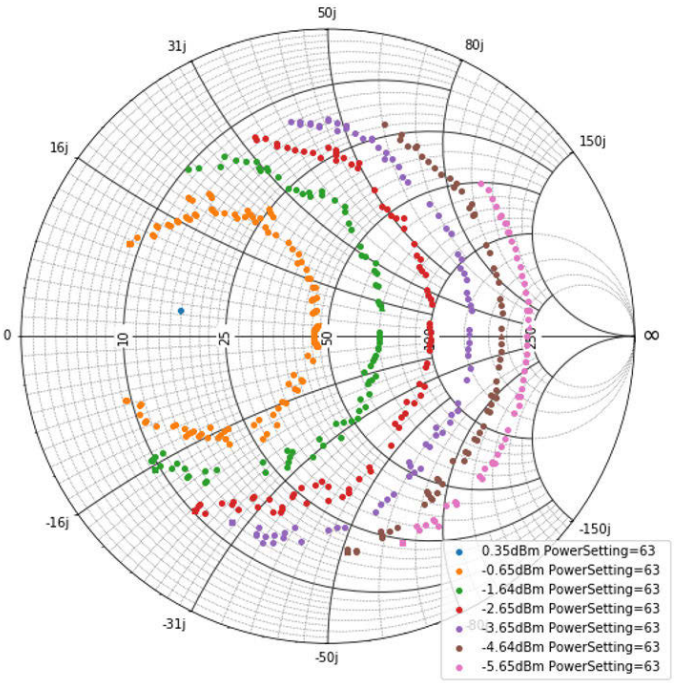


Figure 6.3. Load-pull curves for the 0 dBm PA

7. Revision History

Revision 0.4

May, 2020

- Added matching recommendation for EFR32xG22 on a 4-layer thin PCB with +8 dBm test data

Revision 0.3

March, 2020

- Added content for EFR32xG22 part

Revision 0.2

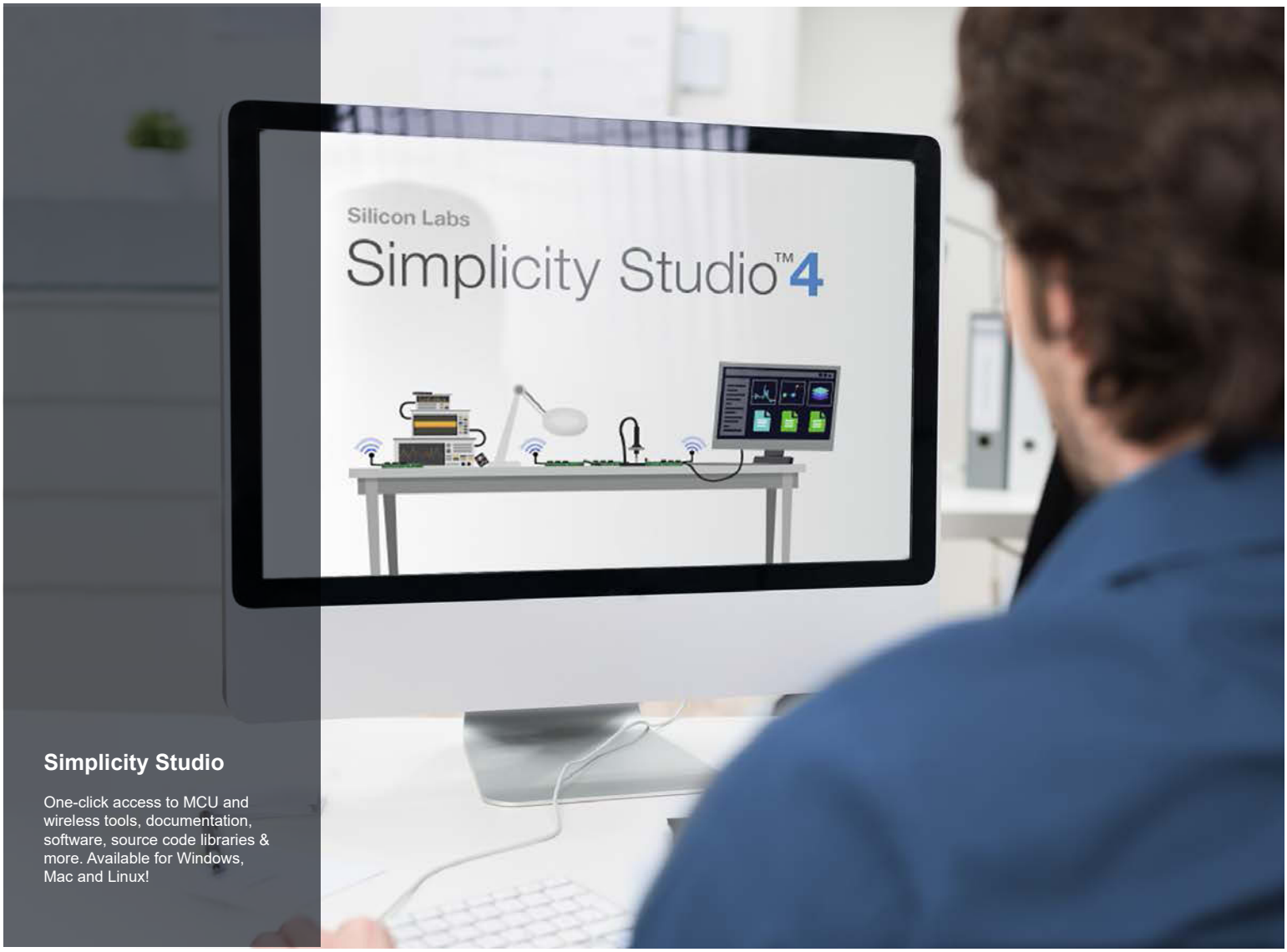
November, 2019

- Highlighting that 0 dBm PA requires to be DC-blocked
- Updating load-pull impedance data and adding load-pull impedance curves for each PA
- Adding discrete 4-element combined 0 / 10 dBm PA match

Revision 0.1

February, 2019

Initial release.



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