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An Adaptable 14-Bit Dual Slope ADC with Wide Input Range

Andriana Voulkidou, Lambros Mountrichas, Stylianos Siskos*

Electronics Laboratory of Physics Department
Aristotle University of Thessaloniki
Thessaloniki, Greece

Abstract

This paper presents the design of an adjustable 14-bit dual slope ADC with wide input range for low frequency applications. The proposed topology can handle both negative and positive input voltage signal with high accuracy. The adaptation in the polarity of the input signal is achieved by exploiting a sign bit in the digital part of the topology. The ADC has been implemented in 0.18μm technology with 3.3V power supply and provides Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) less than 1.6LSBs and 1.3LSBs, respectively. Simulations at transistor level corroborate the validity of the design.

Keywords: Dual slope ADC; adaptable ADC; wide input range;

1. Introduction

In recent years, an area of increasing interest is that of the efficient acquisition of temperature sensor signals. In these applications, the main concern is on accuracy, resolution and power dissipation, therefore proper integration of low noise and high accuracy in analog and digital component is required [1]. Dual slope ADC are well known for their excellent noise rejection, mismatches immunity and lower circuit complexities [2]. Given the strict cost limitations imposed by the sensor market and the increasingly

* Corresponding author. Tel.: +302310998056; fax: +302310998018.
E-mail address: siskos@physics.auth.gr.

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demand for high resolution performance, by including auto-zeroing techniques in these systems the advantages of this ADC are made available to a large range of applications.

In this work, a high resolution dual slope ADC, which can handle input signal voltages as small as 100μV and aimed to be used in the signal processing chain of a MEMS based temperature sensing system, is implemented and verified using post-layout simulations in the Cadence framework. In the proposed architecture, the great conversion accuracy is achieved by using autozero technique. The rest of the paper is organized as follows. In section 2, a description of architecture-level design of the converter is given. Section 3 presents the transistor level simulations validating the approach. Section 4 concludes the paper by summarizing the results and the total performance of the proposed ADC.

2. A/D Architecture

The architecture of the proposed ADC is depicted in Fig. 1. The main buildings blocks in the proposed dual slope integrating ADC are: voltage integrators, a comparator, an N+1 counter, an N register and control logic based on a finite state machine. The integrator utilizing a low noise amplifier for integration of signals followed by a comparator consist the analog part of the converter. In this design the input signal V_{in} lies in the range from *0* to *Vref* volts and it is centered around *Vref/2=1.65V*. Thus, it can be expressed as V_{in} = (*Vref/2*)± *vin* resulting in a large range of input signal. The ADC operation is controlled by the digital block. After the release of the reset signal (RS) the ADC cycles through three phases: Auto-zero, Integration and Deintegration.

In the Auto-zero phase, the integrator and the comparator are connected in unity gain configuration and the offset is stored in the auto-zero capacitor, C_{AZ}, during the first 100 cycles of the counter. Then switch *Sw2*, *Sw1* open and *Sw3* closes allowing the integrator to integrate V_{in} for a fixed time. Simultaneously, the digital counter starts count again. After $2^{14}T_{CLK}$ cycles, the carry output of the counter toggle the T flip-flop FF1, which in turn opens the switch sw4 and closes the switch sw3. At this instance, the Integration phase ends and the Deintegration phase begins.

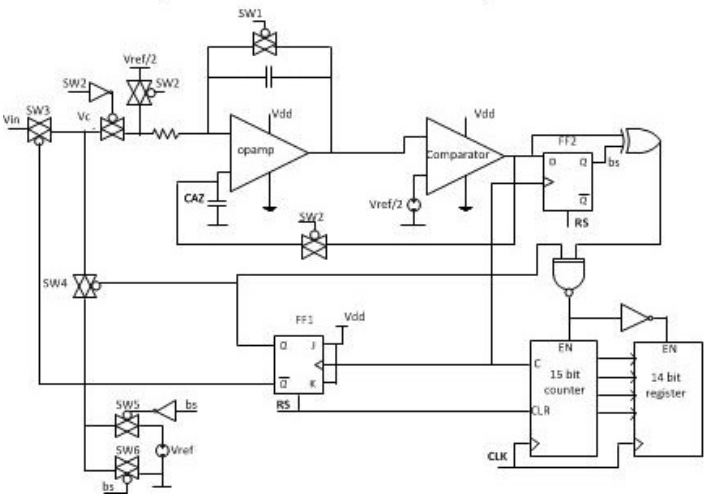


Fig. 1. Architecture of the proposed dual slope ADC

The rising edges of the carry signal also triggers the D flip-flop FF2 and stores the output of the comparator. The Q output of the flip flop constitutes the control bit and determines the suitable reference voltage (Vc) during the Deintegration phase. Depending on the polarity of the input signal, the voltage V_c is set to ground or $V_{ref}=3.3V$ through the switches sw6 and sw5, respectively. The time the Deintegration phase begins, the counter value is set to zero and the counting process starts over again. When the output of the integrator crosses the comparator threshold $V_{ref}/2 = 1.65V$, the counter stops, stores its output in register and signals the end of the conversion.

3. Simulation Results

The integrator and comparator's basic building block is a low power, two stage opamp. The primary sources of error in this type of ADC is the finite gain and settling errors in the opamp [3], thus a 72db gain opamp with small settling time is designed to minimize the errors. As the proposed architecture targets a high resolution ADC, the charge injection of the switches should be less than the one LSB. This is accomplished by using the bridge NMOS switch and by connecting dummy transistors at the CMOS switch output [4]. The digital part of the A/D converter was written in VHDL and was synthesized and P&R with Cadence tools. It incorporates an SPI compatible interface with the ability to subtract a user specified offset value. When the conversion is finished, the LSB of the output word is sent to the output port, and at every falling edge of the SPI clock the next bit is sent to the output. After 16 SPI clock pulses the input data is ready for reading and a new conversation can take place. The layout of the digital control logic is occupies an area of 0.02mm^2.

Mixed-signal analysis has been performed to verify the operation of the proposed ADC. In particular, the circuit implementation of the presented ADC was simulated in AMS simulator using the target technology. Fig. 2 depicts the waveform of the integrator's output for $vin<V_{ref}/2$. The blue line represents the integrator's output and the red one the input V_{in}. The counter clock has been set at 32MHz.

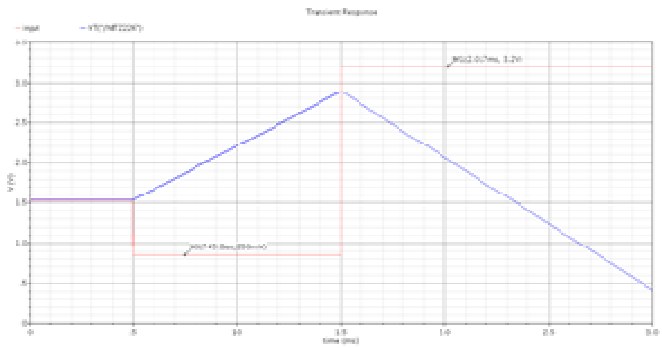
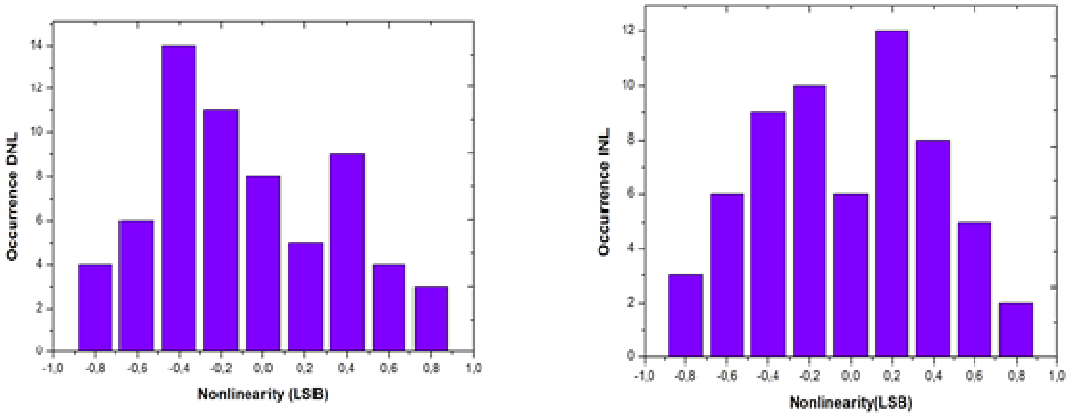


Fig. 2. ADC operation with negative input

The INL and DNL of the overall ADC were also estimated around each transition point and the zero crossing. Simulations ensure high yield across all conditions and provide information about the INL and DNL of the overall ADC At the worst corner, 60 statistical runs are simulated and provide a mismatch induced INL of ±1.6 LSBs (Fig 3.a) and DNL of ±1.3 LSBs (Fig 3.b).



(a) (b)

Fig. 3. (a) Simulated DNL of ADC; (b) Simulated INL of ADC

4. Conclusions

In this paper, an adaptable ADC using 0.18μm technology for low frequency signals has been presented. The proposed A/D converter targets a resolution of 14 bits and operates well in a wide range of input signals. It is highly linear while requires a longer conversion time due to the duration of the counting process at each conversion. The accuracy of the design also based on the applied offset correction technique which eliminates the problems related to the input offset voltages of the opamp and the speed of the comparator. The specifications of the presented ADC meet the bandwidth and precision requirements of temperatures sensors used in a large number of applications ranging from healthcare to environmental monitoring.

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