POWER SEMICONDUCTOR SWITCHING LOSSES EXPERIMENTAL CHARACTERIZATION SYSTEM

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Abstract - **With the current quest for ever more efficient, smaller and better power converters, the role of the power semiconductors becomes very important. Increasing switching frequencies seems key to the development of this area. This is based on the steady development of turn-off switching devices, in which switching losses is perhaps the most important figure in the mentioned context. Thus, the accurate characterization of such losses leads to optimized converter designs. This work presents the practical development of a flexible test system that aims in the reduction of lab test time to perform switching losses measurements.**

Keywords – **The author shall provide a maximum of 6 keywords (in alphabetical order) to help identify the major topics of the paper.**

I. INTRODUCTION

The late technological advances in power semiconductor technology deliver increasingly faster devices, with higher blocking voltage and current-carrying capabilities. These innovations and improvements arise in order to meet emerging technologies trends and the necessities of modern electronics application segments, such as in industrial, commercial, residential and aerospace applications.

However, the non-ideal behavior of the power semiconductor devices generate losses during their current conduction and switching intervals. Since power semiconductor are the core components for static power converters, the precise knowledge about each relevant characteristic of this elements are in close relation to the achievable efficiency, power density and reliability of a converter as a whole. Furthermore, the losses characterization gives important information subsidy to define cooling strategies and switching frequency. Thus, having great impact in the costs of a power converter.

In accordance to the purpose and required accuracy, different models can be used for simulation and design oriented calculations involving semiconductors. For the static behavior, i.e. current conduction characterization, simplified models for the semiconductor are typically used. These models incorporate mathematical expression or circuit models with dc voltage sources and/or resistors [1, 2] and are based on reliable commercially available datasheets. For the dynamic behavior, i.e. voltage and current state transitions that ultimately define the switching losses, the energy lost is often modeled by complex device characterization based on datasheet information [3] or by geometric approximations [2]. The two methods are simple and the necessary data are available in the manufacturers catalogs. However, such datasheet based models are produced on a given test setup and, therefore, their accuracy for an application is good if the semiconductor of interest is used under similar layout, operating temperature and gate driver configuration. Alternatively, numerical simulation of electronic circuits have embedded component physically based models with good accuracy. However, they present some disadvantages such as high cost, difficulty to represent the layout related impedances. The latter has a great relevance with the switching losses behavior. Furthermore, the models for the latest semiconductor devices typically take time to be available as is the case now for modern SiC power transistors. As the data available in catalogs for the modeling of conduction losses are typically reliable, this work focuses on the experimental characterization of switching losses behavior.

More accurate method for obtaining information from the energy involved in switching have been proposed in the literature [4]. They are based on measurement of the energy involved in each switching event. This method lead to data collection with great precision, since the relevant aspects of the process, such as the impedance of the layout and the operating temperature are considered during the tests. The information obtained from the tests can then be processed and used in simulations [4, 5], as well as directly in the converter design, which enables the pre-evaluation of aspects such as efficiency, cost and power density optimization of the structure. In contrast, the disadvantage of this procedure is requiring an appropriate system for testing and processing of data.

In this context, this work presents the study and implementation of a lab platform for the analysis of switching losses in power semiconductors, which allows tests in a semi-automated and temperature controlled way. Section II presents a brief review of the switching losses modeling method. In section III are exposed aspects of design and implementation of the implemented system. Experimental results obtained from practical modern semiconductor devices testing are presented in section IV, conducted with the proposed test platform. Finally, conclusions about the test platform development and critical issues are given.

II. SWITCHING LOSS CHARACTERIZATION METHOD

Several studies in the literature [4–6] used experiments on semiconductors to determine the static and dynamic behavior of these devices. This work uses the approach presented

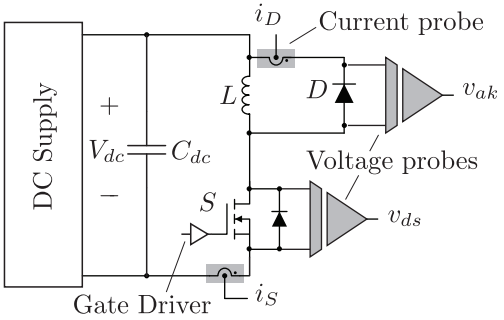

Fig. 1. Test circuit and measurements.

in [4]. As mentioned, the static characteristics of semiconductors are typically accurately presented in manufacturers catalogs, for different temperature values and thus are not further discussed. The main goal of this work is to obtain parameters that describe the dynamic characteristics for a given set of power semiconductors. To this end, the circuit shown in Fig. 1 is considered. The semiconductor set is composed of a controlled switch S and a diode D. This test setup allows to very well represent the switching process involved in a variety of power converters, and will be used here to illustrate the method. However, the developed test platform is able to test a semiconductor set with up to four controlled devices. It is noteworthy that, although the controlled switch circuit shown in Fig. 1 is a MOSFET, the procedure is valid for other technologies transistors such as IGBTs, BJTs and others. The amount of lost energy during turn-on and turn-off transitions of the transistor are extracted through current and voltage probes connected to all semiconductor devices that take part in the commutation process. These probes must supply information to a high bandwidth data acquisition system or oscilloscope. Test runs are conducted under controlled junction temperature, up to the desired blocking voltage and switched current values. Several tests for a given test condition are advisable to reduce stochastic errors. Switching energy loss curves are obtained and can be approximated through polynomial equations that express the total energy involved in switching as a function of the switched current, temperature and blocking voltage.

A. Test Procedure

The devices of the circuit shown in Fig. 1 are properly fixed to a preheated base, under controlled temperature and with a thermal capacity that is sufficiently large for the semiconductor junction temperature not to change during a complete test run. It is also considered that the supply voltage value V_{dc}, which is the blocking voltage, is constant during a test.

Switch S is initially blocked and currents i_D and i_S are null. A finite sequence of command pulse signals, with frequency f_s and appropriate duty cycle δ, is applied to switch S. The command sequence applies $j = 1..N$ pulses with corresponding duty cycle δ_j. The values of f_s and δ ensure that the total current at the end of the test is not destructive to any of the devices. Thus, the restriction

$$\frac{V_{dc}}{Lf_s}\sum_{j=1}^{N}\delta_j \leq I_{\max} \tag{1}$$

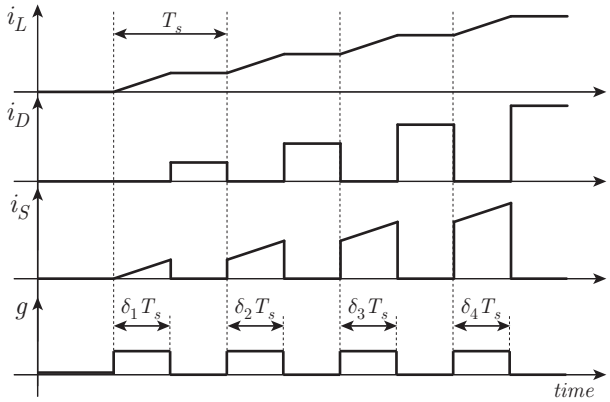

Fig. 2. Theoretical waveforms during the switching losses measurement procedure.

must be respected, so that during the tests the maximum current through any of the semiconductors is not larger than their capacity. It is worth noting that the employed inductor should not enter its core saturation region. Therefore, current $I_{\max}$ in restriction (1) must also consider the maximum non-saturation current for the inductor. Another important aspect is the the magnetic element must be constructed so that the capacitances between the windings are minimal, so as not to influence the results. Another option is to include any capacitances that will be present in the final power converter layout.

During the time instants that the switch is activated, the inductor current linearly increases, while during the remaining time $(1-\delta_j)/f_s$ it circulates through the freewheeling diode D. The Fig. 2 illustrates the theoretical waveforms for this method.

The data obtained from the measurement of currents i_D and i_D, and the voltages v_{ak} and v_{ds} are then processed by the data acquisition system (oscilloscope) and processed in a personal computer. The accuracy of the results is a direct function of the accuracy of the transducers and measurement equipment. In this work, measurements are acquired with a high bandwidth oscilloscope and low capacitance voltage non-differential probes are employed. The current measurements are consequently more complex, since the use of conventional probes imply changes in the layout due to its dimensions, a fact which is not desired for the reasons mentioned. Thus, currents measurement are made using Rogowsky coils or low inductance current transformers, which allow for the direct measurement on the terminal of the devices. The time delays between the transducers must be compensated (deskew) on an oscilloscope or during the data processing stage. Likewise, offset voltages on both measures should also be compensated.

The instantaneous power p_S on the transistor and on the diode p_D are determined by

$$p_S = v_{ds} i_S \tag{2}$$

and

$$p_D = v_{ak} i_D. \tag{3}$$

Each switching event, turn-on or -off, are readily identified on the power stage signals, as shown in Fig. 3. The energy lost in each commutation, bounded by the time instants t_k and t_{k+1}

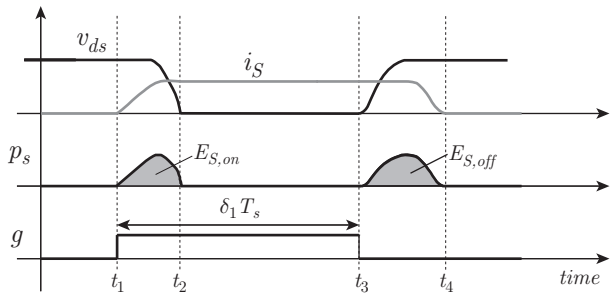

Fig. 3. Time behavior of exemplary theoretical waveforms for the computation of switching losses.

corresponds to the power area in this period. For the waveforms exemplarily shown Fig. 3 the energy lost during turn-on ($E_{S,on}$) and turn-off ($E_{S,off}$) for the transistor are given, respectively, by:

$$E_{S,on} = \int_{t1}^{t2} p_s \, dt = \int_{t1}^{t2} v_{ds} i_S \, dt \tag{4}$$

and

$$E_{S,off} = \int_{t3}^{t4} p_s \, dt = \int_{t3}^{t4} v_{ds} i_S \, dt. \tag{5}$$

III. TEST SYSTEM DESCRIPTION

A heat source is required to drive the power semiconductors to a specified operating temperature. The proposed system consists of a rectangular piece of aluminum without fins, where the switches are attached during testing. This body is heated to a given defined temperature T_{set}, currently up to 160°C from 25°C, through a power resistor attached to one of its surfaces. This resistor is fed from a Buck converter. A Proportional-Integral (PI) controller is programed in the Digital signal Controller (DSC) TMS320LF2407 to control the temperature. This device was chosen for its high processing speed, which allows the simultaneous use of different Pulse Width Modulation (PWM) channels. Four PWM pulses of same frequency are programmed in this project, where each pulse is applied during four switching periods with the possibility of choosing distinct duty-cycles and pulse position in a period. Fig. 4 illustrates the operation of the proposed system, where the DSC controls the device temperature and after it reaches the desired value (T_{set} it warns the user that the temperature is controlled. It then waits for the user command to generate the PWM pulses sequence. When the command starts, the DSC turns-off the buck converter ($BuckEN = 0$) not to generate any electromagnetic interference during the measurements. The temperature control routine stars again after the pulse sequence is finished and waits for another command. Fig. 5 shows the implemented algorithm. The dimensions of the heated body were chosen in order to fit up to four TO-247 packages.

A. Test System Components

The block diagram of the designed test system is presented in Fig. 6, which presents some important elements of the structure including its temperature sensor, the signal conditioning circuits and the Buck converter with its gate drive circuit. The

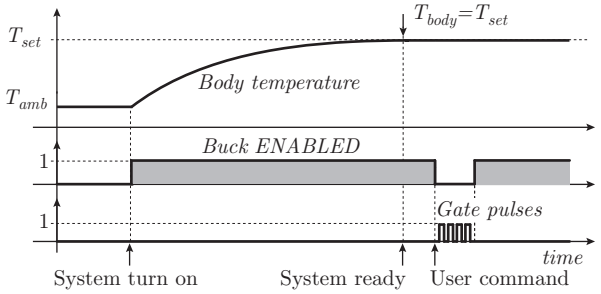

Fig. 4. Typical operation of the built system.

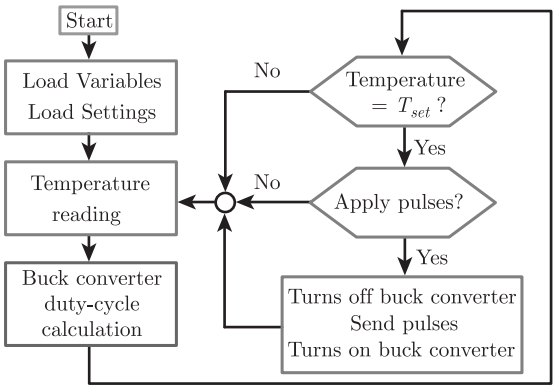

Fig. 5. Software flowchart.

LM35 is used to measure the temperature of the heated aluminum body. This component presents a resolution of 0.5 °C which is sufficient for this application. A TL072 operational amplifier implements the signal conditioning circuit to adjust the voltage levels from the LM35 to the required ones at the DSC in order to use the full range of the DSC. The built main board of the system is presented in Fig. 7.

B. Heated Body Design

The aluminum body to be heated presents the following dimensions: 94 mm, 66 mm and 21 mm as shown in Fig. 8. From these values a thermal model was developed for use both in the control routine as to determine the required rated power of the Buck converter. The thermal capacitance is computed with

$$C_t = mc_{AL}, \tag{6}$$

which is the product of the body mass m by the thermal conductivity of aluminum c_{AL}. This capacitance is given in J/°C. The heat transfer coefficient h must be found in order to determine the thermal resistance. This is given [7] for natural air convection by

$$h = 1,32\sqrt[4]{\frac{\Delta t}{c}}, \tag{7}$$

where Δt is the difference between the operating temperature (T_{set}) and the ambient temperature and c is the length of the body. The thermal resistance, measured in °C/W, is obtained with

$$R_t = \frac{1}{hA_s}, \tag{8}$$

where A_s is the total surface area of the aluminum body. The

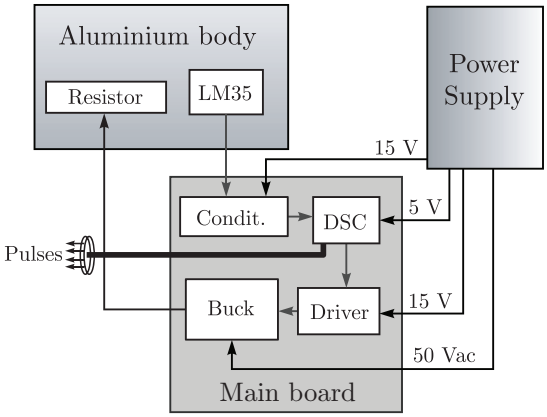

Fig. 6. Test system block diagram showing the heated aluminum body, the power supply, the DSC driving the buck converter to control the LM35 sensed temperature and to generate the programed sequence of pulses.

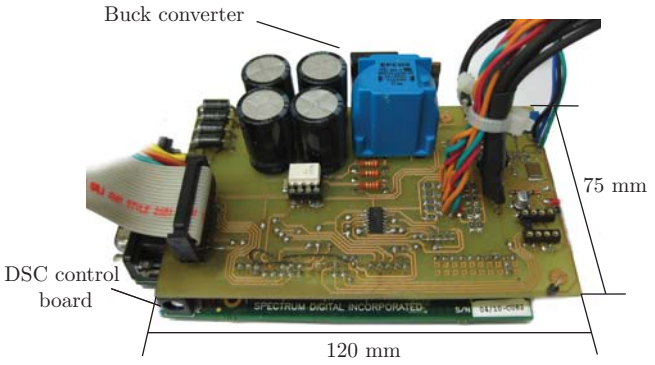

Fig. 7. The main system board.

power required from the Buck converter P to heat the aluminum body to the desired temperature is given by

$$P = \frac{\Delta t}{R_t}. \tag{9}$$

The behavior of the block temperature is illustrated in Fig. 9. These results were obtained applying a power of 50 W to the heating resistor, inside an air conditioned room to maintain the ambient temperature at 25°C. Additionally to the experimentally measured temperature curve, Fig. 9 shows an approximated curve and a third curve with the theoretical values employing the modeled thermal resistance and capacitance given by

$$T(t) = T_i + (T_f - T_i)\left(1 - e^{\frac{-t}{\tau}}\right), \tag{10}$$

where

$$\tau = R_t C_t. \tag{11}$$

For the approximate result, the thermal resistance value R_t was computed with (9), since both the power and the temperature variation are known. The thermal capacitance C_t was then obtained from (11) by computing the time constant τ from the experiment. The difference between the theoretical and experimental results are due to the fact that the heat transfer coefficient h depends on external conditions such as temperature and air flow in the environment where the tests are made.

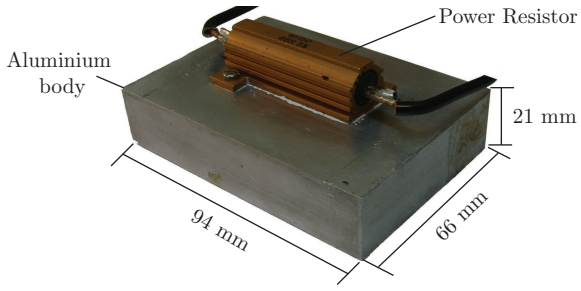

Fig. 8. Heated aluminum body attached to its heating element (power resistor).

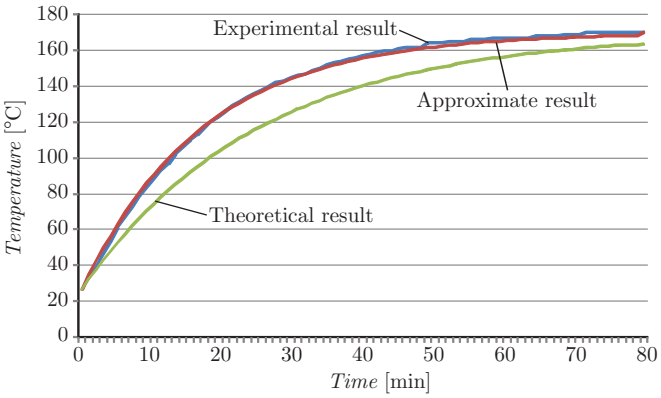

Fig. 9. Heated body temperature behavior.

C. PWM Pulse Generation

The chosen DSC allows for the use of up to five independent PWM channels. Four of these channels are employed in the generation of the four independent switching pulses included in the programable sequence. For increasing the versatility of the prototype, a user interface was developed. It provides the possibility to adjust the duty cycles and the switching frequency of the gate pulses for a given test. The four output signals were buffered to obtain higher current capacity that is needed to command the gate drivers for the power semiconductors. An embedded power supply is included, which delivers two dc voltage levels, namely: 5 V and 15 V, which can be selected and used according to the needs of the test.

IV. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed system, this section presents data collected during experimental tests realized in the laboratory. The results of these tests were used to model switching losses in different types of semiconductors.

Fig. 11 shows the results for the semiconductor set applied in [8], where CoolMOS MOSFETs SPP24N60C3 (600 V / 160mΩ) and SiC-diodes SDT12S60 (600 V/ 12 A) are employed. Switch current and voltage waveforms obtained during a test pulse sequence show the increasing overvoltage with increasing switched current. Part of the processing power is lost during the switching intervals. Fig. 12 shows the current turn-off transition in detail, where it is seen that the voltage/current overlaping time is very short (≅ 8 ns) and is followed by strong oscilations.

In another experiment, the data shown in Fig. 13 was ac-

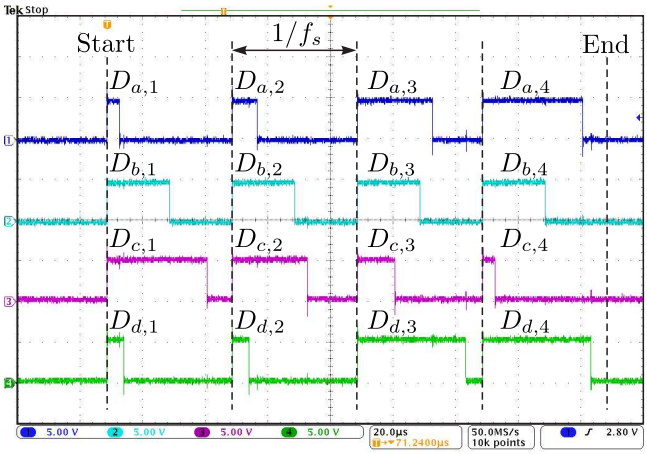

Fig. 10. Exemplary acquisition of the gate driver four pulses sequence generation with a switching frequency $f_s \cong 50$ kHz and variable duty cycles.

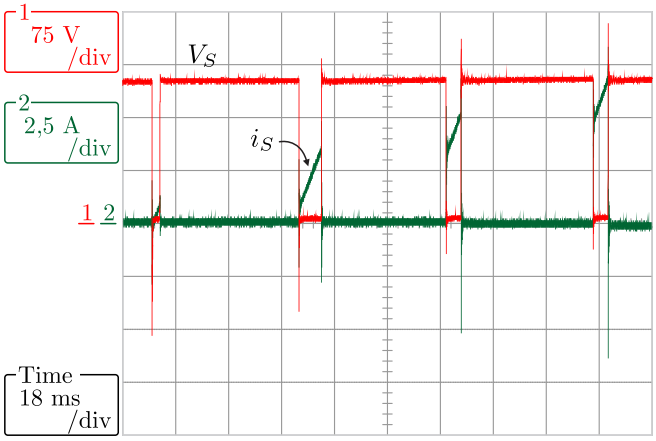

Fig. 11. Test run waveforms employing a semiconductor set composed of a CoolMOS SPP24N60C3 and a SiC diode SDT12S60.

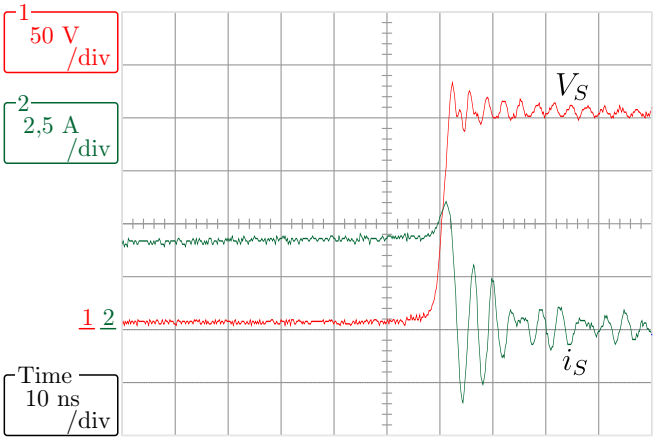

Fig. 12. Detailed turn-off behavior for a test employing a semiconductor set composed of a CoolMOS SPP24N60C3 and a SiC diode SDT12S60.

quired for modern 1200 V Silicon Carbide (SiC) JFETs commercially available from [9] with part number SJEP120R100 (1200 V / 100 mΩ), here referred to as SiC-JFET. The diodes

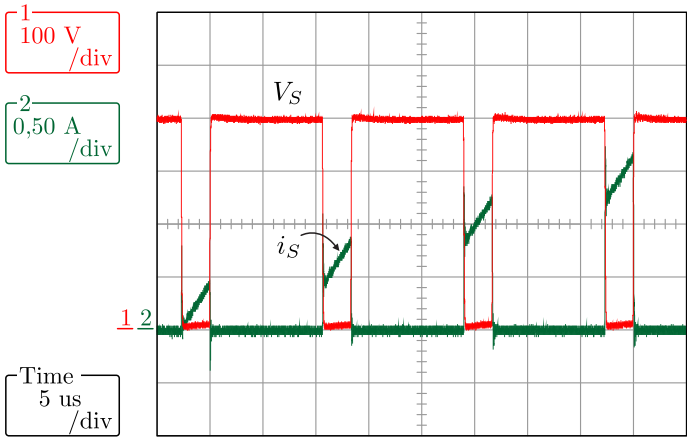

Fig. 13. Test run waveforms employing a semiconductor set composed of a SiC JFET SJEP120R100 and a SiC diode SDP30S120.

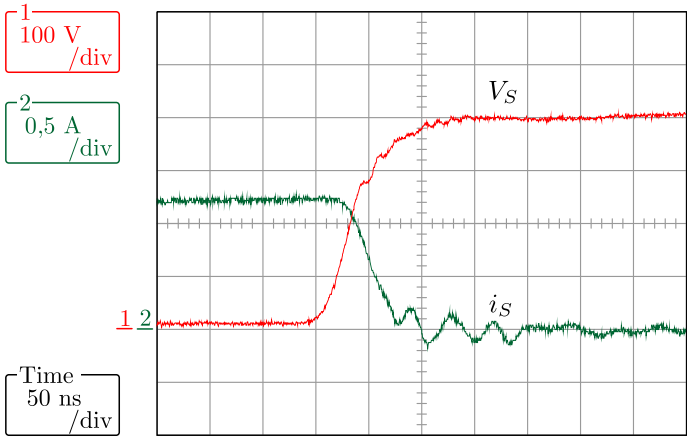

Fig. 14. Detailed turn-off behavior for a test employing a semiconductor set composed of a SiC JFET SJEP120R100 and a SiC diode SDP30S120.

used in the test are also from [9] with part number SDP30S120 (1200 V/30 A), here referred to as SiC-diode. These exemplary results were applied in [10]. Fig. 14 shows a detail of the turn-off commutation, where the SiC-JFET blocks 400 V in approximately 85 ns. More experimental results will be included in the final version of this work along with the instantaneous power curves.

Computer softwares, such as MATLAB, are applied to post-process the data and estimate the energy involved during each switching action interval. From the acquisitions made during the testing of a given semiconductor set, the values of energy for each situation can be calculated and presented graphically.

V. CONCLUSIONS

This work presented the development of a power semiconductor switching losses test system. The capabilities of this system include the temperature control of the semiconductors under test and the generation of a pulse test sequence with up to four PWM channels. Each PWM channel can have its duty-cycle independently programmed. The proposed test system

was successfully used in the characterization of modern power semiconductor devices, including SiC JFETs and CoolMOS MOSFETs employed in research efforts to drive high power high switching frequency power converters. The benefits of such a system are the reduction of experimental test time and the experimental characterization of switching losses. These benefits are crucial for modern power electronics converter research and development efforts including new semiconductor devices.

ACKNOWLEDGEMENT

The authors would like to thank CNPq for the financial support.

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