HAILO
Empowering Intelligence

Hailo-8L™

Datasheet

Revision 1.4
December 2023

Part Numbers

Industrial: HNC1LBI11BH

See Table 1 for ordering information.

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Documentation Control

History Table

Revision	Date	Description
0.1	July 2022	Initial release
1.0	November 2022	Removal of commercial part details
1.1	December 2022	Section 2.2-U5 removed from GND Replaced V3 with A19 Section 2.2 U5 and J3 added to RESERVED
1.2	August 2023	Updated voltages in Section 4.2 Recommended Operating Conditions Revised Section 4.3 Power-up Sequence New sequence description, drawing and timing requirements table
1.3	October 2023	Updated system modes and usage scenarios
1.4	December 2023	Section 4.4.1 updated VDDIO to 300 mA, Max VDD_Core to 7.2A and Max VDD_Top to 1A Typo correction on pin names PCIE_REFCLK, FUSE_VQPS and CSI_TX _CLK

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1. Overview

1.1. Introduction

This datasheet provides a technical description of the Hailo-8L™ System on a Chip (SoC), an Artificial Intelligence (AI) processor. The Hailo-8L shares all of its features and innovative architecture with the Hailo-8, however features lower performance grade, specifically tailored for applications which emphasize cost and power over performance, yet requires NN engine with incomparable compute power at the relevant operating point with respect to cost and TOPS/W efficiency.

This document must be read in conjunction with the Hardware Integration Guide to ensure proper design.

1.2. General Description

The Hailo-8L SoC provides groundbreaking efficiency for neural network (NN) deployment based on unique design elements within the Hailo-8L NN Core, including:

- **Distributed memory fabric with purpose-built pipeline** elements that allow very low-power memory access during NN processing
- **Extremely efficient computational** elements that can be applied variably, as needed
- **Dataflow-oriented interconnect** that adapts to the structure of the NN and allows high resource utilization

The NN Core can be coupled with multiple industry-leading interfaces and subsystems to deliver high efficiency and high compute, leading-edge AI solutions.

Hailo-8L enables a broad range of applications by integrating an optimal mix of performance, low power and sophisticated video analytics processing.

1.3. Features

- MCU
  - 2 ARM Cortex-M4 @ 200 MHz
  - 640 KB internal SRAM (ECC protected)
  - FPU, MPU
- Neural Processing Unit (NN-Core)
  - Up to 13 [TOPS]
  - High-performance, Hailo NN multi-stream, multi-network core
  - Hardware offload engines for Deep Neural Networks (DNN) with pre and post processing:
    - Tensor manipulation (crop & resize, ROI pooling, reshape)
    - Non Maximum Suppression (NMS)
    - Bi-linear transformation
    - Softmax
- 4-lane PCI Express Gen3 endpoint with integrated PHY
- MIPI CSI 1.3, 2 RX and TX interfaces
  - Integrated 4-lane DPHY
  - 2.5 Gbps per lane
  - TX interfaces can be used as DSI TX
- Camera Parallel LVCMOS Interface: up to 24 bits wide @ 100MHz
- 1Gbps Ethernet controller, IEEE1588 compliant, 100/1000 Mbps
- 4 UARTs
- 4 I2C interfaces
- 4 timers
- 2 x multi-channel programmable DMA engines
- 32 configurable GPIOs with interrupt support
- Quad SPI Flash Interface
  - Up to 50MHz clock supported
  - Includes Flash cache hardware

- Vision Subsystem
  - H.264 encoder
  - Image Signal Processor (ISP) for a single sensor
  - Input formats: RAW8, RAW10, RAW12, RAW14
  - Output formats: RGB888, YUV422
  - Maximum input resolution: 4096X4096 P
  - Throughput: 4k @ 40 FPS, 1080p @ 120 FPS
- Security Features
  - Hardware crypto accelerators
  - Firewall
  - Secure ROM and boot
- Power, reset and clock management
- Voltage monitor
- Temperature monitor
- Package
  - 400-pin HFCBGA
  - 17mm x 17mm, 0.8mm pitch

1.4. Applications

The Hailo-8L SoC enables a broad range of applications, including:

- Smart cities: public safety, intelligent mobility, health monitoring, infrastructure & services management
- Industry 4.0: manufacturing automation, robotic vision, safety & security
- Smart retail: automated store, smart analytics, targeted advertising
- Smart home: lifestyle & entertainment, safety & security
- Drones: sense, avoid and navigate

1.5. Block Diagram

Figure 1 shows the subsystems and functional modules of the Hailo-8L SoC.

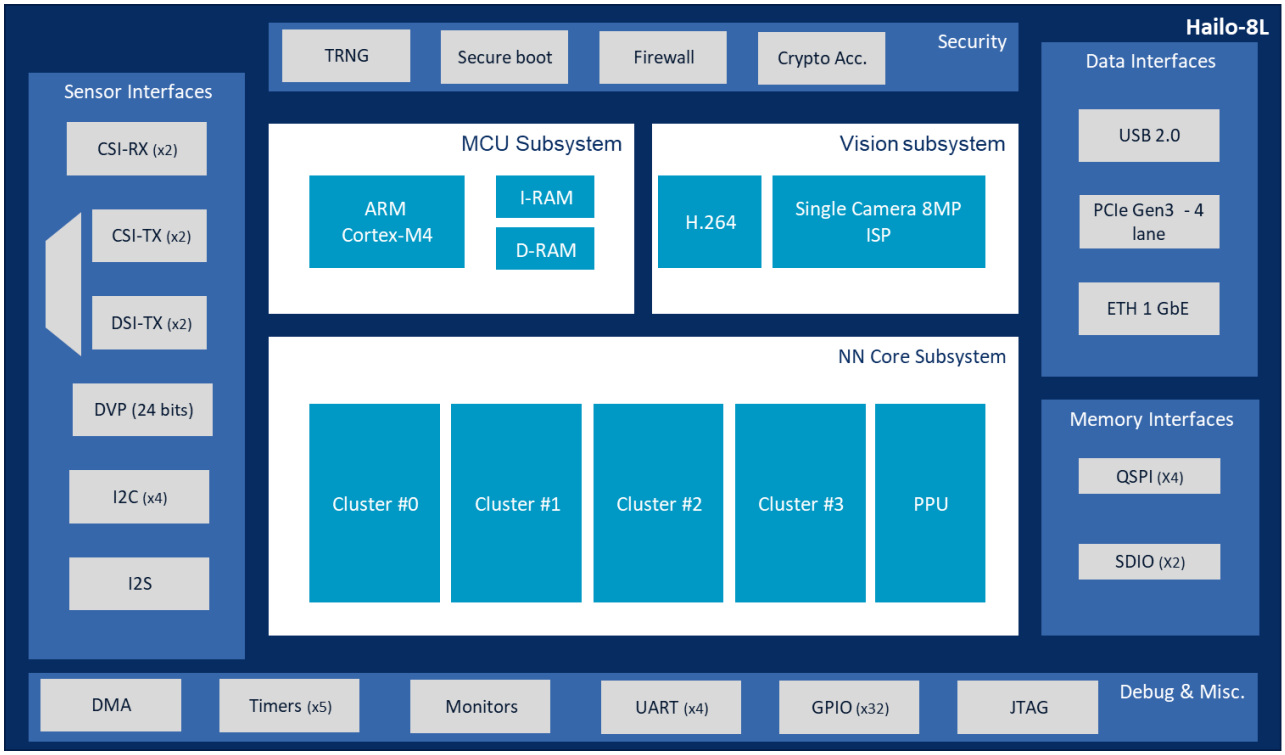


Figure 1: Hailo-8L Block Diagram

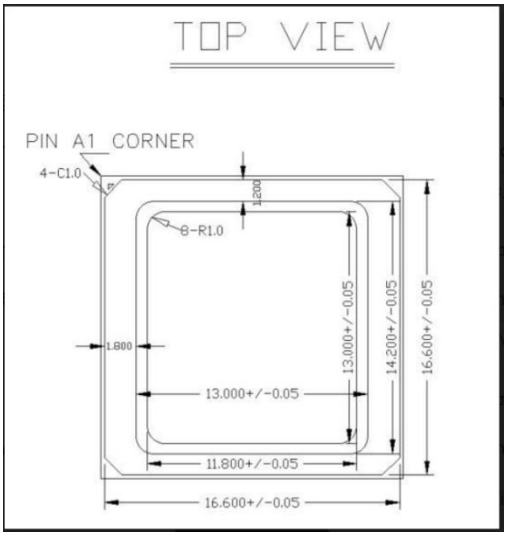
1.6. Ordering Information

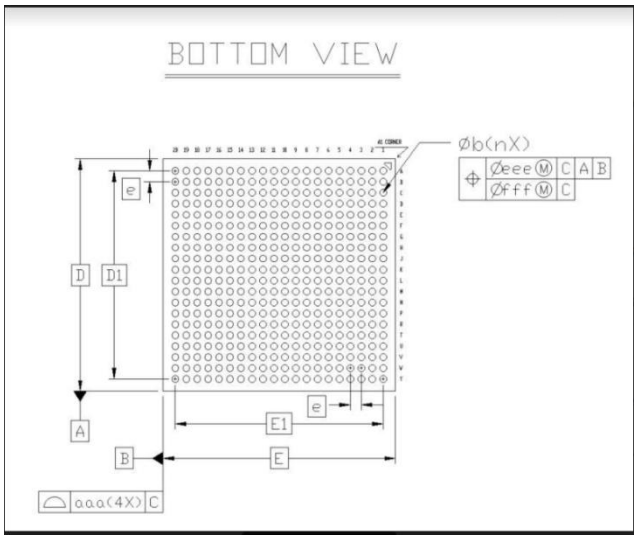
Table 1: Ordering Information

Part Number	Device Grade	Temperature Range
HNC1LBI11BH	Industrial	-40° to 85° C

1.7. Mechanical Details

Figure 2 shows the top, bottom and side views of the 400-pin HFCBGA package including package dimensions.





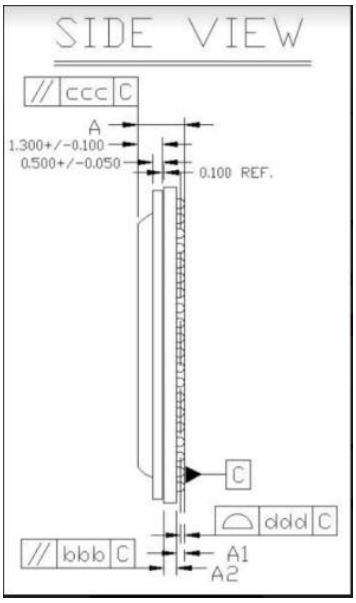


Figure 2: Hailo-8L Package Views

Table 2: Hailo-8L Package Dimensions

Description	Symbol	Common Dimensions		
		Min	Nom	Max
Total thickness	A	2.326	2.476	2.626
Standoff	A1	0.300	-	0.500
Substrate thickness	A2	C676 Ref		
Thickness from substrate surface to die backside	A3	-		
Body size	E	17 BSC		
	D	17 BSC		
Ball diameter		C.500		
Ball width	b	0.400	-	0.600
Ball pitch	e	C.800 BSC		
Ball count	d	400		
Edge ball center to center	E1	15.200 BSC		
	D1	15.200 BSC		
Expose die size	E2	BSC		
	D2	BSC		
Package edge tolerance	aaa	C.200		
Substrate parallelism	bbb	C.250		
Top parallelism	ccc	C.350		
Coplanarity	ddd	C.150		
Ball offset (package)	eee	C.250		
Ball offset (ball)	fff	C.100		

1.8. Glossary

Table 3 shows a list of the abbreviations used in this document.

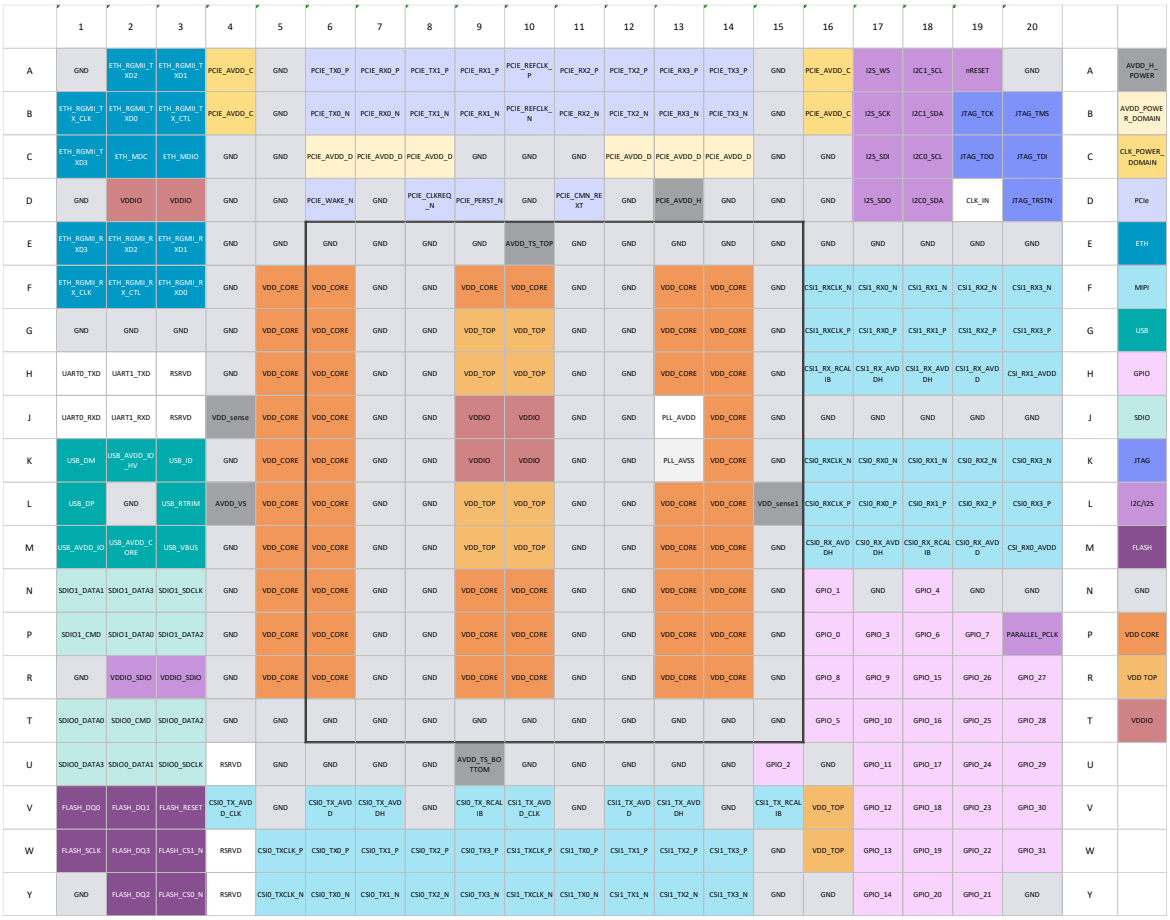
Table 3: Glossary

Abbreviation	Description
BS	Boot strap
CMOS	Complementary Metal-Oxide
CS	Chip Select
CSI	Camera Serial Interface
DMA	Direct Memory Access
DNN	Deep Neural Network
DSI	Display Serial Interface
ECC	Error Correction Code
ETM	Electronic Trace Management
FPU	Floating Point Accelerator Unit
FS	Full Speed
GPIO	General-Purpose Input Output
HS	High Speed
I/O	Input Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
LP	Low Power
MCU	Microcontroller Unit
MIPI	Mobile Industry Processor Interface
MMU	Memory Management Unit
MPU	Memory Protection Unit
NMS	Non-Maximum Suppression

Abbreviation	Description
NN	Neural Network
PCIe	Peripheral Component Interconnect
PHY	Physical Layer
PLL	Phase-Locked Loop
PVT	Process, Voltage, and Temperature
QSPI	Queued Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media-Independent Interface
ROI	Region of Interest
RoT	Root of Trust
RX	Receiver
SRP	Session Request Protocol
SDIO	Secure Digital Input Output
SoC	System on a Chip
TEE	Trusted Execution Environment
TOPS	Tera Operations Per Second
TX	Transmitter
UART	Universal Asynchronous Receiver
USB	Universal Serial Bus
XIP	Execute in Place

2. Pinout Description

2.1. Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	GND	ETH_RGMII_TXD2	ETH_RGMII_TXD1	PCIE_AVDD_C	GND	PCIE_TX0_P	PCIE_RX0_P	PCIE_TX1_P	PCIE_RX1_P	PCIE_REFCLK_P	PCIE_RX2_P	PCIE_TX2_P	PCIE_RX3_P	PCIE_TX3_P	GND	PCIE_AVDD_C	I2S_WS	I2C1_SCL	nRESET	GND	A	AVDD_H_POWER
B	ETH_RGMII_TX_CLK	ETH_RGMII_TXD0	ETH_RGMII_TX_CTL	PCIE_AVDD_C	GND	PCIE_TX0_N	PCIE_RX0_N	PCIE_TX1_N	PCIE_RX1_N	PCIE_REFCLK_N	PCIE_RX2_N	PCIE_TX2_N	PCIE_RX3_N	PCIE_TX3_N	GND	PCIE_AVDD_C	I2S_SCK	I2C1_SDA	JTAG_TCK	JTAG_TMS	B	AVDD_POWER_DOMAIN
C	ETH_RGMII_TXD3	ETH_MDC	ETH_MDIO	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	I2S_SDI	I2C0_SCL	JTAG_TDO	JTAG_TDI	C	CLK_POWER_DOMAIN
D	GND	VDDIO	VDDIO	GND	GND	PCIE_WAKE_N	GND	PCIE_CLKREQ_N	PCIE_PERST_N	GND	PCIE_CMN_REXT	GND	PCIE_AVDD_H	GND	GND	GND	I2S_SDO	I2C0_SDA	CLK_IN	JTAG_TRSTN	D	PCIe
E	ETH_RGMII_RXD3	ETH_RGMII_RXD2	ETH_RGMII_RXD1	GND	GND	GND	GND	GND	GND	AVDD_TS_TOP	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	E	ETH
F	ETH_RGMII_RX_CLK	ETH_RGMII_RX_CTL	ETH_RGMII_RXD0	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_N	CSI1_RX0_N	CSI1_RX1_N	CSI1_RX2_N	CSI1_RX3_N	F	MIPI
G	GND	GND	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_P	CSI1_RX0_P	CSI1_RX1_P	CSI1_RX2_P	CSI1_RX3_P	G	USB
H	UART0_TXD	UART1_TXD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RX_RCAL IB	CSI1_RX_AVDDH	CSI1_RX_AVDDH	CSI1_RX_AVDD	CSI_RX1_AVDD	H	GPIO
J	UART0_RXD	UART1_RXD	RSRVD	VDD_sense	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVDD	VDD_CORE	GND	GND	GND	GND	GND	GND	J	SDIO
K	USB_DM	USB_AVDD_IO_HV	USB_ID	GND	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVSS	VDD_CORE	GND	CSI0_RXCLK_N	CSI0_RX0_N	CSI0_RX1_N	CSI0_RX2_N	CSI0_RX3_N	K	JTAG
L	USB_DP	GND	USB_RTRIM	AVDD_VS	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	VDD_sense1	CSI0_RXCLK_P	CSI0_RX0_P	CSI0_RX1_P	CSI0_RX2_P	CSI0_RX3_P	L	I2C/I2S
M	USB_AVDD_IO	USB_AVDD_CORE	USB_VBUS	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI0_RX_AVDDH	CSI0_RX_AVDDH	CSI0_RX_RCAL IB	CSI0_RX_AVDD	CSI_RX0_AVDD	M	FLASH
N	SDIO1_DATA1	SDIO1_DATA3	SDIO1_SDCLK	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_1	GND	GPIO_4	GND	GND	N	GND
P	SDIO1_CMD	SDIO1_DATA0	SDIO1_DATA2	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_0	GPIO_3	GPIO_6	GPIO_7	PARALLEL_PCLK	P	VDD CORE
R	GND	VDDIO_SDIO	VDDIO_SDIO	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_8	GPIO_9	GPIO_15	GPIO_26	GPIO_27	R	VDD TOP
T	SDIO0_DATA0	SDIO0_CMD	SDIO0_DATA2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GPIO_5	GPIO_10	GPIO_16	GPIO_25	GPIO_28	T	VDDIO
U	SDIO0_DATA3	SDIO0_DATA1	SDIO0_SDCLK	RSRVD	GND	GND	GND	GND	AVDD_TS_BOTTOM	GND	GND	GND	GND	GND	GPIO_2	GND	GPIO_11	GPIO_17	GPIO_24	GPIO_29	U	
V	FLASH_DQ0	FLASH_DQ1	FLASH_RESET	CSI0_TX_AVDD_CLK	GND	CSI0_TX_AVDD	CSI0_TX_AVDDH	GND	CSI0_TX_RCAL IB	CSI1_TX_AVDD_CLK	GND	CSI1_TX_AVDD	CSI1_TX_AVDDH	GND	CSI1_TX_RCAL IB	VDD_TOP	GPIO_12	GPIO_18	GPIO_23	GPIO_30	V	
W	FLASH_SCLK	FLASH_DQ3	FLASH_CS1_N	RSRVD	CSI0_TXCLK_P	CSI0_TX0_P	CSI0_TX1_P	CSI0_TX2_P	CSI0_TX3_P	CSI1_TXCLK_P	CSI1_TX0_P	CSI1_TX1_P	CSI1_TX2_P	CSI1_TX3_P	GND	VDD_TOP	GPIO_13	GPIO_19	GPIO_22	GPIO_31	W	
Y	GND	FLASH_DQ2	FLASH_CS0_N	RSRVD	CSI0_TXCLK_N	CSI0_TX0_N	CSI0_TX1_N	CSI0_TX2_N	CSI0_TX3_N	CSI1_TXCLK_N	CSI1_TX0_N	CSI1_TX1_N	CSI1_TX2_N	CSI1_TX3_N	GND	GND	GPIO_14	GPIO_20	GPIO_21	GND	Y	

Figure 3 shows the Hailo-8L top view of the ball diagram.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	GND	ETH_RGMII_TXD2	ETH_RGMII_TXD1	PCIE_AVDD_C	GND	PCIE_TX0_P	PCIE_RX0_P	PCIE_TX1_P	PCIE_RX1_P	PCIE_REFCLK_P	PCIE_RX2_P	PCIE_TX2_P	PCIE_RX3_P	PCIE_TX3_P	GND	PCIE_AVDD_C	I2S_WS	I2C1_SCL	nRESET	GND	A	AVDD_H_POWER
B	ETH_RGMII_TX_CLK	ETH_RGMII_TXD0	ETH_RGMII_TX_CTL	PCIE_AVDD_C	GND	PCIE_TX0_N	PCIE_RX0_N	PCIE_TX1_N	PCIE_RX1_N	PCIE_REFCLK_N	PCIE_RX2_N	PCIE_TX2_N	PCIE_RX3_N	PCIE_TX3_N	GND	PCIE_AVDD_C	I2S_SCK	I2C1_SDA	JTAG_TCK	JTAG_TMS	B	AVDD_POWER_DOMAIN
C	ETH_RGMII_TXD3	ETH_MDC	ETH_MDIO	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	I2S_SDI	I2C0_SCL	JTAG_TDO	JTAG_TDI	C	CLK_POWER_DOMAIN
D	GND	VDDIO	VDDIO	GND	GND	PCIE_WAKE_N	GND	PCIE_CLKREQ_N	PCIE_PERST_N	GND	PCIE_CMN_REXT	GND	PCIE_AVDD_H	GND	GND	GND	I2S_SDO	I2C0_SDA	CLK_IN	JTAG_TRSTN	D	PCIe
E	ETH_RGMII_RXD3	ETH_RGMII_RXD2	ETH_RGMII_RXD1	GND	GND	GND	GND	GND	GND	AVDD_TS_TOP	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	E	ETH
F	ETH_RGMII_RX_CLK	ETH_RGMII_RX_CTL	ETH_RGMII_RXD0	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_N	CSI1_RX0_N	CSI1_RX1_N	CSI1_RX2_N	CSI1_RX3_N	F	MIPI
G	GND	GND	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_P	CSI1_RX0_P	CSI1_RX1_P	CSI1_RX2_P	CSI1_RX3_P	G	USB
H	UART0_TXD	UART1_TXD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RX_RCALIB	CSI1_RX_AVDDH	CSI1_RX_AVDDH	CSI1_RX_AVDD	CSI_RX1_AVDD	H	GPIO
J	UART0_RXD	UART1_RXD	RSRVD	VDD_sense	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVDD	VDD_CORE	GND	GND	GND	GND	GND	GND	J	SDIO
K	USB_DM	USB_AVDD_IO_HV	USB_ID	GND	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVSS	VDD_CORE	GND	CSI0_RXCLK_N	CSI0_RX0_N	CSI0_RX1_N	CSI0_RX2_N	CSI0_RX3_N	K	JTAG
L	USB_DP	GND	USB_RTRIM	AVDD_VS	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	VDD_sense1	CSI0_RXCLK_P	CSI0_RX0_P	CSI0_RX1_P	CSI0_RX2_P	CSI0_RX3_P	L	I2C/I2S
M	USB_AVDD_IO	USB_AVDD_CORE	USB_VBUS	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI0_RX_AVDDH	CSI0_RX_AVDDH	CSI0_RX_RCALIB	CSI0_RX_AVDD	CSI_RX0_AVDD	M	FLASH
N	SDIO1_DATA1	SDIO1_DATA3	SDIO1_SDCLK	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_1	GND	GPIO_4	GND	GND	N	GND
P	SDIO1_CMD	SDIO1_DATA0	SDIO1_DATA2	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_0	GPIO_3	GPIO_6	GPIO_7	PARALLEL_PCLK	P	VDD CORE
R	GND	VDDIO_SDIO	VDDIO_SDIO	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_8	GPIO_9	GPIO_15	GPIO_26	GPIO_27	R	VDD TOP
T	SDIO0_DATA0	SDIO0_CMD	SDIO0_DATA2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GPIO_5	GPIO_10	GPIO_16	GPIO_25	GPIO_28	T	VDDIO
U	SDIO0_DATA3	SDIO0_DATA1	SDIO0_SDCLK	RSRVD	GND	GND	GND	GND	AVDD_TS_BOTTOM	GND	GND	GND	GND	GND	GPIO_2	GND	GPIO_11	GPIO_17	GPIO_24	GPIO_29	U	
V	FLASH_DQ0	FLASH_DQ1	FLASH_RESET	CSI0_TX_AVDD_CLK	GND	CSI0_TX_AVDD	CSI0_TX_AVDDH	GND	CSI0_TX_RCALIB	CSI1_TX_AVDD_CLK	GND	CSI1_TX_AVDD	CSI1_TX_AVDDH	GND	CSI1_TX_RCALIB	VDD_TOP	GPIO_12	GPIO_18	GPIO_23	GPIO_30	V	
W	FLASH_SCLK	FLASH_DQ3	FLASH_CS1_N	RSRVD	CSI0_TXCLK_P	CSI0_TX0_P	CSI0_TX1_P	CSI0_TX2_P	CSI0_TX3_P	CSI1_TXCLK_P	CSI1_TX0_P	CSI1_TX1_P	CSI1_TX2_P	CSI1_TX3_P	GND	VDD_TOP	GPIO_13	GPIO_19	GPIO_22	GPIO_31	W	
Y	GND	FLASH_DQ2	FLASH_CS0_N	RSRVD	CSI0_TXCLK_N	CSI0_TX0_N	CSI0_TX1_N	CSI0_TX2_N	CSI0_TX3_N	CSI1_TXCLK_N	CSI1_TX0_N	CSI1_TX1_N	CSI1_TX2_N	CSI1_TX3_N	GND	GND	GPIO_14	GPIO_20	GPIO_21	GND	Y	

Figure 3: Hailo-8L Ball Diagram – top view

2.2. Functional Assignment

Hailo-8L functional pin assignment is described in Table 4 .

Pin Types are categorized as follows:

- Power: SoC power rails
- I: input signals (Analog/Digital)
- O: output signals (Analog/Digital)
- OD: Open Drain IO

Table 4: Hailo-8L Functional Pin Assignment

Pin Name	Type	Description	Pin Numbers	Default Pull Type
Main Power and Sensing				
GND	Power	Digital ground for device	A1, A5, A15, A20, B5, B15, C4, C5, C9, C10, C11, C15, C16, D1, D4, D5, D7, D10, D12, D14, D15, D16, E4, E5, E6, E7, E8, E9, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, F4, F7, F8, F11, F12, F15, G1, G2, G3, G4, G7, G8, G11, G12, G15, H4, H7, H8, H11, H12, H15, J7, J8, J11, J12, J15, J16, J17, J18, J19, J20, K4, K7, K8, K11, K12, K15, L2, L7, L8, L11, L12, M4, M7, M8,	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
			M11, M12, M15, N4, N7, N8, N11, N12, N15, N17, N19, N20, P4, P7, P8, P11, P12, P15, R1, R4, R7, R8, R11, R12, R15, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, U6, U7, U8, U10, U11, U12, U13, U14, U16, V5, V8, V11, V14, W15, Y1, Y15, Y16, Y20	
VDDCORE	Power	Digital supply for SoC NN core domain	F5, F6, F9, F10, F13, F14, G5, G6, G13, G14, H5, H6, H13, H14, J5, J6, J14, K5, K6, K14, L5, L6, L13, L14, M5, M6, M13, M14, N5, N6, N9, N10, N13, N14, P5, P6, P9, P10, P13, P14, R5, R6, R9, R10, R13, R14	
VDDTOP	Power	Digital supply for SoC top domain	G9, G10, H9, H10, L9, L10, M9, M10, V16, W16	
VDDIO	Power	Digital supply for IO pads	D2, D3, J9, J10, K9, K10	
PLL_VSSA	Power	Analog ground for PLL	K13	
PLL_VDDA	Power	Analog supply for PLL	J13	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
AVDD_TS	Power	Analog supply for temperature sensor	E10, U9	
AVDD_VS	Power	Analog supply for voltage sensor	L04	
FUSE_VQPS	Power	Power pin for fuse programming	U4	
VDD_SENSE	Sensing	Sense for VDDCORE	J4	
VDD_SENSE1	Sensing	Sense for VDDTOP	L15	
PCI Express (PCIe) Interface				
PCIE_WAKE_N	O/OD	PCIe wake signal to host	D6	
PCIE_CLKREQ_N	I/OD	PCIe clock request to host	D8	
PCIE_PERST_N	I	PCIe reset in	D9	
PCIE_TX[0:3]_P	O	PCIe positive signal of data transmit diff-pair	A6, A8, A12, A14	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
PCIE_TX[0:3]_N	O	PCIe negative signal of data transmit diff-pair	B6, B8, B12, B14	
PCIE_RX[0:3]_P	I	PCIe positive signal of the data receive diff-pair	A7, A9, A11, A13	
PCIE_RX[0:3]_N	I	PCIe negative signal of data receive diff-pair	B7, B9, B11, B13	
PCIE_REFCLK_N	I	PCIe ref clock in negative	B10	
PCIE_REFCLK _P	I	PCIe ref clock in positive	A10	
PCIE_CMN_REXT	I	PCIe calibration connection to external resistor	D11	
PCIE_AVDD_C	Power	Analog power for high-speed clock and digital functions	A4, A16, B4, B16	
PCIE_AVDD_D	Power	Clean analog power	C6, C7, C8, C12, C13, C14	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
		for high speed clock		
PCIE_AVDD_H	Power	PCIe Analog I/O voltage	D13	
MIPI CSI TX Interface				
CSI0_TX[0:3]_N	O	Negative output of MIPI CSI TX interface[0] data lanes	Y6, Y7, Y8, Y9	
CSI0_TX[0:3]_P	O	Positive output of MIPI CSI TX interface data lane	W6, W7, W8, W9	
CSI1_TX[0:3]_N	O	Negative output of MIPI CSI TX interface[1] data lanes	Y11, Y12, Y13, Y14	
CSI1_TX[0:3]_P	O	Positive output of MIPI CSI TX interface[1] data lanes	W11, W12, W13, W14	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
CSI[0:1]_TXCLK_N	O	Negative output of MIPI CSI TX interface clock	Y5, Y10	
CSI[0:1]_TXCLK_P	O	Positive output of MIPI CSI TX interface clock	W5, W10	
CSI[0:1]_TX_RCALIB	I/O	Pin connected to external resistor for calibrating on-SoC resistors for MIPI CSI TX interface	V9, V15	
CSI[0:1]_TX_AVDD	Power	Analog power supply for MIPI CSI TX core	V6, V12	
CSI[0:1]_TX_AVDDH	Power	Analog power supply for MIPI CSI TX bias and PLL	V7, V13	
CSI[0:1]_TX_AVDD_CLK	Power	Clean analog power supply for high-speed clock applications	V4, V10	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
MIPI CSI RX Interface				
CSI0_RX[0:3]_N	I	Negative input of MIPI CSI RX[0] interface data lane	K17, K18, K19, K20	
CSI0_RX[0:3]_P	I	Positive input of MIPI CSI RX[0] interface data lane	L17, L18, L19, L20	
CSI1_RX[0:3]_N	I	Negative input of MIPI CSI RX[1] interface data lane	F17, F18, F19, F20	
CSI1_RX[0:3]_P	I	Positive input of MIPI CSI RX[1] interface data lane	G17, G18, G19, G20	
CSI[0:1]_RXCLK_N	I	Negative input of MIPI CSI RX interface clock	, K16, F16	
CSI[0:1]_ RXCLK_P	I	Positive input of MIPI CSI RX interface clock	L16, G16	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
CSI[0:1]_RX_RCALIB	I/O	Pin connected to external resistor for calibrating on-SoC resistors for MIPI CSI RX interface	M18, H16	
CSI0_RX_AVDD	Power	Analog power supply for MIPI CSI RX[0] core	M19, M20	
CSI1_RX_AVDD	Power	Analog power supply for MIPI CSI RX[1] core	H19, H20	
CSI0_RX_AVDDH	Power	Analog power supply for MIPI CSI RX[0] bias and PLL	M16, M17	
CSI1_RX_AVDDH	Power	Analog power supply for MIPI CSI RX[1] bias and PLL	H17, H18	
Universal Serial Bus (USB) Interface				
USB_DP	I/O	USB2.0 positive data	L1	
USB_DN	I/O	USB2.0 negative data	K1	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
USB_ID	I	USB2.0 ID	K3	
USB_RTRIM	I	Pin connected to external resistor for calibrating on-SoC resistors	L3	
USB_AVDD_CORE	Power	Analog power supply for USB core	M2	
USB_AVDD_IO	power	Analog power supply for USB I/Os	M1	
USB_AVDD_IO_HV		Analog power supply for USB	K2	
USB_VBUS	Power	USB2.0 VBUS	M3	
Secure Digital Input Output (SDIO) Interface				
SDIO[0-1]_CLK	O	SDIO/eMMC clock	U3, N3	
SDIO[0-1]_CMD	O	SDIO /eMMC control	T2, P1	
SDIO[0-1]_DATA [0:3]	I/O	SDIO /eMMC data I/O	T1, U2, T3, U1 P2, N1, P3, N2	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
VDDIO_SDIO	Power	Digital power supply for SDIO I/O	R2, R3	
Ethernet Interface				
ETH_RGMII_TXD [0:3]	O	Transmit data signal to PHY	B2, A3, A2, C1	
ETH_RGMII_TX_CLK	O	Transmit clock signal to PHY	B1	
ETH_RGMII_TX_CTL	O	Transmit control signal to PHY	B3	
ETH_RGMII_RXD [0:3]	I	Receive data signal from PHY	F3, E3, E2, E1	
ETH_RGMII_RX_CLK	I	Receive clock signal from PHY	F1	PD
ETH_RGMII_RX_CTL	I	Receive control signal from PHY	F2	PD
ETH_MDC	O	Management interface clock	C2	PU

Pin Name	Type	Description	Pin Numbers	Default Pull Type
ETH_MDIO	I/O	Management interface Data input output	C3	PU
Camera Parallel LVCMOS Interface				
PARALLEL_PCLK	I	Parallel input clock	P20	PD
PARALLEL_VSYNC	I	Parallel VSYNC	Pin multiplexed with GPIOs	
PARALLEL_HSYNC	I	Parallel HSYNC	Pin multiplexed with GPIOs	
PARALLEL_DATA [0:23]	I	Parallel data in	Pin multiplexed with GPIOs	
Flash Interface				
FLASH_RESET	O	Flash reset out	V3	
FLASH_CS[0:1]_N	O	Flash chip select, active low	Y3, W3	
FLASH_CS[2:3]_N		Flash chip select, active low	Pin multiplexed with GPIOs	
FLASH_DQ[0:3]	I/O	Flash data in/out	V1, V2, Y2, W2	PD

Pin Name	Type	Description	Pin Numbers	Default Pull Type
FLASH_SCLK	O	Flash clock	W1	
Universal Asynchronous Receiver Transmitter (UART) Interface				
UART[0:1]_RXD	I	UART receive data	J1, J2	PD
UART[0:1]_TXD	O	UART transmit data	H1, H2	
Inter-Integrated Circuit (I2C) Interface				
I2C[0:1]_SDA	I/O	I2C[0-1] serial data	D18, B18	PU
I2C[0:1]_SCL	O	I2C[0-1] clock	C18, A18	PU
I2C[0:3]_CURRENT_SRC_EN	I/O	Fast mode I2C pin	Pin multiplexed with GPIOs	
I2C[2:3]_SDA	I/O	I2C[2-3] serial data	Pin multiplexed with GPIOs	
I2C[2:3]_SCL	O	I2C[2-3] clock	Pin multiplexed with GPIOs	
Inter-IC Sound (2S) Interface				
I2S_WS	I	I2S word select	A17	
I2S_SCK	O	I2S serial clock	B17	
I2S_SDI	I	I2S serial data in	C17	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
I2S_SDO	O	I2S serial data out. Used as BS_IO_SEL[0] during Bootup. See section 5.2 below	D17	
Reset and Clock				
CLK_IN	I	SoC main clock	D19	
NRESET	I	Chip reset, active low	A19	PD
JTAG				
JTAG_TDI	I	JTAG data input	C20	PU
JTAG_TDO	O	JTAG data output	C19	PD
JTAG_TMS	I	JTAG mode select	B20	PU
JTAG_TCK	I	JTAG clock	B19	PD
JTAG_TRSTN	I	JTAG reset. Active low	D20	PU
GPIO[0-5]	I/O	General configurable pins. Output during Bootup.	P16, N16, U15, P17, N18, T16	

Pin Name	Type	Description	Pin Numbers	Default Pull Type
GPIO[6-31]	I/O	General configurable pins	P18, P19, R16, R17, T17, U17, V17, W17, Y17, R18, T18, U18, V18, W18, Y18, Y19, W19, V19, U19, T19, R19, R20, T20, U20, V20, W20	PD
MCU GPIOS				
MCU_GPIO[0-31]	I/O	GPIOs	Pin multiplexed with GPIOs	
Timers				
TIMER[0-3]_EXT_IN	I	External timer clock input	Pin multiplexed with GPIOs	
Electronic Trace Management (ETM)				
ETM_TRACE_CLOCK	O	ETM clock out	Pin multiplexed with GPIOs	
ETM_DATA[0-3]	O	ETM trace data out	Pin multiplexed with GPIOs	
Miscellaneous				
RESERVED	I	Factory use only. Do not connect.	U5, H3, J3	PD

2.3. Pin Multiplex Specifications

This section describes the possible multiplex configurations available for Hailo-8L GPIOs. Each of the 32 GPIOs has up to 8 options.

Important: Each group of pins can only be set to the same option.

- Option1 – pads_pinmux_mode[3:0] = [0000]
- Option2 – pads_pinmux_mode[3:0] = [0010]
- Option3 – pads_pinmux_mode[3:0] = [0011]
- Option4 – pads_pinmux_mode[3:0] = [0100]
- Option5 – pads_pinmux_mode[3:0] = [0101]
- Option6 – pads_pinmux_mode[3:0] = [0110]
- Option7 – pads_pinmux_mode[3:0] = [0111]
- Option8 – pads_pinmux_mode[3:0] = [1000]
- Option9 – pads_pinmux_mode[3:0] = [1001]

2.3.1 GPIO Group [0-1]

The multiplex options for GPIO[0] and GPIO[1] are listed in Table 5.

Table 5: GPIO Group [0-1] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO0	INITIAL_DEBUG_BUS [0]	GPIO[0]	I2C0_CURRENT_SRC_EN	FLASH_CS[2]	PWM[0]	Reserved	SDIO0_GP_OUT	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO1	INITIAL_DEBUG_BUS [1]	GPIO[1]	I2C1_CURRENT_SRC_EN	FLASH_CS[3]	PWM[1]	Reserved	SDIO1_GP_OUT	UART3_TXD	I2C3_CURRENT_SRC_EN

2.3.2 GPIO Group [2-3]

The multiplex options for GPIO[2] and GPIO[3] are listed in Table 6.

Table 6: GPIO Group [2-3] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO2	INITIAL_DEBUG_BUS [2]	GPIO[2]	I2C0_CURRENT_SRC_EN	FLASH_CS [2]	PWM[0]	Reserved	SDIO0_GP_OUT	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO3	INITIAL_DEBUG_BUS [3]	GPIO[3]	I2C1_CURRENT_SRC_EN	FLASH_CS [3]	PWM[1]	Reserved	SDIO1_GP_OUT	UART3_TXD	I2C3_CURRENT_SRC_EN

2.3.3 GPIO Group [4-5]

The multiplex options for GPIO[4] and GPIO[5] are listed in Table 7.

Table 7: GPIO Group [4-5] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO4	INITIAL_DEBUG_BUS [4]	GPIO[4]	I2C0_CURRENT_SRC_EN	FLASH_CS[2]	PWM[0]	Reserved	SDIO0_GP_OUT	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO5	INITIAL_DEBUG_BUS [5]	GPIO[5]	I2C1_CURRENT_SRC_EN	FLASH_CS [3]	PWM[1]	Reserved	SDIO1_GP_OUT	UART3_TXD	I2C3_CURRENT_SRC_EN

2.3.4 GPIO Group [6-7]

The multiplex options for GPIO[6] and GPIO[7] are listed in Table 8.

Table 8: GPIO Group [6-7] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8
GPIO6	PARALLEL_HSYNC	GPIO[6]	SDIO0_GP_IN	TIMER0_EXT_IN	TIMER2_EXT_IN	UART2_RXD	I2C2_SDA	I2C3_SDA
GPIO7	PARALLEL_VSYNC	GPIO[7]	SDIO1_GP_IN	TIMER1_EXT_IN	TIMER3_EXT_IN	UART3_RXD	I2C2_SCL	I2C3_SCL

2.3.5 GPIO Group [8-15]

The multiplex options for GPIO[8] to GPIO[15] are listed in Table 9.

Table 9: GPIO Group [8-15] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO8	SDIO0_GP_IN	GPIO[8]	PARALLEL_DATA[0]	I2C2_SDA	TIMER0_EXT_IN	Reserved	FLASH_CS [2]
GPIO9	SDIO1_GP_IN	GPIO[9]	PARALLEL_DATA[1]	I2C2_SCL	TIMER1_EXT_IN	Reserved	FLASH_CS[3]
GPIO10	SDIO0_GP_OUT	GPIO[10]	PARALLEL_DATA[2]	I2C3_SDA	PWM[0]	I2C0_CURRENT_SRC_EN	UART2_RXD
GPIO11	SDIO1_GP_OUT	GPIO[11]	PARALLEL_DATA[3]	I2C3_SCL	PWM[1]	I2C1_CURRENT_SRC_EN	UART2_TXD
GPIO12	TIMER0_EXT_IN	GPIO[12]	PARALLEL_DATA[4]	Reserved	PWM[2]	I2C2_CURRENT_SRC_EN	UART3_RXD

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO13	TIMER1_ EXT_IN	MCU GPIO[13]	PARALLEL_ DATA[5]	Reserved	PWM[3]	I2C3_CURR ENT_ SRC_EN	UART3_TXD
GPIO14	TIMER2_ EXT_IN	MCU GPIO[14]	PARALLEL_ DATA[6]	PARALLEL_ HSYNC	PWM[4]	PARALLEL_ HSYNC	PARALLEL_ HSYNC
GPIO15	TIMER3_ EXT_IN	MCU GPIO[15]	PARALLEL_ DATA[7]	PARALLEL_ VSYNC	PWM[5]	PARALLEL_ VSYNC	PARALLEL_ VSYNC

2.3.6 GPIO Group [16-31]

The multiplex options for GPIO[16] to GPIO[31] are listed in Table 10.

Table 10: GPIO Group [16-31] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO16	UART2_RXD	GPIO[16]	PARALLEL_DATA[8]	PARALLEL_DATA[0]	Reserved	SDIO0_GP_IN	SDIO0_GP_IN
GPIO17	UART2_TXD	GPIO[17]	PARALLEL_DATA[9]	PARALLEL_DATA[1]	Reserved	SDIO0_GP_OUT	SDIO0_GP_OUT
GPIO18	UART3_RXD	GPIO[18]	PARALLEL_DATA[10]	PARALLEL_DATA[2]	Reserved	PWM[0]	SDIO1_GP_IN
GPIO19	UART3_TXD	GPIO[19]	PARALLEL_DATA[11]	PARALLEL_DATA[3]	Reserved	PWM[1]	SDIO1_GP_OUT
GPIO20	I2C2_SDA	GPIO[21]	PARALLEL_DATA[12]	PARALLEL_DATA[4]	Reserved	PWM[2]	UART2_RXD
GPIO21	I2C2_SCL	GPIO[21]	PARALLEL_DATA[13]	PARALLEL_DATA[5]	Reserved	PWM[3]	UART2_TXD

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO22	I2C3_SDA	GPIO[22]	PARALLEL_DATA[14]	PARALLEL_DATA[6]	reserved	PWM[4]	UART3_RXD
GPIO23	I2C3_SCL	GPIO[23]	PARALLEL_DATA[15]	PARALLEL_DATA[7]	Reserved	PWM[5]	UART3_TXD
GPIO24	I2C0_CURRENT_SRC_EN	GPIO[24]	PARALLEL_DATA[16]	PARALLEL_DATA[8]	TIMER0_EXT_IN	Reserved	PWM[0]
GPIO25	I2C1_CURRENT_SRC_EN	GPIO[25]	PARALLEL_DATA[17]	PARALLEL_DATA[9]	TIMER1_EXT_IN	Reserved	PWM[1]
GPIO26	I2C2_CURRENT_SRC_EN	GPIO[26]	PARALLEL_DATA[18]	PARALLEL_DATA[10]	TIMER2_EXT_IN	Reserved	I2C2_SDA
GPIO27	I2C3_CURRENT_SRC_EN	GPIO[27]	PARALLEL_DATA[19]	PARALLEL_DATA[11]	ETM_TRACE_CLK	Reserved	I2C2_SCL

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO28	PWM[0]	GPIO[28]	PARALLEL_DATA[20]	PARALLEL_DATA[12]	ETM_DATA[0]	Reserved	I2C3_SDA
GPIO29	PWM[1]	GPIO[29]	PARALLEL_DATA[21]	PARALLEL_DATA[13]	ETM_DATA[1]	Reserved	I2C3_SCL
GPIO30	Reserved	GPIO[30]	PARALLEL_DATA[22]	PARALLEL_DATA[14]	ETM_DATA[2]	Reserved	Reserved
GPIO31	Reserved	GPIO[31]	PARALLEL_DATA[23]	PARALLEL_DATA[15]	ETM_DATA[3]	Reserved	Reserved

3. Thermal Characteristics

Package thermal resistance at various junctions and under various airflow conditions is shown in Table 11. The board that achieved these results is defined by JEDEC (please refer to JEDEC standard JESD51-9, Test Board for Array Surface Mount Package Thermal Measurements) as follows:

- 8 PCB layers
- PCB dimensions [mm X mm] - 101.5 X 114.5
- PCB thickness [mm X mm] - 1.6 mm

Table 11: Thermal Resistance

Location	Airflow	Thermal Resistance (° C/W)
Junction to ambient $\boldsymbol{\theta_{JA}\_0}$	No airflow	8.9
Junction to ambient $\boldsymbol{\theta_{JA}\_1}$	1 m/s airflow	7.8
Junction to ambient $\boldsymbol{\theta_{JA}\_2}$	2 m/s airflow	7.3
Junction to board $\boldsymbol{\theta_{JB}}$	No airflow	2.28
Junction to case $\boldsymbol{\theta_{JC}}$	No airflow	0.35

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 13 may cause permanent damage to the device and affect device reliability. These are stress ratings only and functional operation of the device at these conditions is not implied.

4.1.1 Power Rails

Table 12 provides the absolute maximum ratings of the power rails.

Table 12: Absolute Maximum Power Rail Ratings

Supply Name	Description	Min	Max	Unit
Digital Power Rails				
VDD_TOP	Top logic	-0.3	1.05	V
VDD_CORE	NN core	-0.3	1.05	V
VDDIO	IO banks	-0.3	1.98	V
VDDIO_SDIO	SDIO IO	-0.3	1.98	V
MIPI DPHY Analog Power Rails				
CSI_RX_AVDD CSI_TX_AVDD	MIPI DPHY RX/TX core supply for analog and digital	-0.3	1.05	V
CSI_RX_AVDD_H CSI_TX_AVDD_H	High voltage power for the RX/TX analog, bias and PLL (PLL only for TX)	-0.3	1.98	V
CSI_TX_CLK	MIPI DPHY TX (only) clean core supply for analog high-speed clocking circuits	-0.3	1.05	V

Supply Name	Description	Min	Max	Unit
PCIe PHY Analog Power Rails				
PCIE_AVDD_D	Analog power for non-high speed clock and digital functions	-0.3	1.05	V
PCIE_AVDD_C	Clean analog power for high speed clock applications	-0.3	1.05	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	-0.3	1.98	V
USB PHY Analog Power Rails				
USB_AVDD_CORE	USB core	-0.3	1.05	V
USB_AVDD_IO	USB IO	-0.3	1.98	V
USB_AVDD_IO_HV	Clean analog power supply for USB IO	-0.3	3.63	V
Miscellaneous				
PLL_AVDD	PLL analog power rail	-0.3	1.05	V
FUSE_VQPS	Factory use only. Connect to GND.	-	-	V
AVDD_TS	Temperature sensor analog power rail	-0.3	1.98	V
AVDD_VS	Voltage sensor analog power rail	-0.3	1.98	V
Input voltage applied to digital IOs	Input Low Voltage	-0.3	1.98	V
V_ESD (HBM)	Electrostatic discharge voltage (Human Body Model)	2000		V
V_ESD (CDM)	Electrostatic discharge voltage (Charged Device Model)	500		V

Supply Name	Description	Min	Max	Unit
Latch UP (LU)	class II of JESD78E immunity level	A[1]		-

4.1.2 Thermal Ratings

Table 13 provides the storage and maximum junction temperature values.

Table 13: Absolute Maximum Thermal Ratings

Parameter	Description	Value	Unit
T_Storage	Storage temperature	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

1 Immunity level A: Pass the ±100mA and 1.5xVdd or MSV

4.2. Recommended Operating Conditions

Table 14 describes the recommended operating conditions for power rails, clocks and ambient temperature.

Table 14: Hailo-8L Operating Ranges

Supply Name	Description	Min	Nom	Max	Unit
Digital Domain Power Rails					
VDD_TOP	Top logic power rail	0.78	0.83	0.88	V
VDD_CORE	Neural Network Core Power rail	0.78	0.83	0.88	V
VDDIO	Digital Power Rail for IO banks	1.62	1.8	1.98	V
VDDIO_SDIO[1]	Digital Power Rail for SDIO IO	1.08/ 1.62	1.2/ 1.8	1.32/ 1.98	V
MIPI DPHY Analog Power Rails					
CSI_RX_AVDD CSI_TX_AVDD	MIPI RX/TX MIPI DPHY Core supply for analog and digital	0.78	0.83	0.88	V
CSI_RX_AVDD_H CSI_TX_AVDD_H	High voltage power for the RX/TX MIPI DPHY analog, bias and PLL (PLL only for TX)	1.62	1.8	1.98	V
CSI_TX_CLK	MIPI DPHY TX (only) clean core supply for analog high-speed clocking circuits	0.78	0.83	0.88	V
PCIe PHY Analog Power Rails					
PCIE_AVDD_D	Analog power for non-high speed clock and digital functions	0.78	0.83	0.88	V

[1] Depending on the selected mode of SDIO IO power rail. 1.2V or 1.8V.

Supply Name	Description	Min	Nom	Max	Unit
PCIE_AVDD_C	Clean analog power for high speed clock applications	0.78	0.83	0.88	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	1.08	1.8	1.98	V
USB PHY Analog Power Rails					
USB_AVDD_CORE	Analog power supply for the USB core	0.78	0.83	0.88	V
USB_AVDD_IO	Analog power supply for the USB's IO	1.62	1.8	1.98	V
USB_AVDD_IO_HV	Clean analog power supply for USB's IO	2.97	3.3	3.63	V
Other Power Rails					
PLL_AVDD	PLL analog power rail	0.78	0.83	0.88	V
FUSE_VQPS	Factory use only. Connect to GND.	-	-	-	V
AVDD_TS	Temperature sensor analog power rail	1.62	1.8	1.98	V
AVDD_VS	Voltage sensor analog power rail	1.62	1.8	1.98	V
External Clocks					
CLK_IN[1] Main Input clock signal (square wave)	Frequency	25±100PPM			MHz
	Duty Cycle	40	50	60	%
Ambient Operating Temperature					
T_A	Consumer grade	0		70	°C
	Industrial grade	-40		85	°C

[1] CLK_IN clock pin must receive a square wave clock signal (oscillator output clock signal).

4.3. Power-up Sequence

The power-up sequence should follow these guidelines: [1]

1. Initial state: NRESET pin is asserted (held low).
2. VDDIO rises to 1.8V. Slew rate should be less than 18V/ms.
3. VDD_CORE rises to 0.83V. VDD_CORE must hold VDD_CORE <VDDIO-0.3V. Slew rate of VDD_CORE should be less than 18V/ms.
4. PLL_VDDA should rise with VDD_CORE and be powered from VDD_CORE power regulator with filtering.
5. After the VDD_CORE reaches final level:
   a) Power-up CSI_RX/TX_AVDD and CSI_RX/TX_AVDDH. Each power ramp-up should be between 100us and 2ms. CSI_RX/TX_AVDDH and CSI_RX/TX_AVDD can power-up in any order.[2]
   b) Power-up PCIE_AVDD_D, PCIE_AVDD_C, PCIE_AVDD_H in any order. There are no timing limitations (minimum or maximum) when powering-up multiple power supplies.
   c) PCIE_AVDD_D, PCIE_AVDD_C can be powered from VDD_CORE power regulator as long as noise target is met.[5][5]
   d) Power-up USB_VBUS, USB_AVDD_CORE, USB_AVDD_IO and USB_AVDD_IO_HV in any order.
      - There are no timing limitations (minimum or maximum) when powering-up multiple power supplies.
      - Between the supplied and VBUS – there is no specific ramp up, and VBUS can be present in cases when there are both supplies and are no supplies provided to the USB 2.0[5] [5]
6. Enable reference clock after VDDIO reached final voltage level.

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[1] T12 requirement derived from PCI Express Specification Rev 3.0, Section 2.6.2. AC Specifications:

Symbol	Parameter	Min	Max	Units	Notes
T_{PVPERL}	Power stable to PERST# inactive	100		ms	1

"De-asserted NRESET such having enough margin to the end point enter LTSSM Detect State within 20 ms of the end of Fundamental Reset (PERSTn) , and 100ms before system sending a Configuration Request to the device".

[2] On PCIe Only configuration – x_AVDD can be derived from with VDD_CORE, and x_AVDDH can be derived from VDDIO. Refer to 3.1.2.2 PCIe Only (Minimum Configuration).

7. De-assert NRESET after clock is stable for 10 cycles. clock is stable when it meets the requirements for CLK_IN.
8. For PCIe application: De-assert NRESET before or up to 500us PCIe PERST is de-asserted. For non-PCIe application: Add 1K-2K PU on PERSTn

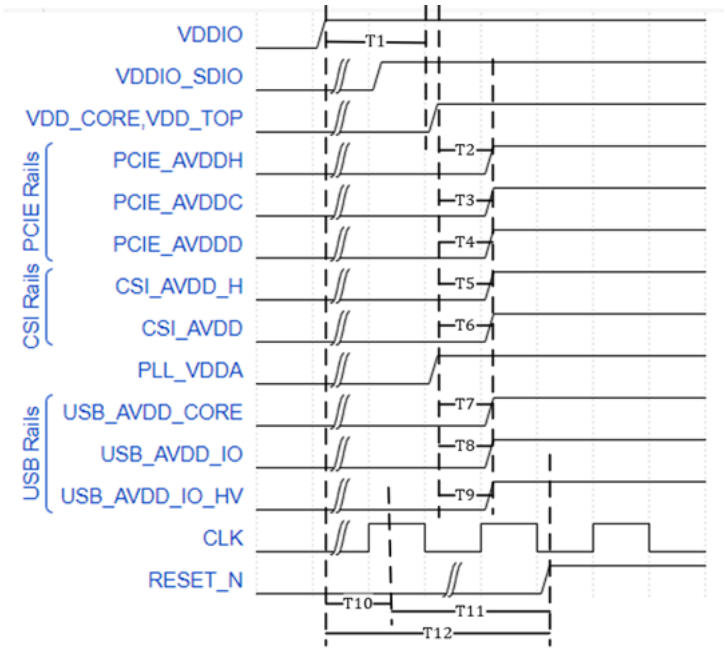

Figure 4: Power-up Sequence

Table 15: Power-up Sequence Timing Requirements

	Description	Min	Nom	Max	Unit
T1	VDDIO to VDD_CORE and VDD_TOP	1	-	-	us
T2	VDD_CORE to PCIE_AVDD_H	1	-	-	us
T3	VDD_CORE to PCIE_AVDD_C	1	-	-	us
T4	VDD_CORE to PCIE_AVDD_D	1	-	-	us
T5	VDD_CORE to CSI_AVDD_H	1	-	-	us
T6	VDD_CORE to CSI_AVDD	1	-	-	us
T7	VDD_CORE to USB_AVDD_CORE	1	-	-	us
T8	VDD_CORE to USB_AVDD_IO	1	-	-	us
T9	VDD_CORE to USB_AVDD_IO_HV	1	-	-	us
T10	VDDIO to Stable Clock	1	-	-	ms
T11	Stable CLK to RESET_N de-assertion	100	-	-	us
T12	VDDIO to RESET_N de-assertion	-	-	70	ms

4.4. Power Consumption

4.4.1 Maximum Supply Current

The maximum current that can be drawn from each power rail is application-dependent. The measurements in Table 16 were made during device characterization and represent worst-case results across all PVT corners. The numbers are provided here only as general guidelines for power supply design.

Table 16: Maximum Supply Current

Supply Name	Max Current	Unit
VDD_CORE[1]	7.2	A
VDD_TOP	1	A
VDDIO[2]	0.3	A
VDDIO_SDIO[3]	60 (4)	mA
CSI0_RX_AVDD	25	mA
CSI0_RX_AVDDH	30	mA
CSI1_RX_AVDD	25	mA
CSI1_RX_AVDDH	30	mA
CSI0_TX_AVDD	100	mA

1 The maximum current assumes heavy compute networks, for lowering the values, if needed, please evaluate the specific neural model and SoC integration for the specific network and add an adequate margin to cover all PVT corners and current spikes.

2 $VDDIO[V] \cdot \sum_{IO_i}\left(C_i[F] \cdot \frac{1}{2} \cdot f_{switching}[Hz]\right)$ Each IO_i drives a capacitance C_i[F] and is switched from 1 to 0 and vice versa at a frequency of 0.5f[Hz]. Add C_i[F]x0.5f[Hz] of all the IOs and multiply this sum by the VDDIO[V] voltage rail to obtain the VDDIO current consumption I_VDDIO[A].

3 For 1.8V IO power rail

Supply Name	Max Current	Unit
CSI0_TX_AVDDH	14	mA
CSI0_TX_AVDD_CLK	10	mA
CSI1_TX_AVDD	100	mA
CSI1_TX_AVDDH	14	mA
CSI1_TX_AVDD_CLK	10	mA
PCIE_AVDD_D	280	mA
PCIE_AVDD_C	180	mA
PCIE_AVDD_H	21	uA
USB_AVDD_CORE	7	mA
USB_AVDD_IO	17	mA
USB_AVDD_IO_HV	1.1	mA
PLL_AVDD	1.2	mA
AVDD_TS	0.5	mA
AVDD_VS	0.3	mA

4.4.2 Supply Current in Selected Test Cases

TBD

4.4.3 Power Modes

When powered on, Hailo-8L can be operated in fully functional, normal mode or in any of three low-power modes: doze, sleep and hibernate.

Doze, sleep and hibernate modes are designed to help system integrators to optimally manage the exit latency vs. power tradeoff.

- **Doze** mode retains all memory and register-stored data to minimize reconfiguration time. The PLL remains powered-on to eliminate PLL lock time. Unused logic is clock-gated, and analog macros are held in the protocols' relevant low power states.
- **Sleep** mode minimizes power consumption more than Doze mode by powering off the PLL and the NN Core logic. This significantly reduces power requirements but requires additional wake-up time for PLL stabilization and register reconfiguration.
- **Hibernate** is the most aggressive low-power mode. It powers off NN Core memories in addition to NN Core logic and the PLL, requiring complete reconfiguration at wake-up.

See Table 17 for the power values of the three low-power modes.

Table 17: Low-Power Modes, Power Consumption

Mode	Power Consumption VDD_CORE + VDD_TOP [mW]
Doze	TBD
Sleep	TBD
Hibernate	TBD

Note: VDDIO and all MIPI power rails can only be powered off when the SoC is powered off.

4.5. Digital I/O DC Characteristics

There are two groups of I/O types:

Failsafe I/Os with strong PU/PD: Signals using this I/O type are: PCIE_PERST_N, PCIE_CLKREQ_N, PCIE_WAKE_N, GPIO0, GPIO1, CLK_IN and NRESET.

Regular I/Os: All other GPIOs use this I/O type.

Table 18 describes the DC characteristics of the failsafe digital pins as characterized across all PVT corners.

Table 18: Failsafe Digital Pin DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDD_IO	V
V_{IH}	Input High Voltage	0.65*VDD_IO		1.98	V
V_T	Threshold Point	0.91	1	1.13	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.97	1.09	1.2	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.75	0.86	0.97	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.95	1.07	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.91	1.01	1.14	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.87	1	1.13	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point	0.69	0.8	0.92	V

Symbol	Parameter	Min	Typ	Max	Unit
	with Pull-Up Resistor Enabled				
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.98	1.09	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.86	0.98	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	31	46	84	KΩ
R_{PD}	Pull-Down Resistor	31	44	71	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance	-	1.05	-	pF

Table 19 describes the DC characteristics of the regular GPIOs pins, as characterized across all PVT corners.

Table 19: Regular GPIOs DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDD_IO	V
V_{IH}	Input High Voltage	0.65*VDD_IO		1.98	V
V_T	Threshold Point	0.82	0.92	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.98	1.1	1.21	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.74	0.82	0.9	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.91	1	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.83	0.93	1.02	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.97	1.09	1.2	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.73	0.81	0.89	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.99	1.11	1.22	V

Symbol	Parameter	Min	Typ	Max	Unit
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.83	0.91	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	17	24	40	KΩ
R_{PD}	Pull-Down Resistor	17	23	36	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance for all other pads	-	0.88	-	pF

4.6. PCIE Characteristics (DC And AC)

The following tables describe the PCIe characteristics as characterized across all PVT corners.

Table 20: PCIe Gen1 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	876	1130	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	489.33	669.19	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 21: PCIe Gen2 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	810	1070	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	445	625	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.235	ns

Table 22: PCIe Gen3 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1010	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	401	547	mV

Parameter	Description	Min	Max	Unit
VTX-EIEOS-FS	Minimum voltage swing during EIEOS for full swing signaling	262	-	mVPP
VTX-EIEOS-RS	Minimum voltage swing during EIEOS for reduced swing signaling	256	-	mVPP
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 23: PCIe Transmitter Data Rate Independent Characteristics

Parameter	Description	Min	Max	Unit
VTX-AC-CM-PP	Tx AC peak-peak common mode voltage	-	134	mVPP
VTX-DC-CM	Tx DC peak-peak common mode voltage	0.396	0.404	V
VTX-CM-DC-LINE-DELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	2.1	7.2	mV
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	8.09	19.98	mV
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage	0.1	1.4	mV
ZTX-DIFF-DC	DC differential Tx impedance	69.2	75.3	Ω

Table 24:PCIe Receiver Electrical Idle Detect Threshold

Parameter	Description	Min	Max	Unit
VRX-IDLE-DET-DIFF-PP	Electrical Idle Detect threshold	92	154	mV

Table 25:PCIe Receiver Termination Characteristics

Parameter	Description	Min	Max	Unit
ZRX-DC	Receiver DC single ended impedance	49.7	54.9	Ω
ZRX-HIGH-IMP-DC-POS (0-200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	53k	-	Ω
ZRX-HIGH-IMP-DC-POS (> 200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	144k	-	Ω
ZRX-HIGH-IMP-DC-NEG	DC input CM input impedance for V<0 during Reset or power-down	4.6k	-	Ω

4.7. MIPI DPHY RX Characteristics

The following tables describe the MIPI RX DPHY characteristics as characterized across all PVT corners.

Table 26: MIPI RX DPHY Clock Lane LP Voltage and Timing Characteristics

Parameter	Description	Value	Unit
LP-RX Logic 1 Input Voltage (VIH)	Minimum voltage level where LP receiver consistently detects Logic 1	665	mV
LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Maximum voltage level where non-ULP LP receiver consistently detects Logic 0	605	mV
LP-RX Input Hysteresis (VHYST)	Maximum Logic 1 hysteresis	25	mV
LP-RX Minimum Pulse Width Response (TMIN-RX)	Maximum Pulse width which LP receiver can detect without any error.	15	ns

Table 27: MIPI RX DPHY Data Lane LP Voltage and Timing Characteristics

Parameter	Description	Value	Unit
LP-RX Logic 1 Input Voltage (VIH)	Minimum voltage level where LP receiver consistently detects Logic 1	665	mV
LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Maximum voltage level where non-ULP LP receiver consistently detects Logic 0	605	mV
LP-RX Input Hysteresis (VHYST)	Maximum Logic 1 hysteresis	25	mV
LP-RX Minimum Pulse Width c (TMIN-RX)	Maximum Pulse width which LP receiver can detect without any error	15	ns

Table 28: MIPI RX DPHY HS DC Differential Input Impedance

Parameter	Description	Value	Unit
HS-RX DC Differential Input Impedance (ZID)	Data Lane: DC Differential Input Impedance (ZID)	100.1/122.9	Ohm
	Clock Lane: DC Differential Input Impedance (ZID)	102.9/117.1	Ohm

4.8. MIPI DPHY TX Characteristics

The following tables describe the MIPI TX DPHY characteristics as characterized across all PVT corners.

4.8.1 LP Characteristics

Table 29: MIPI TX DPHY Data Lane LP DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX Thevenin output high voltage level (VOH)	C_{LOAD} = 70 pF	0.969	1.153	1.217	V
Data Lane LP-TX Thevenin Output Low Level Voltage (VOL)	C_{LOAD} = 70 pF	-35	-0.87	49	mV

Table 30: MIPI TX DPHY Data Lane LP AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX 15%-85% Rise Time (TRLP)	C_{LOAD} = 70 pF		18.136	21.02	ns
Data Lane LP-TX 15%-85% Fall Time (TFLP)	C_{LOAD} = 70 pF		17.66	22.04	ns
Data Lane LPTX Runtime XOR Clock Pulse Width (TLP-PULSE-TX)	C_{LOAD} = 70 pF	21.18	34.49		ns
Data Lane LPTX Runtime XOR Clock Pulse Width (TLP-PULSE-TX) (Initial)	C_{LOAD} = 70 pF	47.91	49.71		ns

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX Period of Exclusive-OR Clock (TLP-PER-TX)	C_{LOAD} = 70 pF	92.83	97.06		ns
Data Lane Slew Rate Max	C_{LOAD} = 70 pF			115.9	mV/ns
Data Lane Slew Rate Min	C_{LOAD} = 70 pF	26.34	36.238		mV/ns
Data Lane Slew Rate Margin	C_{LOAD} = 70 pF	0.19	9.352		mV/ns

Table 31: MIPI TX DPHY Clock Lane LP DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane LP-TX Thevenin output High Voltage Level (VOH)	C_{LOAD} = 70 pF	1.036	1.185	1.23	V
Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL)	C_{LOAD} = 70 pF	-36	-16.6	30	mV

Table 32: MIPI TX DPHY Clock Lane LP AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane LP-TX 15%-85% Rise Time (TRLP)	C_{LOAD} = 70 pF		18.27	23.23	ns
Clock Lane LP-TX 15%-85% Fall Time (TFLP)	C_{LOAD} = 70 pF		17.38	19.75	ns
Clock Lane Slew Rate Max	C_{LOAD} = 70 pF			113.98	mV/ns

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane Slew Rate Min	C_{LOAD} = 70 pF	34.57			mV/ns
Clock Lane Slew Rate Margin	C_{LOAD} = 70 pF	0.29			mV/ns

4.8.2 HS Characteristics

Table 33: MIPI TX DPHY Data Lane HS DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
HS Data TX Differential Voltage (VOD(0) Pulse)	Termination=80,100, 125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	-263.4	-212	-176.5	mV
HS Data TX Differential Voltage (VOD(1) Pulse)		170.16	201.91	268.61	mV
Data Lane HS-TX Differential Voltage Mismatch (ΔVOD)		-13.93		2.73	mV
Data Lane HS-TX Single Ended Output High Voltage (VOHHS)			293.36	349.73	mV
Data Lane HS-TX Static Common-Mode Voltage (VCMTX)		158.9	172.7	248.27	mV
Data Lane HS-TX Static Common-Mode Voltage Mismatch (ΔVCMTX)				4.92	mV
Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz			9.02	23.15	mV_{PEAK}

Parameter	Conditions	Min	Typ	Max	Unit
(ΔVCMTX(LF))					
Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz (ΔVCMTX(HF))			5.63	11.21	mV_{rms}

Table 34: MIPI TX DPHY Data Lane HS AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane HS-TX 20%-80% Rise time tR (bit rate <=1Gbps)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	153.64	248.37	356.51	ps
Data Lane HS-TX 20%-80% Rise time tR (bit rate >1Gbps)		146.08	179.76	249.23	ps
Data Lane HS-TX 20%-80% Rise time tR (bit rate >1.5 Gbps)		105.55	124.24	145.73	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate< = 1Gbps)		182.27	248.4	356.13	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate >1Gbps)		145.55	179.34	240.22	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate > 1.5 Gbps)		107.14	125.83	148.87	ps

Table 35: MIPI TX DPHY Clock Lane HS DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
HS Clock TX Differential Voltage(VOD(0) Pulse)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps				
HS Clock TX Differential Voltage(VOD(1) Pulse)		159.53	192.13	245.06	mV
Clock Lane HS-TX Differential Voltage Mismatch (Δ VOD)		-13.9		8.65	mV
Clock Lane HS-TX Single Ended Output High Voltage (VOHHS)			269.2	345.8	mV
Clock Lane HS-TX Static Common-Mode Voltage (VCMTX)		179.74	188.87	243.68	mV
Clock Lane HS-TX Static Common-Mode Voltage Mismatch (Δ VCMTX)			1.01	3.84	mV
Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz (Δ VCMTX(LF))			7.53	23.54	mV_{PEAK}

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz (Δ VCMTX(HF))			5.53	11.77	mV_{rms}

Table 36: MIPI TX DPHY Clock Lane HS AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane HS-TX 20%-80% Rise time tR (bit rate <=1Gbps)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	186.29	232.91	296.69	ps
Clock Lane HS-TX 20%-80% Rise time tR (bit rate > 1Gbps)		144.94	171.32	243.25	ps
Clock Lane HS-TX 20%-80% Rise time tR (bit rate > 1.5 Gbps)		112.54	128.45	159.25	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate< = 1Gbps)		188.54	231.1	292.18	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate > 1Gbps)		143.11	168.71	241.65	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate > 1.5 Gbps)		110.12	129.1	157.89	ps

Table 37: MIPI TX DPHY Data Lane HS AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane HS-TX Single Ended Output impedance (ZOS)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	40.61	51.75	55.92	Ω
Clock Lane HS-TX Single Ended Output impedance (ZOS)		40.67	49.25	53.58	Ω
Data Lane Single Ended Output Impedance Mismatch (delta ZOS)			1.06	9.94	%
Clock Lane Single Ended Output Impedance Mismatch (delta ZOS)			0.65	9.66	%
Data Lane LP-TX Output Impedance (ZOLP)		117.34	136.55		Ω
Clock Lane LP-TX Output Impedance (ZOLP)		116.31	135.05		Ω

4.9. USB Characteristics

The following tables describe the USB PHY characteristics as characterized across all PVT corners.

4.9.1 HS Characteristics

Table 38: USB PHYHS Transmitter – DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Idle Level	V_{Idle}	-2.3	-1.5	-0.9	mV
Low Level	V_{OL}	-2.4	-1.6	-0.9	mV
Device Chirp K	Dev CK	-742	-663	-604	mV
Host Chirp K	Host CK	-896	-808	-759	mV
Host Chirp J	Host CJ	807	854	940	mV

Table 39: USB PHY HS Transmitter – AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Signal Rate	SR	479.99	480.01	480.03	Mbps
Rising Edge Rate	RER		990	1127	V/us
Falling Edge Rate	FER		990	1127	V/us
Rise Time	RT	567	646		ps
Fall Time	FT	567	646		ps
EOP Width	EOPW	7.86	7.89	7.92	bits

4.9.2 FS Characteristics

Table 40: USB PHY FS Transmitter – DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Low Level (Idle)	V_{OL}		0.005	0.05	V
Low Level (Driven)	V_{OL}		0.03	0.07	V
High Level (Driven)	V_{OH}	2.95	3.26	3.57	V
Crossover Voltage	V_{CRS}	1.17	1.49	1.83	V

Table 41: USB PHY FS Transmitter – AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Signal Rate	TFDRATHS	11.995	12	12.005	Mbps
Rise Time	TFR	9.8	11.5	13.5	ns
Fall Time	TFF	10.5	12.7	14.9	ns
Rise Fall Matching	TFRFM	90	91.5	93.4	%
Consecutive Jitter	TDJ1	-891	-18	603	ps
Paired JK Jitter	TDJ2	-963	81	967	ps
Paired KJ Jitter	TDJ2	-518	62	806	ps
EOP Width	TFEOPT	166	166.5	167	ns

Table 42: USB PHY FS Single-Ended Receiver – DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level (Driven)	V_{IH}	2			V
Input Low Level	V_{IL}			0.8	V
Differential Input Sensitivity	V_{DI}	0.2			V
Differential Common Mode Range	V_{CM}		1.7		V

Table 43: USB PHY FS Single-Ended Receiver – AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Jitter (to Next Transition)	TJR1	-18.5		18.5	ns
Jitter (Paired Transition)	TJR2	-9		9	ns

4.9.3 LS Characteristics

Table 44: USB PHY LS Transmitter – DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Low Level (Idle)	V_{OL}		0.005	0.056	V
Low Level (Driven)	V_{OL}		0.03	0.07	V
High Level (Driven)	V_{OH}	2.95	3.26	3.56	V
Rise Time	T_R	113	132	151	ns
Fall Time	T_F	116	142	165	ns

Table 45: USB PHY LS Transmitter – AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Rise Fall Matching	TLRFM	94.4	97.42	99.6	%
Signal Rate	TLDRATHS	1.5	1.5	1.5	Mbps
Crossover Voltage	VCRS	1.35	1.52	1.72	V
Consecutive Jitter (Upstream)	Consecutive Jitter-UP	-3.5	0.3	3.6	ns
Paired JK Jitter (Upstream)	Paired JK Jitter-UP	-3.4	0.2	3.1	ns
Paired KJ Jitter (Upstream)	Paired KJ Jitter-UP	-2.6	0.1	2.6	ns
Consecutive Jitter (Downstream)	Consecutive Jitter-Down	-3.5	0.3	3.6	ns
Paired JK Jitter (Downstream)	Paired JK Jitter-Down	-3.4	0.2	3.1	ns
Paired KJ Jitter (Downstream)	Paired KJ Jitter-Down	-2.6	0.1	2.6	ns
EOP Width	TLEOPT	1.33	1.33	1.34	us

Table 46: USB PHY LS Single-Ended Receiver – DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level (Driven)	V_{IH}	2			V
Input Low Level	V_{IL}			0.8	V
Differential Input Sensitivity	V_{DI}	0.2			V
Differential Common Mode Range	V_{CM}		1.7		V

Table 47: USB PHY LS Single-Ended Receiver – AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Jitter (to Next Transition)	TJR1	-152		152	ns
Jitter (Paired Transition)	TJR2	-199		199	ns

4.9.4 Termination Characteristics

Table 48: USB PHY Termination Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Pullup Resistance (Idle Bus)	RPU2	1.2	1.3	1.3	kΩ
Pullup Resistance (Active Bus)	RPU1	2.1	2.1	2.2	kΩ
Pulldown Resistance	RPD	14.5	18.7	19.1	kΩ
Input Impedance	ZINP		434.4		kΩ

Parameter	Symbol	Min	Typ	Max	Unit
FS Output Impedance	ZFSDRV	43.9	45.2	46.5	Ω
HS Output Impedance	ZHSDRV	43.1	44.2	45.4	Ω

4.10. SDIO Characteristics

The following tables describe the SDIO PHY characteristics as characterized across all PVT corners.

Table 49: SDIO Receiver Thresholds - 1.8V

Parameter	Min	Typ	Max	Unit
Rx Type 1.8V Schmitt Trigger Assertion	0.81	-	1.054	V
Rx Type 1.8V Schmitt Trigger De-assertion	0.772	-	1.009	V
Rx Type 1.8V Schmitt Trigger Hysteresis	0.037	-	0.064	V
Rx Type 1.8V Comparator Vth Assertion	0.787	-	0.998	V
Rx Type 1.8V Comparator Vth De-assertion	0.797	-	1.002	V

Table 50: SDIO Receiver Thresholds - 1.2V

Parameter	Min	Typ	Max	Unit
Rx Type 1.2V Schmitt Trigger Assertion	0.533	-	0.713	V
Rx Type 1.2V Schmitt Trigger De-assertion	0.529	-	0.71	V

Parameter	Min	Typ	Max	Unit
Rx Type 1.2V Schmitt Trigger Hysteresis	-0.001	-	0.007	V
Rx Type 1.2V Comparator Assertion	0.556	-	0.711	V
Rx Type 1.2V Comparator De-assertion	0.56	-	0.715	V

Table 51: SDIO Receiver Duty Cycle

Parameter	Min	Typ	Max	Unit
Duty Cycle Rx Type 1.8V Schmitt Trigger	49.214	-	54.017	%
Duty Cycle Rx Type 1.8V Comparator Vth	46.036	-	50.69	%
Duty Cycle Rx Type 1.2V Schmitt Trigger	47.402	-	54.005	%
Duty Cycle Rx Type 1.2V Comparator Vth	47.143	-	53.417	%

Table 52: SDIO IO Leakage

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance IO Leakage	Internal pull-up and pull-down resistors disconnected	-0.81	-	0.036	uA
PHY 1.2V Instance IO Leakage	Internal pull-up and pull-down resistors disconnected	-1.06	-	0.277	uA

Table 53: SDIO TX Impedance - DC

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance Driver Strength: 50 Ohm	Pull-up	48.937	-	62.474	Ohm
	Pull-down	49.57	-	64.677	Ohm
PHY 1.2V Instance Driver Strength: 50 Ohm	Pull-up	47.421	-	65.557	Ohm
	Pull-down	47.157	-	71.184	Ohm
PHY 1.8V Instance Driver Strength: 40 Ohm	Pull-up	39.55	-	50.488	Ohm
	Pull-down	39.954	-	52.047	Ohm
PHY 1.2V Instance Driver Strength: 40 Ohm	Pull-up	38.324	-	52.949	Ohm
	Pull-down	38.01	-	57.166	Ohm

Table 54: SDIO TX Capacitance - AC

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance Driver Strength: 50 Ohm	Pull-up	3.443	-	4.228	pf
	Pull-down	3.448	-	4.212	pf
PHY 1.2V Instance Driver Strength: 50 Ohm	Pull-up	3.061	-	4.277	pf
	Pull-down	3.075	-	4.269	pf
PHY 1.8V Instance Driver Strength: 40 Ohm	Pull-up	2.163	-	3.435	pf
	Pull-down	2.111	-	3.413	pf
PHY 1.2V Instance Driver Strength: 40 Ohm	Pull-up	1.72	-	3.564	pf
	Pull-down	1.712	-	3.552	pf

Table 55: SDIO TX VOH/VOL

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance Output High Voltage (50 Ohm)	Pull-up	1.508	-	1.886	V
PHY 1.8V Instance Output Low Voltage (50 Ohm)	Pull-down	0.09	-	0.112	V
PHY 1.8V Instance Output High Voltage (50 Ohm)	Pull-up	1.53	-	1.904	V
PHY 1.8V Instance Output Low Voltage (50 Ohm)	Pull-down	0.073	-	0.09	V

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.2V Instance Output High Voltage (50 Ohm)	Pull-up	0.968	-	1.231	V
PHY 1.2V Instance Output Low Voltage (50 Ohm)	Pull-down	0.087	-	0.111	V
PHY 1.2V Instance Output High Voltage (40 Ohm)	Pull-up	0.99	-	1.248	V
PHY 1.2V Instance Output Low Voltage (40 Ohm)	Pull-down	0.07	-	0.09	V

Table 56: SDIO TX Weak Pull-up/Pull-down

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance	Weak pull-up drive Strength =50 ohm	37.878	-	41.933	KOhm
PHY 1.8V Instance	Weak pull-down. drive strength =50 ohm	38.032	-	41.476	KOhm
PHY 1.2V Instance	Weak pull-up. drive strength = 50 ohm	39.185	-	45.752	KOhm
PHY 1.2V Instance	Weak pull-down. drive strength = 50 ohm	39.254	-	44.99	KOhm

Table 57: SDIO Transmitter Rise/Fall Times and Duty-Cycle

Parameter	Conditions	Min	Typ	Max	Unit
PHY 1.8V Instance Transmitter Rise/Fall Time Ratio	Drive strength = 50 Ohm. Slew rate control = fastest	0.822	-	1.263	ns/ns
PHY 1.2V Instance Transmitter Rise/Fall Time Ratio		0.849	-	1.014	ns/ns
PHY 1.8V Instance Transmitter Rise Time		0.482	-	0.971	ns
PHY 1.2V Instance Transmitter Rise Time		0.551	-	0.751	ns
PHY 1.8V Instance Transmitter Fall Time	Drive strength = 50 Ohm. Slew rate control = fastest	0.563	-	0.795	ns
PHY 1.2V Instance Transmitter Fall Time		0.578	-	0.836	ns
PHY 1.8V Instance Transmitter Duty Cycle	Drive strength = 50 Ohm. Slew rate control = fastest	47.327	-	54.171	%
PHY 1.2V Instance Transmitter Duty Cycle		48.752	-	54.175	%

Table 58: SDIO Delay Line Open-Loop

Parameter	Conditions	Min	Typ	Max	Unit
Delay Line Total Delay of Variable Delay Chain[3]	VDD_TOP = 0.8V, dl_step=0	5.355	-	9.269	ns
Delay Line Average Step Size[1]	VDD_TOP = 0.8V, dl_step=0	42.382	-	73.59	ps

[3] The Delay Line Open-Loop characterization test is intended to accurately measure the delay per each programmed delay line code. For this purpose, all the 128 delay codes have been swept and the respective step measured under nominal VT conditions. This characterization has been made exclusively on Delay Line 1. The values included in the tables refer to the highest respective code delay for all the samples.

4.11. RGMII Characteristics

Meeting the timing requirements of the RGMII interface, as described here, is crucial for proper operation when interfacing RGMII compliant devices.

Table 59: RGMII Timing Requirements

Parameter	Description	Min	Typical	Max	Unit
T_cyc[4]	Clock cycle duration	7.2	8	8.8	ns
Duty_G[5]	Duty cycle for Gigabit mode	45	50	55	%
Duty_T[2]	Duty cycle for 100T mode	40	50	60	%
TskewT[6]	Data to clock output skew at transmitter	-500	0	500	ps
TskewR[3]	Data to clock input skew at receiver	1	1.8	2.6	ns
Tr / Tf	Rise/Fall time 20-80%	-	-	0.75	ns

See the Hardware Integration Guide for further design guidelines.

[4] For 100Mbps, Tcyc will scale to 40ns+-4ns.

[5] The duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain on condition that the minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest transitioning speed.

[6] This applies to all versions of RGMII prior to 2.0. This implies that PC board design will require clocks to be routed with an additional trace delay of greater than 1.5ns and less than 2.0ns, to be added to the associated clock signal. For 100Mbps, the maximum value is unspecified.

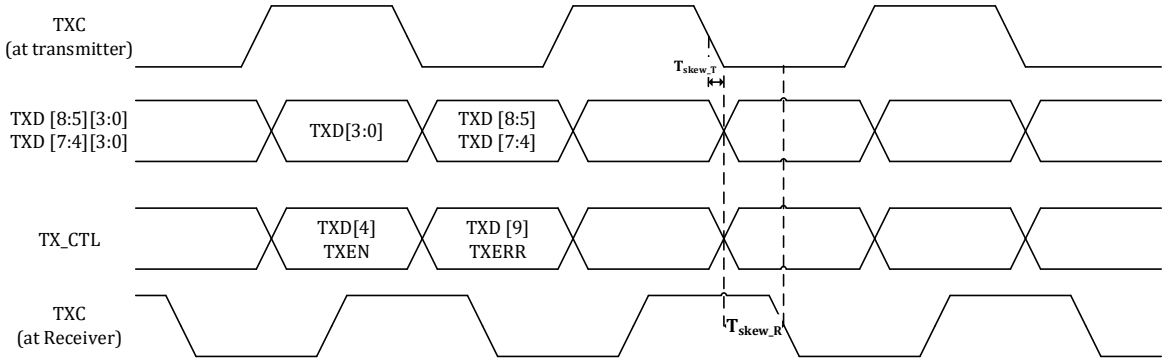

Figure 5: RGMII Multiplexing & Timing Diagram – TX signals

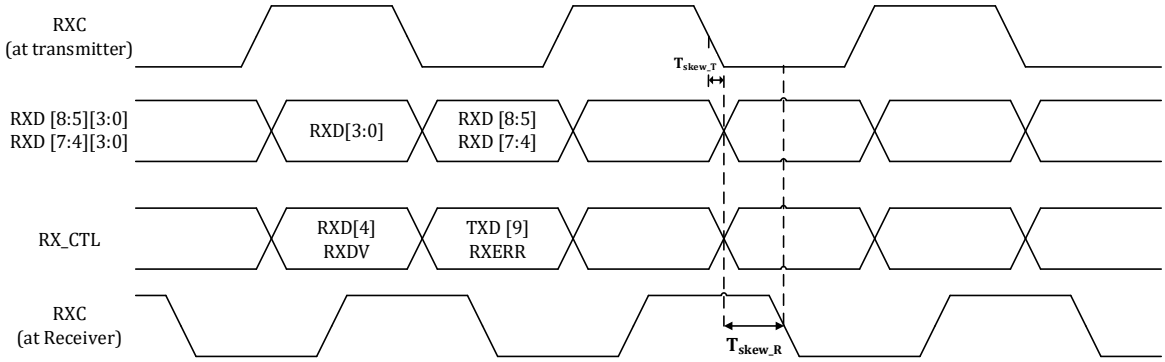

Figure 6: RGMII Multiplexing & Timing Diagram – RX Signals

4.12. Reset Characteristics

The NRESET pad should be driven by a Reset signal that meets the following requirements to provide Hailo-8L with a proper Reset pulse:

Rise and fall time (measured between 20% and 80% of VDDIO) < 5ns

NRESET assertion time (held low) >28us.

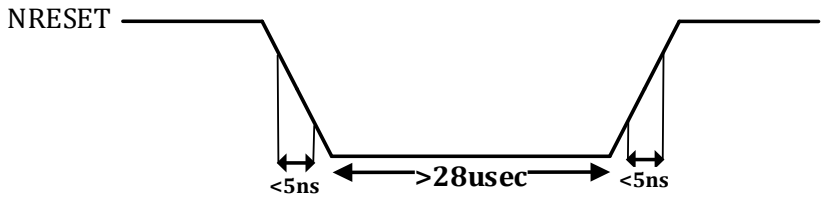

Figure 7: Reset Characteristics

5. Detailed Description

This section describes various system modes and usage scenarios, and provides detailed information on various Hailo-8L subsystems.

See Hailo SW documentation for further elaboration.

https://hailo.ai/developer-zone/documentation/

5.1. System Modes and Usage Scenarios

5.1.1 Hailo-8L as a Companion Device

In companion mode, depicted in Figure *8*, Hailo-8L is used to efficiently offload Neural Network workload from the host application processor. It receives inference data and returns insights. Hailo-8L typically communicates with the application processor over PCIe.

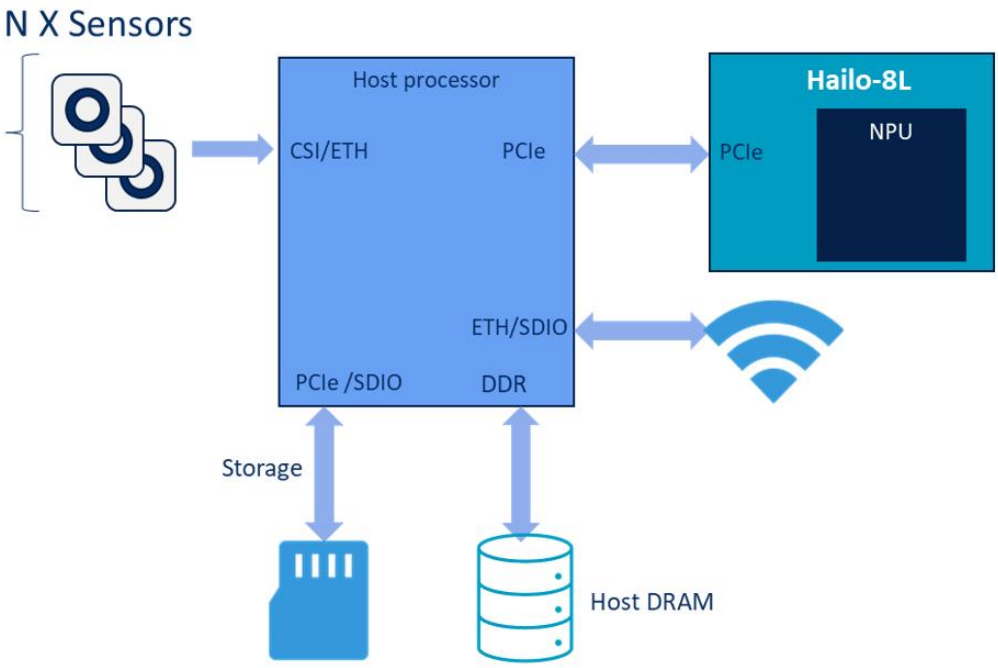

Figure 8: Hailo-8L as a Companion Device

5.2. Bootstraps

Hailo-8L has one functional boot strap, called BS_IO_SEL[0] (multiplexed with I2S_SDO), to enable the selection between two possible boot modes, PCIe when Boot Strap is pulled up, or Flash when Boot Strap is pulled down.

For PCIe boot, the SoC ROM handles the process with the host platform that runs the Hailo RT PCIe driver. Firmware is then fetched over the PCIe link to boot the device firmware.

For Flash boot, the SoC ROM fetches firmware from an on-board SPI flash device to complete the boot process.

The integrator can select the desired boot-flow according to dedicated system characteristics. See section 5.1 for further details.

See the Board Design Guidelines for further implementation and bootstrap connectivity guidelines.

5.3. NN Core

The Hailo-8L NN Core enables deployment of Deep NNs (DNNs) organized in four internal functional units called clusters.

Key features include:

- Up to 13 TOPs, 8-bit precision
- Four clusters that can be used to deploy multiple NNs
  - Compute, control and memory structure optimized for NN primitives
  - Fully programmable architecture to allow instantiation of all common NN building blocks, based on available software support delivered by the Hailo Dataflow Compiler (this includes, but is not limited to, layers such as convolution, pooling, fully connected and activation)
  - Support for advanced NN architecture with native support for split, concatenation and add layers
- Power modes
  - Normal (fully functional), doze, sleep and hibernate
  - Power shutdown can be executed at cluster level
- Up to 16 I/O channels to the NN core
- Configurable interconnect between NN core inputs, outputs and pre/post units
- 8/16-bit precision for both weights and activations, configurable at layer granularity
- 4-bit precision for weights, configurable at layer granularity
- NN pre/post processing hardware accelerator used to offload the following functions from host:
  - NMS engine
    - Up to 128k proposals post score threshold
    - One comparison per cycle, two NMS engines may be aggregated to offer double throughput
    - Configurable intersection over union and score threshold with up to 16 threshold classes

- Bilinear interpolation engine
  - Streaming bilinear up to 8K resolution
  - Crop and Resize operations
- Reshape engine
  - Translates standardized formats to Hailo proprietary format and vice versa
  - Offloads advanced tensor reshape operations
- Softmax engine

5.4. High Bandwidth Interfaces

5.4.1 Ethernet

The Hailo-8L provides an IEEE-802.3-2002-compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry-standard Reduced Gigabit Media-Independent Interface (RGMII) or Reduced Media-Independent Interface (RMII). The Hailo-8L requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The MAC integrates a DMA, 1588 functionality, TSN/AVB and PCS for automotive applications.

Key features include:

- 100, 1000 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers from the dedicated SRAM throughout the
- Tagged MAC frame support (VLAN support)
- TCP/IP and UDP offload
- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast addresses (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are each 2 Kbytes (4 Kbytes total)
- Hardware Precision Time Protocol (PTP) in accordance with IEEE 1588

2008 (PTP V2) with the time stamp comparator connected to the TIM2 input

- Time Stamping Unit (TSU) supports a 102-bit timer
- Credit Based Shaping - TSN, 802.1Qav
- Enhanced Scheduled Traffic - TSN, 802.1Qbv
- Frame Replication and Elimination for Reliability - TSN, 802.1CB

5.4.2 PCI Express (PCIe)

Hailo-8L provides a 4-lane PCI-SIG compliant PCIe gen 3 PHY and controller, enabling it to be integrated as a PCIe endpoint. It integrates a dedicated scatter-gather DMA for efficient memory mapped transactions.

Key features include:

- Up to 32 Gbps bi-directional throughput
  - X1/X2/X4 lanes
  - Supports link rate of 2.5, 5.0, 8.0 GT/s per lane
- Lane reversal support
- L1 PM Substates with CLKREQ
- Latency Tolerance Reporting (LTR)
- Single Physical Function
- Single Virtual Function
- Single Virtual Channel (VC)
- Up to $2.5\mu s$ read latency from host memory in full BW
- Support also Device low power modes - D0, D3
- Up to 512 Byte maximum payload size
- Advanced Error Reporting (AER) support
- ECRC generation and check support
- MSI (up to 32) and INT message support
- Internal DMA (32 channels)
- Dynamic Scatter-Gather DMA configuration, such as interrupt generation or start and end conditions for each specific SG page.
- Diagram

- Core Context switch over PCIe – configuration and data
- FW boot from PCIe
- Control protocol
- Up to 16 dedicated RX and TX channels with low latency streaming FIFOs
- Supports out of order TLP arrival with integrated re-order buffer
- Retransmit buffer of 2KB
- Receive buffer of 2KB
- Up to 32 outstanding read requests
- Integrated safety mechanisms that detect transient and permanent faults in data and control paths
- Full support for link power management including ASPM L0, ASPM L1, L1.1 andL1.2

5.4.3 MIPI CSI

Hailo-8L integrates two MIPI CSI-RX v1.3 controllers and DPHY v1.2 with four lanes per DPHY, as well as two MIPI CSI-TX v1.3 controllers that are also equipped with DPHY v1.2 with four lanes per DPHY. This allows easy interfacing to sensors, displays and other SoCs. Each interface supports up to 10 Gbps throughput, for a total streaming throughput of 40 Gbps. The MIPI interfaces double as chip-to-chip interconnect, allowing a seamless expansion to the Hailo-8L NN core.

5.4.3.1 CSI-RX

The CSI-RX subsystem allows efficient streaming of pixel data to the Hailo-8L NN core. The CSI-RX is responsible for handling a CSI-2 protocol-based camera sensor or sensor data stream, and for unpacking the payload data and forwarding it to the pixel stream interfaces. The CSI-RX allows the selection of multiple independent input streams and supports the control of the destination for each stream (ISP or NN core).

Key features include:

- Operation modes:
  - High-Speed (HS): maximum up to 2.5Gbps per lane
  - Escape mode

        - Remote triggers
        - LP-DT: up to 10Mbps
        - ULPS mode
- Supports up to four streams for each interface over distinct virtual channels and for different data types, which may be forwarded to different destinations in the NN-Core or to the ISP.
- Supports the following data types:
    - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
    - RGB444, RGB555, RGB565, RGB666, RGB888
    - YUV8, YUV10

5.4.3.2 CSI-TX

The CSI-TX subsystem can process pixel data from a source and generate the CSI-2 data packets for short and long types. The CSI-TX also performs ECC/CRC generation and provides data support for frame and line counter packets.

The CSI-TX supports virtual channel and data type selection as well as all primary data types defined by MIPI CSI-2.

5.4.3.3 DSI-TX

The DSI-TX subsystem is intended to interface NN Core output data with a DSI compliant video mode display by embedding a DSI controller. This controller can be multiplexed by static configuration to feed data into the DPHY instead of using the CSI-TX controller.

5.4.4 Camera Parallel LVCMOS Interface

Hailo-8L integrates a camera parallel LVCMOS interface port of up to 24 bits wide at up to 100MHz, that connects to the video data bus from an image sensor.

5.4.5 Universal Serial Bus (USB)

Hailo-8L contains an embedded USB full-speed device peripheral with integrated transceivers. It is compliant with the USB 2.0 specification, has software-configurable endpoint settings, and supports suspend/resume.

It requires a dedicated 48 MHz clock that is generated by a PLL connected to the oscillator.

Key features include:

- Combined RX and TX FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the Session Request Protocol (SRP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support

5.4.6 SDIO

SDI IF Key features include:

- Compliant with
  - eMMC 5.1 (no backward support of HS400)
  - SD6.0 1.8 V low voltage signaling (LVS) host
  - JESD8-7a (1.2 V/1.8 V)
- Six I/O signals – eMMC (4-bit data) operation
- Three delay lines
- Glitch-free, power-sequence free operations
- Hi-Z I/O pad power-up default state
- Clock speeds up to 334MHz and data rate up to 667 MB/s
- SPI operation
- Open drain applications
- ESD protection for I/O signals and for 1.8 V/1.2 V power supply
- eMMC (1.8 V/1.2 V) PHY has four functional receivers per I/O pad:
  - 1.8-V Schmitt trigger
  - 1.2-V Schmitt trigger
  - 1.8-V comparator receiver
  - 1.2-V comparator receiver
- Power supply requirements
  - 1.8 V I/O signaling: 1.8 V and a low-voltage digital power supply
  - 1.2 V I/O signaling: 1.2 V and a low-voltage digital power supply

5.5. Low Bandwidth Interfaces

5.5.1 Inter-Integrated Circuit (I2C)

Hailo-8L integrates up to four I2C interfaces that may double as SCCB (Serial Camera Control Bus) interface to allow the device to be the Master that controls attached sensors.

Key features include:

- Each interface can be Master or Slave
- High and low-speed support
- Bandwidth
  - Fast mode, up to 400Kbps
  - High-speed mode, up to 3.4Mb/s

5.5.2 Quad Serial Peripheral Interface (QSPI)

Hailo-8L integrates a single QSPI to work with external Flash devices.

Key support includes:

- Up to two external Chip Selects (CS)
- Execute in Place (XIP) for external Flash device
- Up to 1Gb of external memory space
- SPI (x1), DSPI (x2) and QSPI (x4) modes
- DDR and SDR modes
- Boot from external Flash
- External device frequency of up to 50MHz

5.5.3 Universal Asynchronous Receiver Transmitter (UART)

Hailo-8L integrates up to four simple UART interfaces (no flow control signal support).

Key features include:

- 8-bit communication with parity and fixed at one stop bit

- Baud rate up to 2Mbaud

5.5.4 Inter-IC Sound (I2S) Input

Hailo-8L integrates a single I2S input interface to process digital audio inputs. The I2S bus is a simple three-wire serial bus protocol. Since it only handles the transfer of audio data, control and sub-coding signals must be transferred separately using a different bus protocol, such as I2C.

Key features include:

- Audio resolution of 12,16,20,24 and 32 bits
- External SCLK gating and enable signals

5.6. MCU

Hailo-8L integrates two Cortex M4 cores with a memory subsystem.

5.6.1 Cortex M4 Cores

Each of the two Cortex M4 MCU cores is equipped with a Memory Protection Unit (MPU) and a Floating Point Accelerator Unit (FPU) engine.

The cores communicate with each other through mailbox and semaphore modules.

Key features include:

- MPU
- FPU
- Embedded Trace Microcell (ETM)
- Support for up to 200MHz frequency
- ARM core based on ARMv7 architecture
- Boot from external Flash or PCIe by external boot strap pins

5.6.2 MCU Memory

The MCU memory is accessible by both cores.

Key features include:

- Six data/code memory ports
- Total of 640KB SRAM memory for code and data with ECC
- 256KB ROM
- Up to 1Gb memory space for external Flash devices

5.6.3 Flash System

Hailo-8L can access external Flash devices either directly through the QSPI controller or through the Flash caching system. The Flash caching system can cache read only instruction memory up to 512B.

Key features include:

- Two-way 512B cache
- Up to 4MB of configurable memory cache
- Configurable fetching
- Configurable ECC on the cached data

5.7. Vision Subsystem

5.7.1 Image Signal Processing (ISP)

Hailo-8L integrates an ISP unit. It can be used to directly connect a CMOS sensor to the SoC.

Key features include:

- Complete and fully configurable ISP pipeline
- Input formats:
  - RAW8, RAW10, RAW12, RAW14
- Output formats:
  - RGB888, YUV422
- 4k resolution: 40 fps videos

- 1080p resolution: 120 fps video
- Up to 4096h x 4096v resolution
- Optimized for low light environment applications
- Video statistics support Auto Focus, Auto White Balance, Auto Exposure
- On-the-fly defective pixel correction
- 10-bit Bayer channel gain supports up to x7.99
- Linear algebra for input pixel level adjustment
- Gb/Gr correction with maximum correction tolerance Gb/Gr rate of 12.5%
- 2D lens-shading correction (8x6)
  - Normal R/Gb/Gr/B channel shading correction
  - Color stain correction
- High resolution RGB interpolation: ES/Hue-Med/Average/Non-Direction based hybrid type algorithm
- Color correction matrix (3x3)
- Bayer gamma correction (19 points)
- High-performance noise reduction for low light environment: Bayer/RGB/YC domain
- High-resolution sharpness control: Multi-sharp filter and individual sharp gain control
- Color enhancement: hue, saturation, Delta-L control (RGBCMY)
- Auto Exposure: supports 16x16 luminance weight window and pixel weighting
- Auto white balance: RGB-based feed-forward method Tone mapping: multi-band scheme using liner transformation as multi-slope
- Auto Focus (AF): 2-type 6-region AF value return

5.7.2 H.264 Encoder

Hailo-8L integrates an advanced ITU-T H.264 high-profile compliant encoder, constrained to All-Intra encoding schemes.

This encoder can also serve other purposes. It can, for instance, compress raw data from a sensor, or processed data (insights).

Key features include:

- Max resolution: 1080x1920P.
- Full compliance to the ITU-T H.264 and ISO/IEC 14496-10 specification
- High 10 intra, High 4:2:2 intra profiles encoding
- All-Intra Constraint Baseline or Main profiles encoding
- 8 and 10 bit per component color depth encoding
- 4:2:2 YCbCr digital video input, interleaved scan
- Level up to 5.2
- ITU-T H.264 Annex B compliant NAL byte stream output
- MCU-less, complete and autonomous operation
- True H.264 compression efficiency and perceptually optimized image quality
- Psychovisual optimizations for better viewer experience
- High throughput implementation
- Sustained 2.4 (in 4:2:0) or 2.7 (in 4:2:2) clock cycles per pixel, worst case processing rate
- Advanced Intra prediction
  - All four Intra 16x16 prediction modes
  - All four Intra Chroma prediction modes
  - All nine Intra 4x4 prediction modes
- CABAC or CAVLC entropy coding

5.8. System Peripherals

5.8.1 Temperature Sensor

The Hailo-8L temperature sensor is a high-precision low-power junction temperature sensor embedded in the chip. Typical temperature sensor applications may include clock speed optimization, power management and thermal management.

Key features include:

- +/- 3.0°C accuracy
- 12-bit resolution (10-bit and 8-bit alternatives at lower accuracy), parallel or serial
- Signature response on demand
- Analog fault coverage

5.8.2 Voltage Monitor

Hailo-8L embeds two on-chip voltage monitors that are low-power self-contained blocks designed to monitor differential voltage levels within the core logic voltage domains.

Key features include:

- 16 monitoring points
- +/-1% accuracy
- Up to 14-bit resolution
- Digital interface
- Signature response on demand
- Analog fault coverage

5.8.3 Direct Memory Access (DMA)

The Hailo-8L integrates two DMA modules to easily move and copy data.

Key features include:

- Four configurable channels per DMA
- Support for advanced HW LLP and scatter-gather features

- Transfer capabilities: peripheral to memory, memory to peripheral, memory to memory and peripheral to peripheral
- Supports hardware handshake interfaces for I2C module

5.8.4 General-Purpose Input Output (GPIO)

Hailo-8L integrates up to 32 GPIOs. Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as a peripheral alternate function. Most of the GPIO pins are shared with digital alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/O registers.

5.8.5 Timer

Hailo-8L integrates four timers that can be programmed through the GPIO interfaces.

Key features include:

- 32-bit counter
- Clock from external clock input or internal clock
- Interrupt output to MCU system

All timer counters can be frozen in debug mode.

5.8.6 Watchdog

Hailo-8L integrates two watchdogs to monitor the MCUs in the system.

Key features include:

- 32-bit counter
- Configurable Interrupt threshold
- Configurable system reset threshold

5.8.7 Mailbox

Hailo-8L integrates eight mailboxes to transfer information between MCU cores.

Each mailbox has one data register to pass pointers to data between MCUs. After one MCU successfully writes data to the mailbox, the other MCU receives an interrupt.

5.8.8 Semaphore

Hailo-8L integrates eight semaphore units to control access to a common resource.

5.8.9 CRC Hardware Offload Engine

Hailo-8L includes an internal CRC generator and calculator to accelerate CRC calculation on data and control.

Key features include:

- Generate and check CRC
- CRC32/CRC16 polynomials
- CRC calculation on 32/16-bit data width

5.9. Security System

5.9.1 Features

Hailo-8L implements a wide range of security features for typical target applications.

The security subsystem includes:

- Secure boot
- Complete Life Cycle Management (LCM)
- User-provided non-volatile hash (enabling RoT behavior)
- User access to hardware-accelerated cryptographic algorithms
- Secure debug access according to the product life cycle
- Inner configurable firewall to block unexpected access to secure system regions

5.9.2 Lifecycle Management

Hailo-8L has lifecycle support for Hailo's production and integrator development processes, as well as for product deployment and Return Merchandise Authorization (RMA).

The debug interface lock depends on the lifecycle state.

5.9.3 True Random Number Generator (TRNG)

Hailo-8L contains a TRNG that delivers 32-bit random numbers produced by an integrated analog circuit.

The TRNG is fully compliant with FIPS 140-2.

5.9.4 Cryptographic Accelerator

Hailo-8L contains a hardware authentication engine and an encryption/decryption engine that support the following algorithms:

- AES (128,192,256)
- SHA1/2
- RSA (2048,3072,4096)

The cryptographic accelerator can be used for secure boot, data-at-rest and data-in-transit.

5.9.5 Trusted Execution Environment (TEE)

The Hailo-8L TEE monitors and controls incoming and outgoing traffic inside the chip based on predetermined security rules set during software boot.

The Hailo-8Lsecurity system has a configurable hardware firewall. It protects access to peripherals inside the chip, internal SRAMs and external memory regions.

