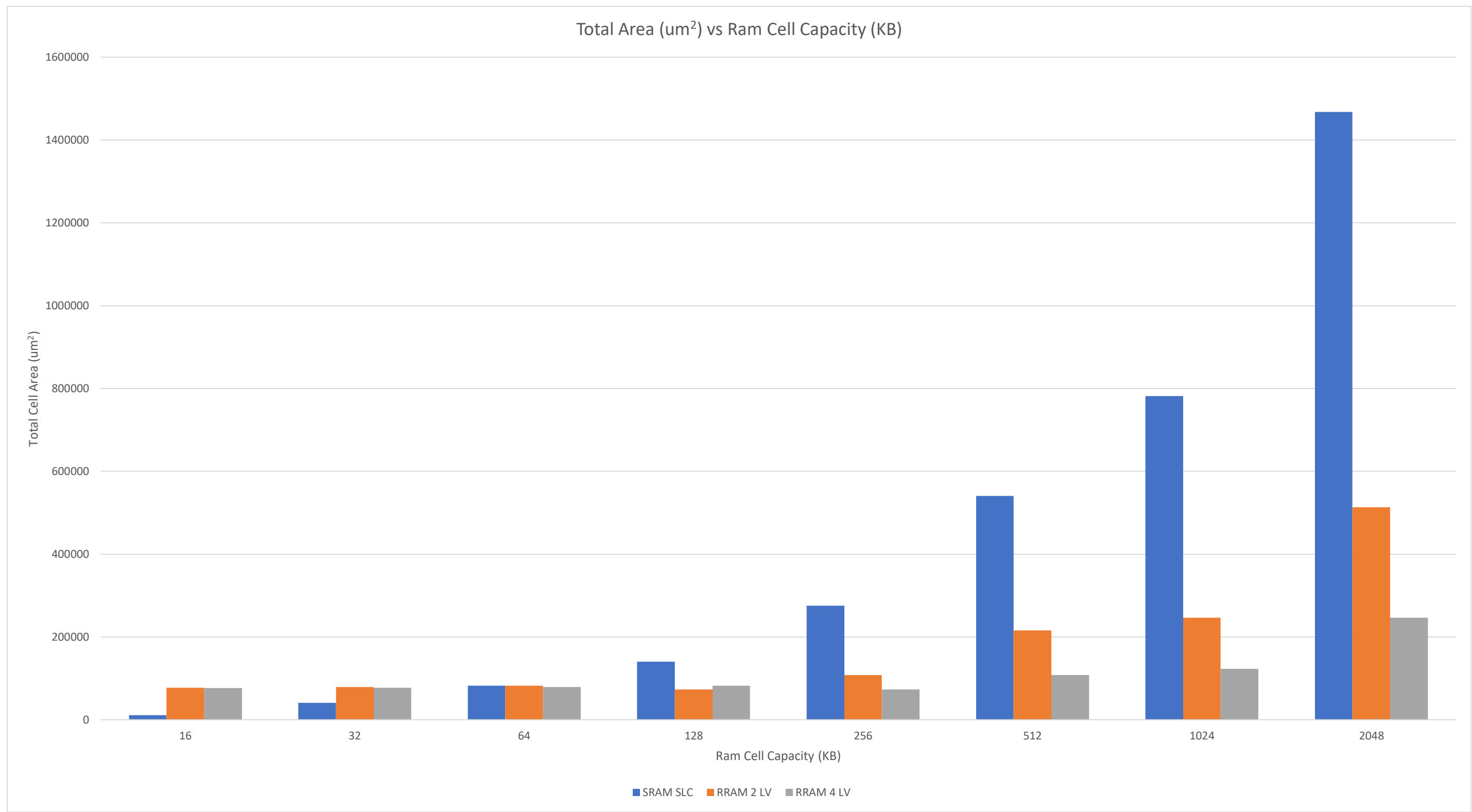
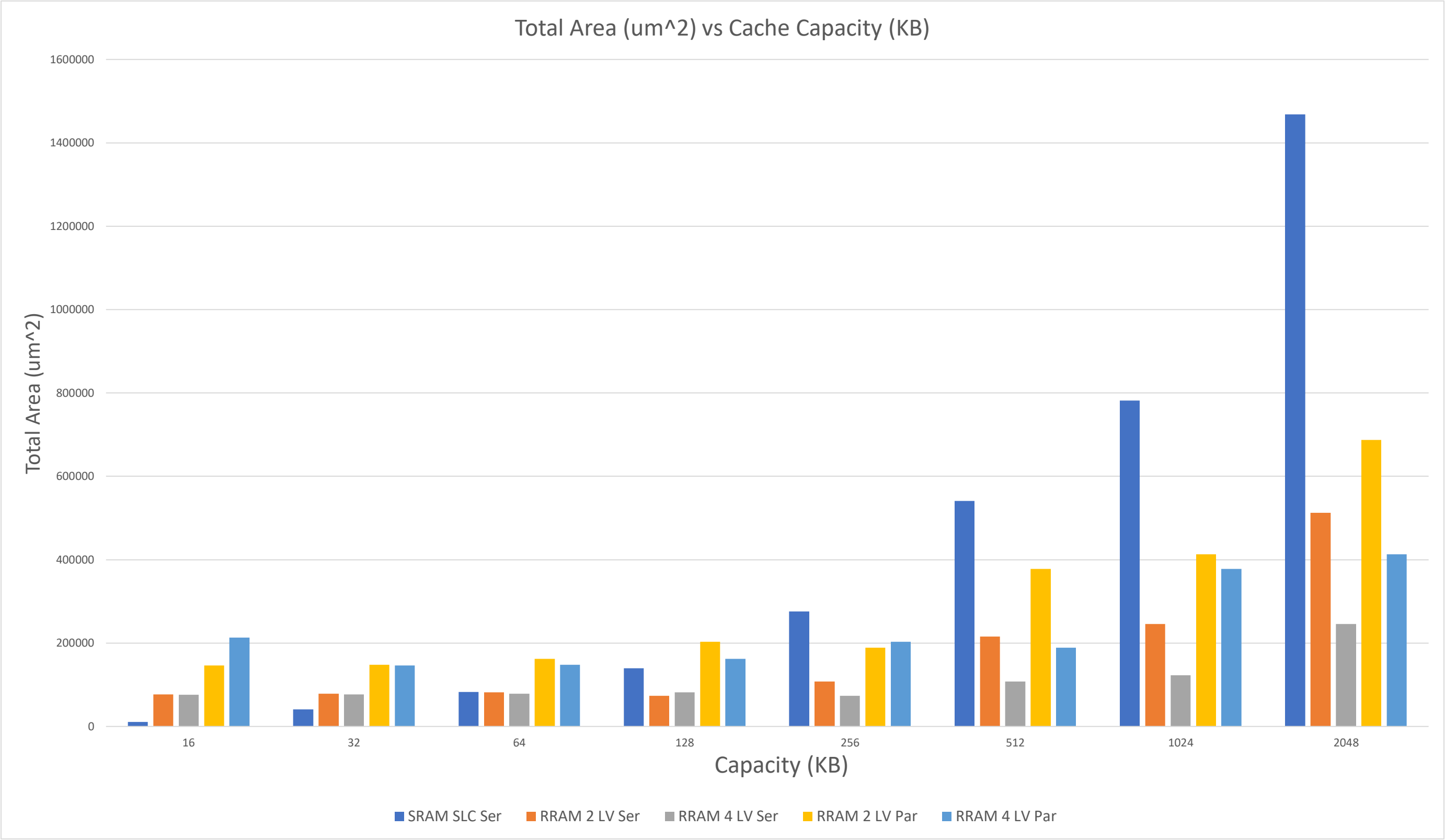
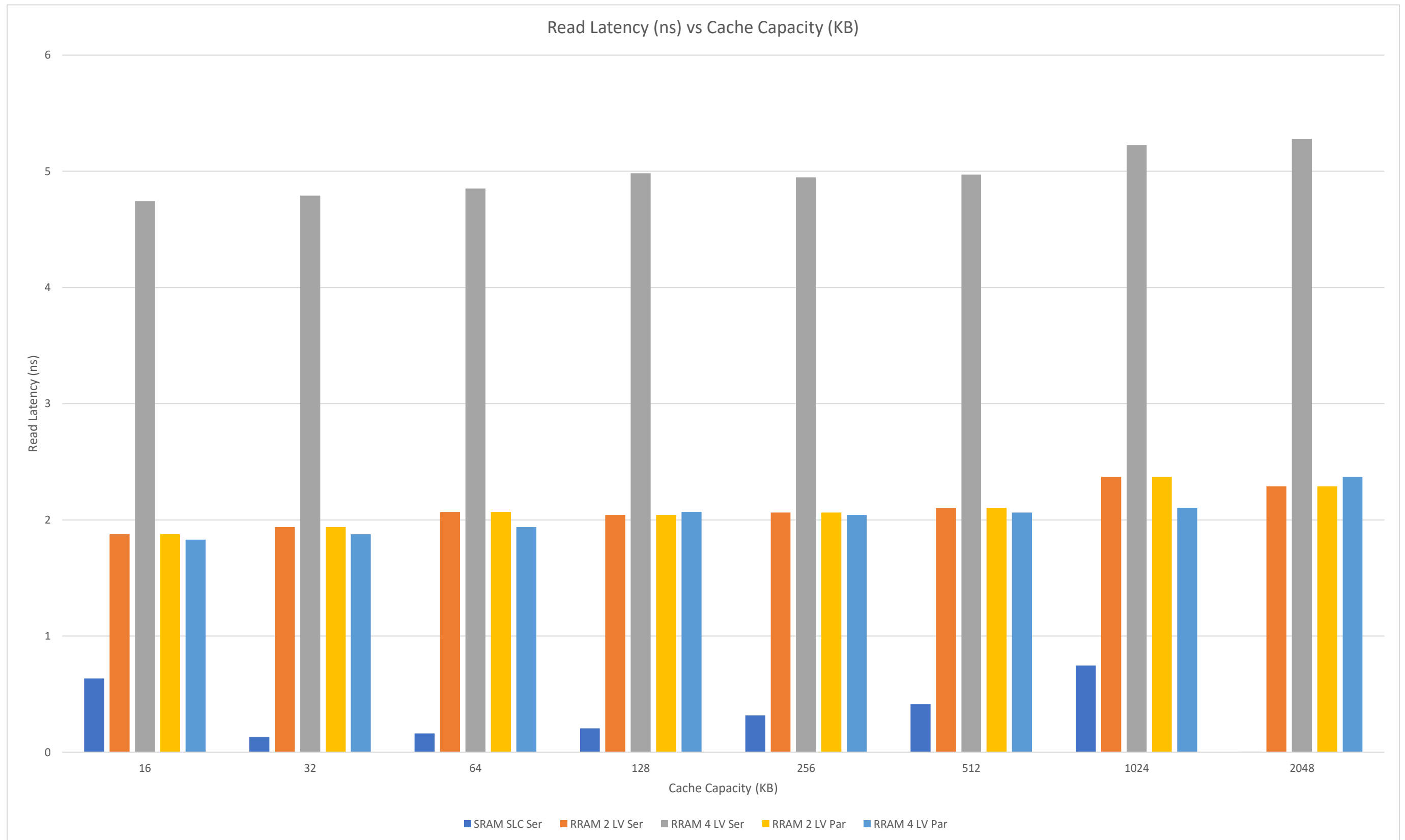


Part 1  
Run iso-capacity simulations for SRAM, SLC RRAM, and MLC RRAM macros by choosing a set of appropriate target capacities. Comment on the results in terms of overall array area.







## Part 1

As expected, the area of MLC cells increases at a much slower rate than the SLC cells. The RRAM 4 levels configuration has smaller area than the 2 levels parallel configuration which shows the benefits of scaling and num bits per cell + level counts.

## Part 2

It makes sense that the RRAM MLC is more dense in serial than parallel as parallel area increases much more due to additional sense amps. On the contrary, RRAM MLC's show that the parallel configuration is much faster for latency as expected. The SLC configurations don't differ much but I was impressed with the low latency of the SRAM cells.

Model Assumptions:

```
# Sample configuration for SRAM cache

-DesignTarget: cache
-CacheAccessMode: Sequential
-OptimizationTarget: ReadEDP
-EnablePruning: Yes

-ProcessNode: 22
-Capacity (KB): 16-2048
-WordWidth (bit): 512
-Associativity (for cache only): 16

-DeviceRoadmap: LSTP
-LocalWireType: LocalAggressive
-LocalWireRepeaterType: RepeatedNone

-LocalWireUseLowSwing: No
-GlobalWireType: GlobalAggressive
-GlobalWireRepeaterType: RepeatedNone
-GlobalWireUseLowSwing: No

-Routing: H-tree
-InternalSensing: true
-MemoryCellInputFile: ./cell_defs/RRAM.cell or ./cell_defs/SRAM.cell

-Temperature (K): 350
-BufferDesignOptimization: latency
-UseCactiAssumption: Yes
```