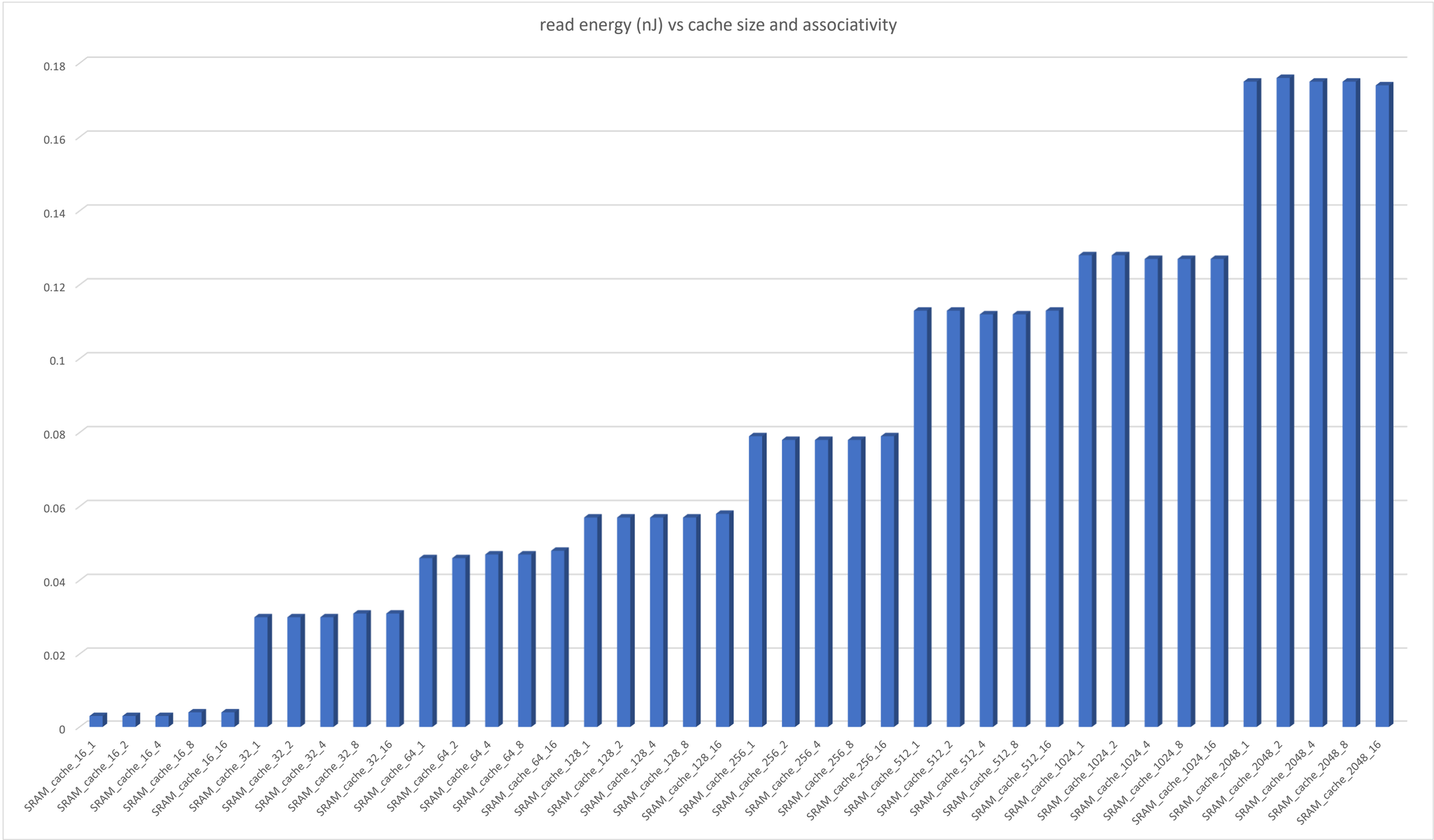
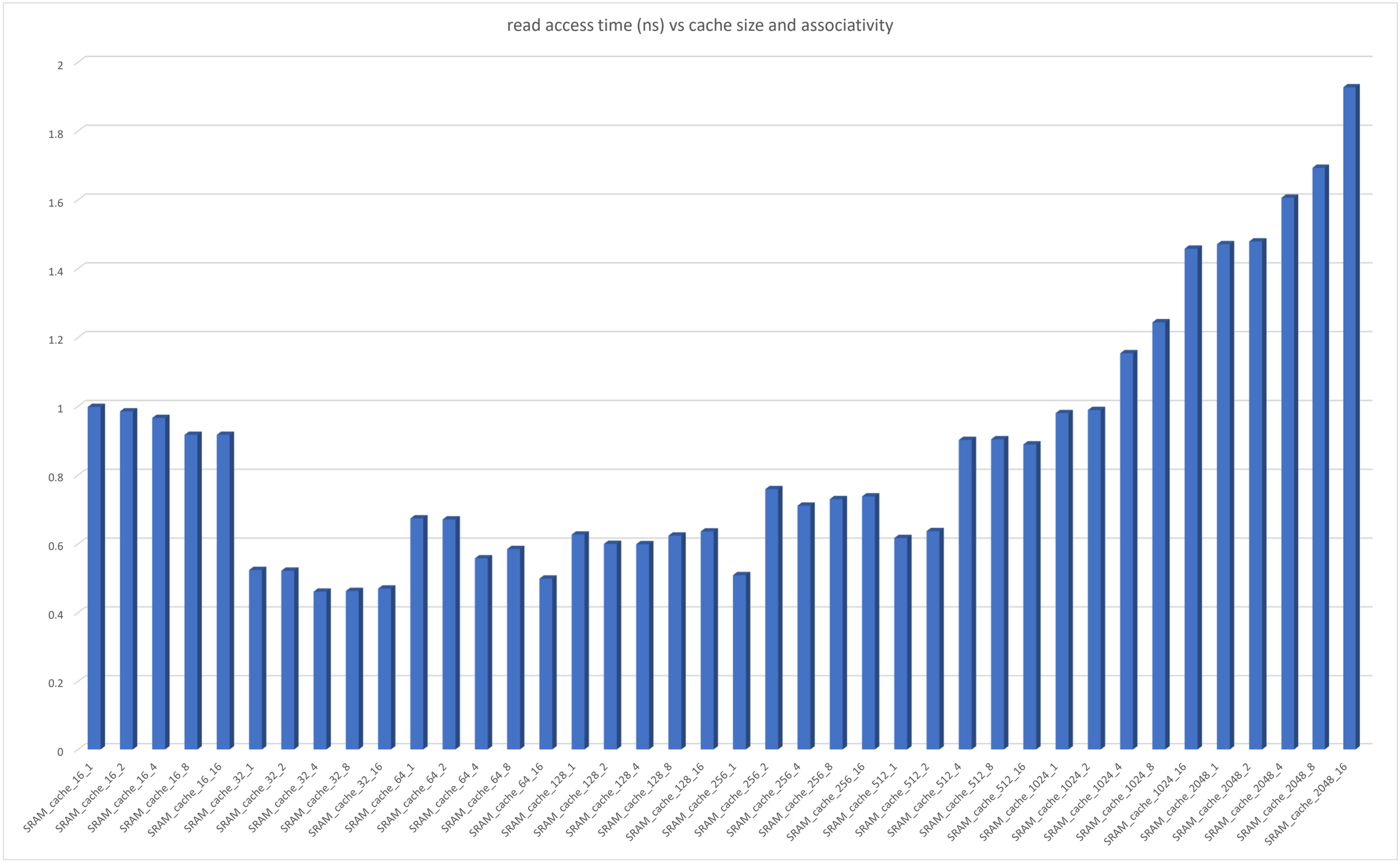
Morgan Rockett

EECE0193 HW2

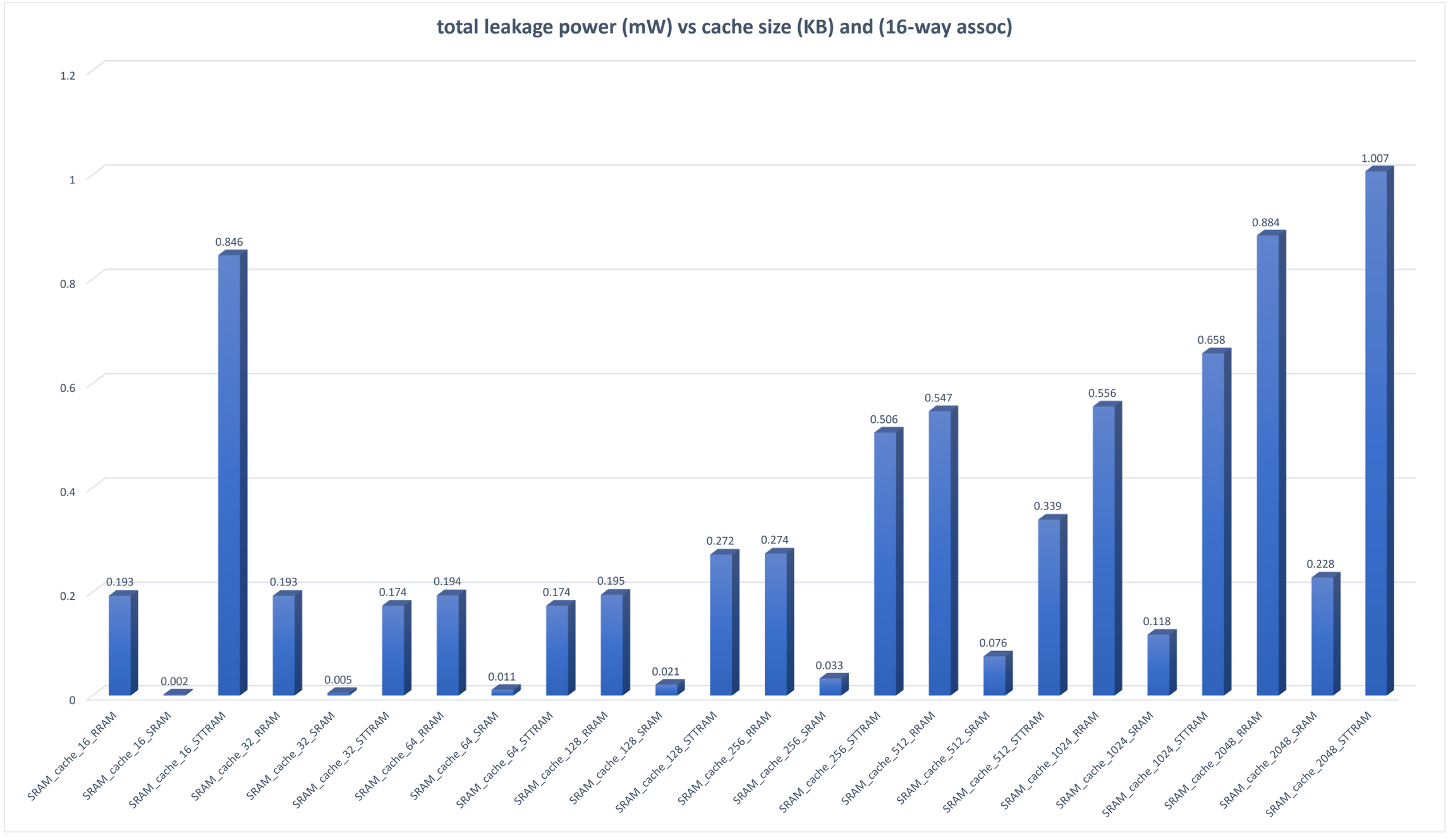
Part 1



Part 1


read access time (ns) vs cache size and associativity
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
SRAM_cache_16_1
SRAM_cache_16_2
SRAM_cache_16_4
SRAM_cache_16_8
SRAM_cache_16_16
SRAM_cache_32_1
SRAM_cache_32_2
SRAM_cache_32_4
SRAM_cache_32_8
SRAM_cache_32_16
SRAM_cache_64_1
SRAM_cache_64_2
SRAM_cache_64_4
SRAM_cache_64_8
SRAM_cache_64_16
SRAM_cache_128_1
SRAM_cache_128_2
SRAM_cache_128_4
SRAM_cache_128_8
SRAM_cache_128_16
SRAM_cache_256_1
SRAM_cache_256_2
SRAM_cache_256_4
SRAM_cache_256_8
SRAM_cache_256_16
SRAM_cache_512_1
SRAM_cache_512_2
SRAM_cache_512_4
SRAM_cache_512_8
SRAM_cache_512_16
SRAM_cache_1024_1
SRAM_cache_1024_2
SRAM_cache_1024_4
SRAM_cache_1024_8
SRAM_cache_1024_16
SRAM_cache_2048_1
SRAM_cache_2048_2
SRAM_cache_2048_4
SRAM_cache_2048_8
SRAM_cache_2048_16

Part 2


total leakage power (mW) vs cache size (KB) and (16-way assoc)
1.2
1
0.8
0.6
0.4
0.2
0
0.193
0.002
0.846
0.193
0.005
0.174
0.194
0.011
0.174
0.195
0.021
0.272
0.274
0.033
0.506
0.547
0.076
0.339
0.556
0.118
0.658
0.884
0.228
1.007
SRAM_cache_16_RRAM
SRAM_cache_16_SRAM
SRAM_cache_16_STTRAM
SRAM_cache_32_RRAM
SRAM_cache_32_SRAM
SRAM_cache_32_STTRAM
SRAM_cache_64_RRAM
SRAM_cache_64_SRAM
SRAM_cache_64_STTRAM
SRAM_cache_128_RRAM
SRAM_cache_128_SRAM
SRAM_cache_128_STTRAM
SRAM_cache_256_RRAM
SRAM_cache_256_SRAM
SRAM_cache_256_STTRAM
SRAM_cache_512_RRAM
SRAM_cache_512_SRAM
SRAM_cache_512_STTRAM
SRAM_cache_1024_RRAM
SRAM_cache_1024_SRAM
SRAM_cache_1024_STTRAM
SRAM_cache_2048_RRAM
SRAM_cache_2048_SRAM
SRAM_cache_2048_STTRAM

Part 3

1) Based on the cell definitions used in your simulations, what area reduction would you expect to achieve by replacing a CMOS SRAM memory array with a RRAM crossbar array?

Based on the slides, I would expect the equivalent of a $8F^2$ drop to $4F^2$.

2) Plot the total memory area for the two technologies as a function of the memory size ("Capacity"). Are the results consistent with your prediction? What trends are you able to observe from your simulation results?

I expected to see a difference in total cell area as cache size changes. Perhaps NVSim is off or my data is. I did not notice issues in parts 1 and 2. The trends question leads me to believe I should be seeing some sort of correlation.

3) Can you identify any aspect in the memory architecture design that may cause any unexpected result?

Simulation glitch? The spacing between contacts could be variable and theoretically cause differences in expected area vs typical if NVSim doesn't use comparable benchmarks to the slides.