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EECE0193 HW2

Part 1

Part 1

Part 2

Part 3

1) Based on the cell definitions used in your simulations, what area reduction would you expect to achieve by replacing a CMOS SRAM memory array with a RRAM crossbar array?

Based on the slides, I would expect the equivalent of a 8F2 drop to 4F2.

2) Plot the total memory area for the two technologies as a function of the memory size (“Capacity”). Are the results consistent with your prediction? What trends are you able to observe from your simulation results?

I expected to see a difference in total cell area as cache size changes. Perhaps NVSim is off or my data is. I did not notice issues in parts 1 and 2. The trends question leads me to believe I should be seeing some sort of

correlation.

3) Can you identify any aspect in the memory architecture design that may cause any unexpected result?

Simulation glitch? The spacing between contacts could be variable and theoretically cause differences in expected area vs typical if NVSim doesn’t use comparable benchmarks to the slides.