Morgan Rockett

EECE0193: Emerging Memory Technologies: HW3

Part 1

Capacity (KB)

16, 32, 64, 128, 256, 512, 1024, 2048

2 levels – 1 bit fine for SLC

4 levels – 2 bits fine for MLC

Focus on just data array (not tag)

1.3

-MemoryCellInputFile: ./cell\_defs/RRAM.cell isMLC F

-MemoryCellInputFile: ./cell\_defs/RRAM.cell isMLC T

-MemoryCellInputFile: ./cell\_defs/SRAM.cell

Part 1 Configs

Cell Capacities LC LV count

RRAM: {16, 32, 64, 128, 256, 512, 1024, 2048} SLC 2 levels

RRAM: {16, 32, 64, 128, 256, 512, 1024, 2048} MLC 4 levels

SRAM: {16, 32, 64, 128, 256, 512, 1024, 2048}

Part 2