B. VISHNU VARDHAN

7569906303 | vishnuvardhan1117kv@gmail.com | www.linkedin.com/in/vishnu1117

Career Objective

As a trained fresher in Advanced VLSI Design and Verification, I have hands-on experience in RTL design using Verilog, IP integration, and verification using System Verilog and UVM. My training has equipped me with a strong understanding of verification planning, coverage analysis, and debugging RTL simulations. I am eager to apply my problem-solving skills, technical knowledge, and ability to collaborate effectively in a professional environment.

Professional Training

Advanced VLSI Design and Verification, Maven Silicon VLSI Training Institute Bangalore. **May 2024 - Present**

Education

Jawaharlal Nehru Technological University Anantapur (2020-2024)
B. Tech (E.C.E) **CGPA: 7.33**

Sri Siddartha Junior College (2018-2020)
Higher Secondary Education | BIEAP **CGPA: 9.75**

Jawahar Navodaya Vidyalaya Chittoor (2013-2018)
Secondary School Education | CBSE **Percentage: 72%**

VLSI Domain Skills

HDL, HVL **:** Verilog, SystemVerilog.
Verification Methodologies: Constraint Random Coverage Driven Verification, Assertion Based Verification-SVA.
TB Methodology **:** Universal Verification Methodology.
EDA Tools **:** QuestaSim, ModelSim, Quartus Prime, Synopsys- VCS.
Core Skills **:** Digital Electronics, Functional Coverage, Code Coverage, Synthesis, STA Basics.

Projects

AHB to APB Bridge Verification using UVM

- Designed a UVM testbench including UVM agents, monitors, drivers, and scoreboards for functional verification.
- Created directed and constrained-random test cases to validate protocol compliance and corner cases.
- Implemented functional coverage and assertions using SystemVerilog to ensure thorough verification.
- Used QuestaSim/VCS for simulation and debugging**.**
- Achieved 100% functional and code coverage, ensuring robust verification of the bridge.

ROUTER 1X3 Design and Verification

- Designed a Router 1x3 using Verilog, including key blocks such as FIFO, Synchronizer, FSM, and Registers.
- Developed and verified the design using UVM methodology, creating a comprehensive test bench to ensure functionality and reliability.
- Performed functional verification with diverse packet sizes small, medium, and large transactions to validate routing and data integrity under different traffic conditions.

4096X64 Dual-Port RAM DESIGN AND VERIFICATION

- The project involves designing a 4096x64 Random Access Memory (RAM) using Register Transfer Level (RTL) coding in Verilog.
- A comprehensive testbench is written in System Verilog to verify the functionality and performance of the design.