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# Fabrication of quantum dots in undoped Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> heterostructures using a single metal-gate layer

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Enhancement-mode Si/SiGe electron quantum dots have been pursued extensively by many groups for their potential in quantum computing. Most of the reported dot designs utilize multiple metal-gate layers and use Si/SiGe heterostructures with Ge concentration close to 30%. Here, we report the fabrication and low-temperature characterization of quantum dots in the Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> heterostructures using only one metal-gate layer. We find that the threshold voltage of a channel narrower than 1  $\mu\text{m}$  increases as the width decreases. The higher threshold can be attributed to the combination of quantum confinement and disorder. We also find that the lower Ge ratio used here leads to a narrower operational gate bias range. The higher threshold combined with the limited gate bias range constrains the device design of lithographic quantum dots. We incorporate such considerations in our device design and demonstrate a quantum dot that can be tuned from a single dot to a double dot. The device uses only a single metal-gate layer, greatly simplifying device design and fabrication. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4961889>]

Electron spins are one of the most promising candidates for implementing solid-state qubits.<sup>1</sup> Si, in particular, is a widely pursued host material for spin qubits, due to its long coherence times<sup>2</sup> resulting from its weak spin-orbit interaction and the possibility of obtaining isotopically pure <sup>28</sup>Si which has zero nuclear spin.<sup>3</sup> In Si, manipulation of individual electron spins can be achieved in electrostatically defined quantum dots in addition to donor-bound electrons as proposed by Kane.<sup>4</sup> A typical starting platform for making quantum dots is a two-dimensional electron gas (2DEG), which either resides at the Si/SiO<sub>2</sub> interface in the case of Si metal-oxide-semiconductor field-effect transistors (MOSFETs) or in a strained Si quantum well in the case of Si/SiGe heterostructures. A Si/SiGe heterostructure has epitaxial interfaces, which are much less disordered than amorphous SiO<sub>2</sub> on Si and result in much higher electron mobilities. For Si/SiGe heterostructures, one can either use modulation-doping<sup>5</sup> and fabricate gates to locally deplete electrons, or employ a MOSFET-like enhancement-mode architecture<sup>6</sup> and induce electrons only where desired. Due to higher starting mobility and better device stability, the enhancement-mode architecture has gained popularity in recent years. Device designs, dot operation, and qubit manipulation have all been reported using this enhancement-mode architecture.<sup>7–10</sup>

In most of the reported dot designs, the starting Si/SiGe heterostructure has a Ge concentration close to 30%, and the gates used to define that the quantum dots are structured in multiple metal layers. There has not been much discussion on the choice of this combination. Since electron mobility is the most obvious and convenient gauge for material quality and the record electron mobility<sup>11</sup> was demonstrated in a heterostructure with a Ge content of 20%, we chose the same composition for the relaxed SiGe buffer layers as we started fabricating Si/SiGe quantum dots. The higher achievable

mobility was expected to reduce the impact of disorder. At a first glance, the main difference between Si/Si<sub>0.7</sub>Ge<sub>0.3</sub> and Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> is simply the barrier height in the 2DEG normal direction. This difference in barrier height is naively not expected to mandate a change in quantum dot design, since most design considerations center around creating lateral confinement of electrons to form quantum dots. Surprisingly, we learned that a reduced Ge concentration affects the device performance indirectly but strongly. In this work, we study the physical mechanisms of this effect through low-temperature experiments and simulations, and discuss the constraints imposed on the device design. Accounting for the constraints, we demonstrate electrical control of quantum dots in a Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> heterostructure. Furthermore, the fabrication process flow presented here uses only a single metal-gate layer, which greatly simplifies device fabrication, shortens device turnaround times, and improves yield by avoiding potentially leaky metal-insulator-metal stacks.

In this work, we used undoped Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> heterostructures grown by Lawrence Semiconductor Research Laboratory. A virtual substrate was made by growing a **2- $\mu\text{m}$  linearly graded buffer layer on a Si wafer** at a grading rate of 10%/ $\mu\text{m}$ , followed by a **1- $\mu\text{m}$  Si<sub>0.8</sub>Ge<sub>0.2</sub> relaxed buffer layer**. Chemical mechanical polishing (CMP) removed 150 nm of the relaxed buffer layer to reduce the surface roughness. After CMP, epilayers of 400 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>, 20 nm Si, 35 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>, and 3 nm Si were grown in order. The heterostructures were processed in the Si foundry at Sandia National Laboratories. A similar process flow for SiGe heterostructures has been reported earlier.<sup>7</sup> Electron-beam lithography (EBL) defined the nanostructured gate patterns. 15 nm Al<sub>2</sub>O<sub>3</sub> and 100 nm Al were then deposited in the same run, followed by lift-off. The Al<sub>2</sub>O<sub>3</sub> layer that insulates the gate from the substrate was formed by depositing Al in the presence of O<sub>2</sub>.

We made a series of narrow transistors with variable channel widths, ranging from 100 nm to 5  $\mu\text{m}$  wide. Each

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narrow gate was  $2\ \mu\text{m}$  long. At each end of a narrow gated region, the enhancement gate was flared quickly to a width exceeding  $10\ \mu\text{m}$  and was extended to overlap two high doped regions on each end of the narrow wire to make two ohmic contacts on each end. The device threshold voltages were characterized at 4 K by monitoring the onset of channel current at a quasi-dc drain-source bias ( $V_{DS}$ ) of 1 mV against the gate voltage ( $V_G$ ). Using the four ohmic contacts for each device, we extracted two threshold voltages, one for the narrow channel, and one for the wide channel. The difference in the two threshold voltages for each device was then tabulated. Some narrow channels did not turn on below  $V_G = 2\ \text{V}$ , the highest voltage applied. These devices were excluded from the calculation of threshold shifts. Fig. 1(c) shows the average shift and the standard deviation of threshold voltages of the narrow channels, and Fig. 1(d) shows the fraction of working devices. The non-uniform standard deviation arises from the outliers that had a threshold voltage much higher than the other devices in the same group.

It is clear from Figs. 1(c) and 1(d) that the threshold voltage of a narrow channel shifts higher and a larger fraction of devices do not turn on as the channel gets narrower. In the case of 100-nm-wide channels, none of the devices showed turn-on below  $V_G = 2\ \text{V}$ . This is in stark contrast to 100-nm channel widths routinely achieved using similar structures with a 30% Ge concentration.<sup>9,10</sup> We attribute the non-working channels and the threshold shifts to the lower Ge concentration used in this work in combination with two other mechanisms, lateral quantum confinement and disorder.

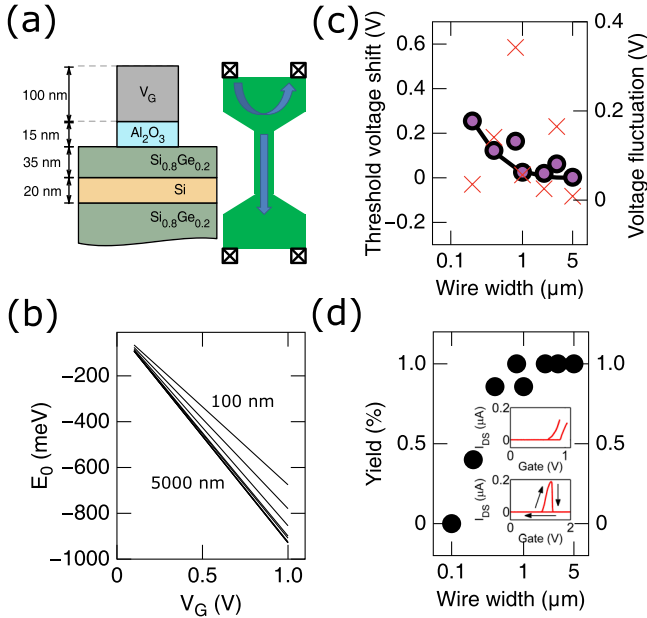


FIG. 1. (a) Schematic cross-section and top view of the measured/ modeled FET. The arrows illustrate the current paths of the wide and narrow channels. (b) Calculated ground state energy of the channel produced by applying a voltage on the gate indicated in (a). The lines correspond to the wire widths measured in panel (c). (c) Threshold voltage shift (solid dots) and its standard deviation (x markers) as a function of wire width. The line is the model fitted to a single-parameter model, obtaining a goodness of fit  $p = 0.9953$ . (d) Fraction of functional devices (yield) as a function of wire width. Top inset: representative turn-on curves at  $V_{DS} = 1\ \text{mV}$  for a 200-nm wide channel (right curve) and an 800-nm wide channel (left curve). Bottom inset: a representative turn-on curve showing that the channel shuts off beyond a critical gate voltage.

To understand the lateral quantum confinement effect, we performed simulations to analyze the nanowire geometry explored by the experiment. For each wire width, we computed the electrostatic landscape by solving Poisson's equation in 2D with the finite element method in COMSOL Multiphysics using the geometry shown in Fig. 1(a). We then used this potential energy landscape as input to Schrödinger's equation, and solved for the energies of the 1D nanowire sub-bands. Since different wire widths produce different 2D ground state energies for the same applied voltage, the lowest sub-band begins filling at different applied voltages for different wire widths.

To check if this model is consistent with our experiment, we note that the ground state energy of the 2D system is linear with gate voltage, as shown by the computational results in Fig. 1(b). Hence, we may write

$$E_0^L = m_L V_G, \quad (1)$$

where  $E_0^L$  is the ground state energy of the wire of width  $L$ ,  $m_L$  is the slope (determined computationally), and  $V_G$  is the applied gate voltage. By inverting this relationship, we can express the voltage shift of a narrow wire compared to an infinitely wide wire as

$$\Delta V_L = \frac{E_0}{m_L m_\infty} (m_\infty - m_L), \quad (2)$$

where  $m_\infty$  is the slope in the infinite wire-width limit and  $E_0$  represents a constant threshold energy independent of wire width. We assume the threshold occurs when the ground state energy level of a specific wire,  $E_0^L$ , reaches  $E_0$ . Noting that the values of  $m_L$  saturate for the wide wires we considered, we take  $m_\infty \approx m_{5000} = -930\ \text{meV/V}$ . Treating  $E_0$  as a free parameter and fitting the model to the data using a Chi-squared test statistic, we obtained a goodness of fit  $p = 0.9953$ , indicating excellent consistency with experiment.

In addition to the quantum confinement, we believe that disorder also plays an important role in the observed threshold voltage shift. In the presence of disorder, a percolation conduction threshold is associated with each narrow channel. The local conduction threshold may be higher for narrow channels if the widths of the channels are smaller than the characteristic length scale of the disorder potential. Statistical variation mandates that some devices would experience stronger disorder than others and show higher threshold voltages. The spread of the experimentally observed threshold voltage shifts for a fixed channel width provide support to the effect.

The two mechanisms discussed above lead to a higher average threshold voltage as well as a wider spread. This is true for all Si-based narrow channels. For Si MOSFETs, a shift in threshold voltage is not a critical problem. In principle, one can always increase the gate voltage to induce more electrons, and eventually the conduction threshold is overcome at high enough densities. *Unfortunately for Si/SiGe heterostructure FETs, there exists an upper density limit.*<sup>12</sup> For shallow Si quantum well channels, this maximum density signals the onset of population of a surface channel at the oxide/semiconductor interface. For deep Si quantum

wells, a non-equilibrium distribution of electrons is collected in the well, with a maximum density controlled by tunneling to a parallel surface channel. A detailed discussion of this non-equilibrium charge distribution can be found in Ref. 12. In both cases, the saturation density is dependent on the barrier height, or in turn, the Ge concentration of the SiGe layers, with the maximum density independent of the channel depth in the latter case.<sup>12</sup> The wells used here are considered deep wells and as such, the electron density can be higher than the thermal equilibrium value and is dynamically limited by slow tunneling. Experimentally this upper density limit is  $\sim 3 \times 10^{11} \text{ cm}^{-2}$  for  $\text{Si}_{0.8}\text{Ge}_{0.2}$  barriers and  $\sim 7 \times 10^{11} \text{ cm}^{-2}$  for  $\text{Si}_{0.7}\text{Ge}_{0.3}$  barriers.<sup>12</sup> We obtained a similar upper density limit in our structures using Hall bar testers fabricated from the same material. This density limit, nonlinear in barrier height, limits the tunable density range in  $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$  to less than half the density range in  $\text{Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$ . The maximum density results in a maximum Fermi energy. For gate voltages beyond the density saturation bias, a possibly more serious effect occurs, namely, the oxide/semiconductor interface forms a second accumulation layer and eventually accumulates a high enough electron density to become conducting.<sup>13</sup> When the surface channel conduction occurs, this surface channel screens the electric fields to the buried Si quantum well channels and reduces the electron density in the Si quantum well to its thermal equilibrium value. The thermal equilibrium value could be below the conduction threshold, such that the channel conductivity drops to zero. This appears to happen in all our samples, in which we observe a sudden drop in current to zero at a gate bias beyond threshold, as shown in the inset of Fig. 1(d).

Since the current in our devices has to flow serially through both the wide and narrow channel areas, the maximal Fermi energy and the sudden turnoff pose a serious problem if the maximum Fermi energy in the wide gated channel area is not much higher or even lower than the conduction threshold energy of the narrow channel. In the former case, the narrow channel barely turns on before the wide channel turns off, and hence the resistance is very high. In the latter case, when the lateral confinement lifts the threshold energy level significantly, the narrow wire will not reach the threshold until the gate is biased beyond the turn-off voltage of the wide channel area. Thus for the narrowest wires there will never be a simultaneous conduction path through both regions. Using  $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$  heterostructures instead of  $\text{Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$ , thus, severely constrains the operational window of  $V_G$ . A multiple-metal-layer architecture with independent controls for the reservoirs and nanostructures circumvents this density limit problem since the potential landscape can be locally tuned.

Having understood the major difference between  $\text{Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$  and  $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$ , we now focus on to our results of fabricating quantum dots using the  $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$  heterostructures. Since the main difficulty in using lower Ge concentration is the high threshold voltages for narrow channels, the quantum dot designs have to be enlarged compared to what are used in Si MOSFETs or in  $\text{Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$ , unless a multiple-metal-layer architecture is adopted. For this work, **we chose to use only one metal layer and therefore chose to make large quantum dots.** A larger quantum dot has lower charging energies and requires lower temperatures to resolve transport features. However, the larger feature sizes are more

**easily fabricated.** Furthermore, the one-metal-layer architecture has fewer fabrication steps and fewer potentially leaky metal-insulator-metal stacks. This simpler process flow, together with the relaxed nano-patterning accuracy, significantly shortens the fabrication turnaround times and improves the device yield.

The starting wafer for the dot work had nominally identical growth parameters as previously described. Here, we did every step at die-level. Ti/Au alignment marks were first deposited, followed by ion implantation of P at 20 keV and 75 keV with a fluence of  $5 \times 10^{14} \text{ cm}^{-2}$  for each energy. A rapid thermal anneal at 625 °C for 30 s activated the implanted dopants for ohmic contacts. A blanket 20-nm-thick  $\text{Al}_2\text{O}_3$  layer was deposited in an atomic-layer-deposition system at 200 °C. After etching vias through  $\text{Al}_2\text{O}_3$ , we deposited a blanket 2 nm Ti and 40 nm Au films. This metal layer was patterned by EBL and etched in an ion mill. The exposed metal areas were milled away, leaving nanostructure gates and bond pads simultaneously. Fig. 2(a) shows a scanning electron micrograph of a fabricated quantum-dot device. Also shown is the circuit setup used for the data presented below. The names of the gates are labeled in yellow. The narrowest point of the channel had a width of  $\sim 200 \text{ nm}$ .

The device shown in Fig. 2(a) was studied in a  $^3\text{He}$  cryostat with a base temperature of  $\sim 0.3 \text{ K}$  at  $V_{DS} = 10 \mu\text{V}$  using standard lock-in techniques. The names of the gates, UL, UC, UR, AGU, AGL, LL, LC, and LR, are shown in yellow in Fig. 2(a). We focused on the upper channel and varied the voltages for UL, UC, and UR to form quantum dots. The voltages used for AGU, AGL, LL, LC, and LR were kept constant at 0.633,  $-0.35$ , 0, 0, and 0 V, respectively, for the data presented here. In Fig. 2(b), we show a series of stability plots against the UL and UR gates at different UC voltages. At low (less negative) UC, single-quantum-dot behavior is dominant in the lower left corner of a UR vs. UL plot, with approximately equal couplings to the UL and UR gates. Upon making UC more negative, the dot is broken up into two halves by the electrostatic potential, and forms a pair of quantum dots coupled by tunneling. The isolated transport peaks observed showed the expected triple points for tunnel-coupled double-quantum-dots.<sup>14</sup> From stability diagrams, we extract the following gate-dot capacitances for the double-dot system:  $C_{UL,L} = 4.0 \text{ aF}$ ,  $C_{UC,L} = 5.2 \text{ aF}$ ,  $C_{UR,L} = 1.2 \text{ aF}$ ,  $C_{AGU,L} = 63 \text{ aF}$ ,  $C_{AGL,L} = 13 \text{ aF}$ ,  $C_{LL,L} = 1.3 \text{ aF}$ ,  $C_{LC,L} = 1.4 \text{ aF}$ ,  $C_{LR,L} = 0.48 \text{ aF}$ ,  $C_{UL,R} = 1.3 \text{ aF}$ ,  $C_{UC,R} = 5.2 \text{ aF}$ ,  $C_{UR,R} = 4.0 \text{ aF}$ ,  $C_{AGU,R} = 79 \text{ aF}$ ,  $C_{AGL,R} = 13 \text{ aF}$ ,  $C_{LL,R} = 0.63 \text{ aF}$ ,  $C_{LC,R} = 1.3 \text{ aF}$ , and  $C_{LR,R} = 0.48 \text{ aF}$ . These capacitances are consistent with a lithographic double-dot defined by the gates. The inter-dot tunnel barrier is tuned not only by the UC gate but also by the UL and UR gates, as is evidenced from the transition from single-dot-like to double-dot-like characteristics moving from the upper right corner to the lower left corner at a fixed UC voltage. This is a trade-off of using a single-metal-gate-layer design; controls over tunnel barriers and dot occupations are more intertwined together and require more sophisticated device tuning.

To corroborate our single to double-dot interpretation of Fig. 2(b), we performed a capacitive modeling of our nanostructure using FastCap to obtain a simulated charge stability diagram. We used voltages identical to our experiment, modeled the electrical leads below AGU as a metallic brick, and



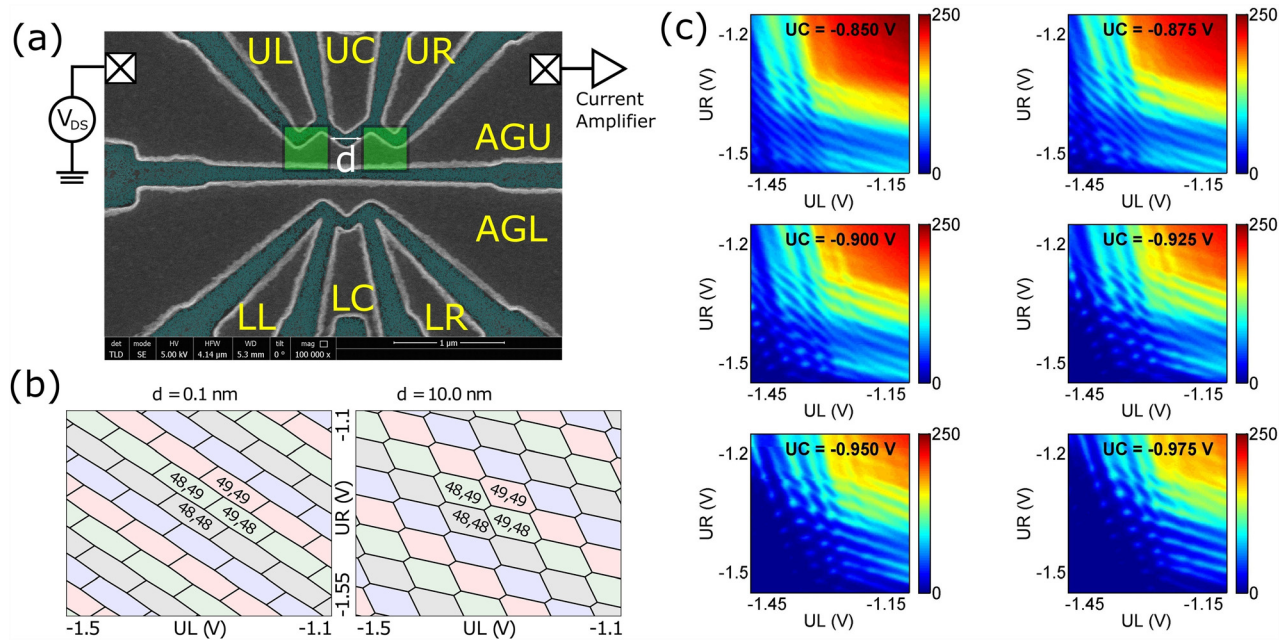


FIG. 2. (a) Scanning electron micrograph of the device. Lighter gray with yellow labels are Ti/Au gates on top of the Si/SiGe substrate. The cyan pseudo-colored regions are exposed  $\text{Al}_2\text{O}_3$ . The capacitance calculations assume two square quantum dots with side length 400 nm as indicated in green. These two dots are separated by a distance  $d$ . (b) Stability diagrams for the quantum dot in the upper channel at  $V_{UC} = -0.85, -0.875, -0.9, -0.925, -0.95$ , and  $-0.975 \text{ V}$ . The measurement temperature was 0.3 K, and the drain-source bias was  $10 \mu\text{V}$ . (c) Capacitance simulations for differing dot separation  $d$ . We see that even a modest dot separation of 10 nm is sufficient to transition from single- to double-dot behavior. These calculations indicate that the observed charge stability diagrams in (b) likely describe a transition between lithographic dots.

the two quantum dots as 10 nm thick conductive bricks with  $400 \times 400 \text{ nm}$  in-plane dimensions, as shown in Fig. 2(a). The two dots were separated by a distance  $d$ , which we varied. As shown in Fig. 2(c), by changing the distance from 0.1 to 10 nm, we are able to achieve a clear transition from a single- to double-dot charge stability signature. These plots are qualitatively consistent with those in Fig. 2(b), indicating that one needs only to consider (plausible) small dot separations when explaining the data.

In summary, we discovered the constraints imposed by using the Si/SiGe heterostructures with a Ge concentration of 20%, lower than what is used in other reports. We found that the limited tunable density range prevents conduction through channels gated by a single layer gate which contains both very narrow and wide channel widths. With a scaled-up quantum dot design, we demonstrated operation of lithographically defined quantum dots using the Si/Si<sub>0.8</sub>Ge<sub>0.2</sub> heterostructures, and were able to induce a single-dot to double-dot transition. The presented fabrication process flow requires only one metal-gate-layer for all gates and bond pads, significantly reducing device fabrication turnaround times. This may found useful in situations where high throughput of simple quantum dots is required, such as studying the statistics of quantum dot properties.

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