LAB 1 DEMO – The Lab Environment and a Little c

Reviewer _____

Team_____

Total_____Out of 190

Counters – Quartus II Implementation   (145)

Four Stage Ripple Down Counter

Gate Level Implementation	20
Active low reset	5
Test Bench, Tester, Module	10

Four Stage Synchronous Down Counter

Dataflow – RTL Implementation	20
Active low reset	5
Test Bench, Tester, Module	10

Four Stage Synchronous Johnson Down Counter

Behavioural Implementation	20
Active low reset	5
Test Bench, Tester, Module	10

Four Stage Synchronous Down Counter

Schematic Capture Implementation	20
Active low reset	5
Test Bench, Tester, Module	10

Multifile iVerilog Program   (15)

andorTop0.v and *andOr0.v* integrated and functional

iVerilog

gtkwave

Signal Tap   **(20)**

Signal Tap Display

    Data capture following third state

Counter 1	5
Counter 2	5
Counter 3	5
Counter 4	5

Currency Calculator   **(15)**

Enter exchange rate	5
Convert foreign to dollars	5
Convert dollars to foreign	5