**Project 1**

**Introduction to the Lab Environment**

**EE 371 AC**

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| **NAME** | **STUDENT ID** |
| Denny Ly | 1231185 |
| Minhhue H. Khuu | 1329349 |
| Ruchira Kulkarni | 1234324 |

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# Abstract

The goal of this lab was to understand different developing environments such as iVerilog and gtkwave and Signal Tap Tool in the Quartus II IDE for developing Verilog code. We achieved this by making four 4-bit down counters, namely the ripple-down counter, a four stage synchronous down counter and a Johnson down counter. We also familiarized ourselves with the basics of C programming by writing a simple currency conversion calculator.

# Introduction

In this lab, our main focus was to analyze the process of model design and testing process by implementing different down counters in Verilog. To understand this process,

The tools we used in this lab are:

* iVerilog
* gtkwave
* Quartus II Signal Tap
* Cyclone V FPGA
* Command line tool
* GCC C Compiler
* CodeBlocks

# Discussion of the Project

## Design Specification

In this project, we implemented 4 counters in Verilog. Each of the counters was implemented at the different levels (gate level, behavioral level, etc.). All the counters were reset to 0000. The 4 bit down counters were displayed on the 4 LEDs (LED[3:0]) on the DE1-SoC board. The active low reset is implemented by one of the DE1­SoC’s keys (KEY[0]).

The 4-bit counters are as follows:

1. Ripple Down Counter (gate level/ structural level), an asynchronous 4-bit down counter with an active low reset.
2. Synchronous Down Counter (dataflow model), a synchronous down 4-bit counter with an active low reset.
3. Synchronous Johnson Counter (behavioral model), a synchronous down 4-bit counter with an active low reset.
4. Synchronous Down Counter (schematic design), a synchronous down 4-bit counter with an active low reset.

### Four Bit Ripple Down Counter

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. The ripple counter ranges from 0000 to 1111. On reset, the counter starts at 0000, then goes to 1111, 1110, 1101, … till 0000 again.

According to the design specifications given to us, we made a gate or structural model with active low reset. Gate level or structural design implies interconnecting logical gates with wires (such as and, nor, or gates) only. The advantages of this design is that it is has a lot of implementation details.

In our design, we drew out the required bit patter results for the ripple counter and formed a Boolean equation from it. We used this Boolean equation as a reference for designing and constructing or circuit at the gate level in Verilog. This table, equations and circuit is shown in the design procedure for ripple down counter. We also used the code snippet provided to us for the D flip flop in the spec.

### Synchronous Down Counter (Dataflow Model)

In a synchronous down counter, all the output bits change state simultaneously. We designed the counter using the data flow model as mentioned in the spec with an active low reset. In a dataflow design, a module is implemented by specifying the movement of the data. This allowed us to use assign statements instead of using AND gates in our module for the counter. We also used the code snippet provided to us for the D flip flop in the spec.

In our design, we drew out the bit pattern which ranged from 0000 to 1111. On reset, the counter starts at 0000, then goes to 1111, 1110, 1101, … till 0000 again. We also made use of K-maps to determine the new state value using combinational logic and present values.

### Synchronous Johnson Counter (Behavioral Model)

The Johnson Counter is a shift register with feedback with inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop.

We designed the Johnson Counter using a behavioral model with reset on active low. In behavioral modelling, the underlying hardware is abstracted away based upon an algorithmic description. The Johnson 4-bit counter only takes 8 different values. At reset the counter is set to 0000. It follows the pattern of 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001.

### Synchronous Down Counter (Schematic Entry)

This synchronous down counter is similar to the synchronous down counter mentioned above. The only difference is the way in which we implemented it. For this counter, we made a .bdf file using the Quartus II IDE environment using existing gate blocks with blocks we made from the slow version of our clock divider. We also used the D-flip flops in our schematic.

## Design Procedure

### Four Bit Ripple Down Counter

Table 1. Four Bit Ripple and Synchronous Down Counter Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Stage** | **Q[3]** | **Q[2]** | **Q[1]** | **Q[0]** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 1 | 0 |
| 3 | 1 | 1 | 0 | 1 |
| 4 | 1 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 0 | 1 | 0 |
| 7 | 1 | 0 | 0 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 |
| 12 | 0 | 1 | 0 | 0 |
| 13 | 0 | 0 | 1 | 1 |
| 14 | 0 | 0 | 1 | 0 |
| 15 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

|  |
| --- |
| module DFlipFlop(q, qBar, D, clk, rst);  input D, clk, rst;  output q, qBar;  reg q;  not n1(qBar, q)  always@ (negedge rst or posedge clk) begin  if (!rst)  q = 0;  else  q = D;  end  endmodule |

Figure **1.** Verilog code for DFlipFlop module.

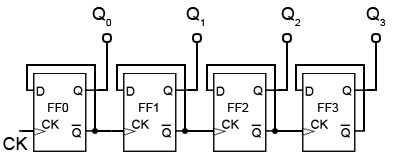


Figure **2.** Ripple Down Counter Structural Diagram from Quartas.

### Synchronous Down Counter (Dataflow Model)

Truth table that we used for the synchronous counter is the same one as the Table 1.

By observation, the Boolean equations are as follows:

(1)

(2)

(3)

(4)

Table 2. Karnaugh Map for new value D[1] for the Synchronous Down Counter

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 1 |
|  | 1 | 0 |

Table 3. Karnaugh Map for new value D[2] for the Synchronous Down Counter

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  | 1 | 0 | 0 | 0 |
|  | 0 | 1 | 1 | 1 |

Table 4. Karnaugh Map for new value D[3] for the Synchronous Down Counter

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  | 1 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 0 |
|  | 1 | 1 | 1 | 1 |
|  | 0 | 1 | 1 | 1 |

### Synchronous Johnson Counter (Behavioral Model)

Table 5. Four Bit Johnson Down Counter Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Stage** | **Q[3]** | **Q[2]** | **Q[1]** | **Q[0]** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

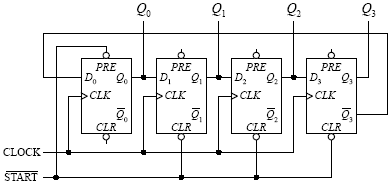


Figure **3.** Johnson Down Counter Structural Diagram Implementation from Quartas.

### Synchronous Down Counter (Schematic Entry)

We created the following schematic in the Quartus IDE. This allowed us to produce a corresponding Verilog file (auto-generated by Quartus) and generate the signal tap wave form at the third state for this.

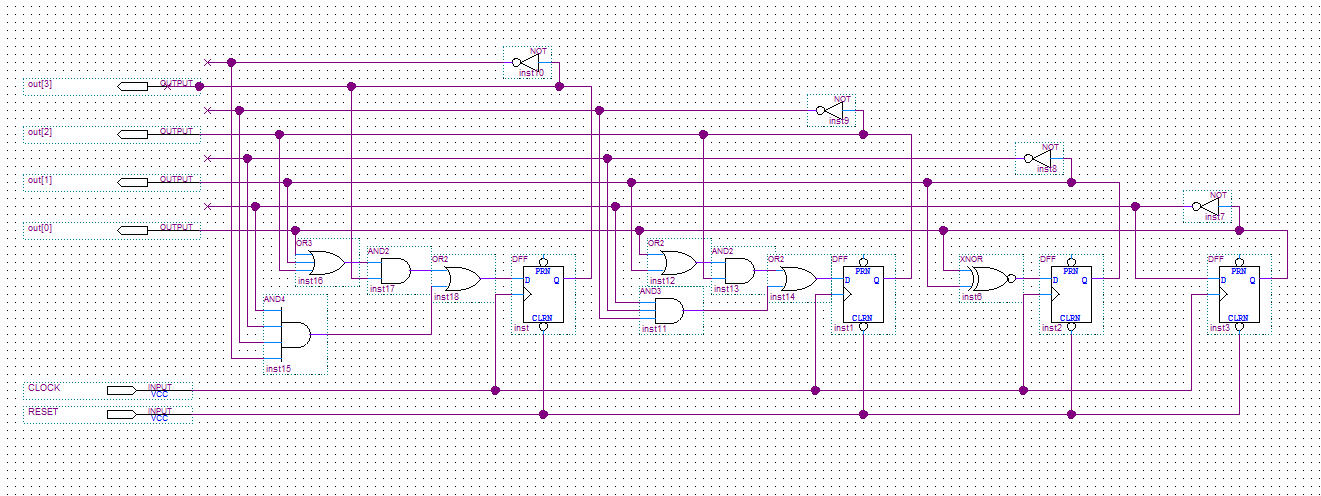


Figure **4.** Synchronous Down Counter Structural Diagram Implementation from Quartas.

## System Description

## Software Implementation

Please refer to the code submitted via canvas dropbox.

## Hardware Implementation

We used the Quartus IDE to load our Verilog modules on to the DE1\_SOC FPGA board. For our hardware, we used simple D- Flip Flops to achieve the functionality of the ripple down, Johnson and synchronous counters. We assigned the required pins on the FPGA board such as LEDS[3:0], KEY[0], system CLOCK (50 MHz) using a pin planner tool in Quartus. The pin assignment layout was imported from an excel spreadsheet we created by studying the DE1\_SOC datasheet for FPGA pin assignments.

Table 6. Signal to FPGA Pin Pairing

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **FPGA Pin No.** | **Description** | **I/O Standard** |
| KEY[0] | PIN\_AA14 | Push-button[0] | 3.3V |
| LEDR[0] | PIN\_V16 | LED[0] | 3.3V |
| LEDR[1] | PIN\_W16 | LED[1] | 3.3V |
| LEDR[2] | PIN\_V17 | LED[2] | 3.3V |
| LEDR[3] | PIN\_V18 | LED[3] | 3.3V |
| CLOCK\_50 | PIN\_AF14 | 50 MHz clock input | 3.3V |

# Testing

## Test Plan

A down counter is a system and a system is purely defined by its output and input relationship. Therefore, to test each of the counters implemented in this lab, each counter of the three 4-bit down counters: (1) Ripple, (2) Synchronous, and (3) Johnson were analyzed for their corresponding output signal given a varying input signal. By using the truth tables derived from Table 1 for the Ripple and Synchronous down counter and Table 5 for the Johnson down counter, their behaviors can be predicted and analyzed for any similarities and irregularities.

In this lab, the followings tools were used to test each of the three counters:

* iVerilog and gtkwave
* Quartas II and Signal Tap
* Quartas II and Waveform tool for schematic files

### iVerilog and gtkwave

The process of testing in iVerilog and gtkwave consists of the following steps:

1. Design a tester module in Verilog to generate the input signals for the unit under test.
2. Design a testbench module in Verilog to generate a .vcd file to view the waveform generated from the unit under test.
3. Synthesize associated Verilog files in iVerilog and run the synthesized Verilog program to generate a .vcd file and run gtkwave to view the waveform.
4. Analyze the waveform to see if the waveform has any similarities or irregularities from predicted results from the test specifications.

### Quartas II and Signal Tap

The process of testing in signal tap consists of the following steps:

1. Design a top level module in Verilog under the Quartas II IDE.
2. Assign the output to the appropriate LED on the DE1-SoC board to display the 4-bit number.
3. Assign the input to a KEY on the DE1-SoC board for a reset signal.
4. Synthesize and open up Signal Tap and set input, output, and clock ports for testing.
5. Set the trigger conditions for test condition.
6. Set clock and sample depth to tBase[19] and 512 samples, respectively.
7. Load the .sof file into the DE1-SoC board.
8. Run the Signal Tap and utilize the input signal to activate the trigger condition.
9. Analyze the waveform to see if the waveform has any similarities or irregularities from predicted results from the test specifications.

### Quartas II and Waveform tool

The process of testing in signal tap consists of the following steps:

1. Create the schematic file using Quartas.
2. Synthesize the schematic file.
3. Open up the waveform tool.
4. Locate the output and input pins for the schematic and insert them into the waveform tool.
5. Set the input signals wave form.
6. Run the analyzing tool to view the output waveform.
7. Analyze the waveform to see if the waveform has any similarities or irregularities from predicted results from the test specifications.

## Test Specification

The test specifications were similar for all of the tools used for testing which includes two cases: (1) reset signal is low and (2) the reset signal is high. For the record, the clock should always behave independently from the reset signal and continue alternating from high and low regardless of the state of the reset signal.

### Reset Signal is set low

* Reset signal is initially set low.
  + Output is 0000 (0 across all four bits).
  + Output remains 0000 while the reset signal is set low.
* Reset signal is set low after being set high.
  + Output is instantly changed from its current state to 0000.
  + The reset is asynchronous, and is independent of the clock cycle.

### Reset Signal is set high

The output behavior of the down counters differs between the Ripple and Synchronous down counter to the Johnson down counter. The Ripple and Synchronous down counter counts from decimal value 15 to decimal value 0 then jumps to decimal value 15 and repeat. The Johnson down counter behaves like a right shift register while having the least significant bit inverted and push back to the most significant bit.

#### Ripple and Synchronous Down Counter

* Reset signal is initially set high.
  + Current output is set to the next output at the next positive (rising edge) of the clock signal.
  + The next output is dependent on the current output.
    - If the current output is 0000, then the next output will jump to 1111.
    - Otherwise, the next output will decrement the current output value, meaning 1111 to 1110 to 1101 until the current output is 0000.
* Reset signal is set high after being set low
  + Current output is set to the next output at the next positive (rising edge) of the clock signal.
  + The next output will always be 1111, then decrements and repeats.

#### Ripple and Synchronous Down Counter

* Reset signal is initially set high
  + Current output is set to the next output at the next positive (rising edge) of the clock signal.
  + The next output is dependent on the current output
    - If the current output is 0000, then the next output will jump to 1000.
    - Otherwise, the next output will “decrement” by shifting to the right.
      * The least significant bit of the current output will be inverted and pushed into the most significant bit of the next output.
      * The other bits will shift towards the right.
      * Example: 0000 to 1000 to 1100 to 1110 to 1111 to 0111 until the current output is 0000 and repeat.
* Reset signal is set high after being set low
  + Current output is set to the next output at the next positive (rising edge) of the clock signal.
  + The next output will always be 1000, then “decrements” by shifting to the right .

## Test Cases

The test cases were conducted using the procedures described in Section 4.1 for each of the corresponding testing methods.

### iVerilog and gtkwave

#### Four Bit Ripple Down Counter

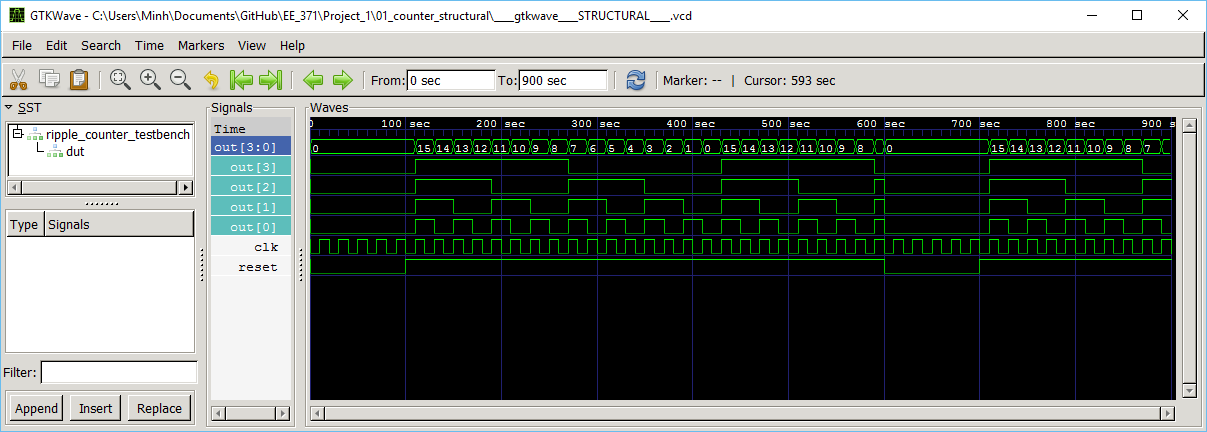


Figure **5.** Four Bit Ripple Down Counter Waveform using gtkwave.

#### Synchronous Down Counter (Dataflow Model)

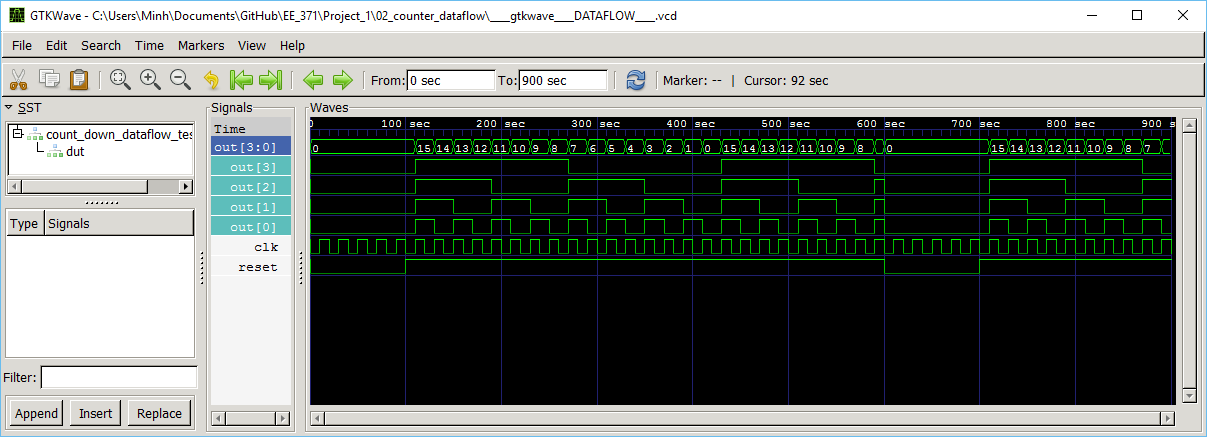


Figure **6.** Four Bit Synchronous Down Counter Waveform using gtkwave.

#### Synchronous Johnson Counter (Behavioral Model)

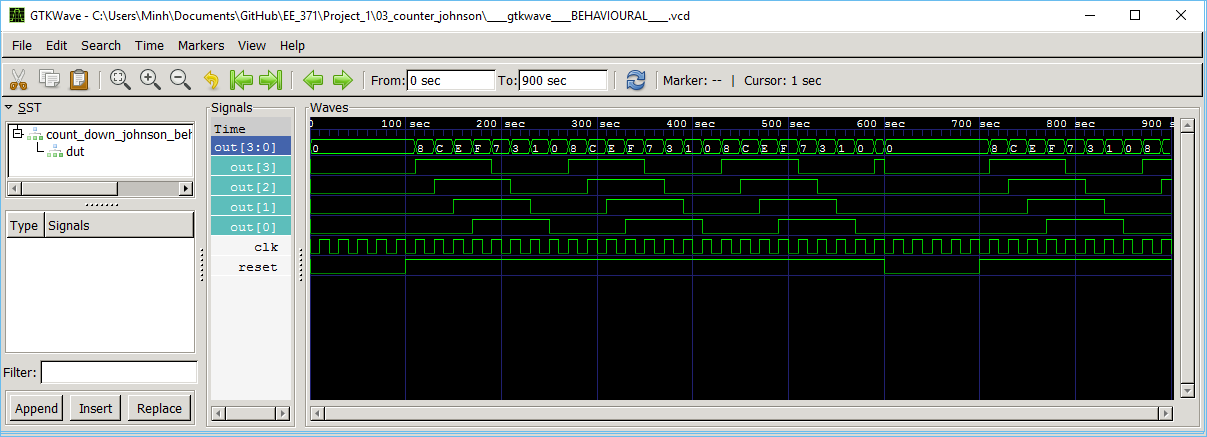
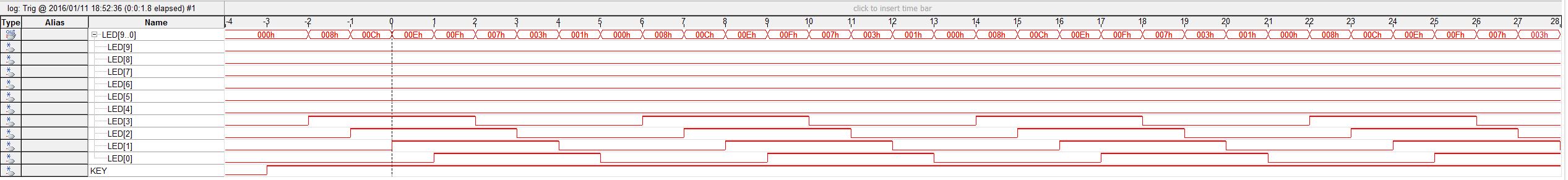


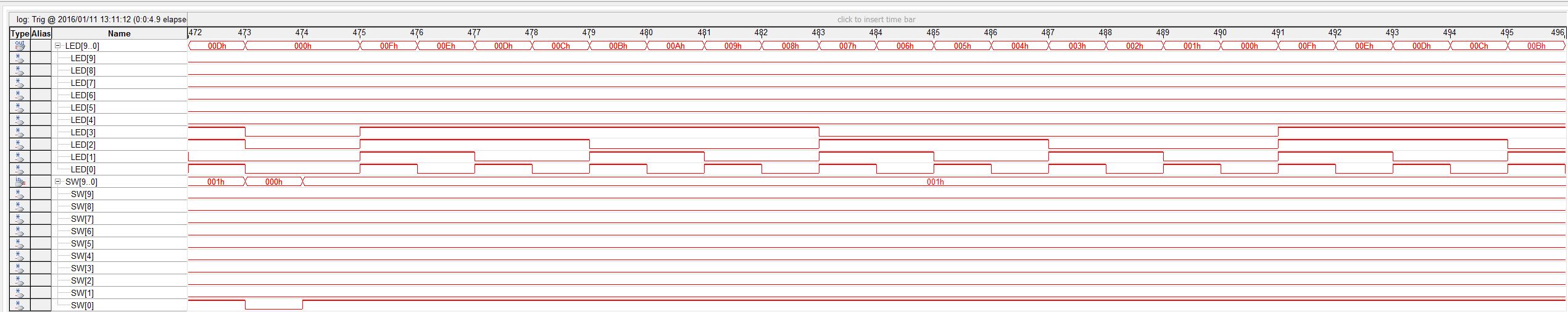
Figure **7.** Four Bit Johnson Down Counter Waveform using gtkwave.

### Quartas II Signal Tap

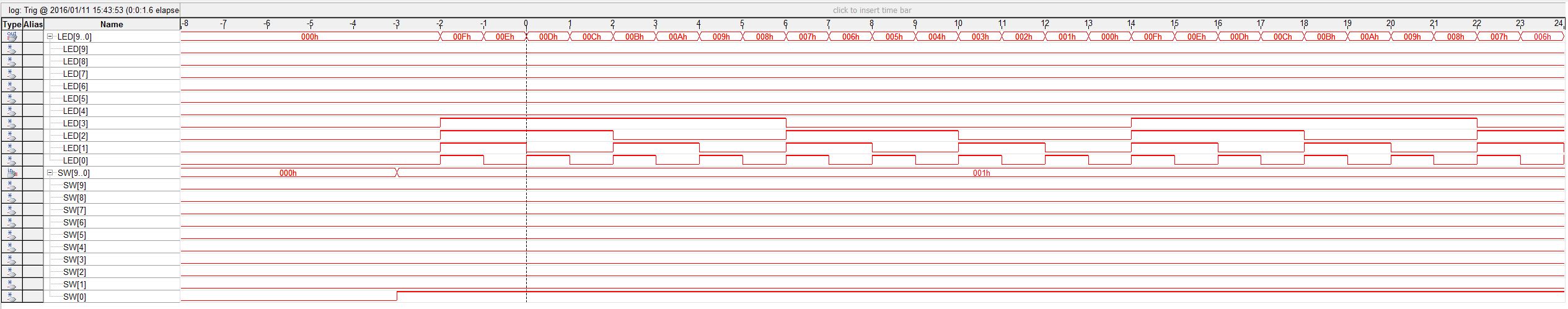
Signal Tap Johnson\_structural



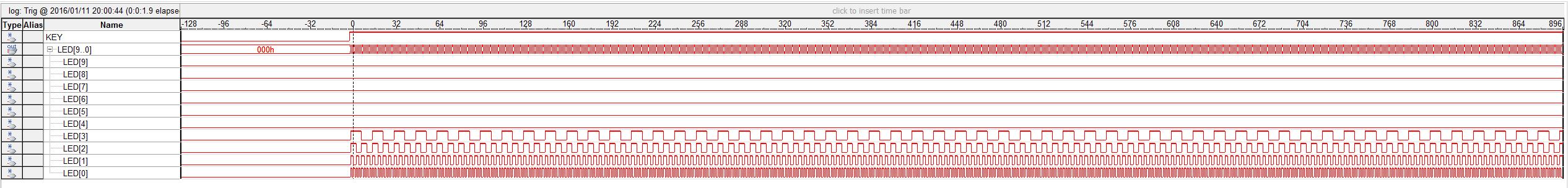
Signal Tap Ripple



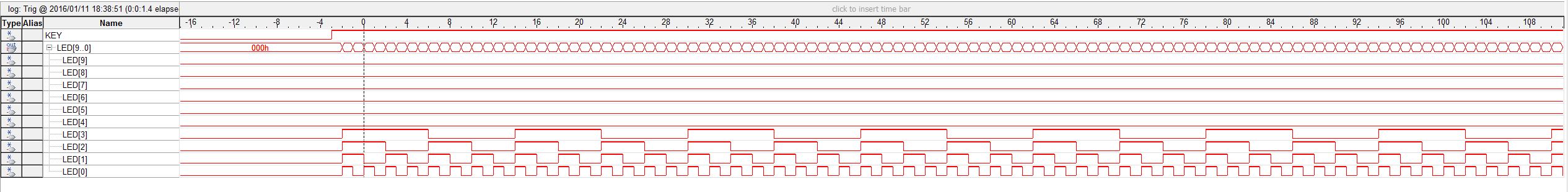
Signal Tap Ripple 3



Signal Tap Schematic



Signal Tap countdown dataflow



### Quartas II Waveform tool

# Presentation, Discussion, and Analysis of the Results

# Analysis

## Analysis of any errors

Software and tool problems. Iverilog not running because it is not included in windows path variable.

Problem wiring modules.

## Analysis of possible errors

One possible error is by selecting a clock speed that is too fast. This causes the gate delays to have a more noticeable effect.

Verilog syntax errors.

## Feedback upon the analysis

# Summary and Conclusion

# Appendices