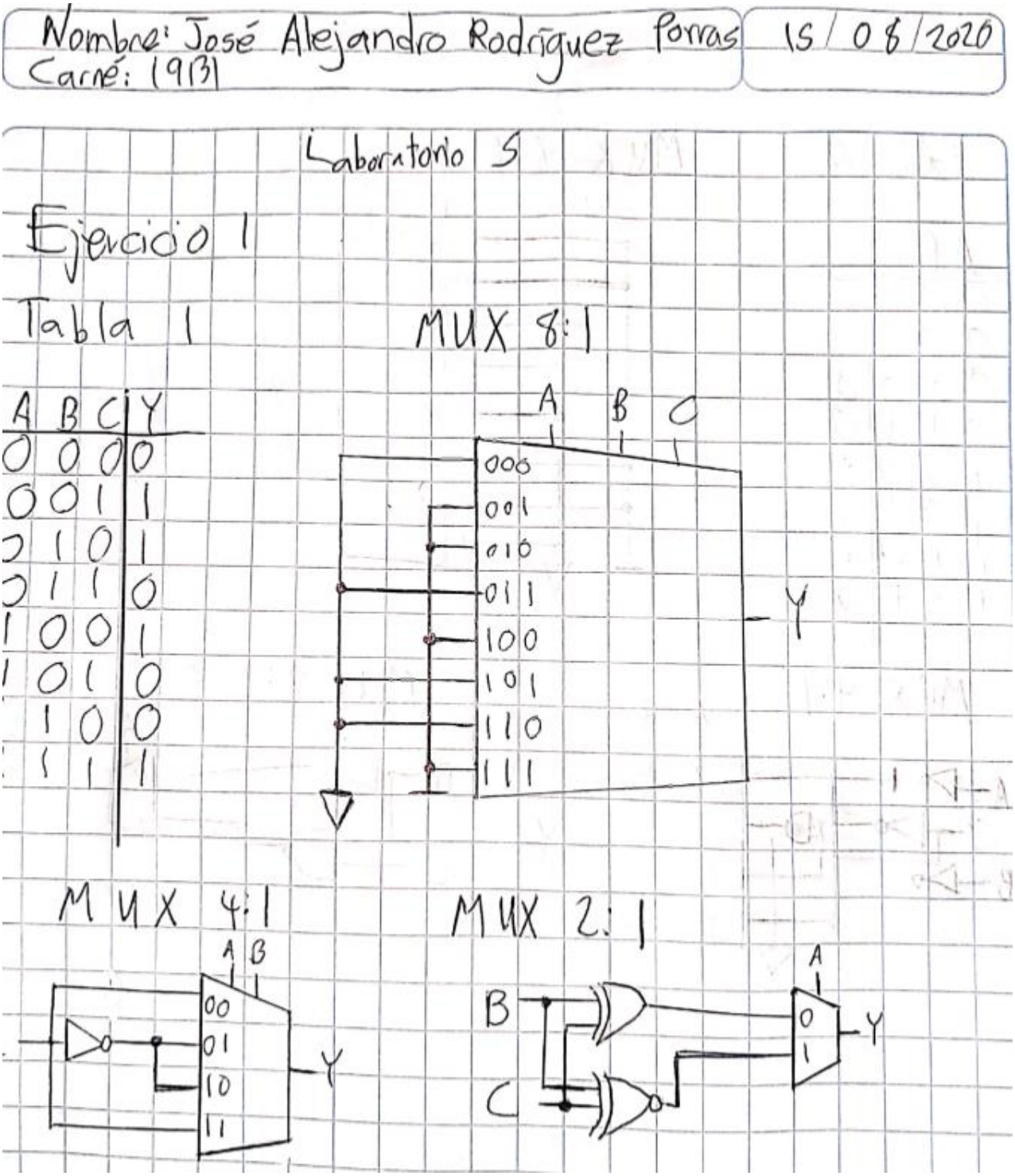
Nombre: José Alejandro Rodríguez Porras Carné: 19131 Sección: 10
Fecha: 16/08/2020

Laboratorio 5

Ejercicio 1



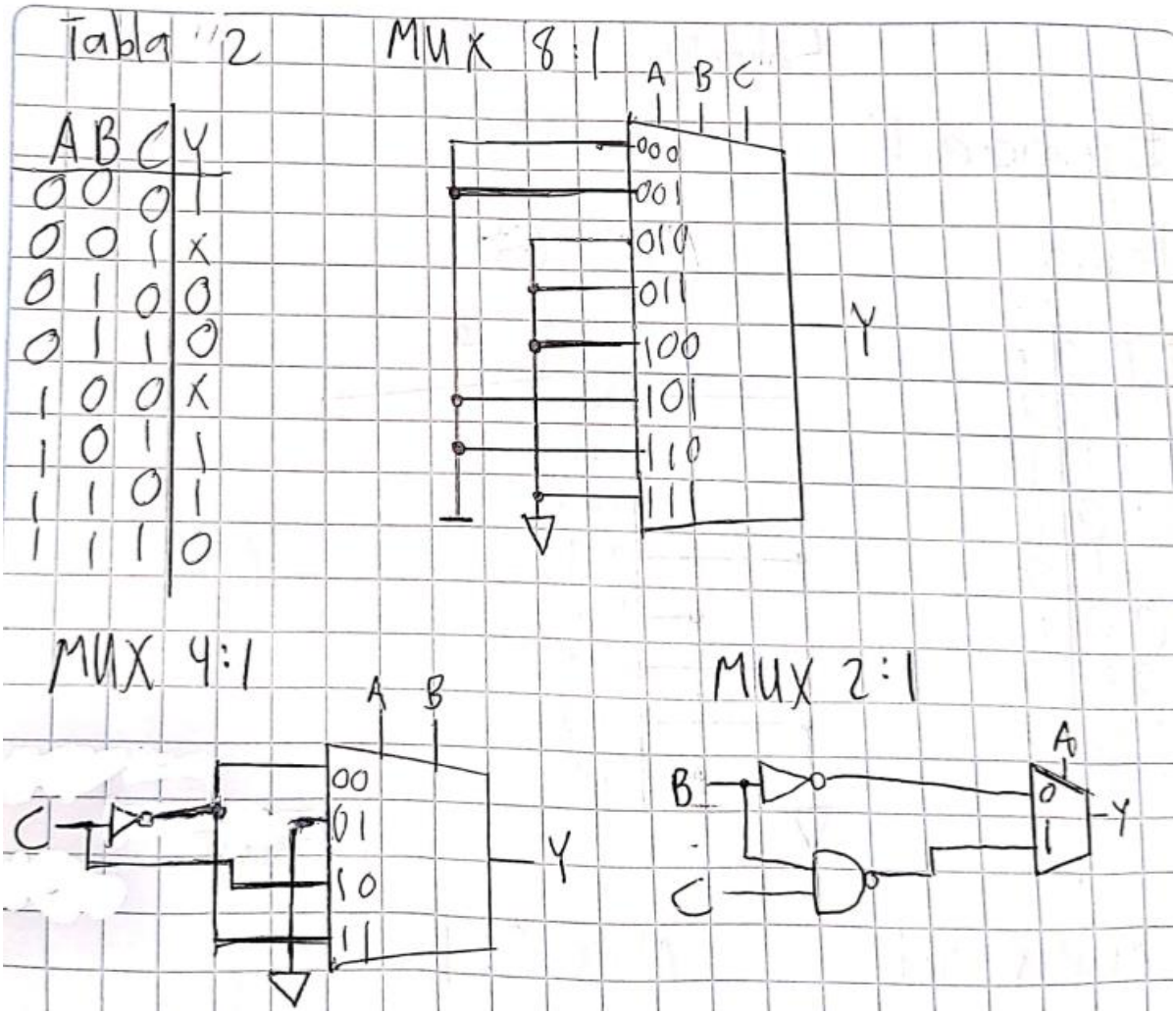
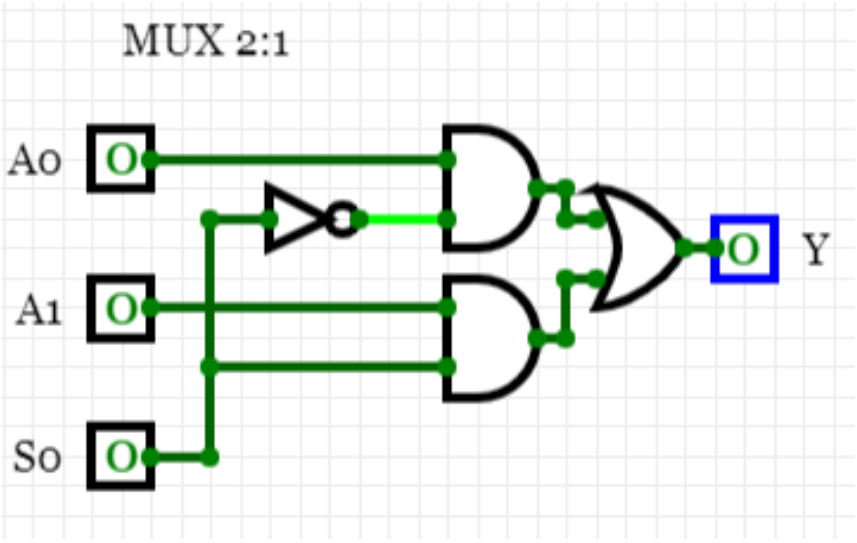
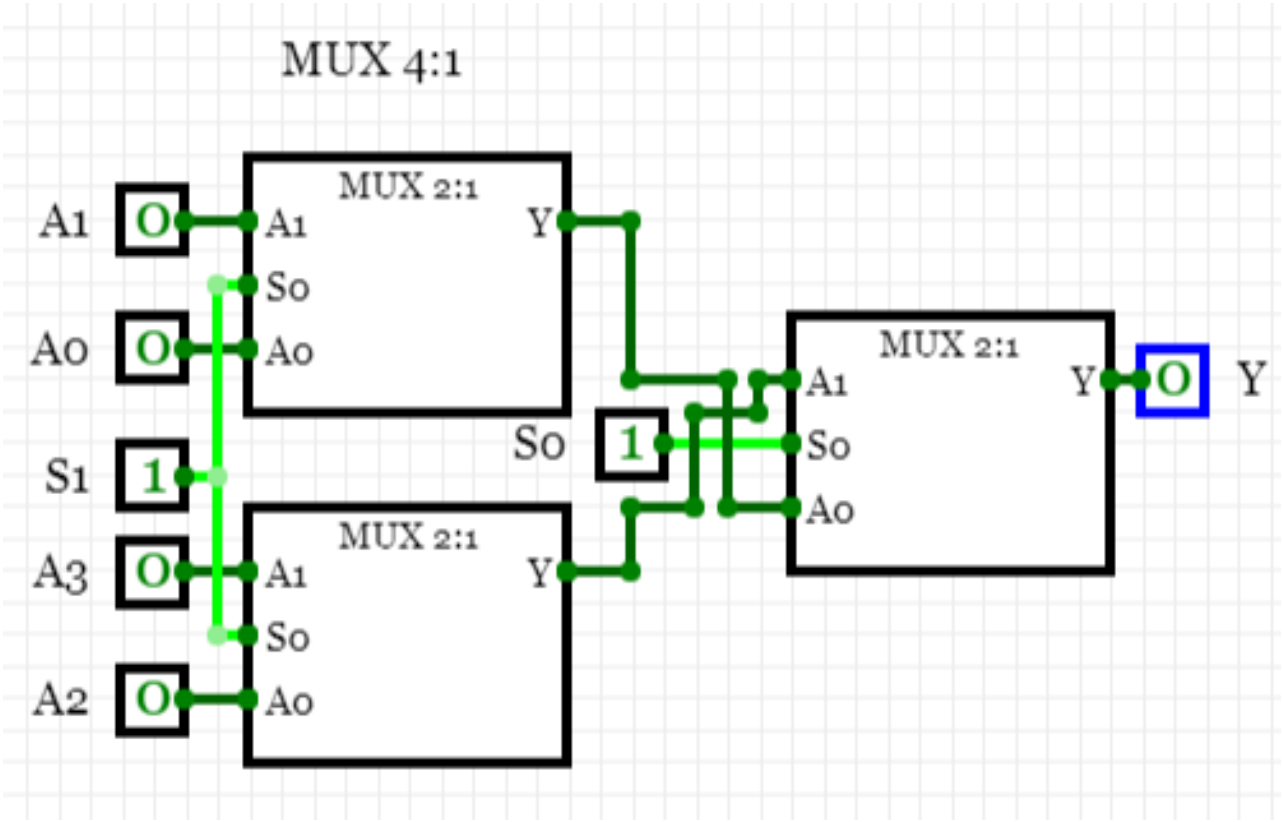


Tabla 2
A B C Y
0 0 0 1
0 0 1 X
0 1 0 0
0 1 1 0
1 0 0 X
1 0 1 1
1 1 0 1
1 1 1 0
MUX 8:1
A B C
000
001
010
011
100
101
110
111
Y
MUX 4:1
A B
00
01
10
11
C
Y
MUX 2:1
A
B
0
1
Y
C

Ejercicio 2


MUX 2:1
A0
A1
S0
Y


MUX 4:1
MUX 2:1
A1
A0
S1
A3
A2
S0
Y
MUX 2:1
MUX 2:1
A1
So
Ao
Y
Y

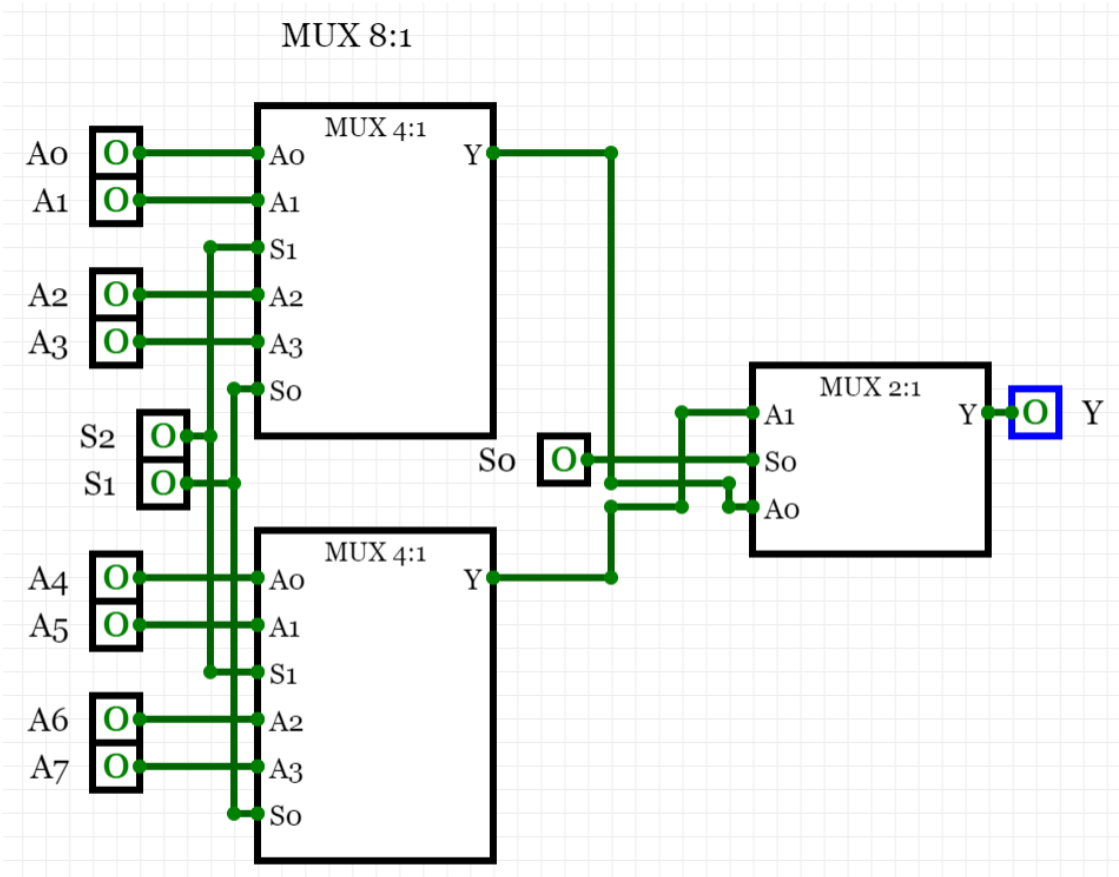

MUX 8:1
MUX 4:1
MUX 4:1
MUX 2:1
A0
A1
A2
A3
A4
A5
A6
A7
S2
S1
So
Y
Y

Tabla 1 MUX 8:1

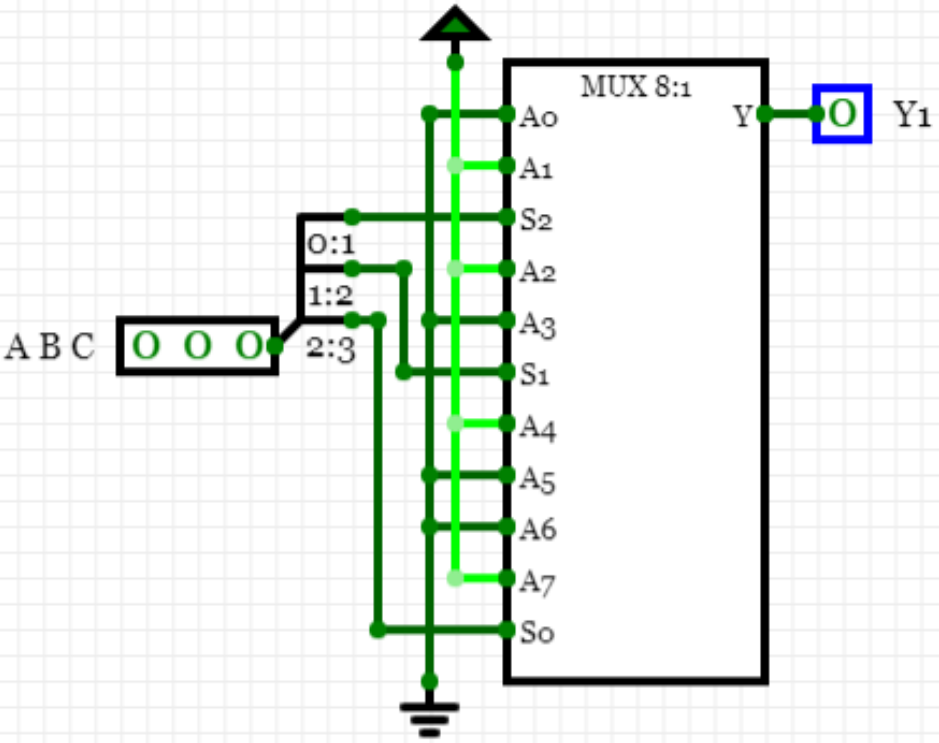


Tabla 1 MUX 4:1

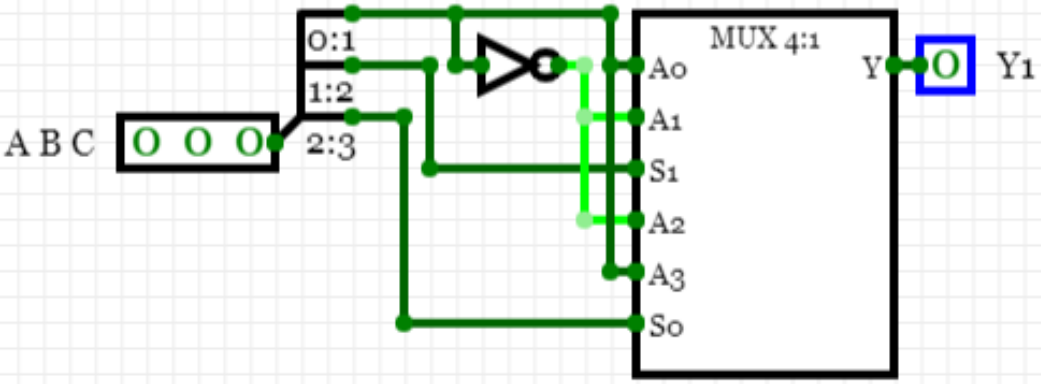


Tabla 1 MUX 2:1

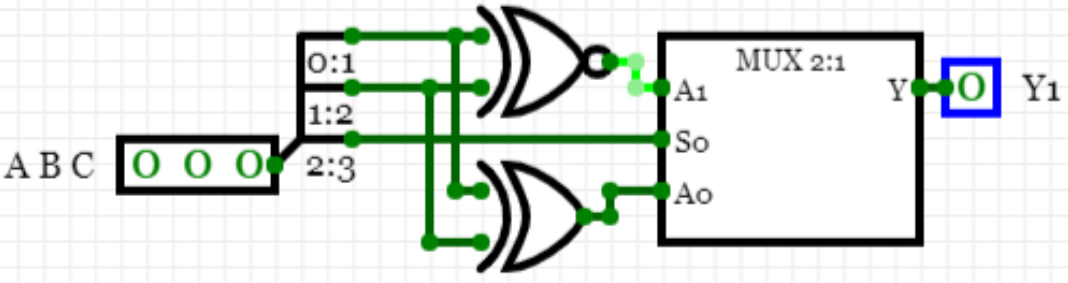


Tabla 2 MUX 8:1

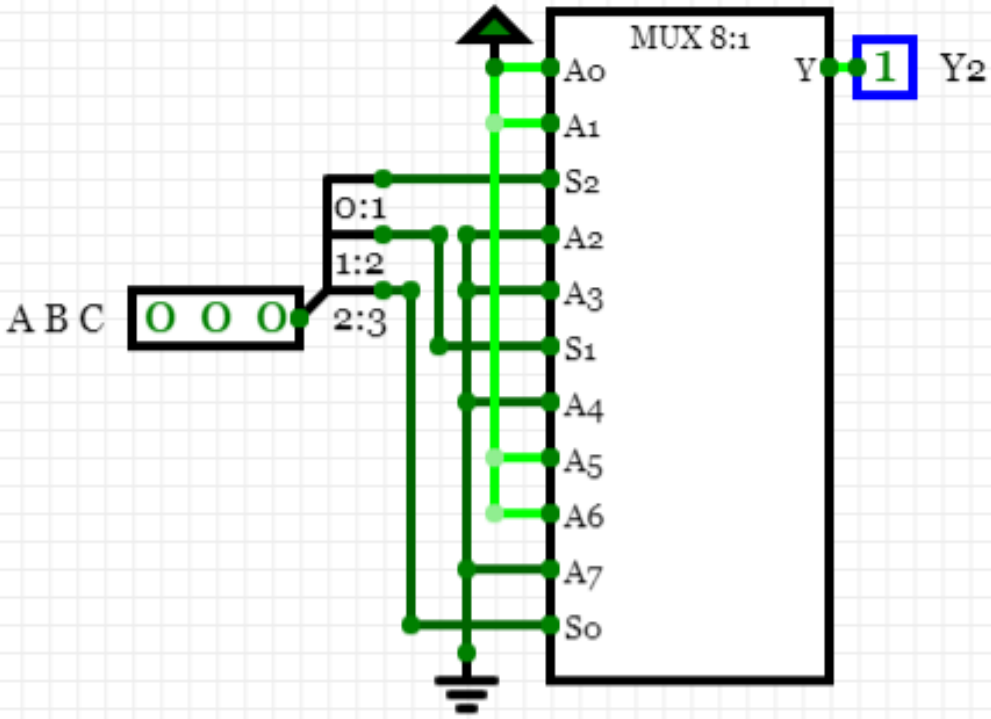


Tabla 2 MUX 4:1

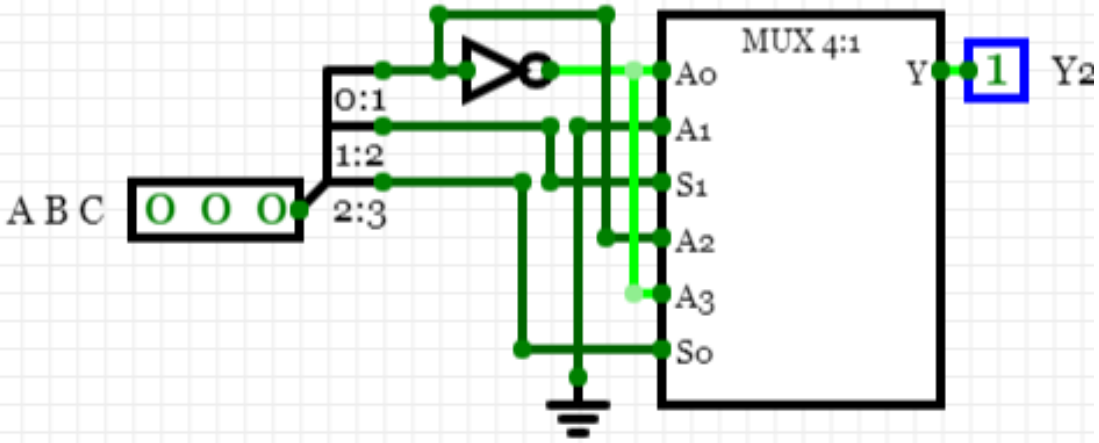
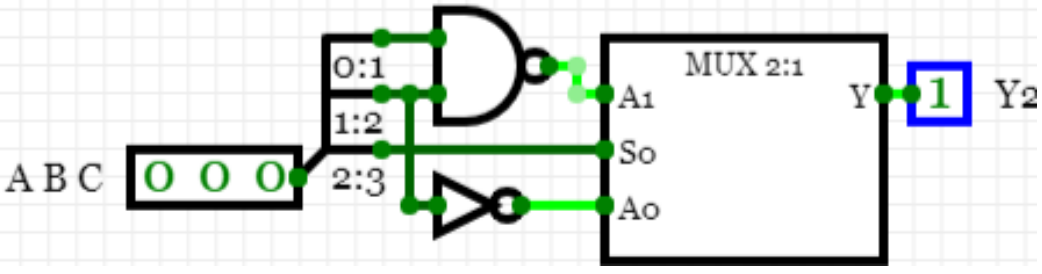


Tabla 2 MUX 2:1



Ejercicio 3

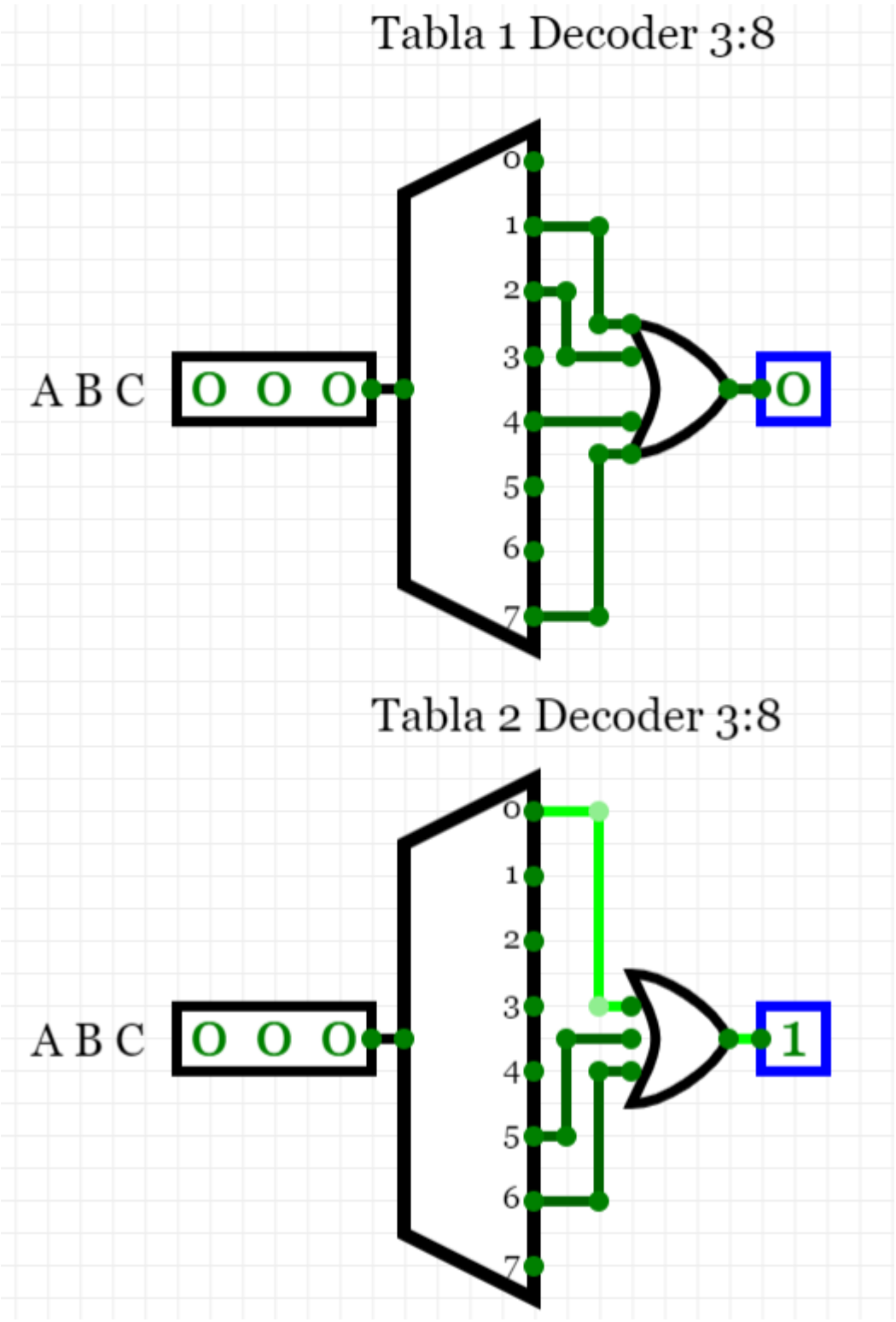


Tabla 1 Decoder 3:8
A B C
O O O
0
1
2
3
4
5
6
7
O
Tabla 2 Decoder 3:8
A B C
O O O
0
1
2
3
4
5
6
7
1

Ejercicio 4

Código del archivo con los módulos: ejercicio04.v

ejercicio04.v ejercicio04_tb.v

D: > AlejandroDigital > electronica_digital1 > lab05dig > ejercicio04 > ejercicio04.v

```
1   //José Alejandro Rodríguez Porras 19131
2   //Electrónica Digital
3   //Lab 5 Ejercicio 4
4   //Módulo MUX 2:1
5   module mux21(input wire a0, a1, s0, output wire y);
6
7       assign y = s0 ? a1 : a0;
8
9   endmodule
10
11  //Módulo MUX 4:1
12  module mux41(input wire a0, a1, a2, a3, s1, s0, output wire y);
13
14      wire y1, y0;
15      mux21 m2_1(a0, a1, s1, y1);
16      mux21 m2_2(a2, a3, s1, y0);
17      mux21 m2(y1, y0, s0, y);
18
19  endmodule
20
21  //Módulo MUX 8:1
22  module mux81(input wire a0, a1, a2 ,a3, a4, a5, a6, a7, s0, s1, s2, output wire y);
23
24      wire y1, y0;
25      mux41 m4_1(a0, a1, a2, a3, s2, s1, y1);
26      mux41 m4_2(a4, a5, a6, a7, s2, s1, y0);
27      mux21 m2(y1, y0, s0, y);
28
29  endmodule
30
31  //Tabla 1 MUX 8:1
32  module t1_81(input wire A, B, C, output wire y);
33
34      wire H, L;
35      assign H = 1;
36      assign L = 0;
37      mux81 T1_8(L, H, H, L, H, L, L, H, A, B, C, y);
38
39  endmodule
40
41  //Tabla 1 MUX 4:1
42  module t1_41(input wire A, B, C, output wire y);
43
44      mux41 T1_4(C, ~C, ~C, C, A, B, y);
45
46  endmodule
47
48  //Tabla 1 MUX 2:1
49  module t1_21(input wire A, B, C, output wire y);
50
51      mux21 T1_2((B^C),~(B^C), A, y);
52
53  endmodule
54
55  //Tabla 2 MUX 8:1
56  module t2_81(input wire A, B, C, output wire y);
57
```

```
58      wire H, L;
59      assign H = 1;
60      assign L = 0;
61      mux81 T2_8(H, H, L, L, L, H, H, L, A, B, C, y);
62
63  endmodule
64
65  //Tabla 2 MUX 4:1
66  module t2_41(input wire A, B, C, output wire y);
67
68      wire L;
69      assign L = 0;
70      mux41 T2_4(~C, L, C, ~C, B, A, y);
71
72  endmodule
73
74  //Tabla 2 MUX 2:1
75  module t2_21(input wire A, B, C, output wire y);
76
77      mux21 T2_2(~B, ~(B & C), A, y);
78
79  endmodule
80
81
```

Código del testbench ejercicio04_tb.v

ejercicio04.v | ejercicio04_tb.v

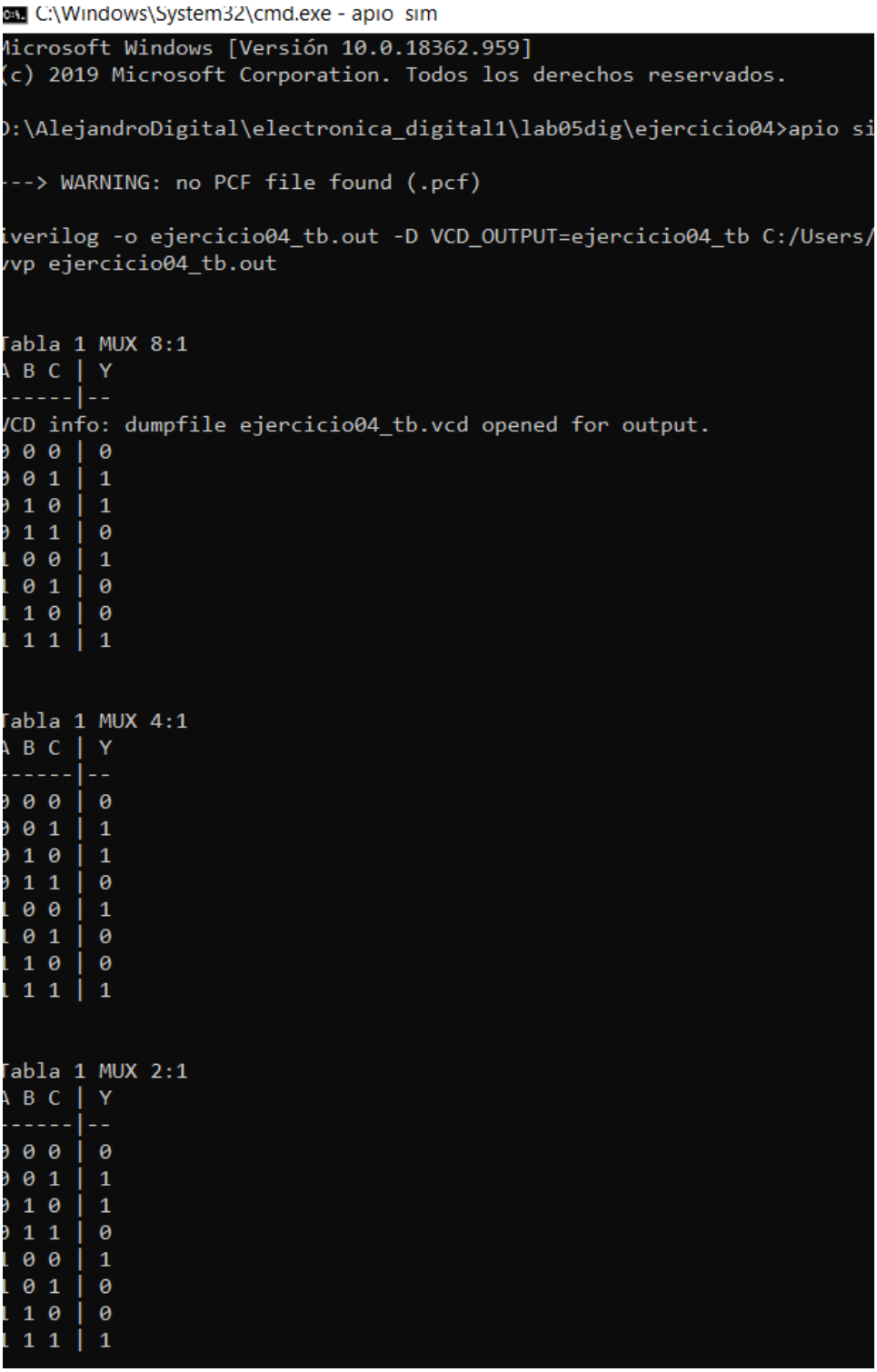
D: > AlejandroDigital > electronica_digital1 > lab05dig > ejercicio04 > ejercicio04_tb.v

```
//José Alejandro Rodríguez Porras 19131
//testbench
module testbench();

//definir variables de inputs para cada ecuación
    reg t1_A8, t1_B8, t1_C8, t1_A4, t1_B4, t1_C4, t1_A2, t1_B2, t1_C2,
    t2_A8, t2_B8, t2_C8, t2_A4, t2_B4, t2_C4, t2_A2, t2_B2, t2_C2;
    wire t1_Y8, t1_Y4, t1_Y2, t2_Y8, t2_Y4, t2_Y2;

 //asignación de las variables a cada uno de los módulos de los mux de cada tabla
 //Tabla 1
    t1_81 T1_8(t1_A8, t1_B8, t1_C8, t1_Y8);
    t1_41 T1_4(t1_A4, t1_B4, t1_C4, t1_Y4);
    t1_21 T1_2(t1_A2, t1_B2, t1_C2, t1_Y2);

//Tabla 2
    t2_81 T2_8(t2_A8, t2_B8, t2_C8, t2_Y8);
    t2_41 T2_4(t2_A4, t2_B4, t2_C4, t2_Y4);
    t2_21 T2_2(t2_A2, t2_B2, t2_C2, t2_Y2);

//Simulación Tabla 1 MUX 8:1
    initial begin
        $display("\n");
        $display("Tabla 1 MUX 8:1");
        $display("A B C | Y");
        $display("------|--");
        $monitor("%b %b %b | %b", t1_A8, t1_B8, t1_C8, t1_Y8);
        t1_A8 = 0; t1_B8 = 0; t1_C8 = 0;
        #1 t1_A8 = 0; t1_B8 = 0; t1_C8 = 1;
        #1 t1_A8 = 0; t1_B8 = 1; t1_C8 = 0;
        #1 t1_A8 = 0; t1_B8 = 1; t1_C8 = 1;
        #1 t1_A8 = 1; t1_B8 = 0; t1_C8 = 0;
        #1 t1_A8 = 1; t1_B8 = 0; t1_C8 = 1;
        #1 t1_A8 = 1; t1_B8 = 1; t1_C8 = 0;
        #1 t1_A8 = 1; t1_B8 = 1; t1_C8 = 1;
    end

//Simulación Tabla 1 MUX 4:1
    initial begin
        #8
        $display("\n");
        $display("Tabla 1 MUX 4:1");
        $display("A B C | Y");
        $display("------|--");
        $monitor("%b %b %b | %b", t1_A4, t1_B4, t1_C4, t1_Y4);
        t1_A4 = 0; t1_B4 = 0; t1_C4 = 0;
        #1 t1_A4 = 0; t1_B4 = 0; t1_C4 = 1;
        #1 t1_A4 = 0; t1_B4 = 1; t1_C4 = 0;
        #1 t1_A4 = 0; t1_B4 = 1; t1_C4 = 1;
        #1 t1_A4 = 1; t1_B4 = 0; t1_C4 = 0;
        #1 t1_A4 = 1; t1_B4 = 0; t1_C4 = 1;
        #1 t1_A4 = 1; t1_B4 = 1; t1_C4 = 0;
        #1 t1_A4 = 1; t1_B4 = 1; t1_C4 = 1;
    end

```

```
//Simulación Tabla 1 MUX 2:1
    initial begin
        #16
        $display("\n");
        $display("Tabla 1 MUX 2:1");
        $display("A B C | Y");
        $display("------|--");
        $monitor("%b %b %b | %b", t1_A2, t1_B2, t1_C2, t1_Y2);
        t1_A2 = 0; t1_B2 = 0; t1_C2 = 0;
        #1 t1_A2 = 0; t1_B2 = 0; t1_C2 = 1;
        #1 t1_A2 = 0; t1_B2 = 1; t1_C2 = 0;
        #1 t1_A2 = 0; t1_B2 = 1; t1_C2 = 1;
        #1 t1_A2 = 1; t1_B2 = 0; t1_C2 = 0;
        #1 t1_A2 = 1; t1_B2 = 0; t1_C2 = 1;
        #1 t1_A2 = 1; t1_B2 = 1; t1_C2 = 0;
        #1 t1_A2 = 1; t1_B2 = 1; t1_C2 = 1;
    end

//Simulación Tabla 2 MUX 8:1
    initial begin
        #24
        $display("\n");
        $display("Tabla 2 MUX 8:1");
        $display("A B C | Y");
        $display("------|--");
        $monitor("%b %b %b | %b", t2_A8, t2_B8, t2_C8, t2_Y8);
        t2_A8 = 0; t2_B8 = 0; t2_C8 = 0;
        #1 t2_A8 = 0; t2_B8 = 0; t2_C8 = 1;
        #1 t2_A8 = 0; t2_B8 = 1; t2_C8 = 0;
        #1 t2_A8 = 0; t2_B8 = 1; t2_C8 = 1;
        #1 t2_A8 = 1; t2_B8 = 0; t2_C8 = 0;
        #1 t2_A8 = 1; t2_B8 = 0; t2_C8 = 1;
        #1 t2_A8 = 1; t2_B8 = 1; t2_C8 = 0;
        #1 t2_A8 = 1; t2_B8 = 1; t2_C8 = 1;
    end

//Simulación Tabla 2 MUX 4:1
    initial begin
        #32
        $display("\n");
        $display("Tabla 2 MUX 4:1");
        $display("A B C | Y");
        $display("------|--");
        $monitor("%b %b %b | %b", t2_A4, t2_B4, t2_C4, t2_Y4);
        t2_A4 = 0; t2_B4 = 0; t2_C4 = 0;
        #1 t2_A4 = 0; t2_B4 = 0; t2_C4 = 1;
        #1 t2_A4 = 0; t2_B4 = 1; t2_C4 = 0;
        #1 t2_A4 = 0; t2_B4 = 1; t2_C4 = 1;
        #1 t2_A4 = 1; t2_B4 = 0; t2_C4 = 0;
        #1 t2_A4 = 1; t2_B4 = 0; t2_C4 = 1;
        #1 t2_A4 = 1; t2_B4 = 1; t2_C4 = 0;
        #1 t2_A4 = 1; t2_B4 = 1; t2_C4 = 1;
    end

```

```
110  //Simulación Tabla 2 MUX 2:1
111      initial begin
112          #40
113          $display("\n");
114          $display("Tabla 2 MUX 2:1");
115          $display("A B C | Y");
116          $display("------|--");
117          $monitor("%b %b %b | %b", t2_A2, t2_B2, t2_C2, t2_Y2);
118          t2_A2 = 0; t2_B2 = 0; t2_C2 = 0;
119          #1 t2_A2 = 0; t2_B2 = 0; t2_C2 = 1;
120          #1 t2_A2 = 0; t2_B2 = 1; t2_C2 = 0;
121          #1 t2_A2 = 0; t2_B2 = 1; t2_C2 = 1;
122          #1 t2_A2 = 1; t2_B2 = 0; t2_C2 = 0;
123          #1 t2_A2 = 1; t2_B2 = 0; t2_C2 = 1;
124          #1 t2_A2 = 1; t2_B2 = 1; t2_C2 = 0;
125          #1 t2_A2 = 1; t2_B2 = 1; t2_C2 = 1;
126      end
127
128      initial
129      #48 $finish;
130
131      initial begin
132          $dumpfile("ejercicio04_tb.vcd");
133          $dumpvars(0,testbench);
134      end
135
136  endmodule
137
```

Output del programa en el cmd



```
Tabla 2 MUX 8:1
A B C | Y
------|--
0 0 0 | 1
0 0 1 | 1
0 1 0 | 0
0 1 1 | 0
1 0 0 | 0
1 0 1 | 1
1 1 0 | 1
1 1 1 | 0


Tabla 2 MUX 4:1
A B C | Y
------|--
0 0 0 | 1
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 0
1 0 1 | 1
1 1 0 | 1
1 1 1 | 0


Tabla 2 MUX 2:1
A B C | Y
------|--
0 0 0 | 1
0 0 1 | 1
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 1
1 1 0 | 1
1 1 1 | 0
gtkwave ejercicio04_tb.vcd ejercicio04_tb.gtkw
```

Diagrama de Timing de todas las señales (entradas y salidas)

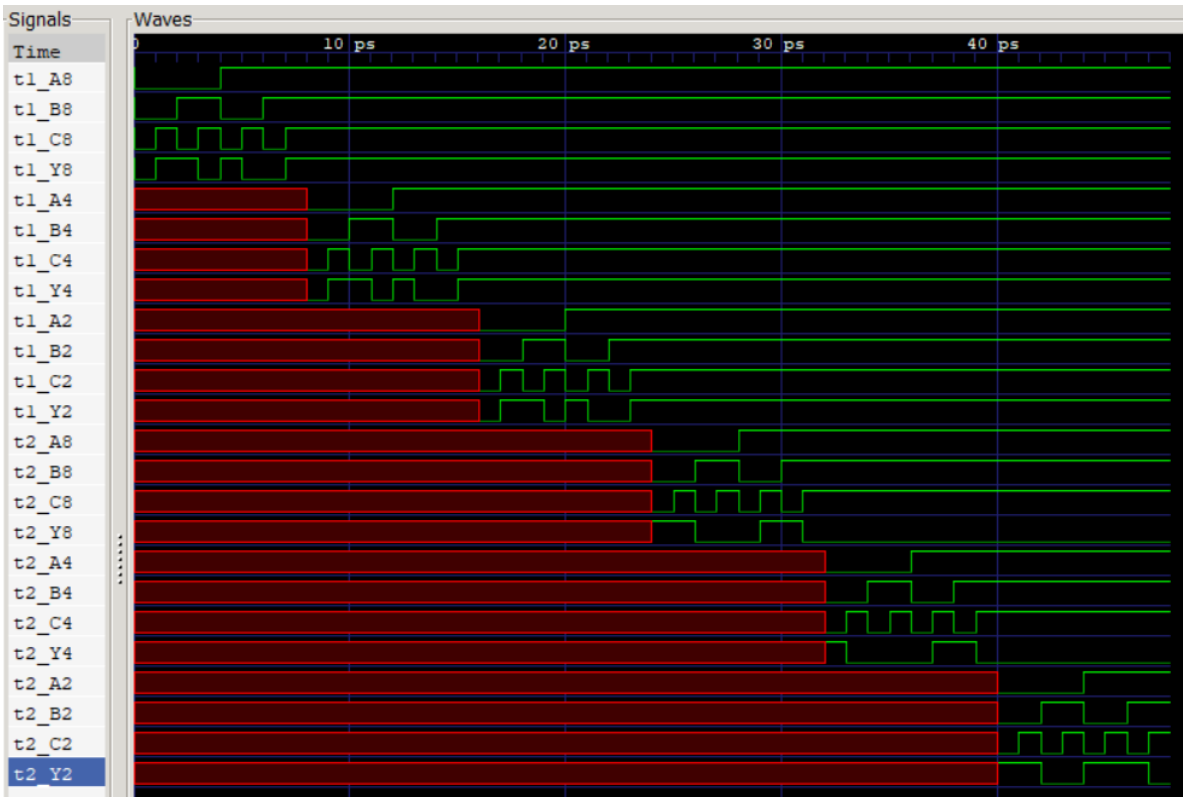
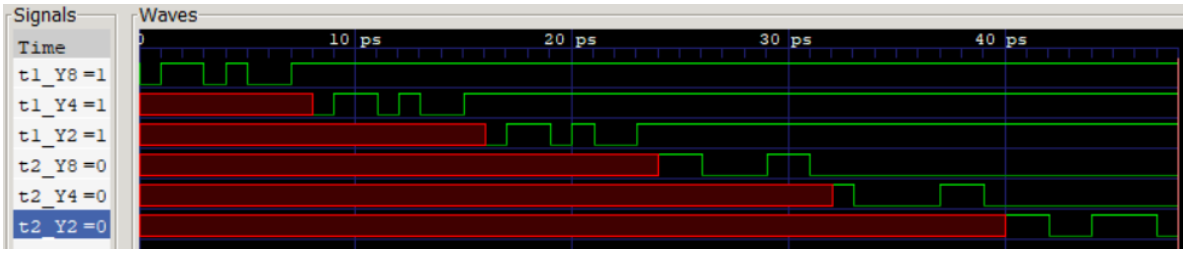


Diagrama de Timing de las salidas de la tabla 1 y 2 para sus MUX 8:1, 4:1 y 2:1



Link repositorio: https://github.com/rod19131/electronica_digital1

Ejercicio 5

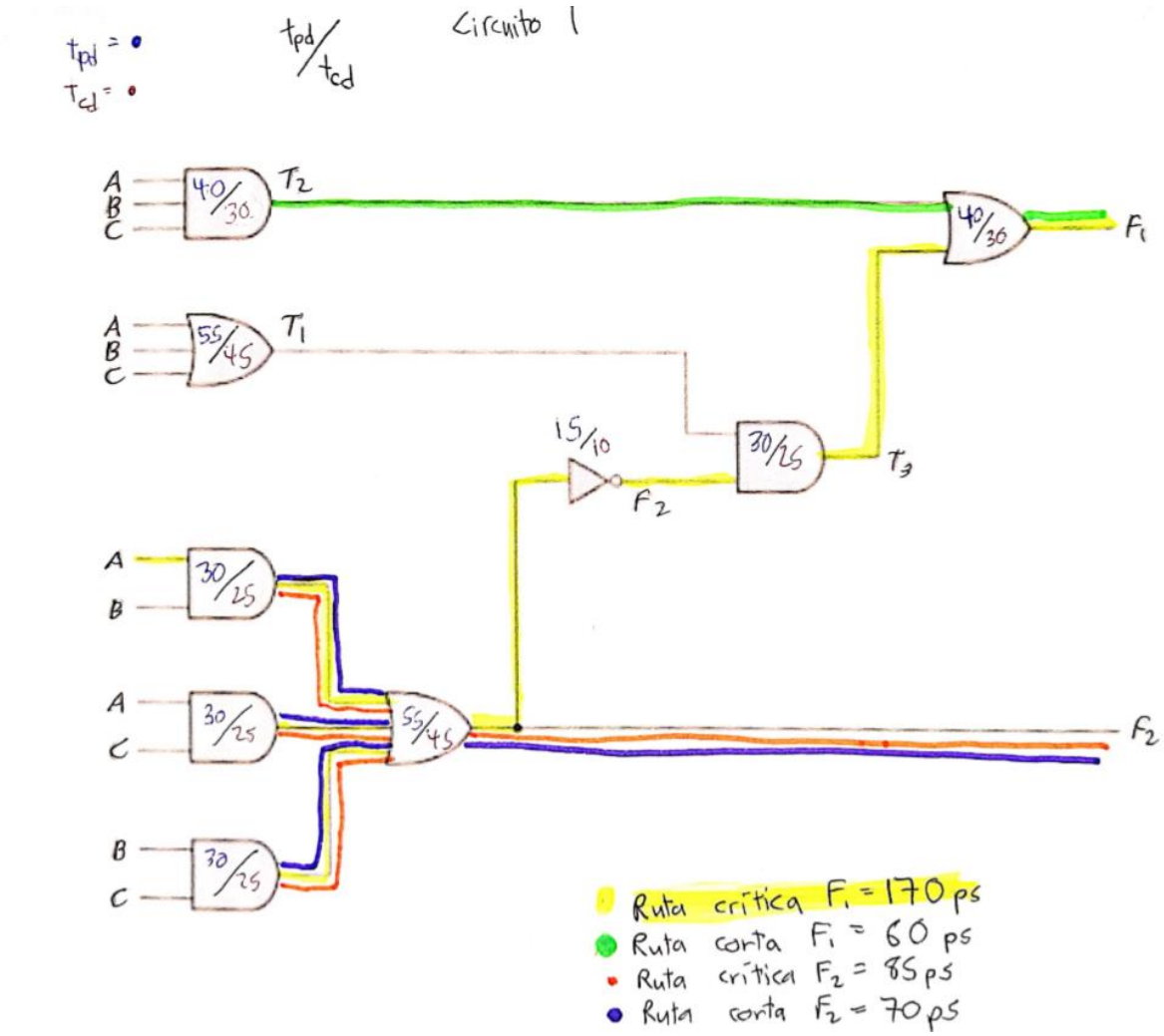
Propagation Delay: Es el tiempo máximo t_{pd} para que la salida del circuito se estabilice.

Contamination Delay: Es el tiempo mínimo t_{cd} para que la salida se desestabilice.

Ruta crítica: Es la ruta a través de puertas lógicas en un circuito donde la sumatoria del t_{pd} de cada puerta es la más alta, es decir el camino por el cual el delay de propagación es el máximo.

Ruta corta: Es la ruta a través de puertas lógicas en un circuito donde la sumatoria del t_{cd} de cada puerta es la más baja, es decir el camino por el cual el delay de contaminación es el mínimo.

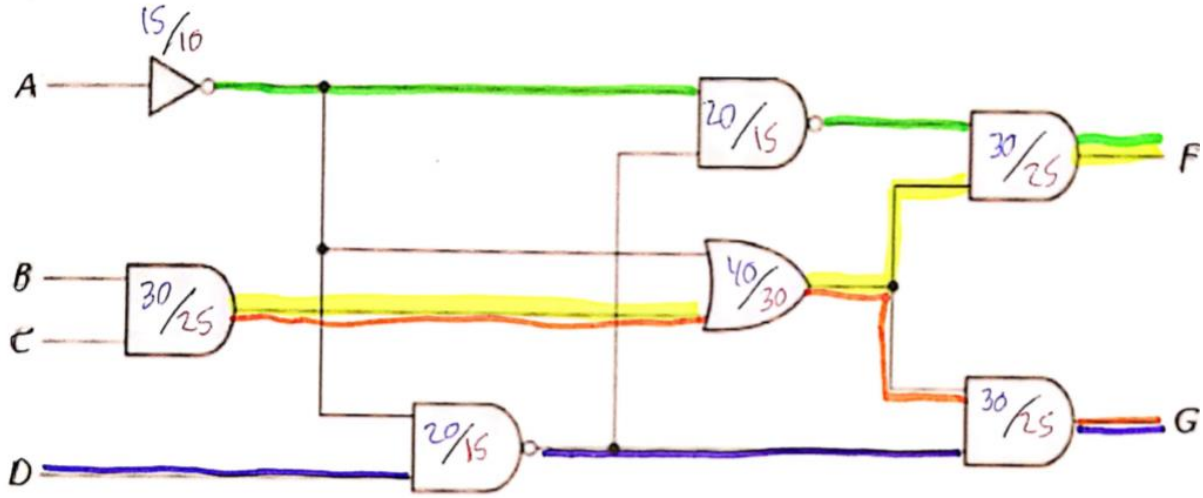
Ejercicio 6



t_{pd} = •
t_{cd} = •

t_{pd}/t_{cd}

Circuito 2



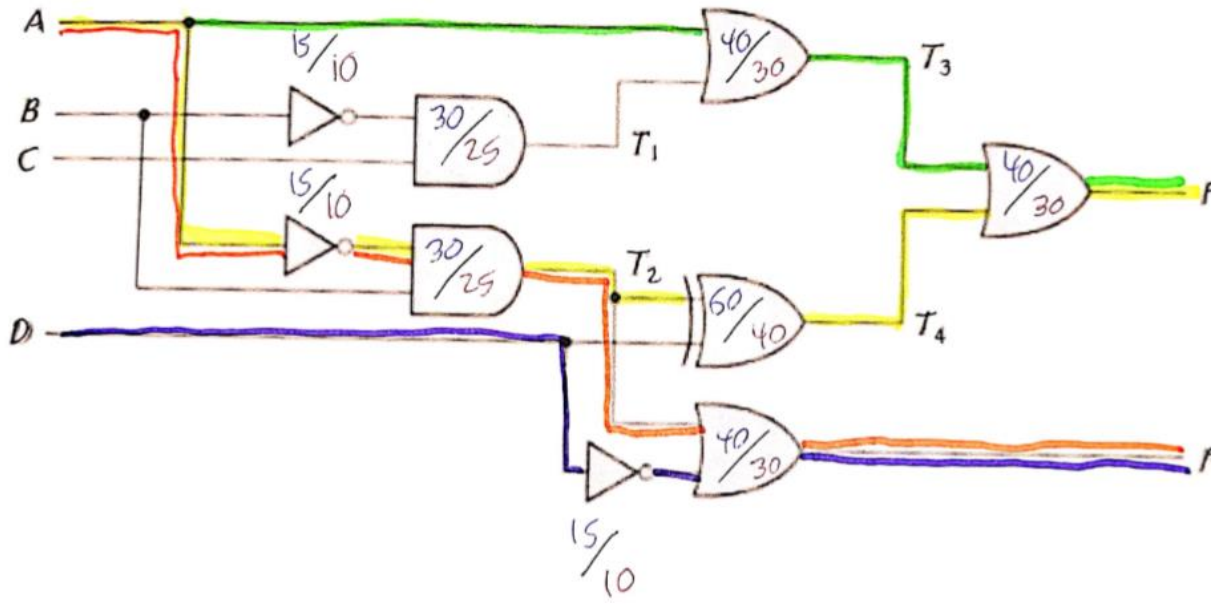
- Ruta crítica F = 100 ps
- Ruta corta F = 50 ps
- Ruta crítica G = 100 ps.
- Ruta corta G = 40 ps

t_{pd} = •

t_{cd} = •

t_{pd}/t_{cd}

Circuito 3

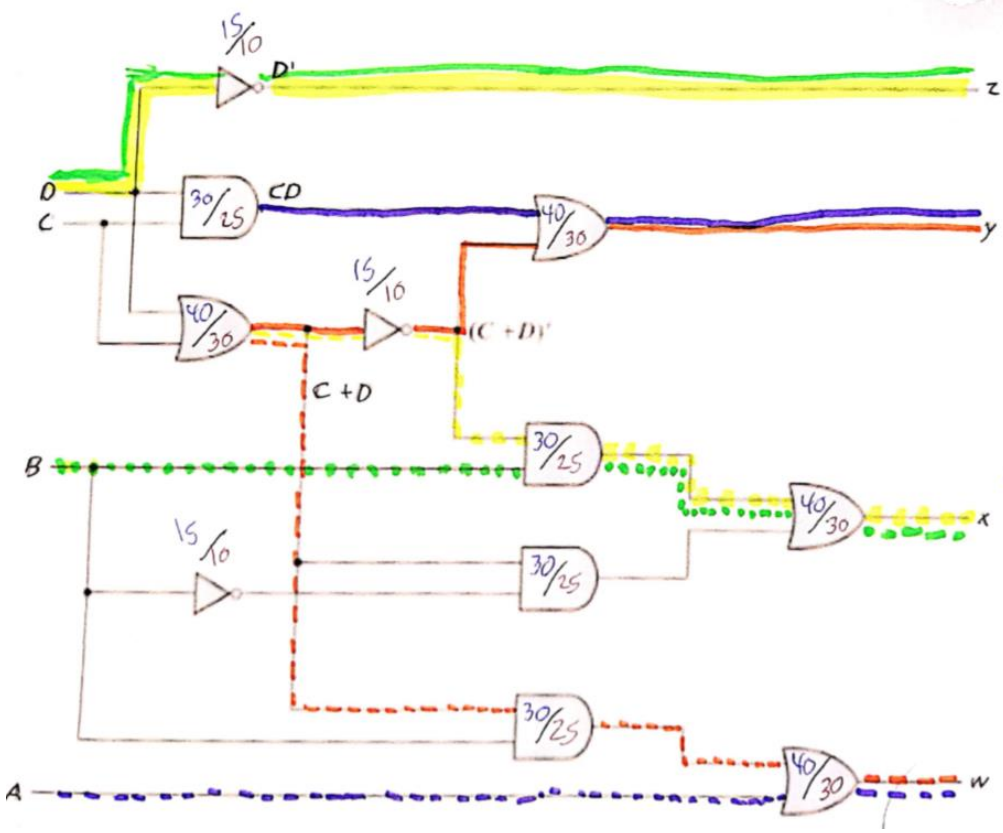


- Ruta crítica F_1 = 145 ps
- Ruta corta F_1 = 60 ps
- Ruta crítica F_2 = 85 ps
- Ruta corta F_2 = 40 ps

$t_{pd} = 0$
$t_{cd} = 0$

t_{pd}/t_{cd}

Circuito 4



- Ruta crítica $z = 15ps$
- Ruta corta $z = 10ps$
- Ruta crítica $y = 95ps$
- Ruta corta $y = 55ps$
- Ruta crítica $x = 125ps$
- Ruta corta $x = 55ps$
- Ruta crítica $w = 110ps$
- Ruta corta $w = 30ps$