Nombre: José Alejandro Rodríguez Porras Carné: 19131 Sección: 10

Laboratorio 4

Ejercicio 1

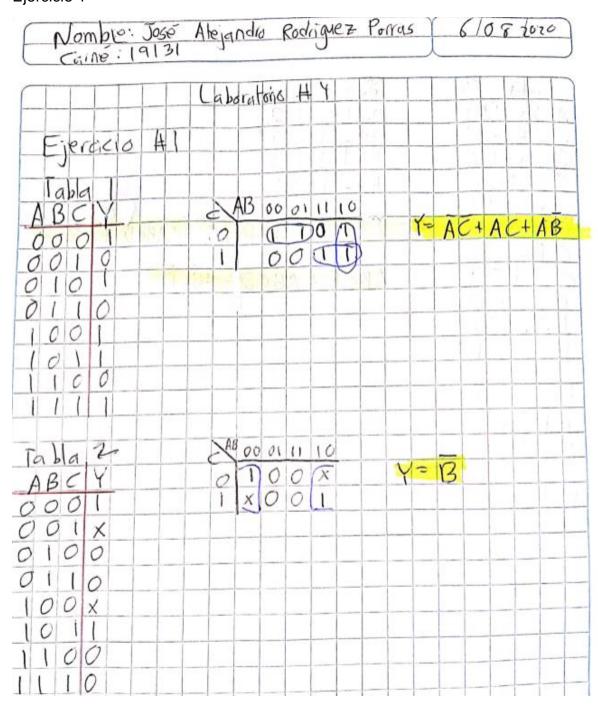
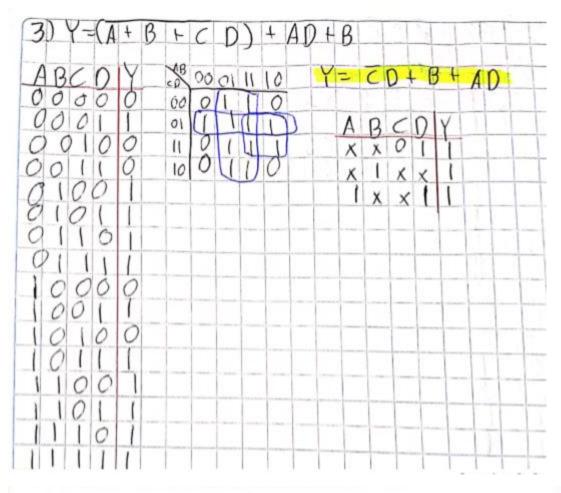


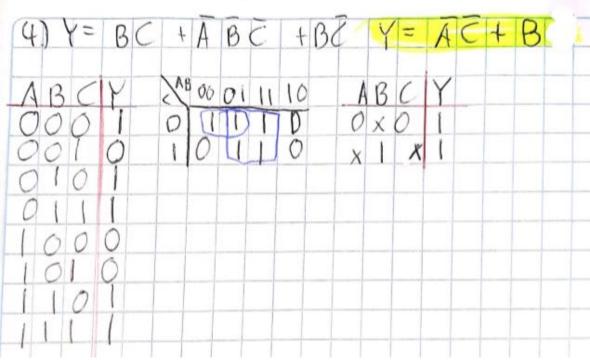
Tabla 3	000011110
ABCDY	00 (1) 0 (1) 0
00001	01000 11000
00100	10 0 DOD
001111	100000000000000000000000000000000000000
01300 4	ABCO + ABCO+ABCO + ABCO +
0 1 10 1	ABCD + ABCD + ABCD
01110	
10011	
101011	
11001	
11010	
11100	

Tabla ABCD 0000 0000	Y X X	01 01 11	00 X 0 X	01 0 X 0	11 1 1	10 10 1	7	5		- 2
00100	0 0 x	Y	>	B	D	+	ΑŌ	+	Ä	C
0001	X I O									
1010	X 							5		
1110	x 1									

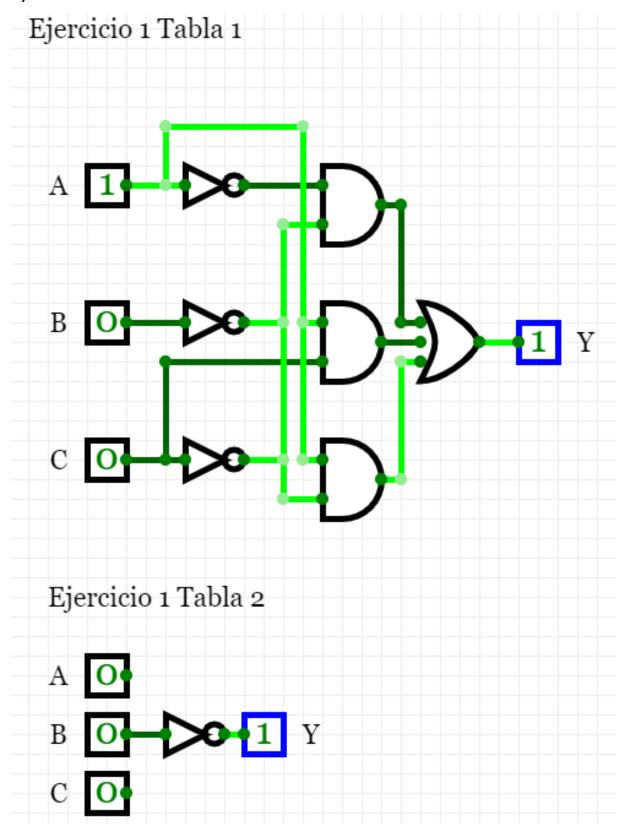
Ejercicio 2

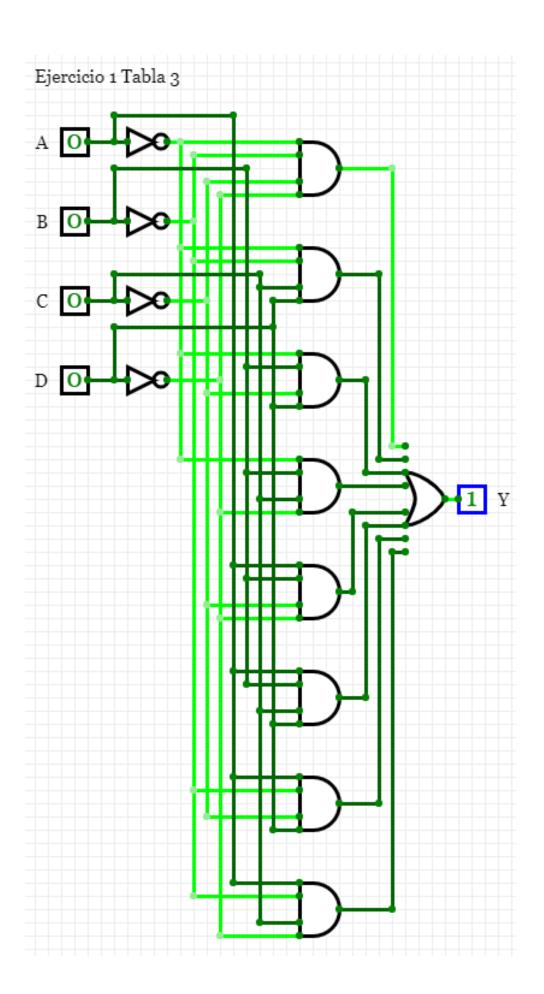
Ejercio	42					Ĭ.	
	CD+AB	300	+(1	+B+	c+p		110
ABCDY 00001 00000 00100 0100 0100 01100 1001 1001 11001	ABCD 11000 1000 1000 1 x 0 x x 1 x x 0	(10 () () () () () () () () () ()	Y			AB	AD
2)Y=ABC+	BZ+BC	Y=	B + A	1+6			
ABCY 0001 0011 0100 0111 1001 1101	00001110	AB 1×					

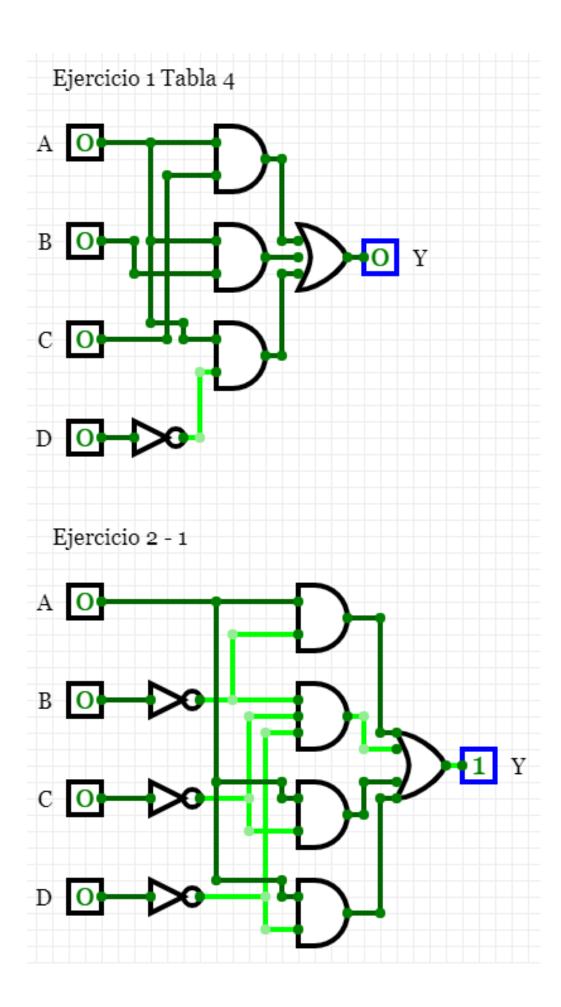


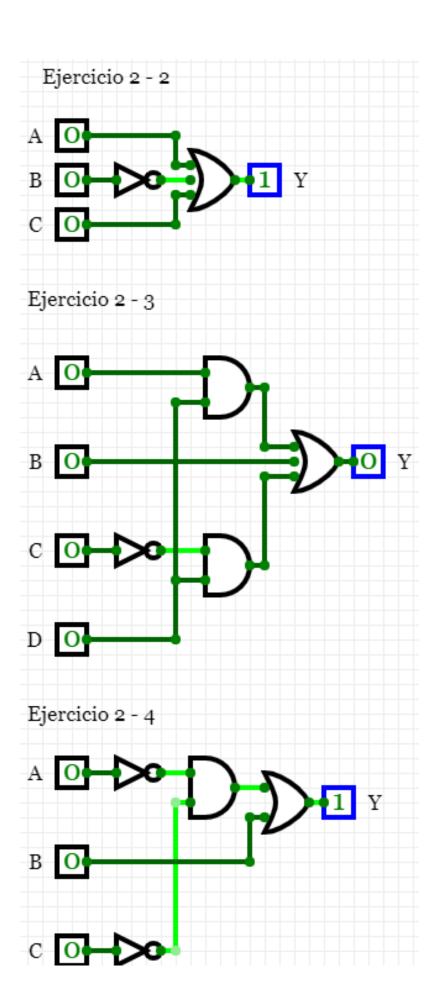


Ejercicio 3









Ejercicio 4 Archivo de módulos del ejercicio04

```
≡ ejercicio04.v ×
                  ≡ ejercicio04_tb.v
D: > AlejandroDigital > electronica_digital1 > lab04dig > ejercicio04 > ≡ ejercicio04.v
       module gle01_1(input wire A, B, C, output wire Y);
           wire na, nb, nc, w1, w2, w3;
           not (na, A);
           not (nb, B);
           not (nc, C);
           and (w1, na, nc);
           and (w2, A, C);
           and (w3, A, nb);
           or (Y, W1, W2, W3);
       endmodule
       module gle01_2(input wire A, B, C, output wire Y);
           wire nb;
           not (nb, B);
           or (Y,nb);
```

```
//Ejercicio 1 Tabla 3: Y=A'B'C'D'+A'B'CD+A'BC'D+A'BCD'+ABC'D'+ABCD+AB'C'D+AB'CD'
module gle01 3(input wire A, B, C, D, output wire Y);
   wire na, nb, nc, nd, w1, w2, w3, w4, w5, w6, w7, w8;
   not (na, A);
   not (nb, B);
   not (nc, C);
    not (nd, D);
   and (w1, na, nb, nc, nd);
    and (w2, na, nb, C, D);
   and (w3, na, B, nc, D);
   and (w4, na, B, C, nd);
   and (w5, A, B, nc, nd);
    and (w6, A, B, C, D);
   and (w7, A, nb, nc, D);
   and (w8, A, nb, C, nd);
   or (Y, w1, w2, w3, w4, w5, w6, w7, w8);
endmodule
//Ejercicio 1 Tabla 4: Y=BD+AD'+AC
module gle01_4(input wire A, B, C, D, output wire Y);
   wire nd, w1, w2, w3;
   not (nd, D);
    and (w1, B, D);
   and (w2, A, nd);
   and (w3, A, C);
   or (Y, W1, W2, W3);
endmodule
```

```
//Módulos con operadores lógicos
     //Ejercicio 2 -1): Y=B'C'D'+AC'+AB'+AD'
67 v module ope02 1(input wire A, B, C, D, output wire Y);
          assign Y = ( B \& C \& D) | (A \& C) | (A \& B) | (A \& D);
70
71
     endmodule
72
     //Ejercicio 2 -2): Y=B'+A+C
74 v module ope02 2(input wire A, B, C, output wire Y);
75
          assign Y = (\sim B) \mid (A) \mid (C);
76
78
     endmodule
79
     //Ejercicio 2 -3): Y=C'D+B+AD
81 ∨ module ope02_3(input wire A, B, C, D, output wire Y);
82
          assign Y = ( ( C \& D) | (B) | (A \& D);
     endmodule
     //Ejercicio 2 -4): Y=A'C'+B
88 v module ope02_4(input wire A, B, C, output wire Y);
          assign Y = (\sim A \& \sim C) \mid (B);
     endmodule
```

Archivo de la simulación del testbench ejercicio04_tb

```
//Simulación Ejercicio 1 Ecuación 2
    initial begin
        #8
        $display("\n");
        $display("A B C | Y");
        $display("----|--");
        $monitor("%b %b %b | %b", e1A2, e1B2, e1C2, e1Y2);
        e1A2 = 0; e1B2 = 0; e1C2 = 0;
        #1 e1A2 = 0; e1B2 = 0; e1C2 = 1;
        #1 e1A2 = 0; e1B2 = 1; e1C2 = 0;
        #1 e1A2 = 0; e1B2 = 1; e1C2 = 1;
        #1 e1A2 = 1; e1B2 = 0; e1C2 = 0;
        #1 e1A2 = 1; e1B2 = 0; e1C2 = 1;
        #1 e1A2 = 1; e1B2 = 1; e1C2 = 0;
        #1 e1A2 = 1; e1B2 = 1; e1C2 = 1;
    end
```

```
//Simulación Ejercicio 1 Ecuación 3
         initial begin
             #16
             $display("\n");
             $display("A B C D | Y");
             $display("----|--");
             $monitor("%b %b %b %b | %b", e1A3, e1B3, e1C3, e1D3, e1Y3);
             e1A3 = 0; e1B3 = 0; e1C3 = 0; e1D3 = 0;
             #1 e1A3 = 0; e1B3 = 0; e1C3 = 0; e1D3 = 1;
             #1 e1A3 = 0; e1B3 = 0; e1C3 = 1; e1D3 = 0;
             #1 e1A3 = 0; e1B3 = 0; e1C3 = 1; e1D3 = 1;
             #1 e1A3 = 0; e1B3 = 1; e1C3 = 0; e1D3 = 0;
             #1 e1A3 = 0; e1B3 = 1; e1C3 = 0; e1D3 = 1;
             #1 e1A3 = 0; e1B3 = 1; e1C3 = 1; e1D3 = 0;
             #1 e1A3 = 0; e1B3 = 1; e1C3 = 1; e1D3 = 1;
             #1 e1A3 = 1; e1B3 = 0; e1C3 = 0; e1D3 = 0;
70
             #1 e1A3 = 1; e1B3 = 0; e1C3 = 0; e1D3 = 1;
71
             #1 e1A3 = 1; e1B3 = 0; e1C3 = 1; e1D3 = 0;
             #1 e1A3 = 1; e1B3 = 0; e1C3 = 1; e1D3 = 1;
             #1 e1A3 = 1; e1B3 = 1; e1C3 = 0; e1D3 = 0;
             #1 e1A3 = 1; e1B3 = 1; e1C3 = 0; e1D3 = 1;
             #1 e1A3 = 1; e1B3 = 1; e1C3 = 1; e1D3 = 0;
             #1 e1A3 = 1; e1B3 = 1; e1C3 = 1; e1D3 = 1;
         end
78
```

```
79 ∨ //Simulación Ejercicio 1 Ecuación 4
         initial begin
             #32
             $display("\n");
             $display("A B C D | Y");
             $display("-----|--");
             $monitor("%b %b %b %b | %b", e1A4, e1B4, e1C4, e1D4, e1Y4);
             e1A4 = 0; e1B4 = 0; e1C4 = 0; e1D4 = 0;
             #1 e1A4 = 0; e1B4 = 0; e1C4 = 0; e1D4 = 1;
             #1 e1A4 = 0; e1B4 = 0; e1C4 = 1; e1D4 = 0;
             #1 e1A4 = 0; e1B4 = 0; e1C4 = 1; e1D4 = 1;
             #1 e1A4 = 0; e1B4 = 1; e1C4 = 0; e1D4 = 0;
             #1 e1A4 = 0; e1B4 = 1; e1C4 = 0; e1D4 = 1;
             #1 e1A4 = 0; e1B4 = 1; e1C4 = 1; e1D4 = 0;
             #1 e1A4 = 0; e1B4 = 1; e1C4 = 1; e1D4 = 1;
             #1 e1A4 = 1; e1B4 = 0; e1C4 = 0; e1D4 = 0;
             #1 \ e1A4 = 1; \ e1B4 = 0; \ e1C4 = 0; \ e1D4 = 1;
             #1 e1A4 = 1; e1B4 = 0; e1C4 = 1; e1D4 = 0;
             #1 e1A4 = 1; e1B4 = 0; e1C4 = 1; e1D4 = 1;
             #1 e1A4 = 1; e1B4 = 1; e1C4 = 0; e1D4 = 0;
             #1 e1A4 = 1; e1B4 = 1; e1C4 = 0; e1D4 = 1;
             #1 e1A4 = 1; e1B4 = 1; e1C4 = 1; e1D4 = 0;
             #1 e1A4 = 1; e1B4 = 1; e1C4 = 1; e1D4 = 1;
```

```
104 ∨ //Simulación Ejercicio 2 Ecuación 1
          initial begin
              #48
              $display("\n");
              $display("A B C D | Y");
              $display("----|--");
110
              $monitor("%b %b %b %b | %b", e2A1, e2B1, e2C1, e2D1, e2Y1);
              e2A1 = 0; e2B1 = 0; e2C1 = 0; e2D1 = 0;
112
              #1 e2A1 = 0; e2B1 = 0; e2C1 = 0; e2D1 = 1;
113
              #1 e2A1 = 0; e2B1 = 0; e2C1 = 1; e2D1 = 0;
114
              #1 e2A1 = 0; e2B1 = 0; e2C1 = 1; e2D1 = 1;
              #1 e2A1 = 0; e2B1 = 1; e2C1 = 0; e2D1 = 0;
116
              #1 e2A1 = 0; e2B1 = 1; e2C1 = 0; e2D1 = 1;
117
              #1 e2A1 = 0; e2B1 = 1; e2C1 = 1; e2D1 = 0;
118
              #1 e2A1 = 0; e2B1 = 1; e2C1 = 1; e2D1 = 1;
119
              #1 e2A1 = 1; e2B1 = 0; e2C1 = 0; e2D1 = 0;
120
              #1 e2A1 = 1; e2B1 = 0; e2C1 = 0; e2D1 = 1;
121
              #1 e2A1 = 1; e2B1 = 0; e2C1 = 1; e2D1 = 0;
122
              #1 e2A1 = 1; e2B1 = 0; e2C1 = 1; e2D1 = 1;
123
              #1 e2A1 = 1; e2B1 = 1; e2C1 = 0; e2D1 = 0;
124
              #1 e2A1 = 1; e2B1 = 1; e2C1 = 0; e2D1 = 1;
125
              #1 e2A1 = 1; e2B1 = 1; e2C1 = 1; e2D1 = 0;
126
              #1 e2A1 = 1; e2B1 = 1; e2C1 = 1; e2D1 = 1;
127
128
```

```
//Simulación Ejercicio 2 Ecuación 2
129
          initial begin
130
              #64
131
132
              $display("\n");
              $display("A B C | Y");
133
              $display("----|--");
134
              $monitor("%b %b %b | %b", e2A2, e2B2, e2C2, e2Y2);
135
              e2A2 = 0; e2B2 = 0; e2C2 = 0;
136
              #1 e2A2 = 0; e2B2 = 0; e2C2 = 1;
137
              #1 e2A2 = 0; e2B2 = 1; e2C2 = 0;
138
139
              #1 e2A2 = 0; e2B2 = 1; e2C2 = 1;
140
              #1 e2A2 = 1; e2B2 = 0; e2C2 = 0;
141
              #1 e2A2 = 1; e2B2 = 0; e2C2 = 1;
142
              #1 e2A2 = 1; e2B2 = 1; e2C2 = 0;
143
              #1 e2A2 = 1; e2B2 = 1; e2C2 = 1;
144
          end
145
```

```
//Simulación Ejercicio 2 Ecuación 3
          initial begin
              #72
              $display("\n");
              $display("A B C D | Y");
150
151
              $display("----|--");
              $monitor("%b %b %b %b | %b", e2A3, e2B3, e2C3, e2D3, e2Y3);
152
              e2A3 = 0; e2B3 = 0; e2C3 = 0; e2D3 = 0;
153
154
              #1 e2A3 = 0; e2B3 = 0; e2C3 = 0; e2D3 = 1;
155
              #1 e2A3 = 0; e2B3 = 0; e2C3 = 1; e2D3 = 0;
156
              #1 e2A3 = 0; e2B3 = 0; e2C3 = 1; e2D3 = 1;
              #1 e2A3 = 0; e2B3 = 1; e2C3 = 0; e2D3 = 0;
157
158
              #1 e2A3 = 0; e2B3 = 1; e2C3 = 0; e2D3 = 1;
159
              #1 e2A3 = 0; e2B3 = 1; e2C3 = 1; e2D3 = 0;
              #1 e2A3 = 0; e2B3 = 1; e2C3 = 1; e2D3 = 1;
              #1 e2A3 = 1; e2B3 = 0; e2C3 = 0; e2D3 = 0;
              #1 e2A3 = 1; e2B3 = 0; e2C3 = 0; e2D3 = 1;
              #1 e2A3 = 1; e2B3 = 0; e2C3 = 1; e2D3 = 0;
              #1 e2A3 = 1; e2B3 = 0; e2C3 = 1; e2D3 = 1;
              #1 e2A3 = 1; e2B3 = 1; e2C3 = 0; e2D3 = 0;
              #1 e2A3 = 1; e2B3 = 1; e2C3 = 0; e2D3 = 1;
              #1 e2A3 = 1; e2B3 = 1; e2C3 = 1; e2D3 = 0;
              #1 e2A3 = 1; e2B3 = 1; e2C3 = 1; e2D3 = 1;
170
```

```
//Simulación Ejercicio 2 Ecuación 4
171
          initial begin
172
173
              #88
174
              $display("\n");
              $display("A B C | Y");
175
              $display("----|--");
176
              $monitor("%b %b %b | %b", e2A4, e2B4, e2C4, e2Y4);
177
              e2A4 = 0; e2B4 = 0; e2C4 = 0;
178
              #1 e2A4 = 0; e2B4 = 0; e2C4 = 1;
179
180
              #1 e2A4 = 0; e2B4 = 1; e2C4 = 0;
181
              #1 e2A4 = 0; e2B4 = 1; e2C4 = 1;
182
              #1 e2A4 = 1; e2B4 = 0; e2C4 = 0;
183
              #1 e2A4 = 1; e2B4 = 0; e2C4 = 1;
              #1 e2A4 = 1; e2B4 = 1; e2C4 = 0;
184
              #1 e2A4 = 1; e2B4 = 1; e2C4 = 1;
185
186
          end
187
          initial
188
          #97 $finish;
189
190
191
        initial begin
          $dumpfile("ejercicio04_tb.vcd");
192
          $dumpvars(0, testbench);
193
194
195
      endmodule
196
```

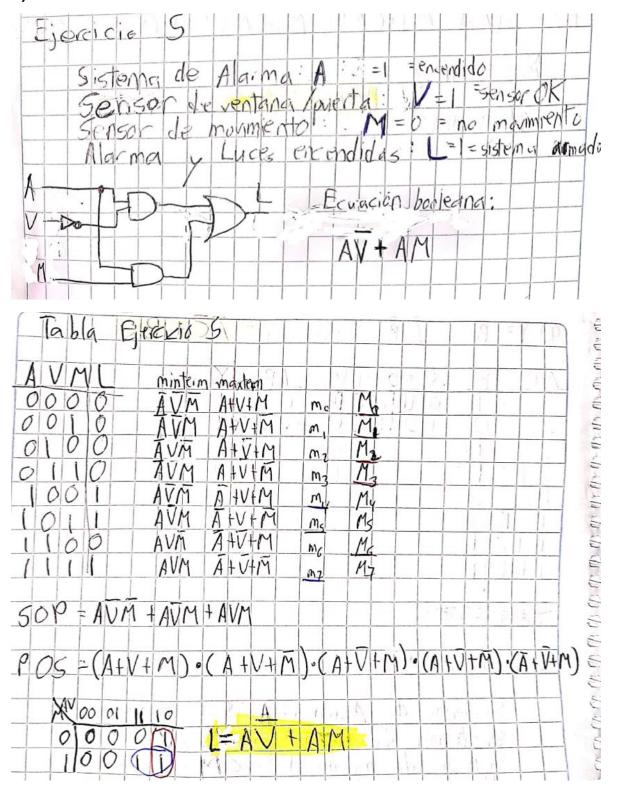
Diagrama de Timing

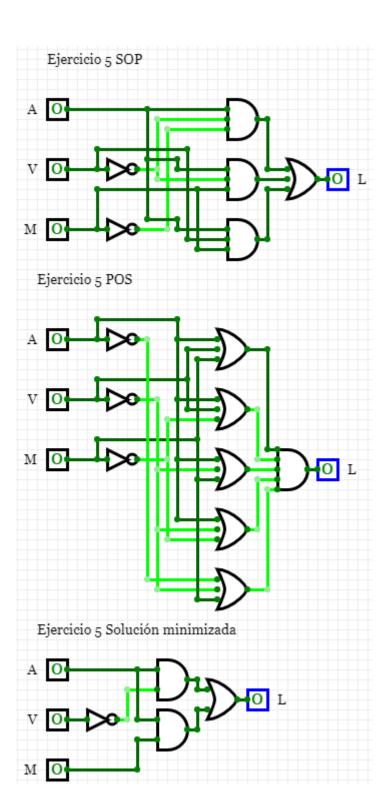


Diagrama de timing de las salidas



Ejercicio 5





Output del programa en cmd

```
-> WARNING: no PCF file found (.pcf)
```

Código de ejercicio05 (módulos de gate level modelling y behavioral modelling)

```
≡ ejercicio05_tb.v

■ ejercicio05_tb.v
                    ≡ ejercicio05.v X
D: > AlejandroDigital > electronica_digital1 > lab04dig > ejercicio05 > ≡ ejercicio05.v
     //Variables:
      //V = sensor de ventana/puerta : 1 = OK
      //L = Alarma y luces encendidas : 1 = se enciende
      //SOP = AV'M'+AV'M+AVM
      module gsop05(input wire A, V, M, output wire L);
           wire nv, nm, w1, w2, w3;
          not (nv, V);
          not (nm, M);
          and (w1, A, nv, nm);
           and (w2, A, nv, M);
           and (w3, A, V, M);
           or (L, w1, w2, w3);
      module gpos05(input wire A, V, M, output wire L);
           wire na, nv, nm, w1, w2, w3, w4, w5;
          not (na, A);
          not (nv, V);
          not (nm, M);
           or (w1, A, V, M);
           or (w2, A, V, nm);
           or (w3, A, nv, M);
          or (w4, A, nv, nm);
           or (w5, na, nv, M);
           and (L, w1, w2, w3, w4, w5);
      endmodule
      //Ecuación minimizada con mapa de Karnaugh: Y = AV'+AM
      module g05(input wire A, V, M, output wire L);
           wire nv, w1, w2;
           not (nv, V);
           and (w1, A, nv);
           and (w2, A, M);
           or (L, w1, w2);
```

```
//Módulos con Behavioral Modelling
//SOP = AV'M'+AV'M+AVM
module opsop05(input wire A, V, M, output wire L);

assign L = (A & ~V & ~M) | (A & ~V & M);

endmodule

//POS = (A+V+M)*(A+V+M')*(A+V'+M)*(A+V'+M')*(A'+V'+M)

module oppos05(input wire A, V, M, output wire L);

assign L = (A | V | M) & (A | V | ~M) & (A | ~V | M) & (A | ~V | ~M) & (A | ~V | M);

endmodule

//Ecuación minimizada con mapa de Karnaugh: Y = AV'+AM
module op05(input wire A, V, M, output L);

assign L = (A & ~V) | (A & M);

assign L = (A & ~V) | (A & M);

endmodule
```

Código de ejercicio05_tb (test bench con las simulaciones para cada uno de los módulos)

```
≡ ejercicio05_tb.v X

    ejercicio05.v

D: > AlejandroDigital > electronica_digital1 > lab04dig > ejercicio05 > ≡ ejercicio05_tb.v
       module testbench();
           //definir variables de inputs para cada ecuación
          reg gsopA, gsopV, gsopM, gposA, gposV, gposM, g5A, g5V, g5M,
          opsopA, opsopV, opsopM, opposA, opposV, opposM, op5A, op5V, op5M;
          wire gsopL, gposL, g5L, opsopL, opposL, op5L;
           //módulos con gate level modelling
          gsop05 GS5(gsopA, gsopV, gsopM, gsopL);
          gpos05 GP5(gposA, gposV, gposM, gposL);
          g05 G5(g5A, g5V, g5M, g5L);
          //módulos con operadores lógicos
           opsop05 OPS5(opsopA, opsopV, opsopM, opsopL);
          oppos05 OPP5(opposA, opposV, opposM, opposL);
          op05 OP5(op5A, op5V, op5M, op5L);
               $display("A B C | Y");
               $display("-----|--");
              $monitor("%b %b %b | %b", gsopA, gsopV, gsopM, gsopL);
               gsopA = 0; gsopV = 0; gsopM = 0;
              #1 gsopA = 0; gsopV = 0; gsopM = 1;
              #1 gsopA = 0; gsopV = 1; gsopM = 0;
              #1 gsopA = 0; gsopV = 1; gsopM = 1;
              #1 gsopA = 1; gsopV = 0; gsopM = 0;
              #1 gsopA = 1; gsopV = 0; gsopM = 1;
              #1 gsopA = 1; gsopV = 1; gsopM = 0;
               #1 gsopA = 1; gsopV = 1; gsopM = 1;
           //Simulación pos
           initial begin
              #8
               $display("\n");
              $display("A B C | Y");
              $display("-----|--");
              $monitor("%b %b %b | %b", gposA, gposV, gposM, gposL);
              gposA = 0; gposV = 0; gposM = 0;
              #1 gposA = 0; gposV = 0; gposM = 1;
              #1 gposA = 0; gposV = 1; gposM = 0;
              #1 gposA = 0; gposV = 1; gposM = 1;
              #1 gposA = 1; gposV = 0; gposM = 0;
              #1 gposA = 1; gposV = 0; gposM = 1;
               #1 gposA = 1; gposV = 1; gposM = 0;
               #1 gposA = 1; gposV = 1; gposM = 1;
```

```
//Simulación ecuación minimizada
initial begin
    #16
    $display("\n");
    $display("A B C | Y");
    $display("-----|--");
    $monitor("%b %b %b | %b", g5A, g5V, g5M, g5L);
    g5A = 0; g5V = 0; g5M = 0;
    #1 g5A = 0; g5V = 0; g5M = 1;
    #1 g5A = 0; g5V = 1; g5M = 0;
    #1 g5A = 0; g5V = 1; g5M = 1;
    #1 g5A = 1; g5V = 0; g5M = 0;
    #1 g5A = 1; g5V = 0; g5M = 1;
    #1 g5A = 1; g5V = 1; g5M = 0;
    #1 g5A = 1; g5V = 1; g5M = 1;
//Simulación de los módulos con behavioral modelling
//Simulación sop
initial begin
    #24
    $display("\n");
    $display("A B C | Y");
    $display("----|--");
    $monitor("%b %b %b | %b", opsopA, opsopV, opsopM, opsopL);
    opsopA = 0; opsopV = 0; opsopM = 0;
    #1 opsopA = 0; opsopV = 0; opsopM = 1;
    #1 opsopA = 0; opsopV = 1; opsopM = 0;
    #1 opsopA = 0; opsopV = 1; opsopM = 1;
    #1 opsopA = 1; opsopV = 0; opsopM = 0;
    #1 opsopA = 1; opsopV = 0; opsopM = 1;
    #1 \text{ opsopA} = 1; \text{ opsopV} = 1; \text{ opsopM} = 0;
    #1 opsopA = 1; opsopV = 1; opsopM = 1;
end
//Simulación pos
initial begin
    #32
    $display("\n");
    $display("A B C | Y");
    $display("-----|--");
    $monitor("%b %b %b | %b", opposA, opposV, opposM, opposL);
    opposA = 0; opposV = 0; opposM = 0;
    #1 opposA = 0; opposV = 0; opposM = 1;
    #1 opposA = 0; opposV = 1; opposM = 0;
    #1 opposA = 0; opposV = 1; opposM = 1;
    #1 opposA = 1; opposV = 0; opposM = 0;
    #1 opposA = 1; opposV = 0; opposM = 1;
    #1 opposA = 1; opposV = 1; opposM = 0;
    #1 opposA = 1; opposV = 1; opposM = 1;
```

```
105
            //Simulación ecuación minimizada
106 🗸
            initial begin
107
                 #40
108
                 $display("\n");
109
                 $display("A B C | Y");
110
                 $display("-----|--");
111
                 $monitor("%b %b %b | %b", op5A, op5V, op5M, op5L);
112
                 op5A = 0; op5V = 0; op5M = 0;
113
                 #1 \text{ op5A} = 0; op5V = 0; op5M = 1;
114
                 #1 \text{ op5A} = 0; op5V = 1; op5M = 0;
                 #1 \text{ op5A} = 0; \text{ op5V} = 1; \text{ op5M} = 1;
115
116
                 #1 \text{ op5A} = 1; \text{ op5V} = 0; \text{ op5M} = 0;
117
                 #1 \text{ op5A} = 1; \text{ op5V} = 0; \text{ op5M} = 1;
118
                 #1 \text{ op5A} = 1; \text{ op5V} = 1; \text{ op5M} = 0;
119
                 #1 \text{ op5A} = 1; \text{ op5V} = 1; \text{ op5M} = 1;
120
            end
121
122
            initial
123
            #49 $finish;
124
125 ∨ //generación del archivo vcd
         initial begin
126 🗸
            $dumpfile("ejercicio05_tb.vcd");
127
128
            $dumpvars(0, testbench);
129
          end
130
131
       endmodule
```

Diagrama de timing del ejercicio 5

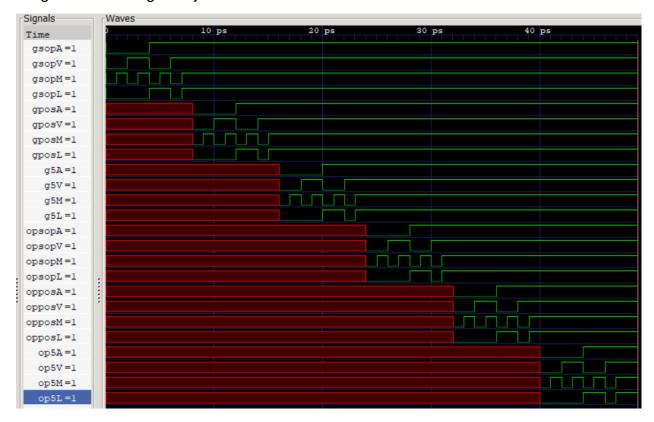


Diagrama de timing de las salidas de las ecuaciones SOP, POS y minimizada con Gate Level Modelling (g) y Behavioral Modelling (op)



Link repositorio: https://github.com/rod19131/electronica_digital1