Introduction to Programmable Logic Devices

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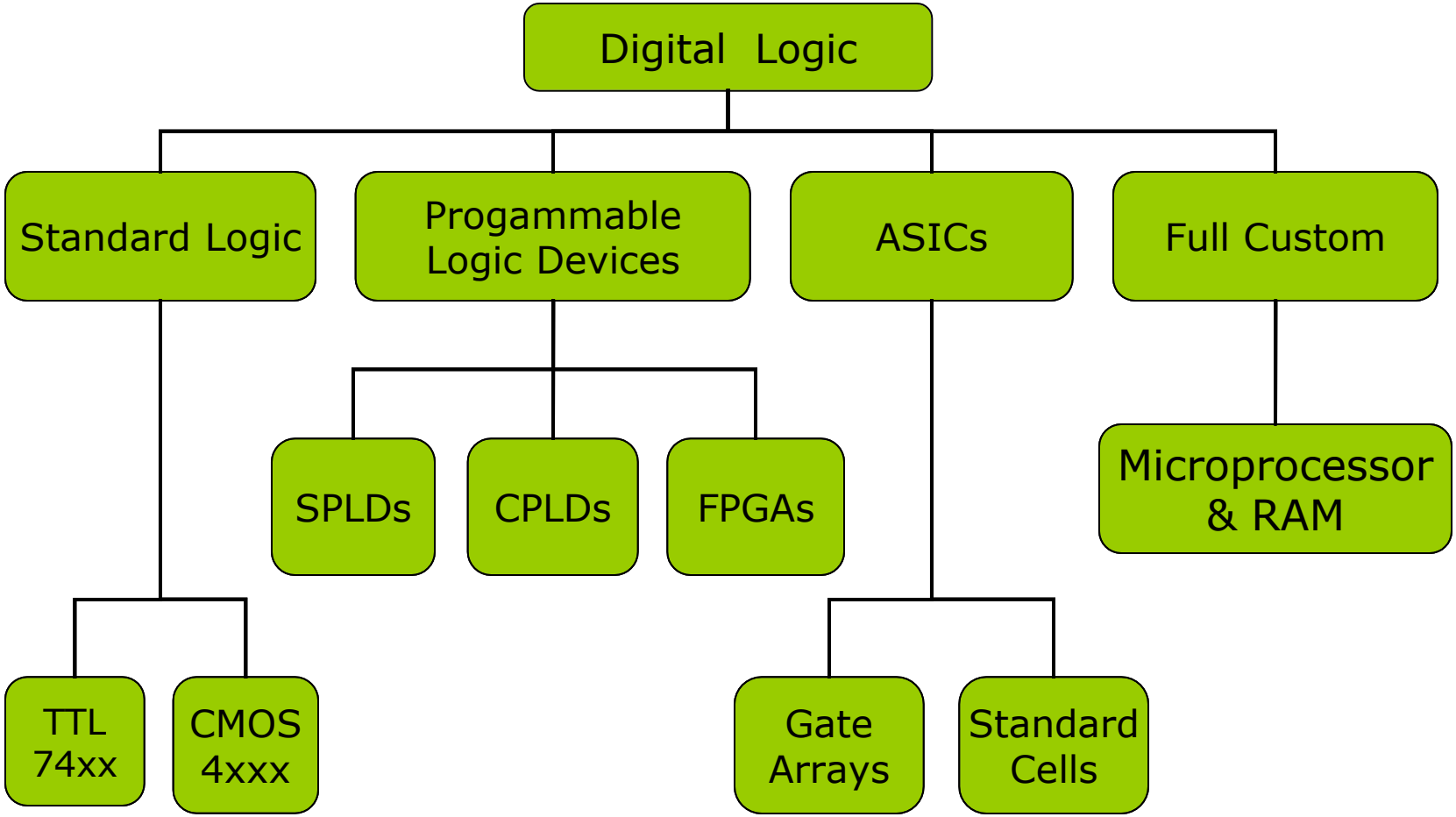
Outline

- Introduction to PLDs
- Programmable Logic Devices Families
- PLDs architecture
- Digital Design Flow
- An Introduction to HDLs
- Verilog and VHDL comparison

Classification



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Programmable Logic Devices

- FPLD (Field-Programmable Logic Device)
- Supplied with no predetermined logic function
- Programmed by user to implement any digital logic function
- Require specialized computer software for design and programming.
- Implementation of digital circuits with low cost and low risk.
- Technology of choice for low to medium volume products (say hundreds to few 10's of thousands per year).
- Good and low cost design softwares.

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Programmable Logic Devices

- SPLDs (Simple PLDs)
  - PLA or PAL
  - Small gate count, fixed internal routing, deterministic propagation delays
- CPLDs
  - Multiple SPLDs onto a single chip
  - Programmable interconnect
- FPGAs
  - An array of logic blocks
  - Large number of gates, user selectable interconnection, delays depending on design and routinig
  - A high ratio of flip-flops to logic resources

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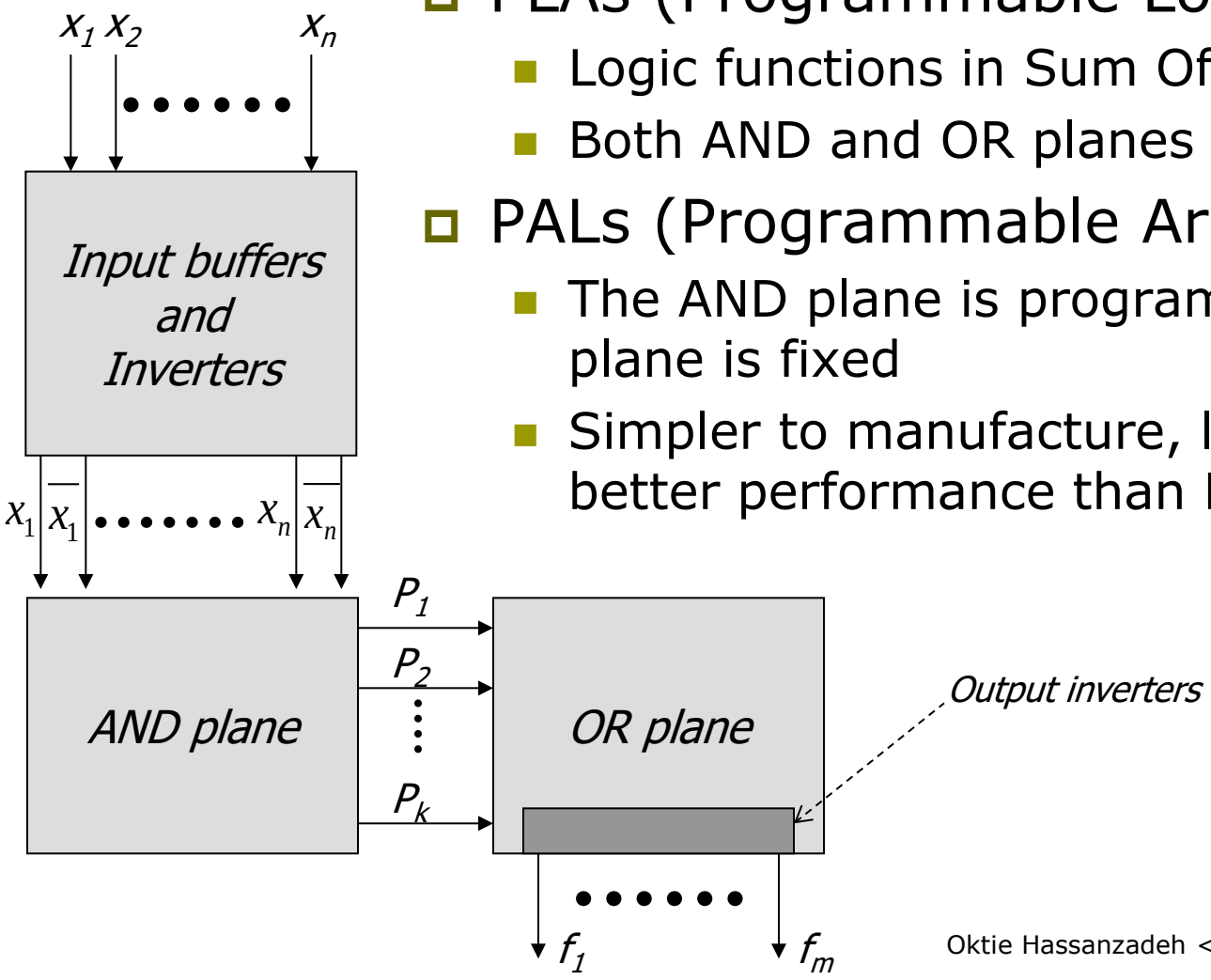
SPLDs



- PLAs (Programmable Logic Arrays)
  - Logic functions in Sum Of Product form
  - Both AND and OR planes are programmable
- PALs (Programmable Array Logics)
  - The AND plane is programmable; the OR plane is fixed
  - Simpler to manufacture, less expensive, better performance than PLAs

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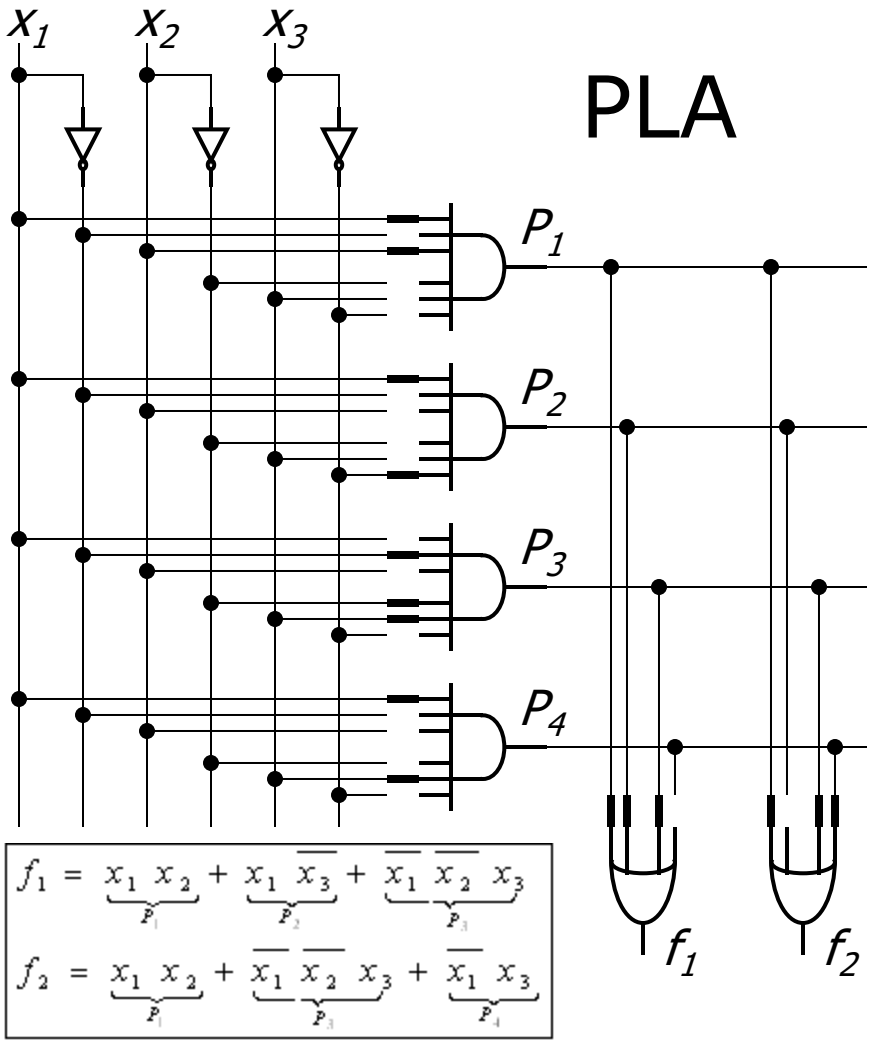
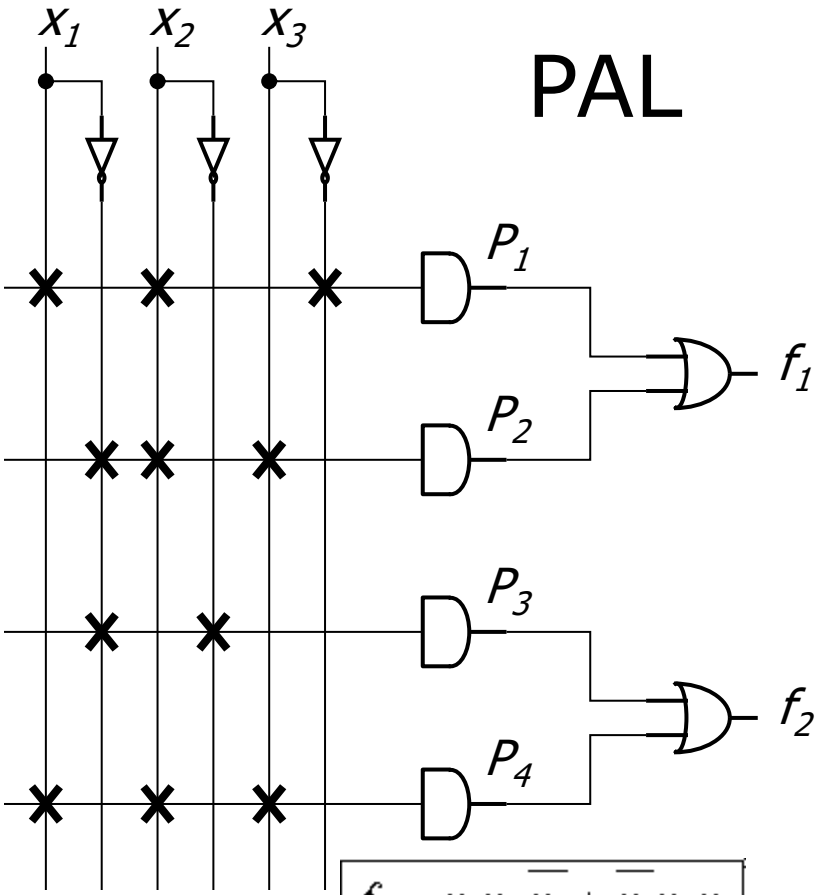
SPLDs' Structure



$$f_1 = \underbrace{x_1\,x_2}_{P_1} + \underbrace{x_1\,\overline{x_3}}_{P_2} + \underbrace{\overline{x_1}\,\overline{x_2}\,x_3}_{P_3}$$

$$f_2 = \underbrace{x_1\,x_2}_{P_1} + \underbrace{\overline{x_1}\,\overline{x_2}\,x_3}_{P_3} + \underbrace{\overline{x_1}\,x_3}_{P_4}$$



$$f_1 = x_1 x_2 \overline{x_3} + \overline{x_1} x_2 x_3$$

$$f_2 = \overline{x_1}\,\overline{x_2} + x_1 x_2 x_3$$

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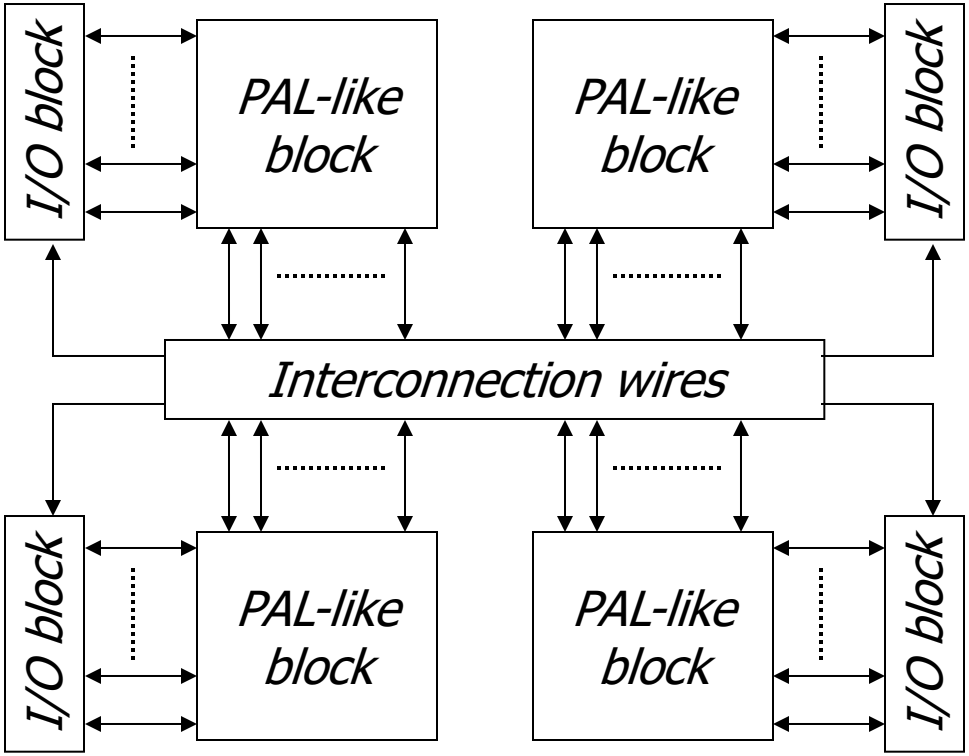
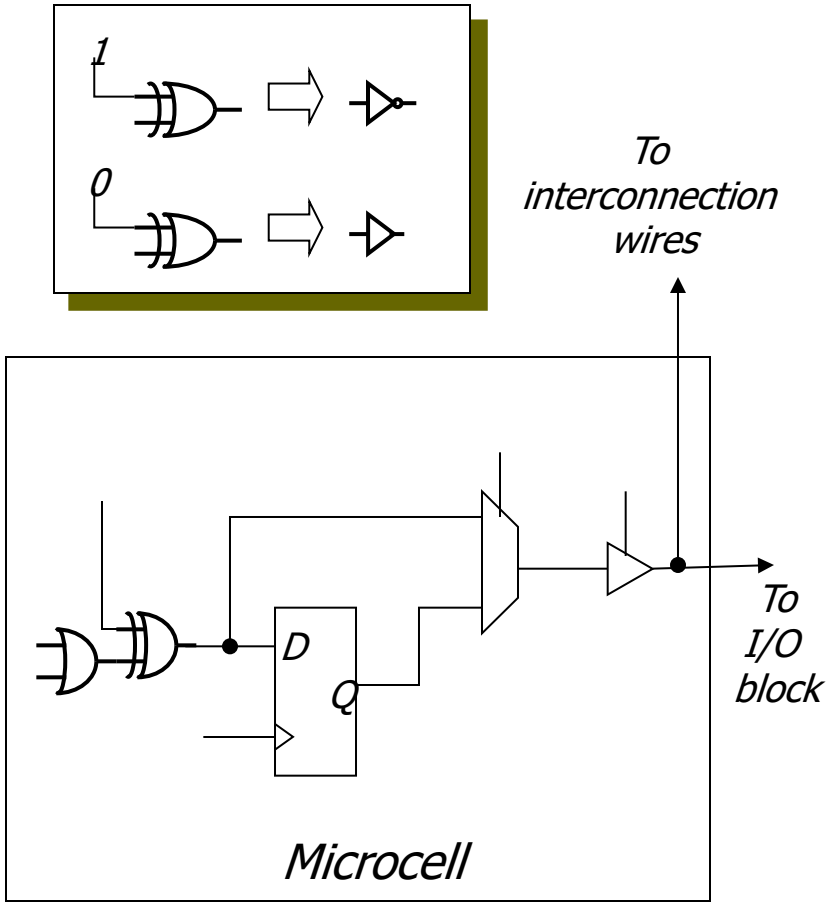
CPLDs



To implement multiple logic circuits



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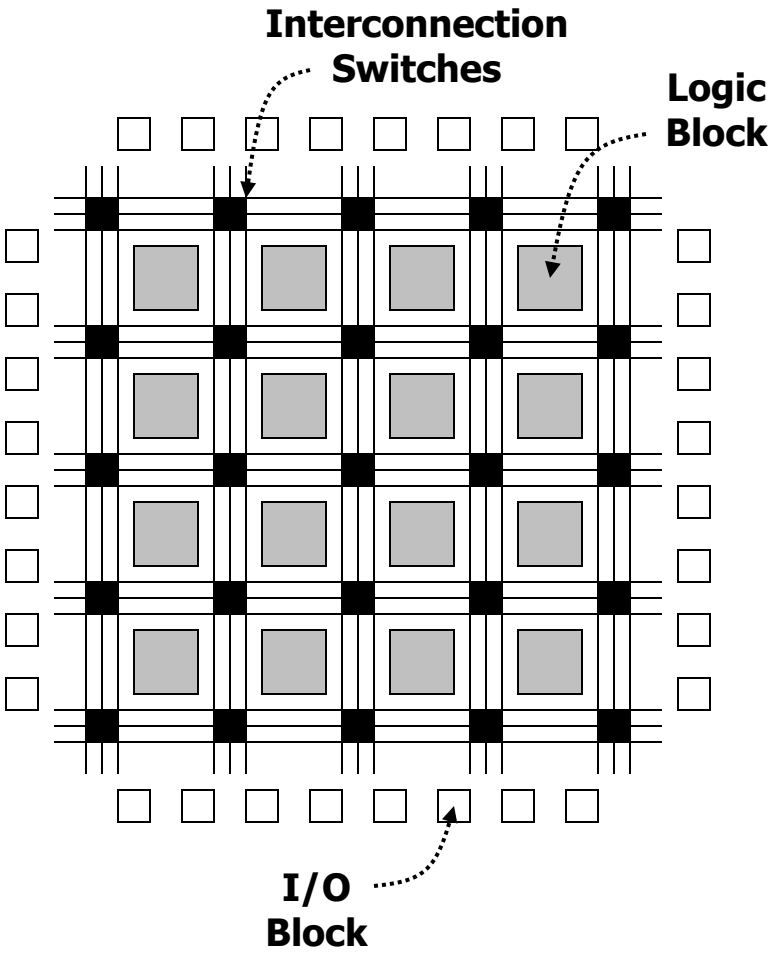
FPGA



- FPGAs do not contain AND or OR planes
- Three elements:
  - Logic blocks
  - I/O blocks
  - Interconnection wires and switches

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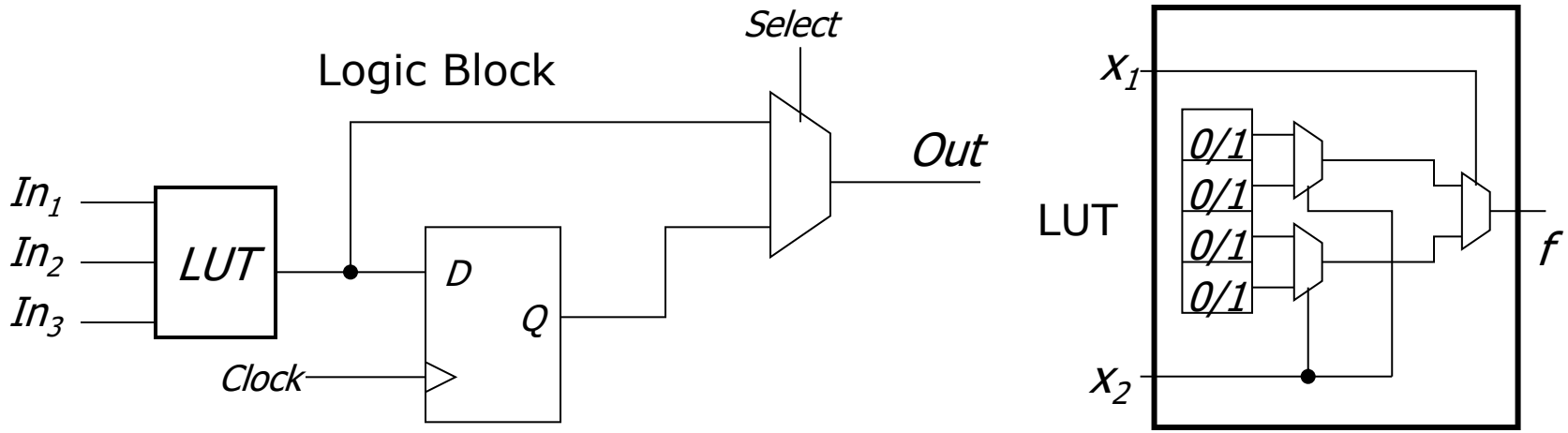
FPGA Logic Block



- The storage cells in the LUTs in an FPGA are volatile
- Volatile: losing stored contents whenever the power is off
- Using PROM to hold data permanently
- The storage cells are loaded automatically from PROM when the chip is initialized

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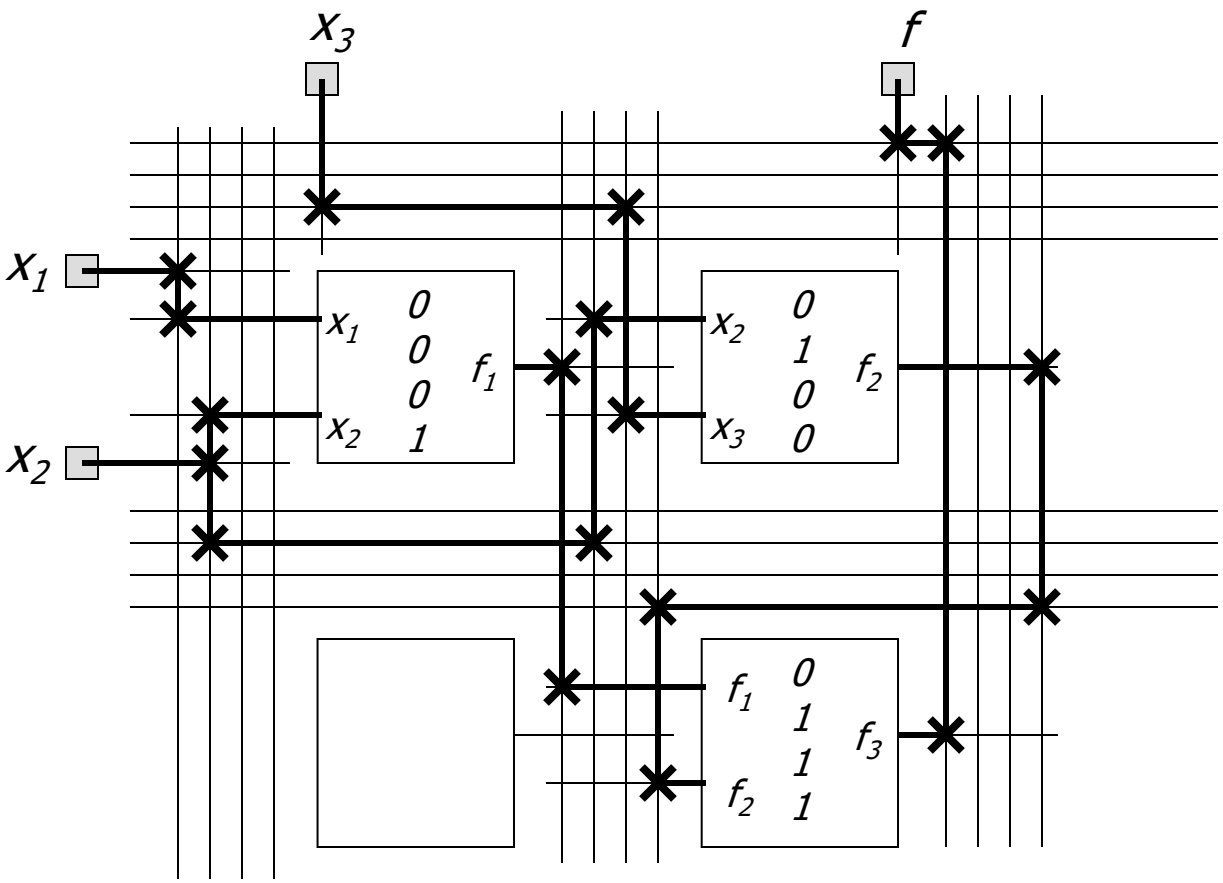
Programming An FPGA



$$f_1 = x_1 x_2$$

$$f_2 = \overline{x_2} x_3$$

$$f = x_1 x_2 + \overline{x_2} x_3$$

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Programming Technologies

- Floating Gate Programming Technology
- SRAM Programming Technology
- Antifuse Programming Technology

In-System Programming (ISP) : performing the programming while the chip is still attached to its circuit board

JTAG (Boundary Scan):
A port added to FPGAs for testing purposes, as a means of downloading the design in the programmable device via serial port of a PC

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The Main Producers

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Altera and Xilinx PLDs

- Altera
  - CPLD
    - MAX3000A – MAX7000
  - FPGA
    - Cyclone
    - Stratix - Stratix GX
    - APEX II - APEX 20K
    - Mercury
    - FLEX 10K
    - ACEX 1K

- Xilinx
  - CPLD
    - CoolRunner-II
    - CoolRunner XPLA3
    - XC9500 Series
  - FPGA
    - Rocket-PHY
    - Virtex - Virtex-II - Virtex-II Pro Series
    - Spartan-3,Spartan-IIE, Spartan-II, Spartan-XL, Spartan Seires

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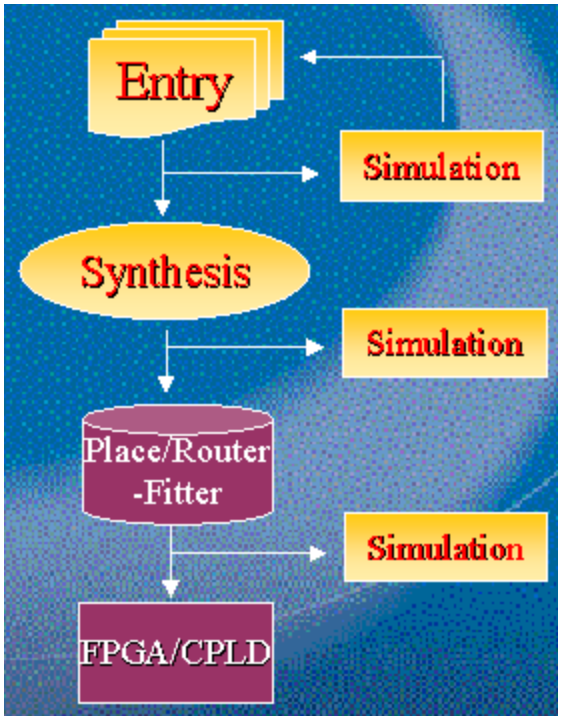
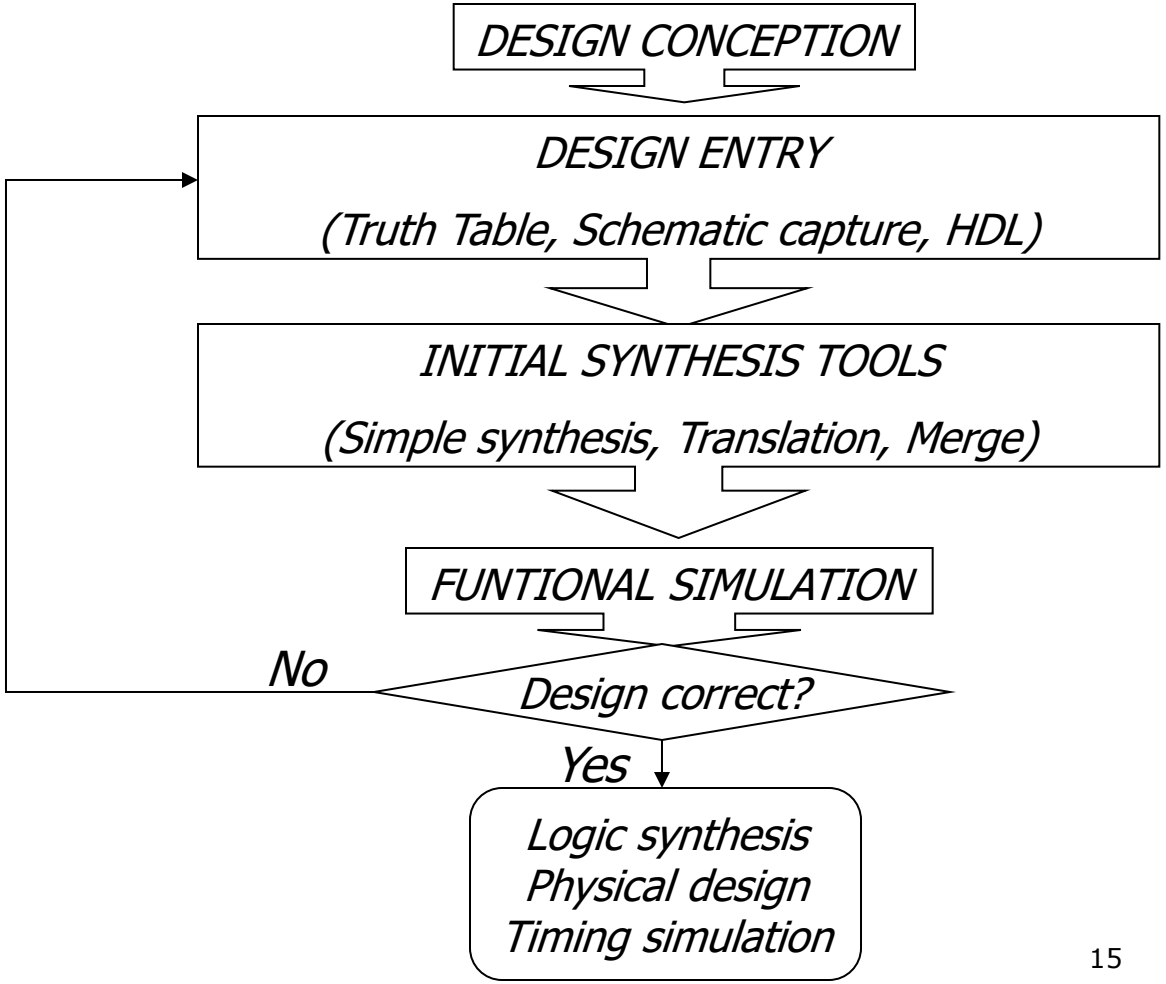
CAD Design Flow





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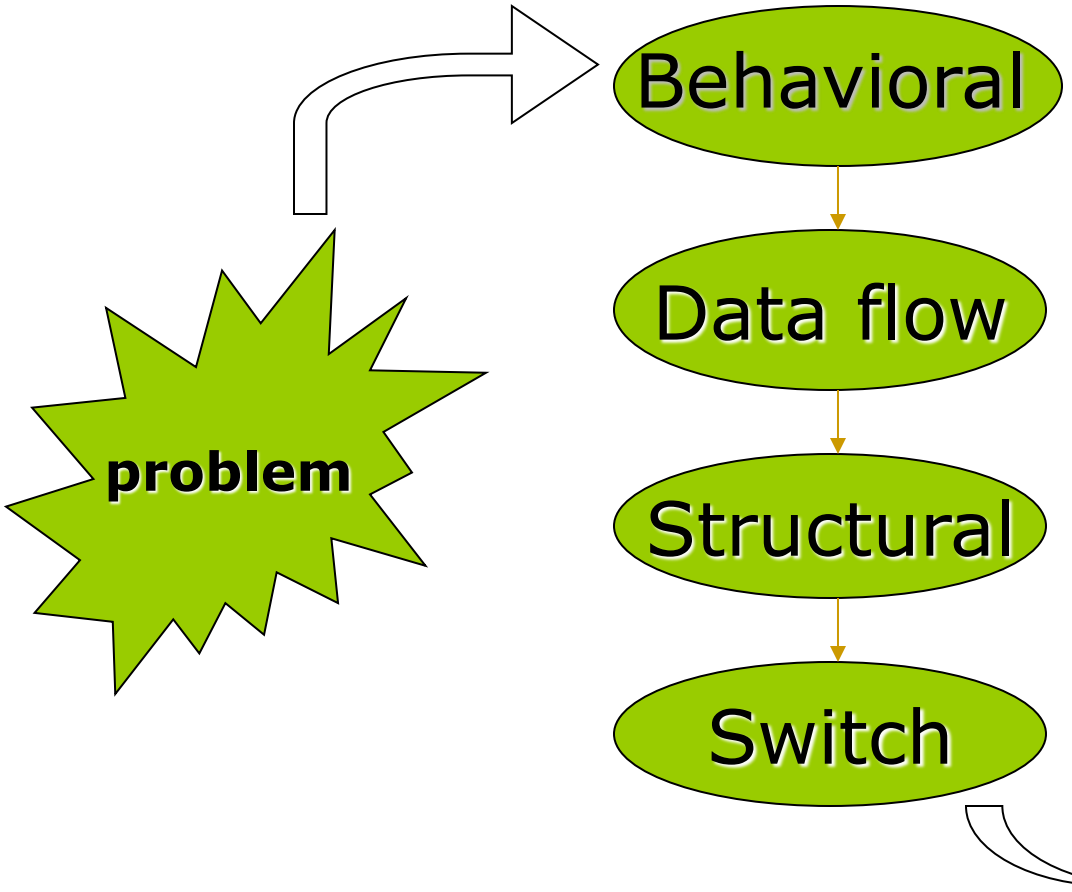
Hardware Description Languages

- Requirments:
  - Concurrency and parallel modeling
  - Timing and delay modeling
  - Ability to describe event-driven functions
  - Readability, Used for documentation
  - Hardware independency

Digital Design Levels



Behavioral

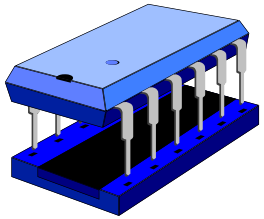
Example: Up/Down Counter

When clock arrival :

If (up=1) then value++

If (down=1) then value --

If (reset=1) then value<=0



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Overview of HDLs

- Two Common Languages
  - Verilog
  - VHDL
- Other
  - SystemC
    - Open source, C++ code for hardware modeling
  - CDL (Computer Design Language)
    - Simple academic language, data flow level, developed in 1965
  - ISPS (Instruction Set Processor Specification)
    - Single level of abstraction, Developed in 1971
  - AHPL (A Hardware Programming Language)
    - Data flow & structural levels, Unfamiliar syntax, Full support by design tools, developed in 1970
  - ABEL (Data I/O Corporation, now Lattice Semiconductor)
  - AHDL (Altera Corp.)
  - CUPL (Logical Devices Inc.)

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Verilog

- Verifying Logic
- Phil Moorby from Gateway Design Automation in 1984 to 1987
- Verilog-XL Simulator from GDA in 1986
- Synopsys synthesis tool in 1988
- In 1990 became open language, OVI
- IEEE standard, Verilog in 1995
- Various levels of abstraction
- most widely used HDL with a user community of more than 50,000 active designers

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VHDL

- VHSIC HDL: Very High Speed Integrated Circuits Hardware Description Language
- DARPA workshop on VHSIC in 1981
- DARPA release requirement in 1983
- A language for hardware documentation
- VHDL 7.2 in 1985
- IEEE standard in 1987
- ANSI standard in 1988
- For RTL design VITAL added
  - VITAL(VHDL Initiative Towards ASIC Library)
- IEEE revised VHDL & VITAL in 1993
- Final review of standard in 2001

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VHDL vs. Verilog

- Complex grammar
  - Complicated compiler
  - Large memory for simulation
  - Hard to learn
- A lot of data types
- High level data types,
  - Pointers
  - Alias

- Easy language
  - Simple & fast compiler
  - Efficient memory usage and faster
  - Easy to learn for beginner
- A few data types
- Hardware related
  - Wires
  - Registers

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VHDL vs. Verilog

- User defined types
- Strong type checking
  - Verbose code for casting
- User defined Library & package
- Open Language
- More EDA support

- All primitive types
- Some castings are allowed
- No user defined packages
  - Include file
- Cadence's language at first
- Less EDA support

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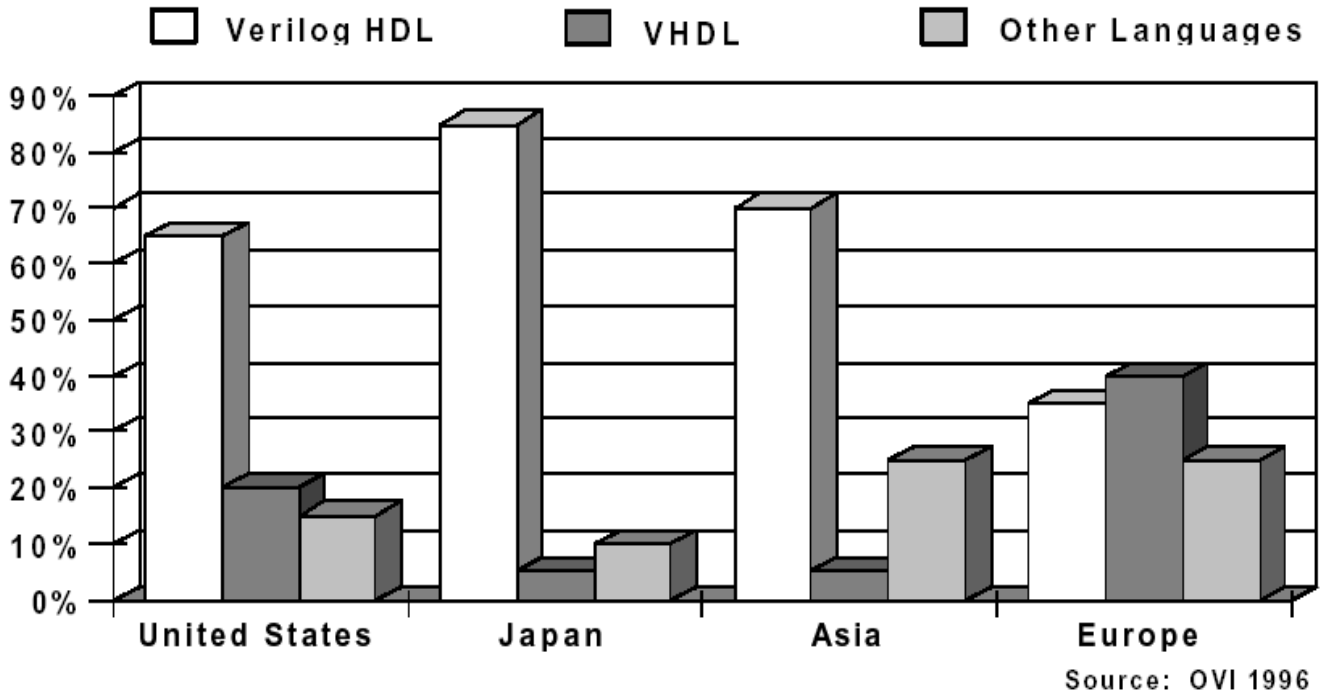
VHDL vs. Verilog

- VHDL, More popular in Europe
- Verilog, In USA and Japan



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Conclusion

- Programmable Logic Devices families
- Architecture of PLDs
- CAD design flow
- Role of HDLs in programming PLDs
- Overview of HDLs
- A comparson between two common HDLs

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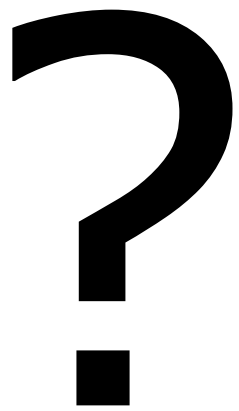
Resources

- Books and Papers
  - SALCIC, Zoran, SMAILAGIC, Asim, *Digital Systems Design and Prototyping using field programmable logic and hardware description languages*, Kluwer Academic Publishers, Massachusetts, 2000
  - SEALS, R.C., WHAPSHOTT, *G.F., Programmable Logic PLDs and FPGAs*, Macmillan Press, London, 1997
  - PALNITKAR, Samir, *Verilog HDL : A Guide to Digital Design and Synthesis*, SunSoft Press, CA, 1996
  - ROSE, Jonathan, BROWN, Stephen, "FPGA and CPLD Architectues: A Tutorial", IEEE Design and Test of Computers, 0740-7475/96, 1996, pp 42-56
- Web Resources
  - Lennon's ASIC page - http://www.cn.nctu.edu.tw/faculty/lennon/ASIC/Viewgraphs
  - Verilog FAQ - http://parmita.com/verilogfaq
  - Verilog Center - http://parmita.com/verilogcenter
  - FPGA Overview - http://www.vcc.com/fpga.html
  - Digital System Design (DSD) Course page of Department of Electrical & Electronic Engineering at Imperial College http://www.ee.ic.ac.uk/pcheung/teaching/ee3_DSD

Any Questions?



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Some Books and Resources

- Publications
  - PLDs
    - *Digital Systems Design and Prototyping using field programmable logic and hardware description languages* by Zoran Salcic and Asim Smailagic, Kluwer Academic Publishers, 2000.
    - *Programmable Logic PLDs and FPGAs* by R.C. Seals and G.F. Whapshott, Macmillan Press, 1997
    - *Application-Specific Integrated Circuits* by Michael John Sebastian Smith , Addison-Wesely, 1997 (Available online at http://www01.edatoolscafe.com/books/ASIC/ASICs.php)
    - *Logic Synthesis* by S. Devadas, A. Ghosh and K. Keutzer, McGraw-Hill, 1994
    - "FPGA and CPLD Architectues: A Tutorial" by Stephen Brown and Jonathan Rose, IEEE Design and Test of Computers, 0740-7475/96, 1996, pp 42-56

Some Books and Resources (Continued)

- HDLs
  - VHDL
    - YALAMANCHILI, Sudhakar, *Vhdl Starter's Guide*, Prentice Hall, 1997
    - ASHENDEN, Peter J., *The Designer's Guide to VHDL, 2nd Edition*, Morgan Kaufmann, 2001
    - DUECK, Robert K., *Digital Design with CPLD Applications and VHDL*, Delmar Learning, 2000
  - Verilog
    - PALNITKAR, Samir, *Verilog HDL : A Guide to Digital Design and Synthesis*, SunSoft Press, CA, 1996
    - THOMAS, D. E., MORRBY, Philip R., *The Verilog Hardware Description Language*, Fourth Edition, Kluwer Academic Publishers, 1998

Some Web Resources

- Web Resources
  - FPGA/CPLDs
    - FPGA Overview - http://www.vcc.com/fpga.html
    - Digital System Design (DSD) Course page of Department of Electrical & Electronic Engineering at Imperial College University of London - http://www.ee.ic.ac.uk/pcheung/teaching/ee3_DSD (Contains useful lecture notes on PLDs and more)
    - The Programmable Logic Jump Station - http://www.optimagic.com
    - PLD FAQ - http://www.optimagic.com/faq.html
    - Altera free literature on the web - http://www.altera.com/literature/lit-index.html
    - Xilinx free literature on the web - http://www.xilinx.com/support/library.htm
    - Xilinx Virtex info - http://www.xilinx.com/products/virtex.htm
    - Actel free literature on the web - http://www.actel.com/techdocs/index.html

Some Web Resources(Continued)

- HDLs
  - All IEEE standards can be obtained from http://www.ieee.org
  - Verilog and VHDL
    - Verilog Center - http://parmita.com/verilogcenter (Contains Verilog FAQ,tips,online books,papers,free stuff,tools,news and more about PLDs)
    - Open Verilog International Homepage - http://www.ovi.org/
    - VHDL Internationl - http://www.vhdl.org
  - SystemC
    - SystemC Community - www.systemc.org
- Newsgroups
  - FPGA - comp.arch.fpga
  - Synthesis - comp.lang.synthesis
  - VHDL – comp.lang.vhdl
  - Verilog - comp.lang.verilog

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