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CISC 340 – Dr. Myre

Porject 2

Multi-Cycle Simulator Overview

The simulator inputs a machine code file (.mc) which has properly assembled machine instructions. The simulator reads through the file one line at a time. For each line, the opcode of the instruction is retrieved by bit shifting the instruction. Based on what opcode is found, the simulator executes the corresponding instruction and bit shifts to get what resources it needs which could include register A, register B, destination register, or the immediate value. Also, the corresponding amount of cycles are added to the cycle count. For example, add counts for 2 cycles and halt counts for 1.

The simulator tracks the contents of memory and the eight registers and prints them after every instruction is executed. along with the program counter. This allows one to observe how memory and the registers are affected throughout the program.

The simulator throws an error and exits if there is an attempt for a branch to a negative memory address. One difficulty we had in revisiting the simulator was identifying runtime errors that we should account for. We felt the branch to a negative was one that we should handle.