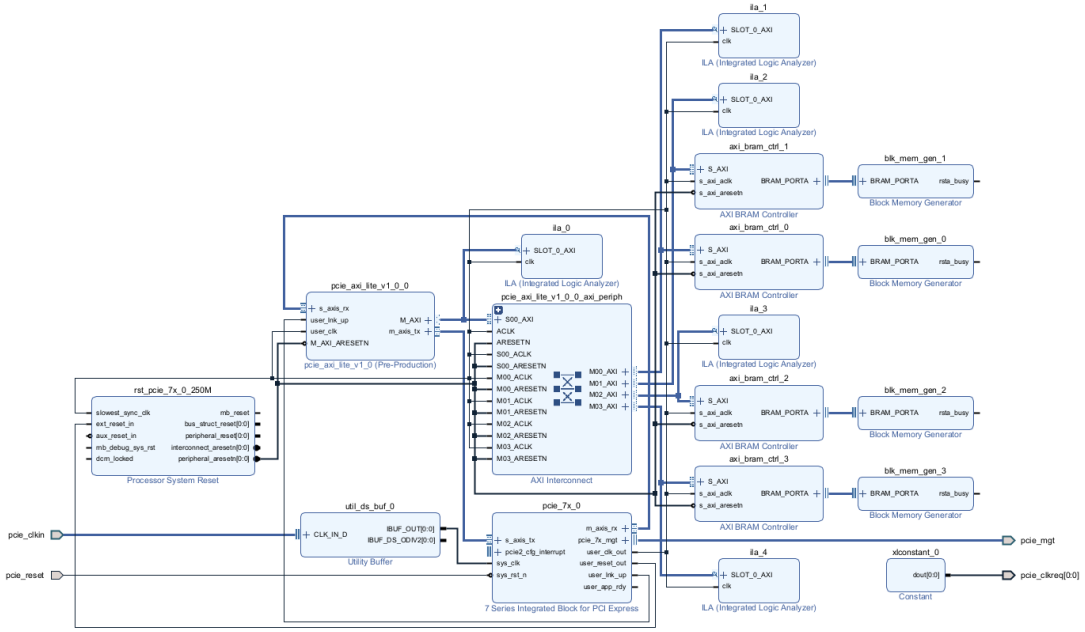
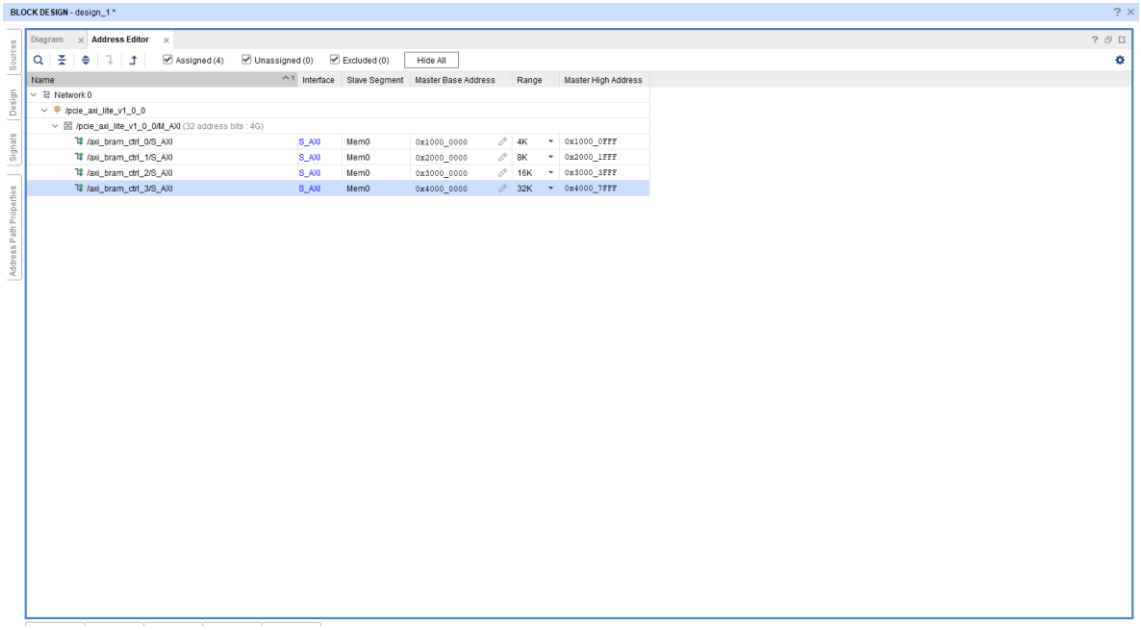
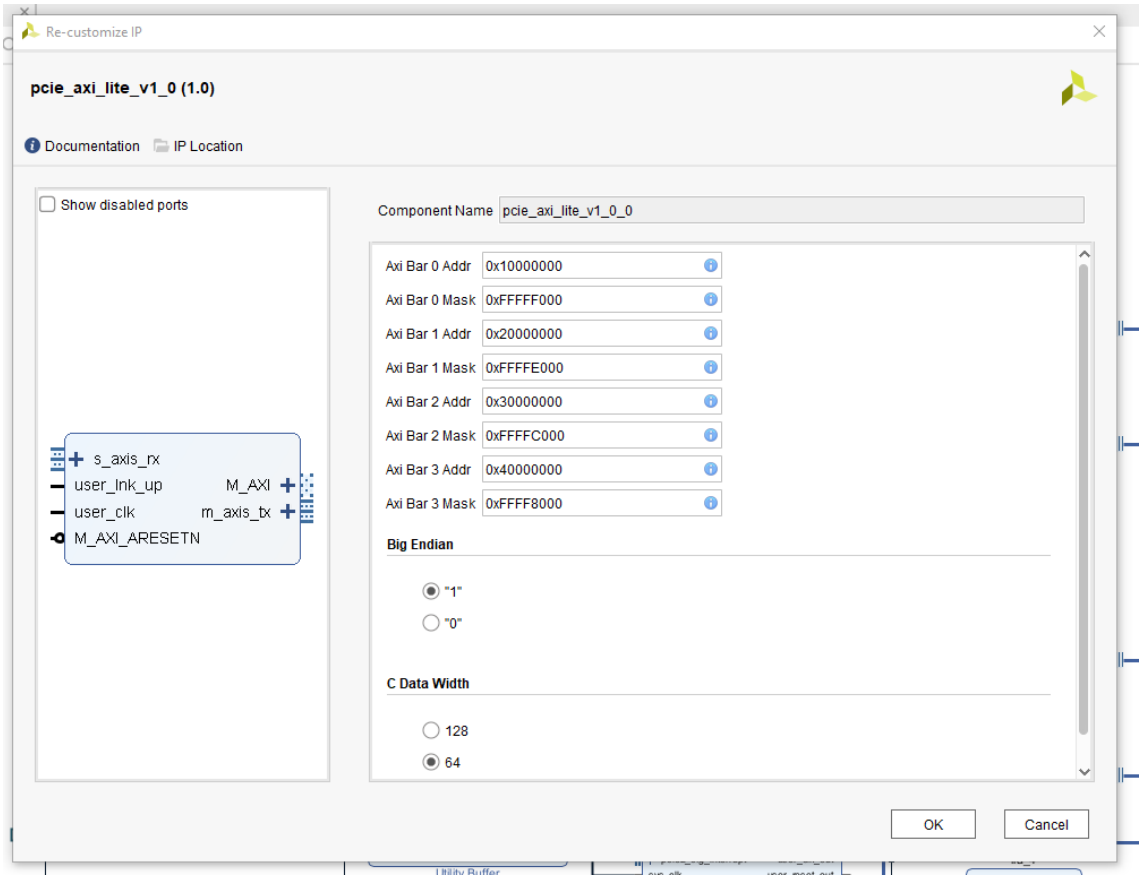
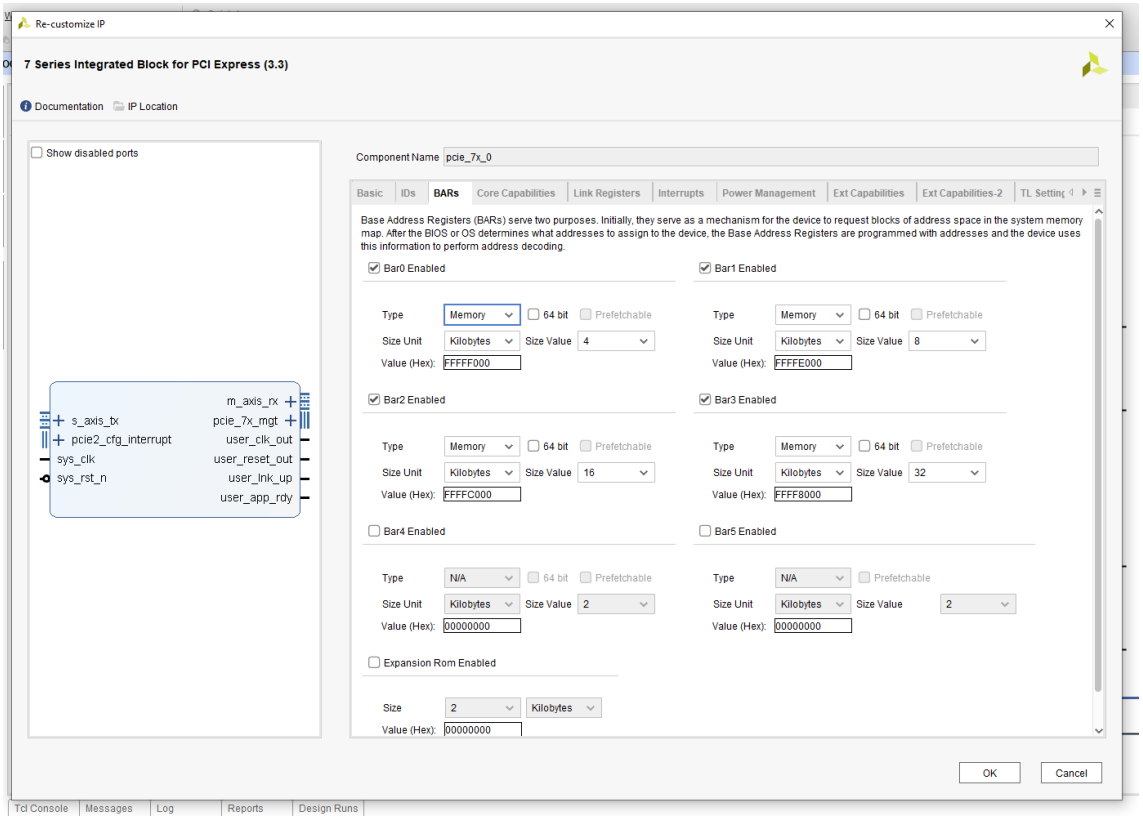

ila_1
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
ila_2
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
axi_bram_ctrl_1
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
blk_mem_gen_1
BRAM_PORTA
rsta_busy
Block Memory Generator
ila_0
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
axi_bram_ctrl_0
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
blk_mem_gen_0
BRAM_PORTA
rsta_busy
Block Memory Generator
pcie_axi_lite_v1_0_0
s_axis_rx
user_lnk_up
user_clk
M_AXI_ARESETN
M_AXI
m_axis_tx
pcie_axi_lite_v1_0 (Pre-Production)
pcie_axi_lite_v1_0_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
ila_3
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
axi_bram_ctrl_2
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
blk_mem_gen_2
BRAM_PORTA
rsta_busy
Block Memory Generator
rst_pcie_7x_0_250M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_bram_ctrl_3
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
blk_mem_gen_3
BRAM_PORTA
rsta_busy
Block Memory Generator
util_ds_buf_0
CLK_IN_D
IBUF_OUT[0:0]
IBUF_DS_ODV2[0:0]
Utility Buffer
pcie_7x_0
s_axis_tx
pcie2_cfg_interrupt
sys_clk
sys_rst_n
m_axis_rx
pcie_7x_mgt
user_clk_out
user_reset_out
user_lnk_up
user_app_rdy
7 Series Integrated Block for PCI Express
pcie_clkin
pcie_reset
pcie_mgt
ila_4
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
xlconstant_0
dout[0:0]
Constant
pcie_clkreq[0:0]


BLOCK DESIGN - design_1 *
Diagram
Address Editor
Assigned (4)
Unassigned (0)
Excluded (0)
Hide All
Name
Interface
Slave Segment
Master Base Address
Range
Master High Address
Network 0
/pcie_axi_lite_v1_0_0
/pcie_axi_lite_v1_0_0/M_AXI (32 address bits : 4G)
/axi_bram_ctrl_0/S_AXI S_AXI Mem0 0x1000_0000 4K 0x1000_0FFF
/axi_bram_ctrl_1/S_AXI S_AXI Mem0 0x2000_0000 8K 0x2000_1FFF
/axi_bram_ctrl_2/S_AXI S_AXI Mem0 0x3000_0000 16K 0x3000_3FFF
/axi_bram_ctrl_3/S_AXI S_AXI Mem0 0x4000_0000 32K 0x4000_7FFF
Sources
Design
Signals
Address Path Properties


Re-customize IP
pcie_axi_lite_v1_0 (1.0)
Documentation
IP Location
Show disabled ports
s_axis_rx
user_lnk_up
M_AXI
user_clk
m_axis_tx
M_AXI_ARESETN
Component Name
pcie_axi_lite_v1_0_0
Axi Bar 0 Addr
0x10000000
Axi Bar 0 Mask
0xFFFFF000
Axi Bar 1 Addr
0x20000000
Axi Bar 1 Mask
0xFFFFE000
Axi Bar 2 Addr
0x30000000
Axi Bar 2 Mask
0xFFFFC000
Axi Bar 3 Addr
0x40000000
Axi Bar 3 Mask
0xFFFF8000
Big Endian
"1"
"0"
C Data Width
128
64
OK
Cancel


Re-customize IP
7 Series Integrated Block for PCI Express (3.3)
Documentation
IP Location
Show disabled ports
s_axis_tx
pcie2_cfg_interrupt
sys_clk
sys_rst_n
m_axis_rx
pcie_7x_mgt
user_clk_out
user_reset_out
user_lnk_up
user_app_rdy
Component Name
pcie_7x_0
Basic
IDs
BARs
Core Capabilities
Link Registers
Interrupts
Power Management
Ext Capabilities
Ext Capabilities-2
Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.
Bar0 Enabled
Bar1 Enabled
Bar2 Enabled
Bar3 Enabled
Bar4 Enabled
Bar5 Enabled
Expansion Rom Enabled
OK
Cancel
Tcl Console
Messages
Log
Reports
Design Runs