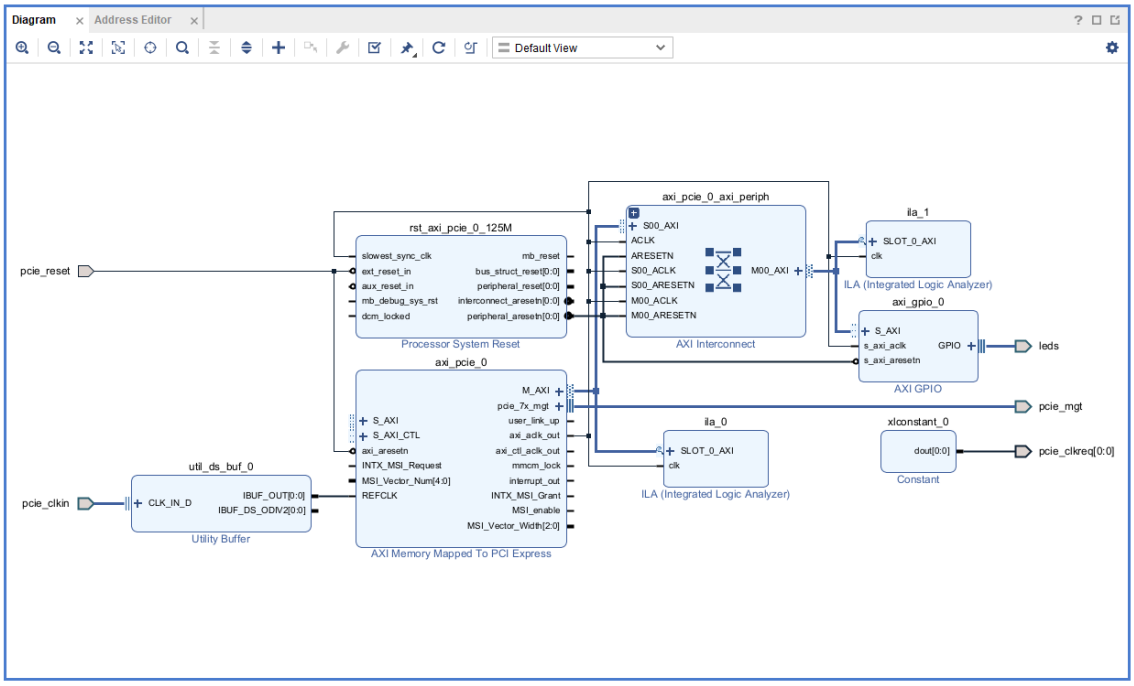
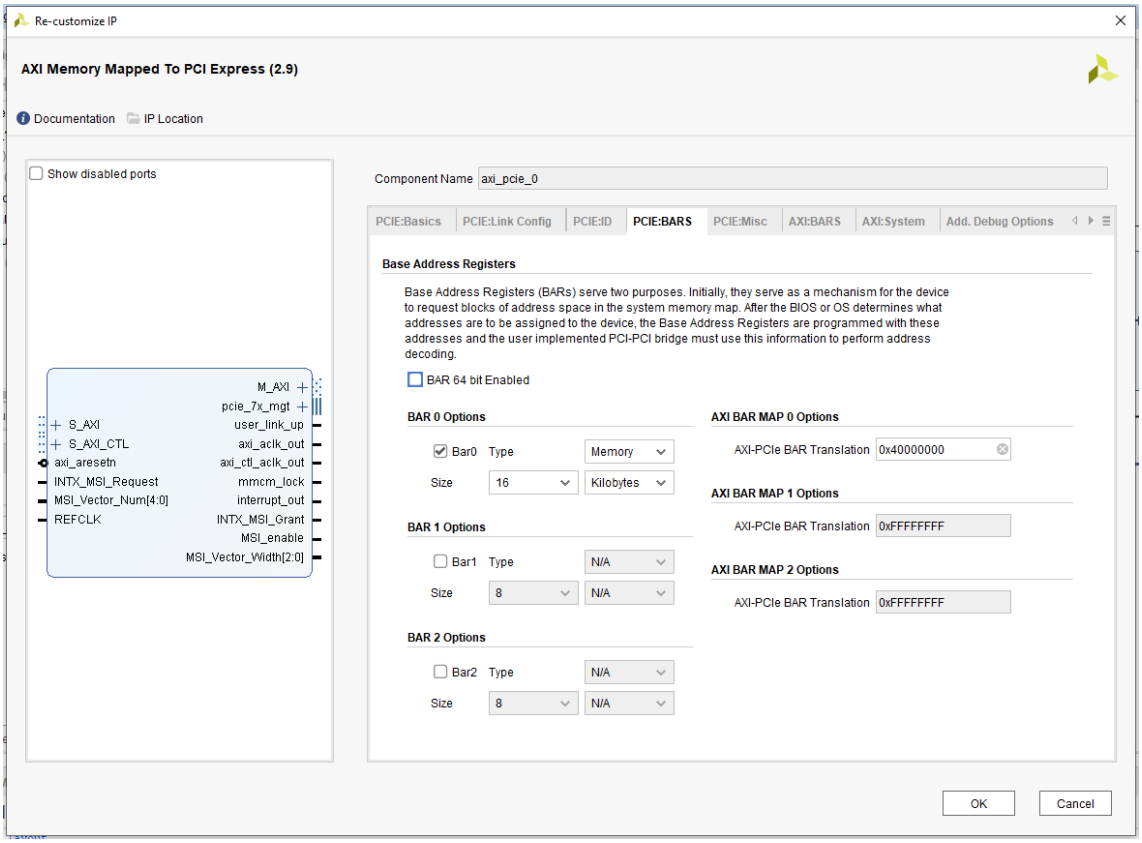
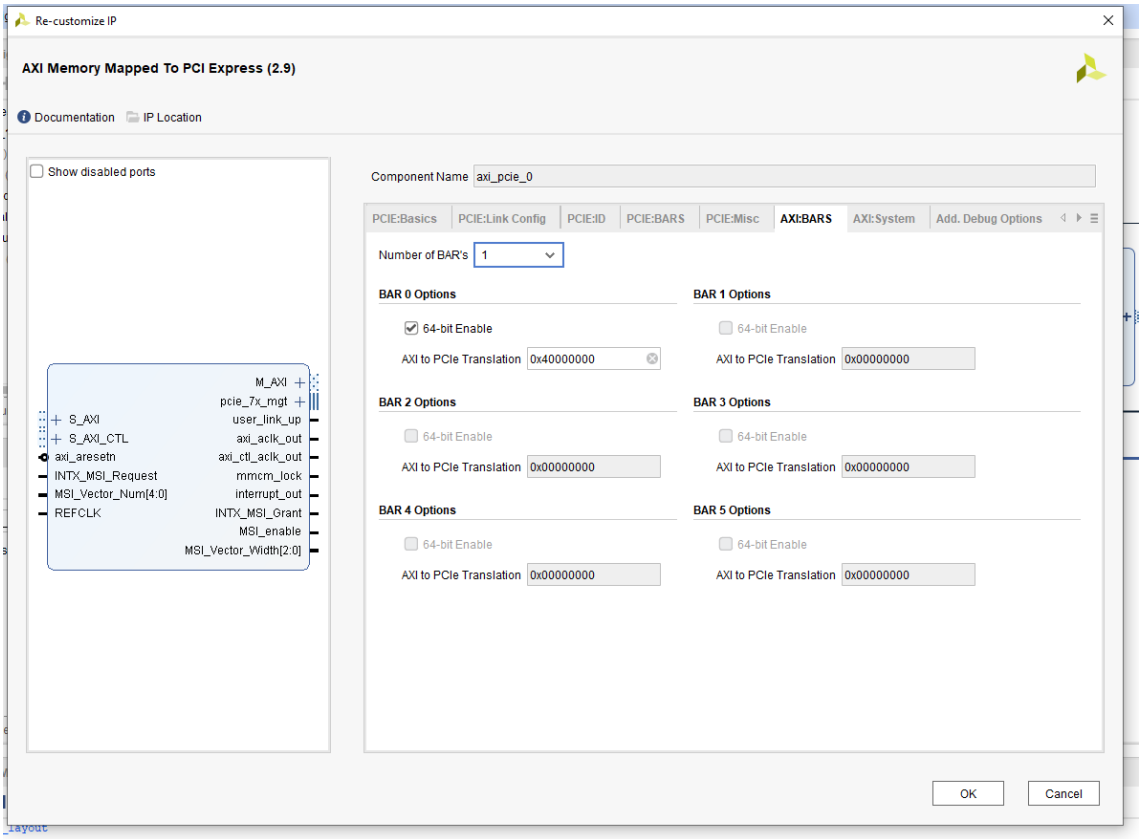


Diagram
Address Editor
Default View
axi_pcie_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
ila_1
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
rst_axi_pcie_0_125M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
pcie_reset
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
leds
AXI GPIO
axi_pcie_0
M_AXI
pcie_7x_mgt
S_AXI
S_AXI_CTL
axi_aresetn
INTX_MSI_Request
MSI_Vector_Num[4:0]
REFCLK
user_link_up
axi_aclk_out
axi_ctl_aclk_out
mmcm_lock
interrupt_out
INTX_MSI_Grant
MSI_enable
MSI_Vector_Width[2:0]
AXI Memory Mapped To PCI Express
pcie_mgt
ila_0
SLOT_0_AXI
clk
ILA (Integrated Logic Analyzer)
xlconstant_0
dout[0:0]
Constant
pcie_clkreq[0:0]
util_ds_buf_0
pcie_clkin
CLK_IN_D
IBUF_OUT[0:0]
IBUF_DS_ODIV2[0:0]
Utility Buffer


Re-customize IP
AXI Memory Mapped To PCI Express (2.9)
Documentation
IP Location
Show disabled ports
M_AXI
pcie_7x_mgt
S_AXI
user_link_up
S_AXI_CTL
axi_aclk_out
axi_aresetn
axi_ctl_aclk_out
INTX_MSI_Request
mmcm_lock
MSI_Vector_Num[4:0]
interrupt_out
REFCLK
INTX_MSI_Grant
MSI_enable
MSI_Vector_Width[2:0]
Component Name
axi_pcie_0
PCIE:Basics
PCIE:Link Config
PCIE:ID
PCIE:BARS
PCIE:Misc
AXI:BARS
AXI:System
Add. Debug Options
Base Address Registers
Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses are to be assigned to the device, the Base Address Registers are programmed with these addresses and the user implemented PCI-PCI bridge must use this information to perform address decoding.
BAR 64 bit Enabled
BAR 0 Options
Bar0
Type
Memory
Size
16
Kilobytes
BAR 1 Options
Bar1
Type
N/A
Size
8
N/A
BAR 2 Options
Bar2
Type
N/A
Size
8
N/A
AXI BAR MAP 0 Options
AXI-PCIe BAR Translation
0x40000000
AXI BAR MAP 1 Options
AXI-PCIe BAR Translation
0xFFFFFFFF
AXI BAR MAP 2 Options
AXI-PCIe BAR Translation
0xFFFFFFFF
OK
Cancel


Re-customize IP
AXI Memory Mapped To PCI Express (2.9)
Documentation
IP Location
Show disabled ports
M_AXI
pcie_7x_mgt
S_AXI
user_link_up
S_AXI_CTL
axi_aclk_out
axi_aresetn
axi_ctl_aclk_out
INTX_MSI_Request
mmcm_lock
MSI_Vector_Num[4:0]
interrupt_out
REFCLK
INTX_MSI_Grant
MSI_enable
MSI_Vector_Width[2:0]
Component Name
axi_pcie_0
PCIE:Basics
PCIE:Link Config
PCIE:ID
PCIE:BARS
PCIE:Misc
AXI:BARS
AXI:System
Add. Debug Options
Number of BAR's
1
BAR 0 Options
64-bit Enable
AXI to PCIe Translation
0x40000000
BAR 1 Options
64-bit Enable
AXI to PCIe Translation
0x00000000
BAR 2 Options
64-bit Enable
AXI to PCIe Translation
0x00000000
BAR 3 Options
64-bit Enable
AXI to PCIe Translation
0x00000000
BAR 4 Options
64-bit Enable
AXI to PCIe Translation
0x00000000
BAR 5 Options
64-bit Enable
AXI to PCIe Translation
0x00000000
OK
Cancel

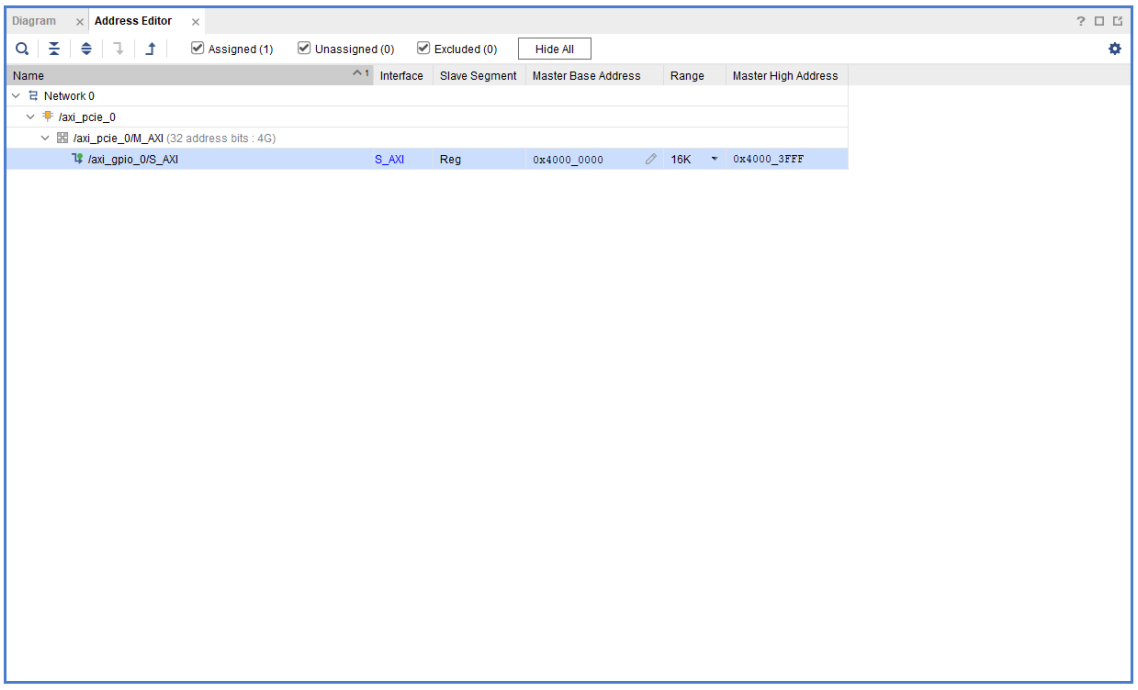


Diagram
Address Editor
Assigned (1)
Unassigned (0)
Excluded (0)
Hide All
Name
Interface
Slave Segment
Master Base Address
Range
Master High Address
Network 0
/axi_pcie_0
/axi_pcie_0/M_AXI (32 address bits : 4G)
/axi_gpio_0/S_AXI
S_AXI
Reg
0x4000_0000
16K
0x4000_3FFF