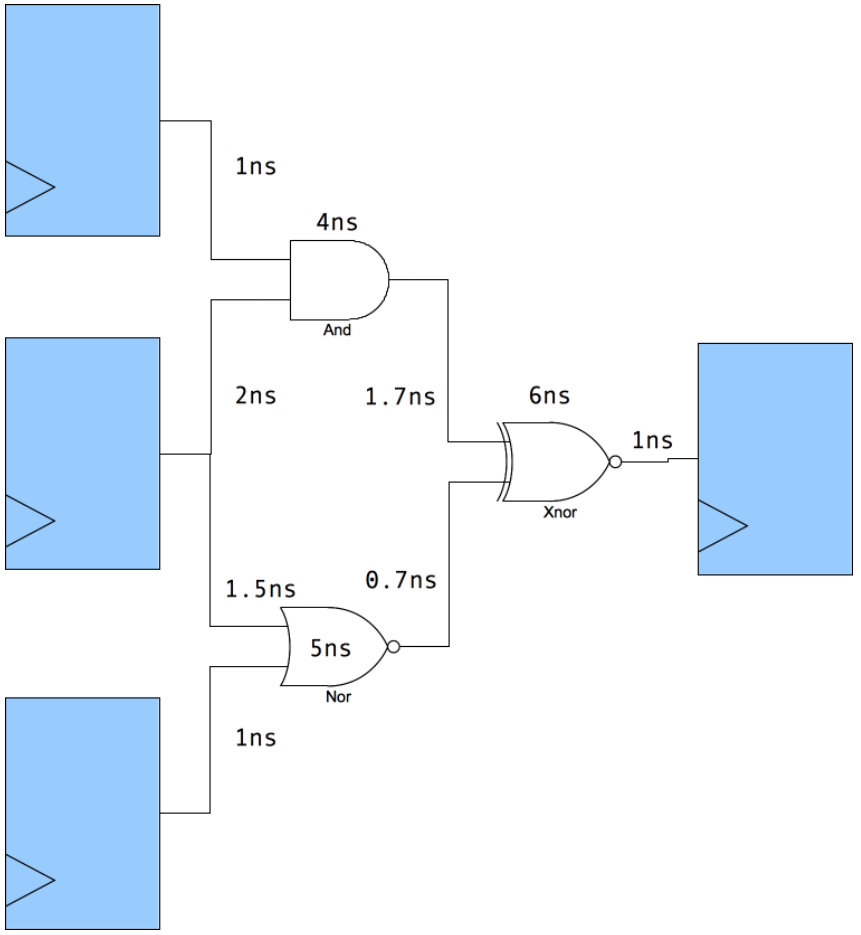
Digital Circuit Timing

What is Timing?

- Ever wonder why your desktop CPU can't run at 10GHz?
- Ever tried to "overclock" your processor with custom cooling systems?
- All physical elements have speed limits, e.g. speed of light, speed of sound, and speed of voltage potential in copper medium
- For digital circuits, the speed is limited by many factors.

Timing Example

- Routing delay
  - Which wire is the fastest?
  - Which wire is the slowest?
- Logic delay
  - Which gate is the fastest?
  - Which gate is the slowest?
- Can you identify the slowest and the fastest paths?



Timing Example, cont.

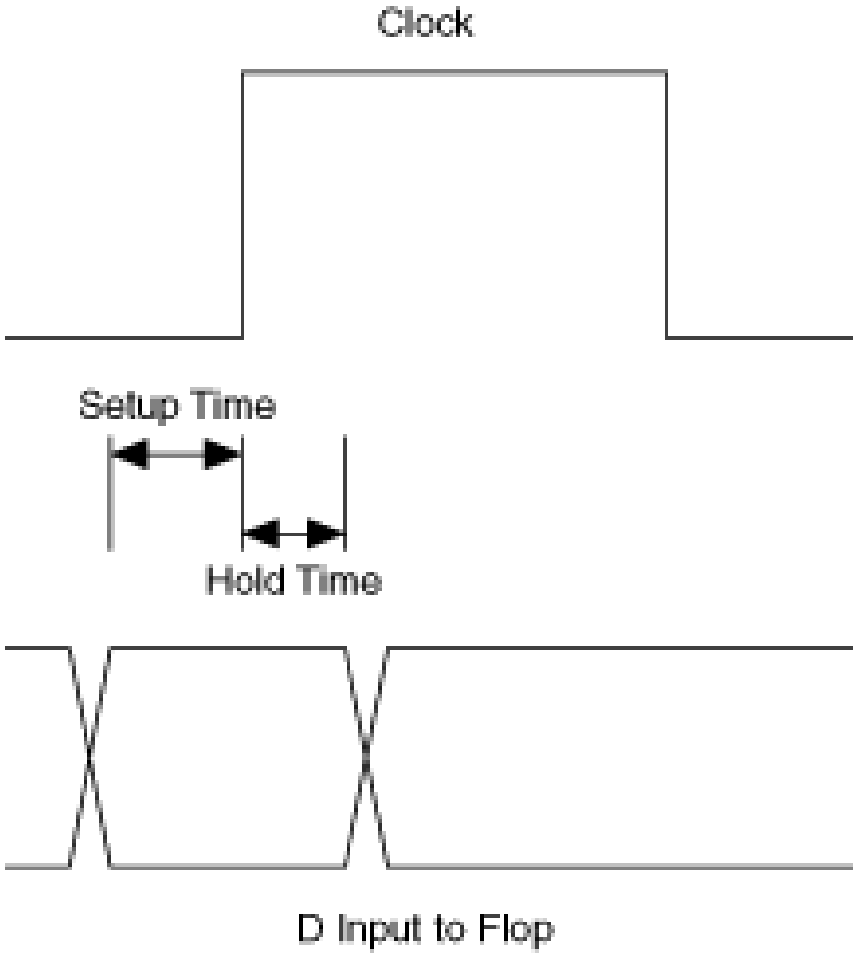
- The fastest wire was 0.7ns
- The slowest wire was 2ns
- The fastest gate was the AND gate (4ns)
- The slowest gate was the XNOR gate (6ns)
- The fastest path was 13.7ns
- The slowest path was 14.7ns
- The slowest path is also called the “critical path”

Other Factors that Affect Timing

- Temperature (electrons move faster at colder temperature)
- Voltage (electrons move faster at higher voltage)
- Gate-level Variations (geometry and doping variations from lot to lot, wafer to wafer, die to die, and within the same die)
- Damage to gates due to use (aging)
- A vendor must provide worst-case band guards that accounts for all of above!

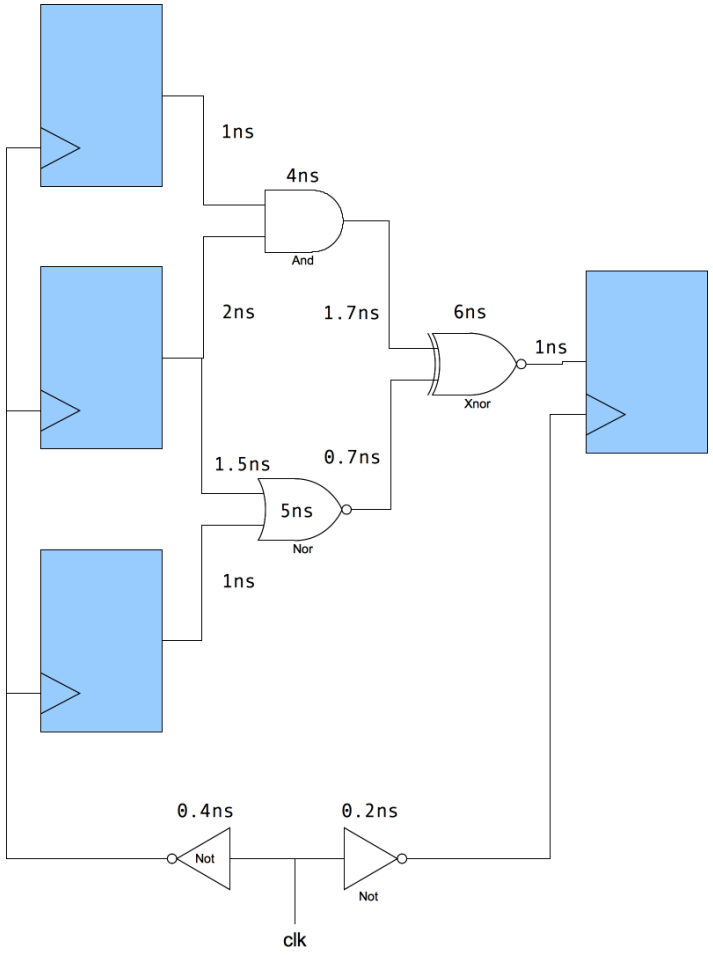
Other Factors: Setup and Hold Time

- Setup time is a short period ***before*** the rising edge of the clock where the input to each flipflop must be steady
- Hold time is a short period ***after*** the rising edge of the clock where the input to each flipflop must be steady
- Failure to meet these requirements is called setup or hold violation
- In FPGA designs, ***setup*** time constraint is the main performance factor.



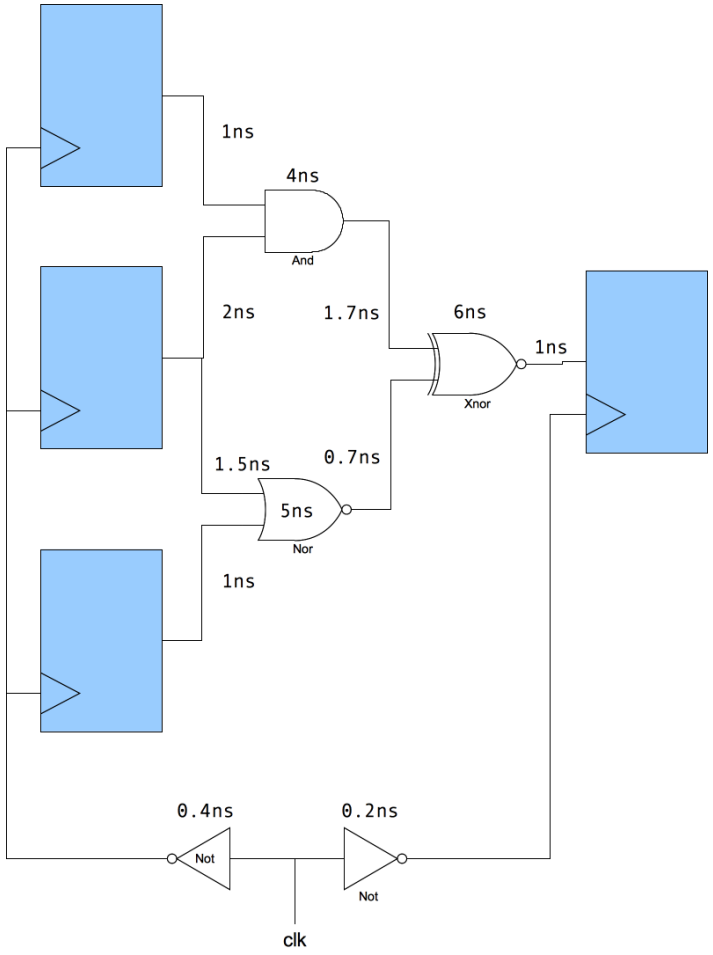
Other Factors: Clock Skew

- Clock distribution networks are not always perfect.
- Sometimes one flipflop sees the rising edge of the clock earlier or later than the another flipflop that drives its source logic tree
- The clock skew on the right is 0.2ns between the two sets of flipflops



All Factors Considered

- Critical path of 14.7ns
- Setup time of 0.2ns
- Clock skew of 0.2ns
- Max(Aging) + Max(Variation) + Max(Temperature) + Min(Vdd) contribute to up to 15% of performance degradation
- Worst case clock cycle is: (14.7 + 0.2 + 0.2)*(1+15%) = 17.36ns
- Or 57.6MHz



Static Timing Analysis

- STA is the process that goes through all logic paths in a digital design and determine whether any part of the circuit fails setup or hold time constraints
- Fortunately, STA is done automatically by the tools (Xilinx ISE).
- Very often, the results of the STA is fed back to the placement and routing tool to improve the performance.
- Take a look at the static timing report from your lab 1. See if you can find the critical path of the system. What's the speed ceiling?