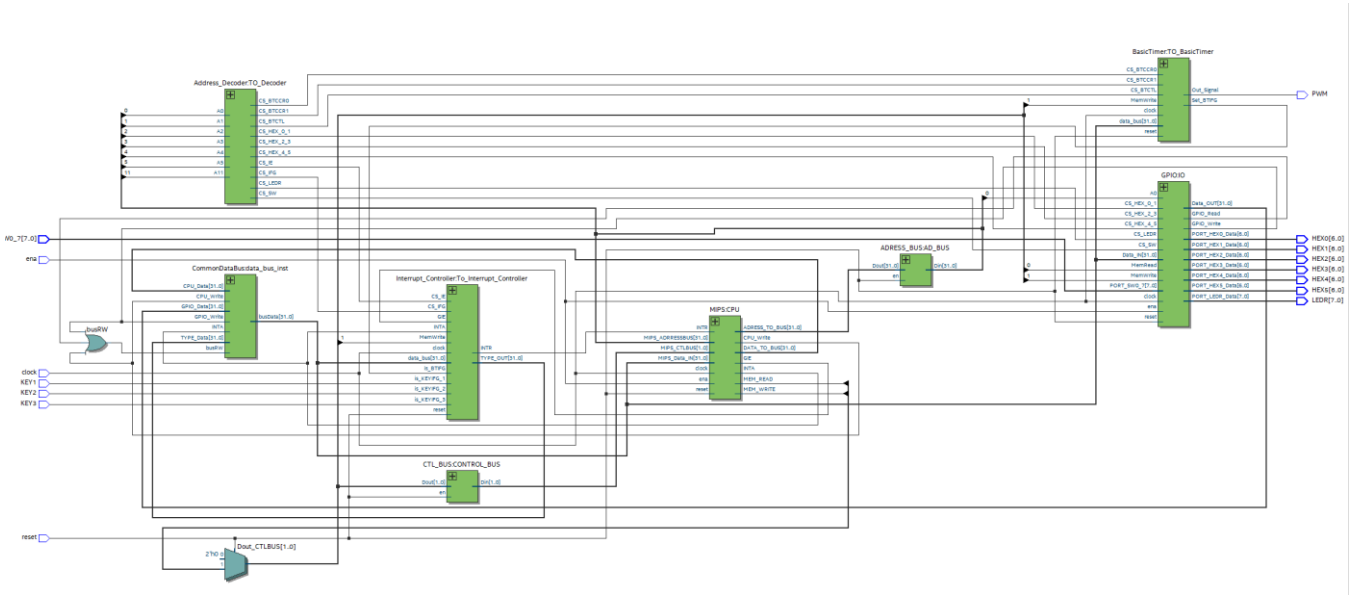
# Final_Project

רועי שחמון 206564759 נעם קליינר 316015411 | מעבדת ארכיטקטורה ומאיצי חומרה |08.08.23

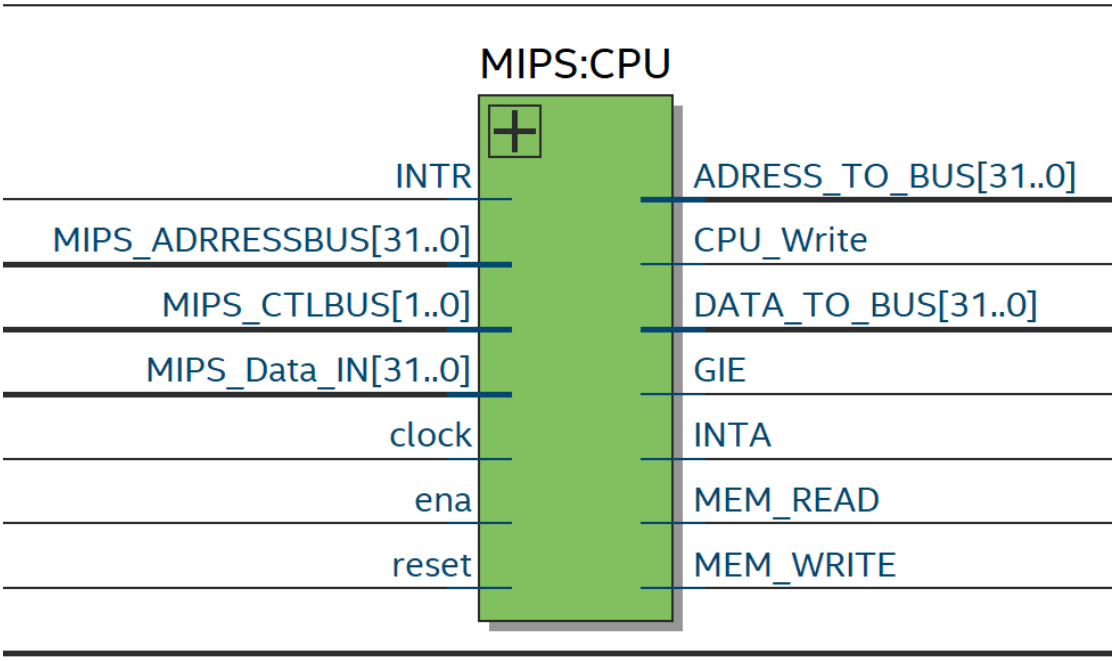
## MCU Top Level Entity

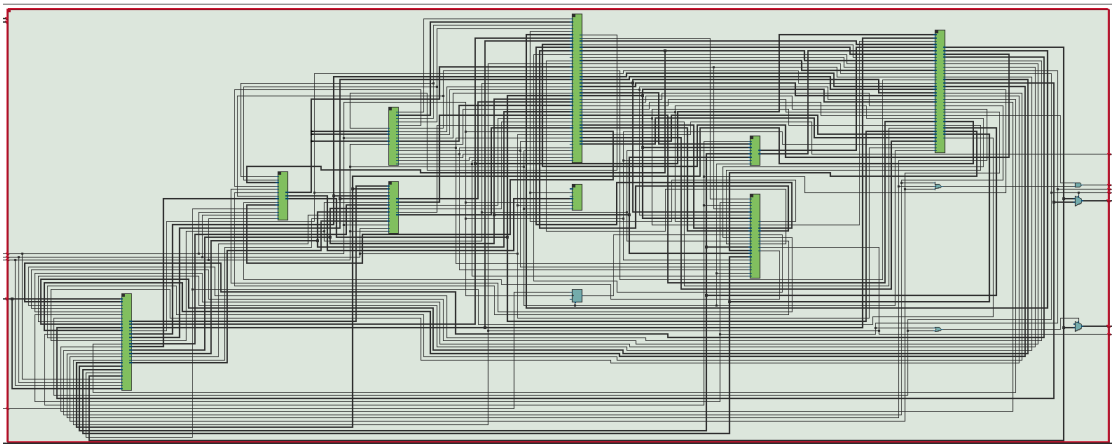



| Flow Summary | |
|---|---|
| <<Filter>> | |
| Flow Status | Successful - Tue Aug 8 08:49:26 2023 |
| Quartus Prime Version | 21.1.0 Build 842 10/21/2021 SJ Lite Edition |
| Revision Name | TESTIMM |
| Top-level Entity Name | MCU |
| Family | Cyclone V |
| Device | 5CSXFC5D6F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 1,783 / 32,070 ( 6 % ) |
| Total registers | 1640 |
| Total pins | 65 / 499 ( 13 % ) |
| Total virtual pins | 0 |
| Total block memory bits | 16,384 / 4,065,280 ( < 1 % ) |
| Total DSP Blocks | 2 / 87 ( 2 % ) |
| Total HSSI RX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA RX Deserializers | 0 / 9 ( 0 % ) |
| Total HSSI TX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA TX Serializers | 0 / 9 ( 0 % ) |
| Total PLLs | 0 / 15 ( 0 % ) |
| Total DLLs | 0 / 4 ( 0 % ) |

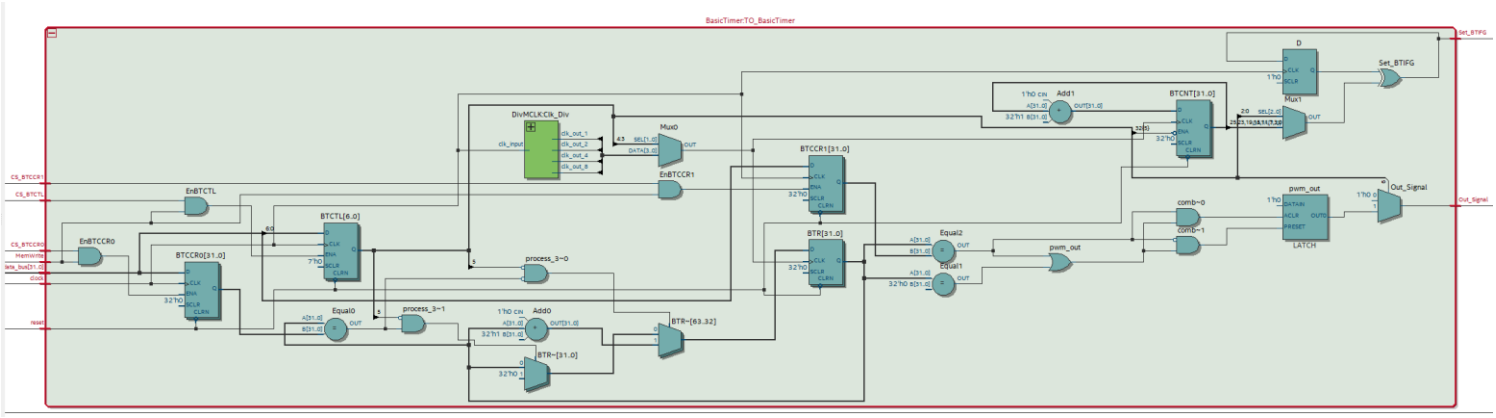
- RTL Viewer results for each  block (of the level underneath top).

**a) Mips CPU**

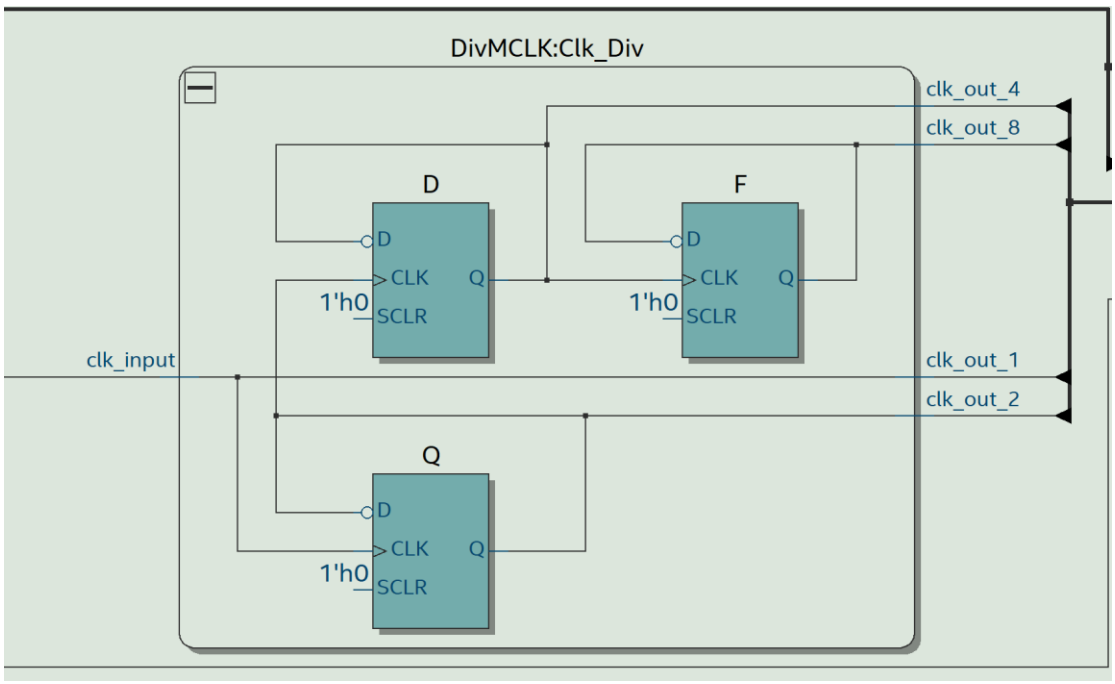


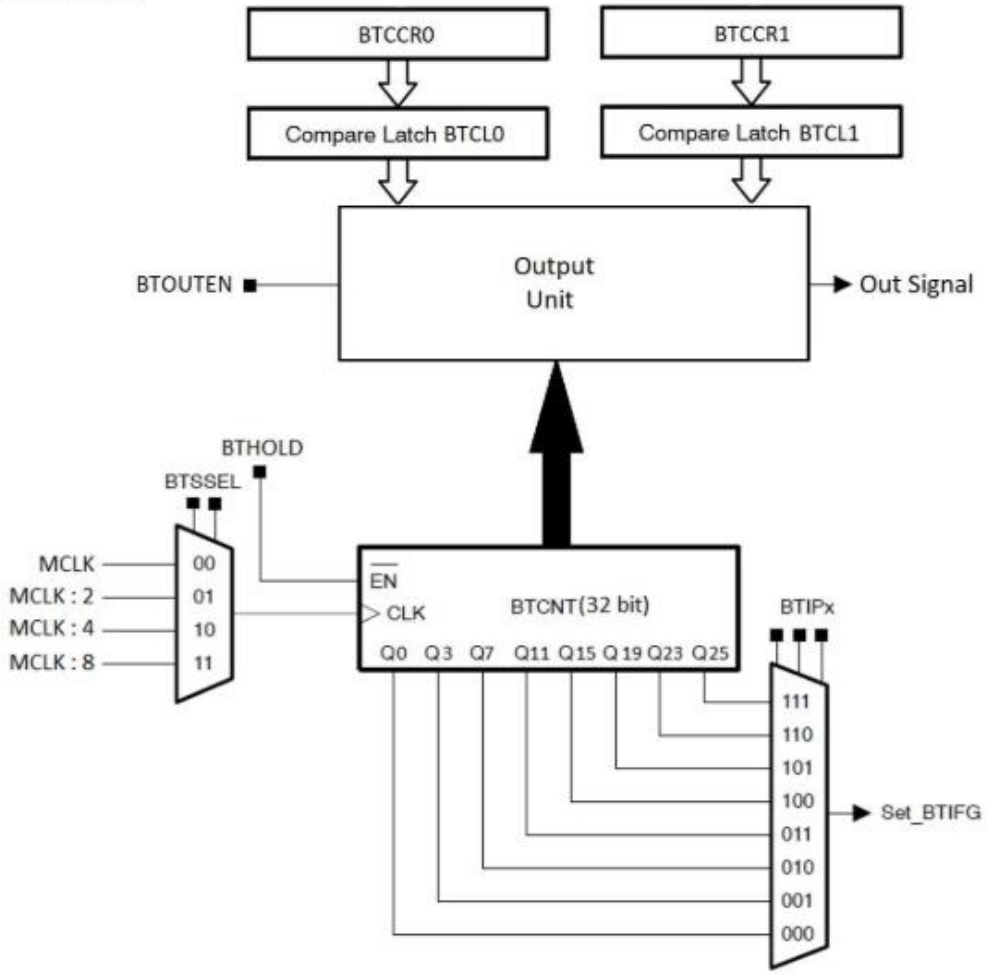
b) Basic Timer:



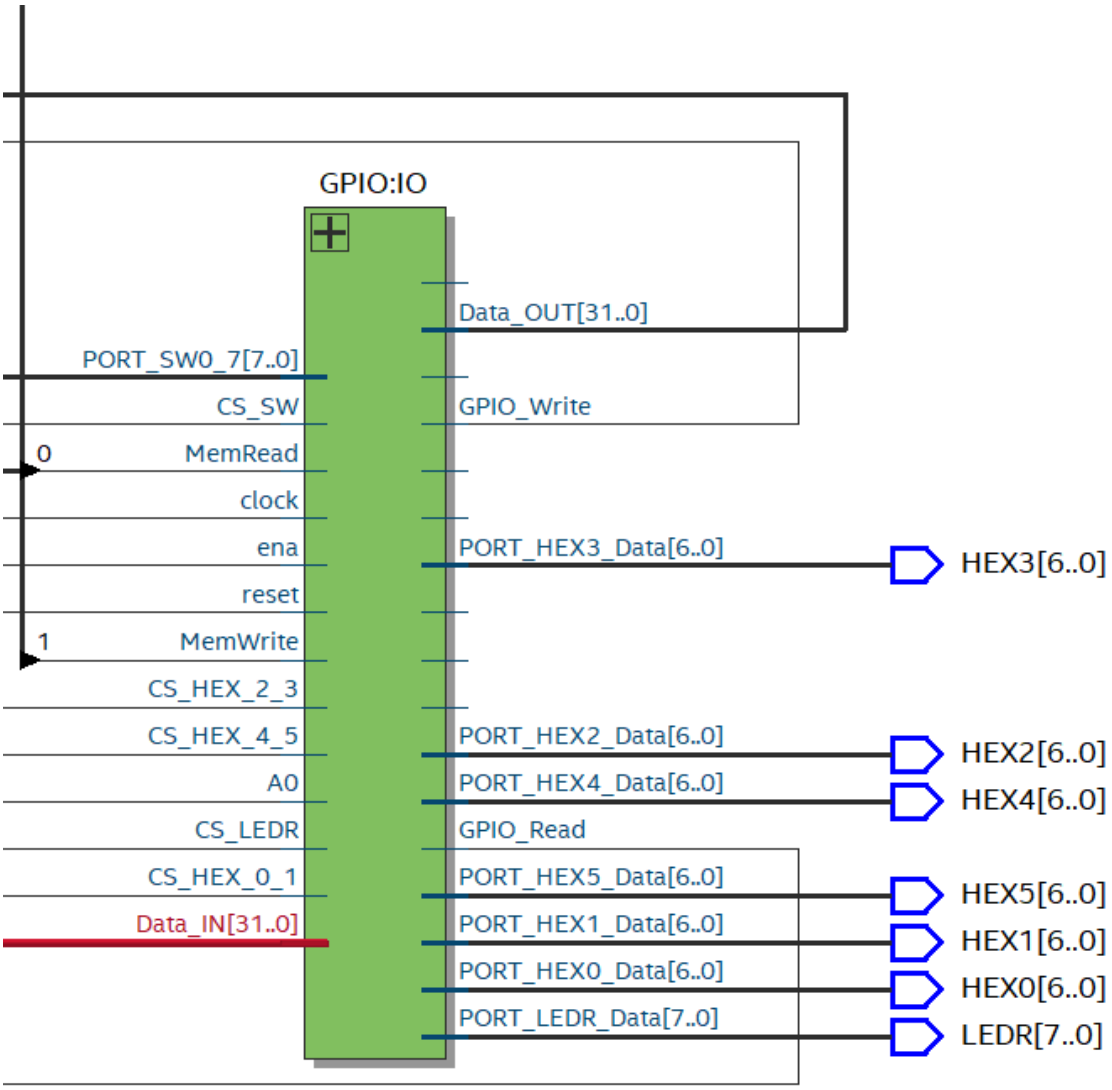

c) DivMCLK:

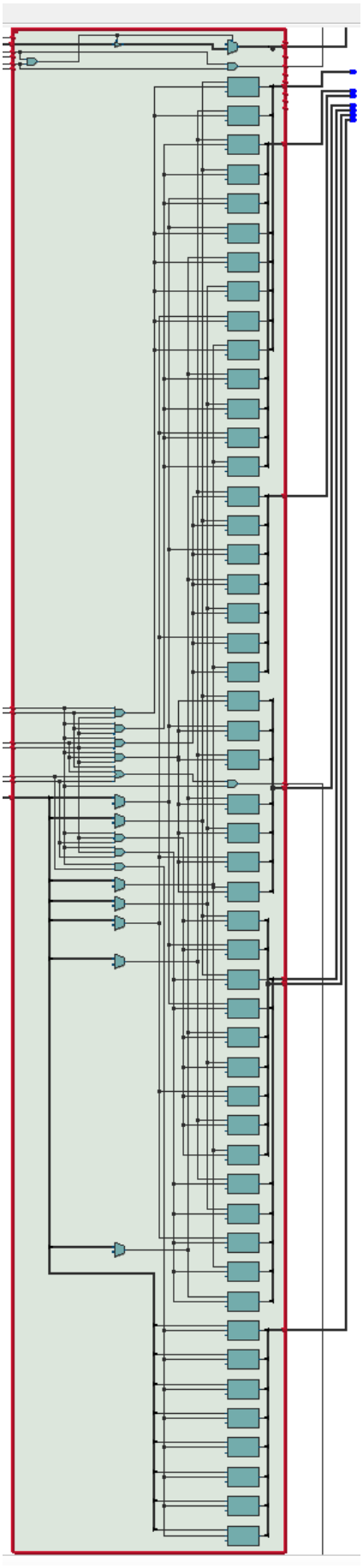


### *iii.* Basic Timer:

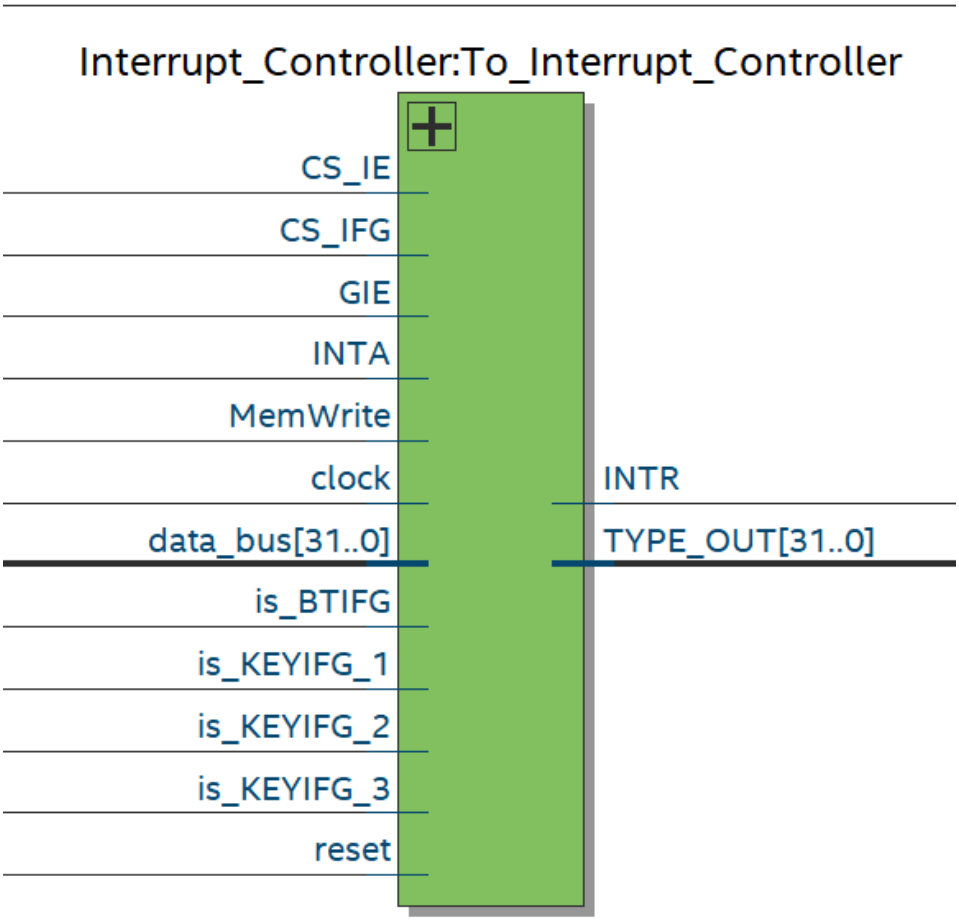


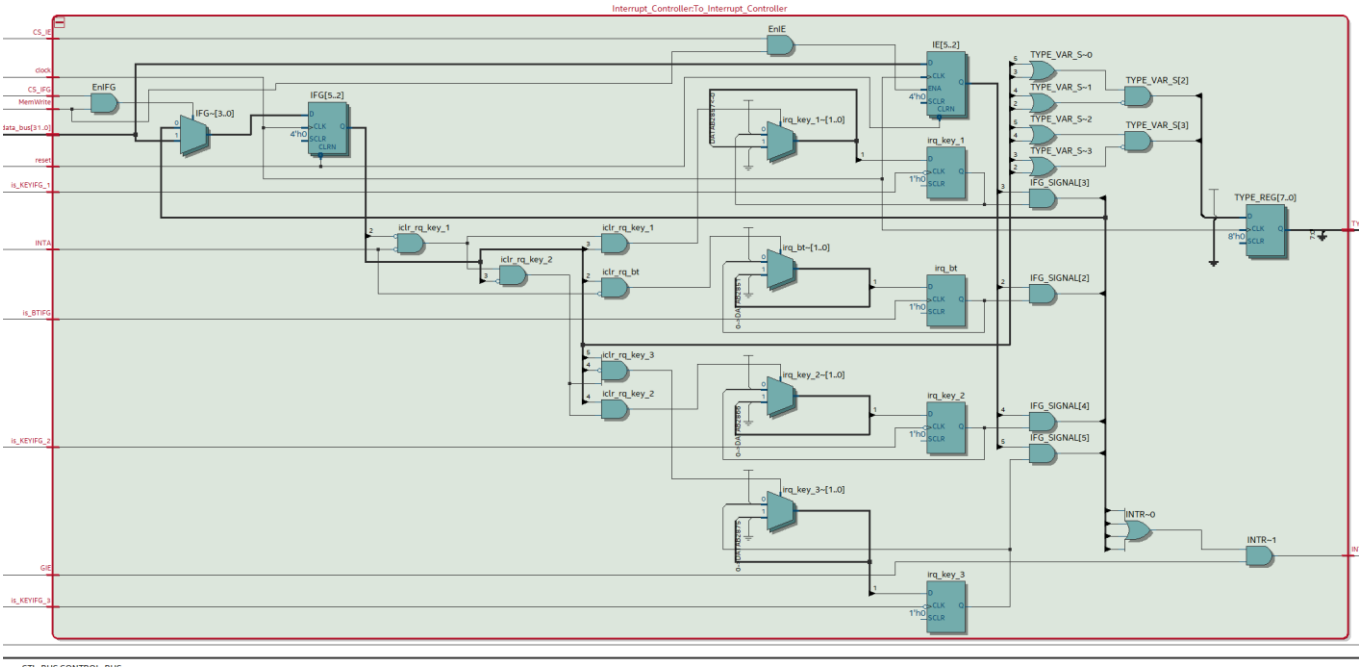
d) GPIO:


GPIO:IO
Data_OUT[31..0]
PORT_SW0_7[7..0]
CS_SW
GPIO_Write
0
MemRead
clock
ena
PORT_HEX3_Data[6..0]
HEX3[6..0]
reset
1
MemWrite
CS_HEX_2_3
CS_HEX_4_5
PORT_HEX2_Data[6..0]
HEX2[6..0]
A0
PORT_HEX4_Data[6..0]
HEX4[6..0]
CS_LEDR
GPIO_Read
CS_HEX_0_1
PORT_HEX5_Data[6..0]
HEX5[6..0]
Data_IN[31..0]
PORT_HEX1_Data[6..0]
HEX1[6..0]
PORT_HEX0_Data[6..0]
HEX0[6..0]
PORT_LEDR_Data[7..0]
LEDR[7..0]

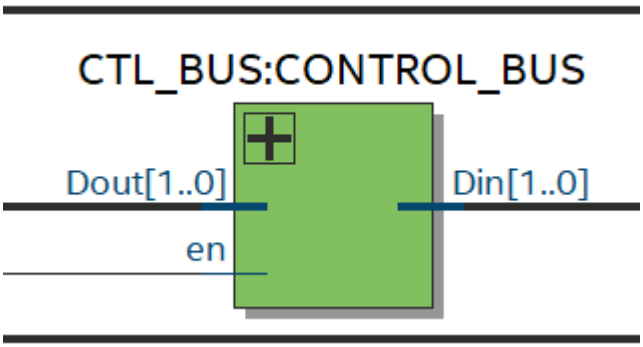


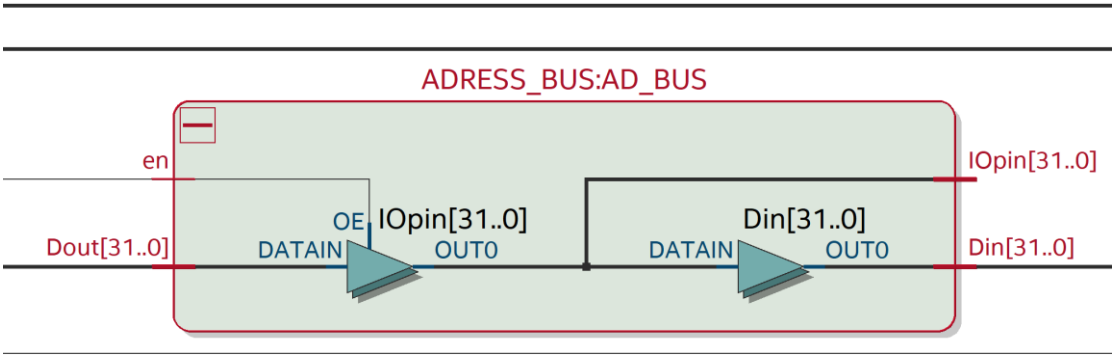
e) Interrupt_Controller :



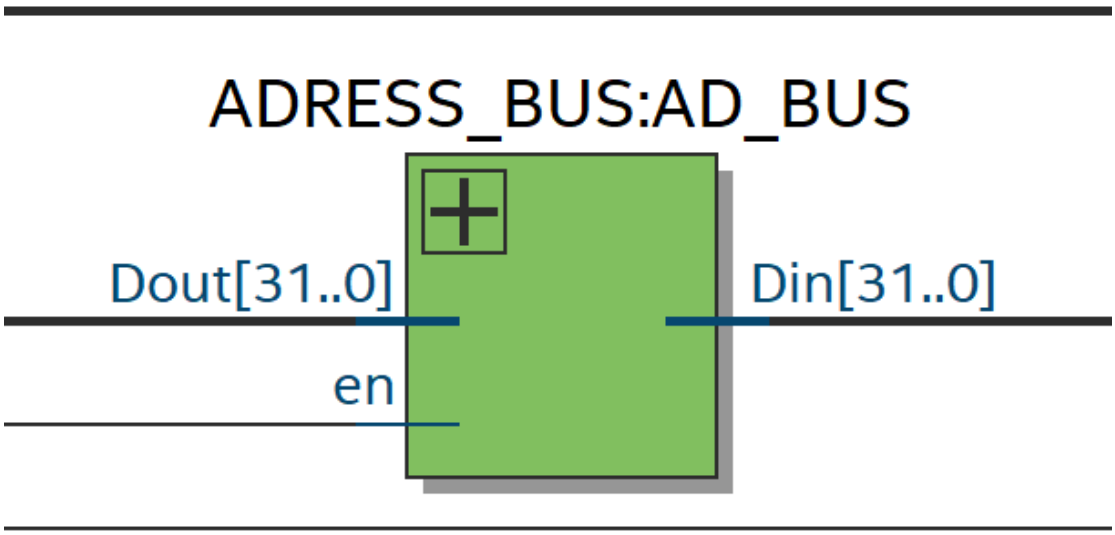


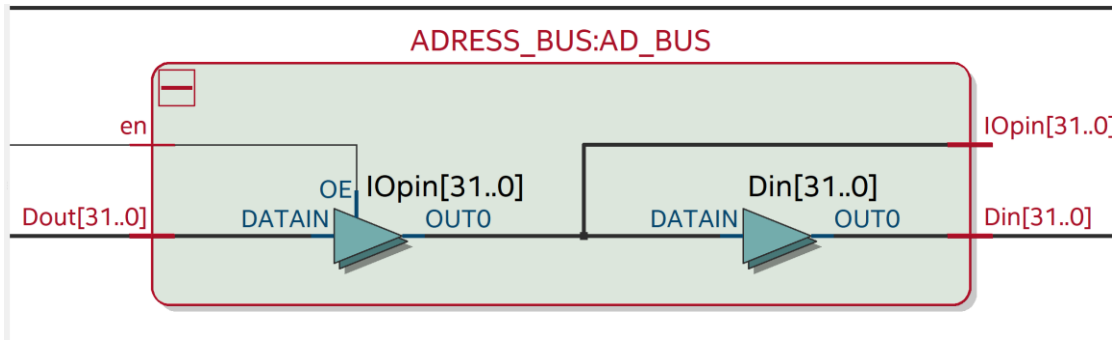

f) Control Bus:



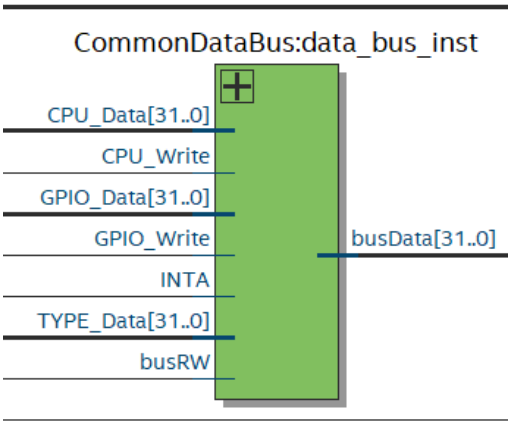



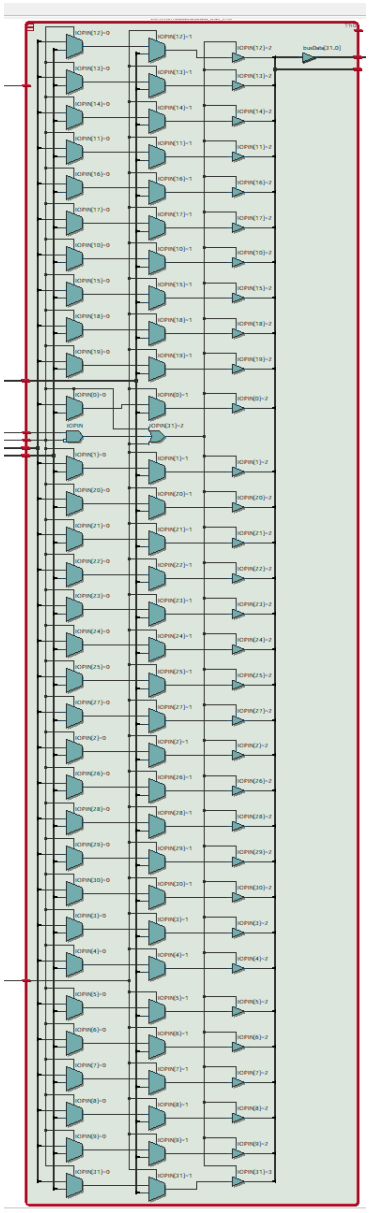
e) Address Bus:



g) Data Bus


CommonDataBus:data_bus_inst
CPU_Data[31..0]
CPU_Write
GPIO_Data[31..0]
GPIO_Write
INTA
TYPE_Data[31..0]
busRW
busData[31..0]



- Logic usage for each block

**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | In progress - Tue Aug 8 10:02:18 2023 |
| Quartus Prime Version | 21.1.0 Build 842 10/21/2021 SJ Lite Edition |
| Revision Name | TESTIMM |
| Top-level Entity Name | MIPS |
| Family | Cyclone V |
| Device | 5CSXFC5D6F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | N/A |
| Total registers | 1478 |
| Total pins | 139 |
| Total virtual pins | 0 |
| Total block memory bits | 16,384 |
| Total DSP Blocks | 2 |
| Total HSSI RX PCSs | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSs | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 |
| Total DLLs | 0 |

MIPS

**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | Successful - Tue Aug 8 10:07:43 2023 |
| Quartus Prime Version | 21.1.0 Build 842 10/21/2021 SJ Lite Edition |
| Revision Name | TESTIMM |
| Top-level Entity Name | BasicTimer |
| Family | Cyclone V |
| Device | 5CSXFC5D6F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 71 / 32,070 ( < 1 % ) |
| Total registers | 148 |
| Total pins | 40 / 499 ( 8 % ) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 ( 0 % ) |
| Total DSP Blocks | 0 / 87 ( 0 % ) |
| Total HSSI RX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA RX Deserializers | 0 / 9 ( 0 % ) |
| Total HSSI TX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA TX Serializers | 0 / 9 ( 0 % ) |
| Total PLLs | 0 / 15 ( 0 % ) |
| Total DLLs | 0 / 4 ( 0 % ) |

Basic Timer

| Flow Summary | |
|---|---|
| <<Filter>> | |
| Flow Status | Successful - Tue Aug 8 10:36:0 |
| Quartus Prime Version | 21.1.0 Build 842 10/21/2021 S. |
| Revision Name | TESTIMM |
| Top-level Entity Name | Interrupt_Controller |
| Family | Cyclone V |
| Device | 5CSXFC5D6F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 8 / 32,070 ( < 1 % ) |
| Total registers | 14 |
| Total pins | 76 / 499 ( 15 % ) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 ( 0 % ) |
| Total DSP Blocks | 0 / 87 ( 0 % ) |
| Total HSSI RX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA RX Deserializers | 0 / 9 ( 0 % ) |
| Total HSSI TX PCSs | 0 / 9 ( 0 % ) |
| Total HSSI PMA TX Serializers | 0 / 9 ( 0 % ) |
| Total PLLs | 0 / 15 ( 0 % ) |
| Total DLLs | 0 / 4 ( 0 % ) |

Interrupt Controller

**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | In progress - Tue Aug 8 10:43:5 |
| Quartus Prime Version | 21.1.0 Build 842 10/21/2021 S. |
| Revision Name | TESTIMM |
| Top-level Entity Name | Address_Decoder |
| Family | Cyclone V |
| Device | 5CSXFC5D6F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | N/A |
| Total registers | 0 |
| Total pins | 20 |
| Total virtual pins | 0 |
| Total block memory bits | 0 |
| Total DSP Blocks | 0 |
| Total HSSI RX PCSs | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSs | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 |
| Total DLLs | 0 |

Address Decoder

- Fmax

| | Fmax | Restricted Fmax | Clock Name | Note |
|---|---|---|---|---|
| 1 | 23.52 MHz | 23.52 MHz | clock | |
| 2 | 66.27 MHz | 36.75 MHz | reset | li...l) |
| 3 | 105.56 MHz | 105.56 MHz | Basic...Div\|D | |
| 4 | 105.56 MHz | 105.56 MHz | Basic...Div\|Q | |

- Conclusions

1. להקפיד על אלגוריתמים שמבוססים על חומרה ופחות על תוכנה.
2. כתיבה נכונה עשויה לחסוך המון רכיבי חומרה\זיכרון שלא לצורך.