Roee Shahmoon

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Click To See My Projects

• Third year student for a bachelor's degree in computer engineering at Ben Gurion University.
• Expected completion degree in three semesters.
• Knowledge in: Python, C, C++, VHDL, System Verilog, Assembly, Linux, TypeScript, SQL, Git.

Work Experience

2023 Aug - Present: Python Backend Developer at Circles AI - Part Time Job

As a Python Backend Developer at Circles AI, I using Python, TypeScript & JavaScript to develop robust and scalable backend solutions. Proficient in database management, I specialize in MySQL, ensuring efficient data handling and retrieval. Additionally, I have experience implementing GraphQL to enhance API functionality, I contribute to the success of Circles AI through my versatile skills in backend development.

Education

2020 - Present: B.Sc. in Computer Engineering, Ben Gurion University of the Negev, GPA 80

• Digital Design and Logic - Front-End processes in chip design, covering hardware design in Verilog, using HDL and Modelsim verification in SystemVerilog, and logic synthesis with Synthesizer and TCL.

• Structure of Digital Computers - Microprocessor Architecture MSP430: DMA, ADC, DAC, Timers, Watchdog, Interrupts, Cache, Memory Management, Virtual Memory, UART, I2C, SPI. Grade: 88

• CPU Architecture & Laboratory design utilizing VHDL and SOC with Intel DE10-standard. Proficient in MIPS and RISC-V processor architectures, specializing in designing pipelined thread processor. cores. Understanding of deep learning principles and their application in processor design. Grade: 86

• Introduction to System Programming - Linux work environment, C/C++ programming, object oriented programming (OOP), experienced in developing complex projects. Grade: 84

• Data Structures & Graph Theory & Algorithm Design: sorting, binary search trees, linked lists, hash tables, applying mathematical models of graphs and network using DFS, Dijkstra etc. Grade: 85

• Fundamentals of Computer Science - Python, Recursion, OOP, NumPy, CSV, Image processing.

Projects

• Hardware Acelerator of Matrix Multiplication written in Verilog & System Verilog: The Design use a Systolic Array Architecture, which enables a highly Parallel and Pipelined computational structure, to achieve high throughput and reduced latency compared to traditional sequential methods.

• Light Sources & Objects Detector System – RT Embedded:
PC side at Python & MCU Side at C, working with Texas Instruments MSP430 using Servo Motor, ADC12, Ultrasonic sensor, UART, PWM, Timers, GPIO, LCD, DMA.

• MIPS based MCU Architecture and Design: Building Single Cycle Mips, upgrade to a processor with a Pipeline core become Microcontroller burn to FPGA intel DE-10 using Quartus and Modelsim.

2011 – 2016: **Alliance Tel Aviv High School**
• Participation in a medical Physics project for outstanding students with a visit to Blinson Hospital.
• Engaged in school's volleyball team, instructor in scout movement, outstanding graduate, GPA 109.

Military Service

2016 – 2019: **Fighter and Commander in the 'Kfir' infantry brigade**
• Graduated from the commanders course led a team of 15 soldiers trained them to be fighters, complex operations in challenging environments, training commander certificate of excellence

Hebrew: native language, **English**: Fluent, **French**: Proficient.