Roee Shahmoon
Computer Engineering

Contact

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Links

Roee – Protfolio

Projects - Overiew

LinkedIn

Github

Skills

- Python
- C and C++
- Linux
- Assembly
- Verilog
- System Verilog
- VHDL
- HDL
- ModelSim
- Quartus
- TypeScript
- JavaScript
- MySQL
- GraphQL
- Git
- Github

Language

- Hebrew: Native
- English: Fluent
- French: Proficient

Occupation

→ 2023 Aug - present

Python Backend Developer at Circles AI - Part Time Job

• I developed and maintained backend services using Python, TypeScript, JavaScript contributing to the successful launch of Relationship Type Clients repo.
• Proficient in database management, specialize in MySQL, optimized database queries and data access patterns, resulting improvement in system performance.
• I have experience implementing GraphQL to enhance API, contribute to success of Startup.

Education

→ 2020 Oct – present

B.Sc. Computer Engineering, Ben Gurion University, GPA 80.

Courses:

• Digital Design and Logic – Front End processes in chip design, covering hardware design in Verilog, using HDL and Modelsim, verification in SystemVerilog.

• Structure of Digital Computers - Microprocessor MSP430: DMA, ADC, DAC, Timers, Watchdog, Interrupts, Cache, Memory Management, Virtual Memory, UART. Grade: 88

• CPU Architecture & Laboratory design utilizing VHDL and SOC with Intel DE10-standard. Proficient in MIPS and RISC-V processor architectures, specializing in designing pipelined thread processor cores. Understanding of deep learning principles and their application in processor design. Grade: 86

• Systems programming : Linux work environment, C/C++ memory management and data storage, develop and test software , top-down design and high-level abstraction, and design patterns. Grade: 84

• Data Structures & Graph Theory & Algorithm Design: Sorting, BST, linked lists, hashtable, applying mathematical models of graphs and network using DFS, Dijkstra etc. Grade: 85

Projects:

• Hardware Acelerator of Matrix Multiplication written in Verilog & System Verilog: The Design use a Systolic Array Architecture, which enables highly Parallel and Pipelined computational structure, to achieve high throughput, reduced latency compared to sequential methods.

• Light Sources & Objects Detector System – RT Embedded:
PC side at Python & MCU Side at C, working with Texas Instruments MSP430 using Servo Motor, ADC12, Ultrasonic sensor, UART, PWM, Timers, GPIO, LCD, DMA.

• MIPS based MCU Architecture and Design: Building Single Cycle Mips, upgrade to a processor with a Pipeline core become Microcontroller burn to FPGA intel DE-10 using Quartus and Modelsim.

→ 2011 - 2016

Alliance Tel Aviv High School

• Participation in a medical Physics program for outstanding students with visit Blinson Hospital.
• Engaged in school's volleyball team, instructor in scout movement. GPA 109.

Military Service

→ 2016 – 2019

Fighter and Commander in the 'Kfir' infantry brigade

• Graduated from the commander's course led a team of 15 soldiers trained them to be fighters.
• Complex operations in challenging environments, training commander certificate of excellence.