

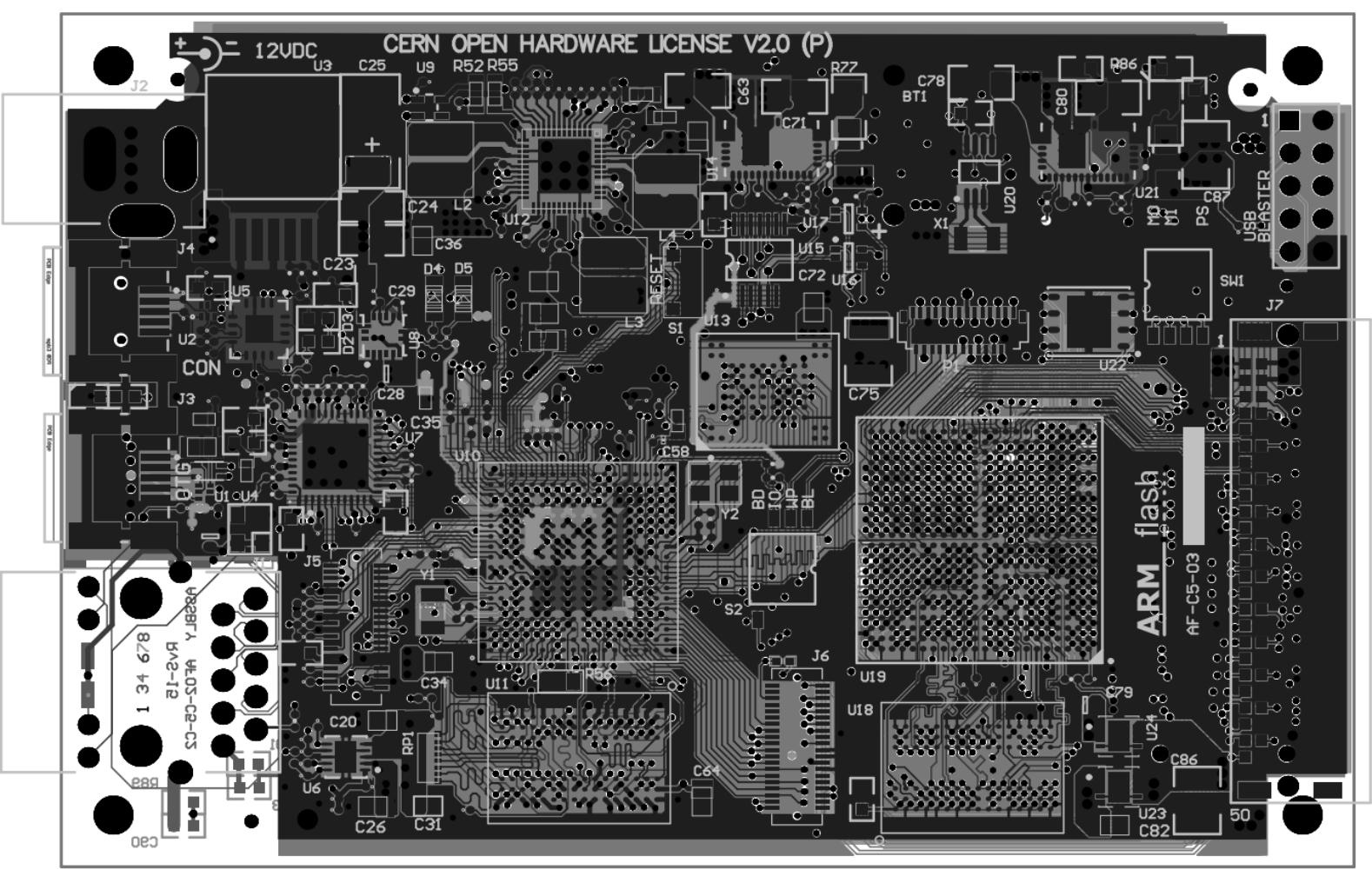


This diagram shows the CERN Open Hardware License V2.0 (P) circuit board. The board is green with various electronic components, including integrated circuits (U1 through U28), capacitors (C1 through C87), resistors (R1 through R56), and connectors (J1 through J7). Key labels on the board include:

- Power:** 12VDC input at J2.
- Components:** U1, U2, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28.
- Connectors:** J1, J2, J3, J4, J5, J6, J7.
- Capacitors:** C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87.
- Resistors:** R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56.
- Other:** CON, OTG, RESET, BD, IO, WP, BL, S1, S2, P1, BT1, M0, M1, PS, SW1, JF-C5-03, ARM flash, 50.

The board is subject to the CERN OPEN HARDWARE LICENSE V2.0 (P).

CERN OPEN HARDWARE LICENSE V2.0 (P)



REV	Description	DATE	BY
A1	Initial Production Release.	10/08/2013	RvS
B1	Revised 1G PHY arrangement, HDMI option & USB	08/1/2014	RvS
B2	Updated footprint Coils, KSZ9021, and bottom layer fiducial cutouts Introduced GND debounce at oscillator CPU Changed WAIT1 on NAND to WAIT0 Freed up resistor for boot setting Mirror bottom legend, removed PHY linear regulator (there is no 1V2 version of the LT1965!) Changed PHY ADDR from 4 to 1 Removed snubbing resistor from PHY links to CPU	17/3/2014	RvS
C1	Changed FPGA: C3 to C5 and change DDR2 to DDR3, increase to CPU memory to 512MB DDR3 Changed console FTDI chip, moved sensors to I2C bus 1 Reduced 0201 caps, added ext VREF, external JTAG option	24/12/2014	RvS
C2	Need to clean up IO banks allocation Removed link to GND from TRST Power LED activated by console port - change IO voltage FT230 Changed Bank3A VCCIO to fix at 3V3 Swapped I2C bus 2 SDA/SCL pins Increased pullups on FPGA programming side to 10k Remove R102 linking Reset switch with PowerON for PMIC Remove pull up resistor on ENET_RESET line		
	Consider moving GPMC connections to reduce latency		

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	PROCESSOR 1 OF 3, JTAG HEADER
3	PROCESSOR 2 OF 3, USB PORTS
4	PROCESSOR 3 OF 3
5	POWER MANAGEMENT
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	HDMI
9	10/100/1000 ETHERNET
10	NAND & SD CARD
11	USB1 PORT
12	UART-USB CONSOLE
13	FPGA CONNECTOR CONNECTIONS
14	FPGA
15	FPGA DDR3 MEMORY
16	POWER SUPPLY



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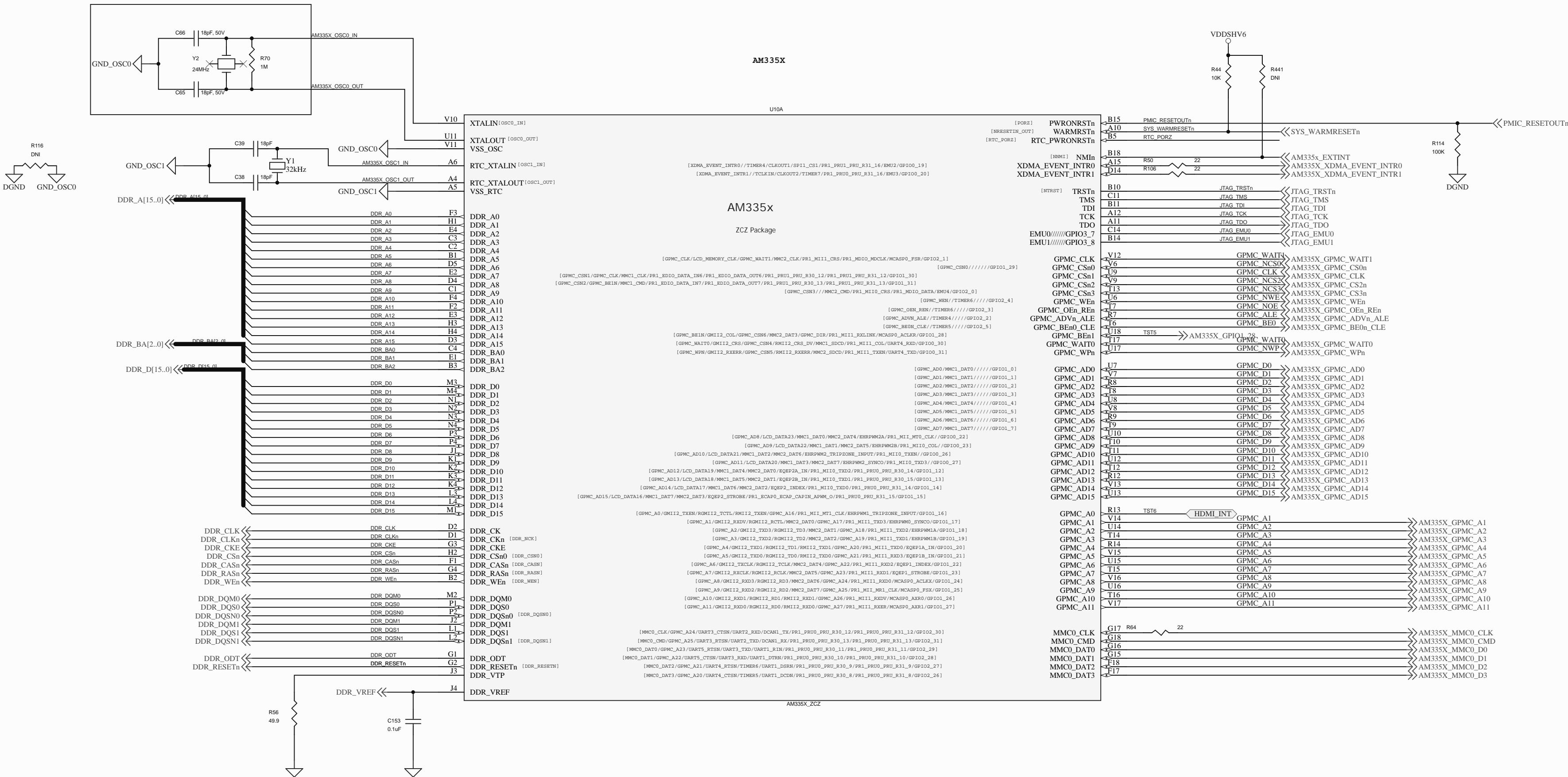
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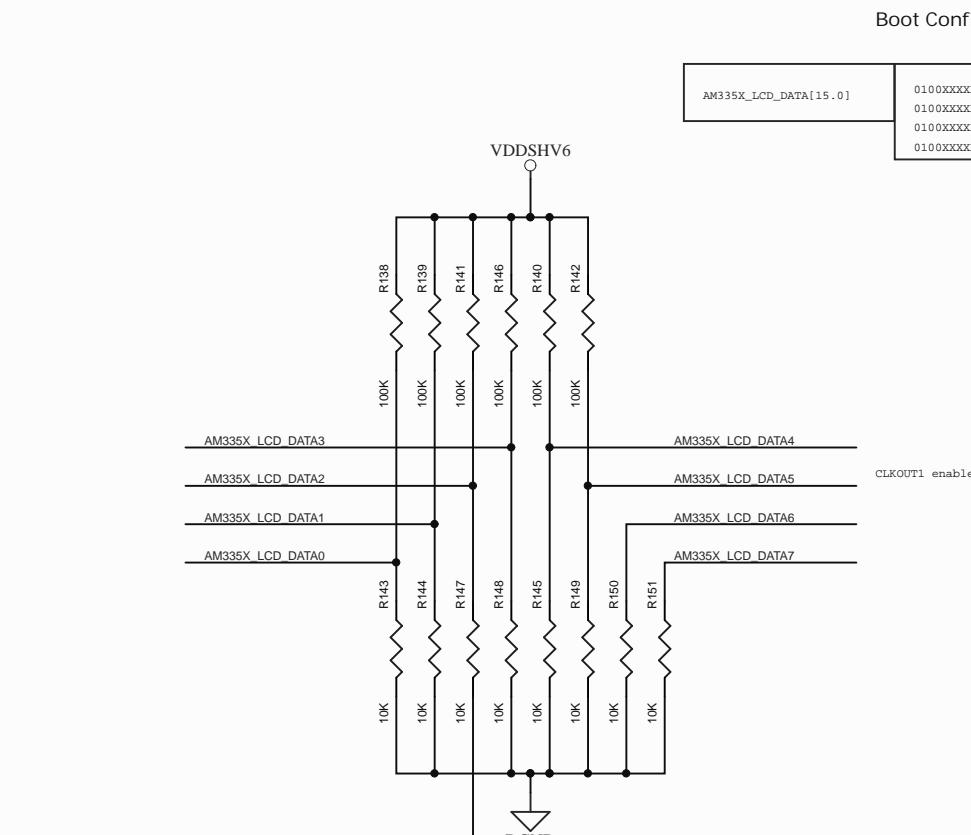
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A





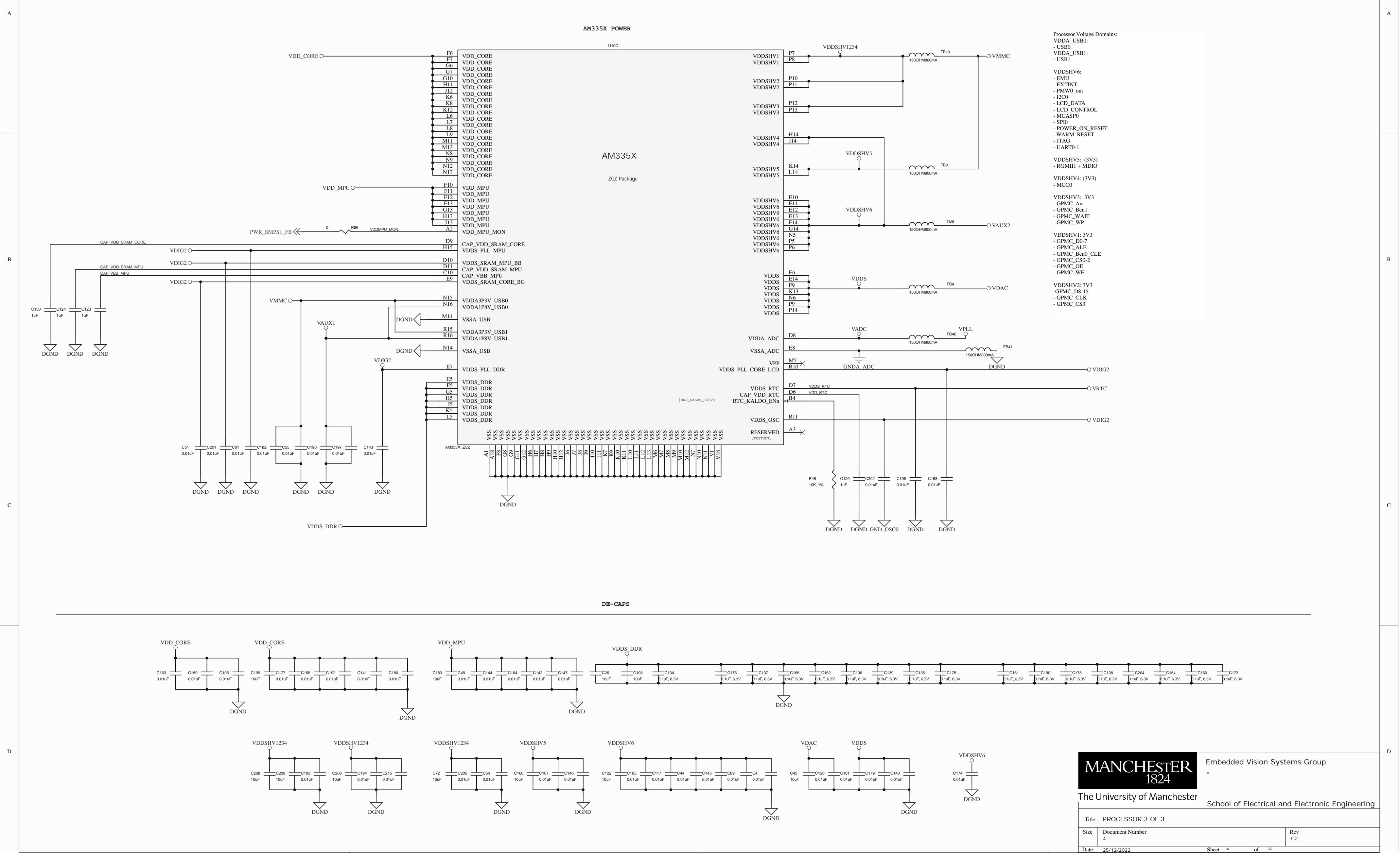
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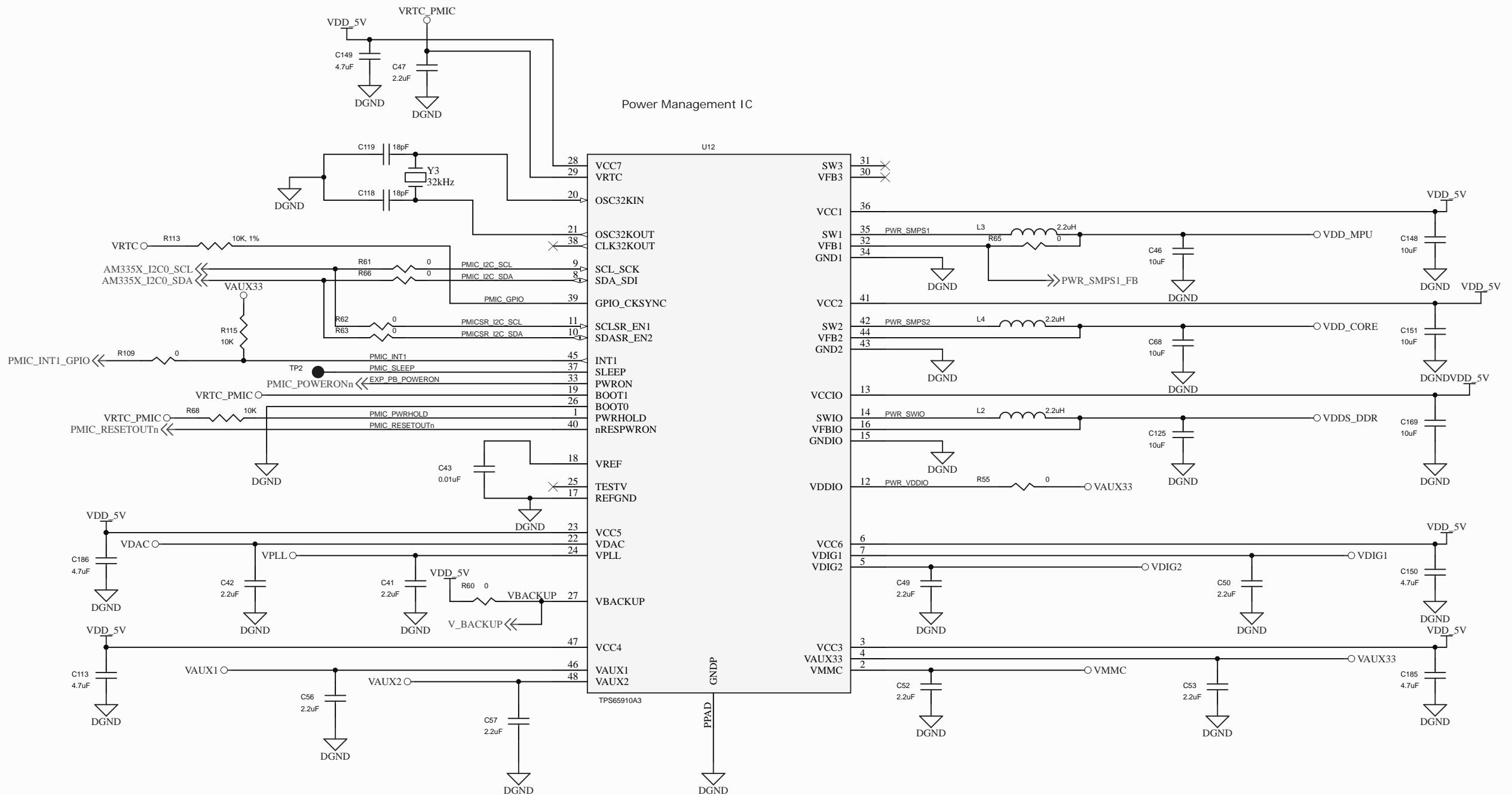
Journal of Health Politics, Policy and Law, Vol. 32, No. 3, June 2007  
DOI 10.1215/03616878-32-3 © 2007 by The University of Chicago

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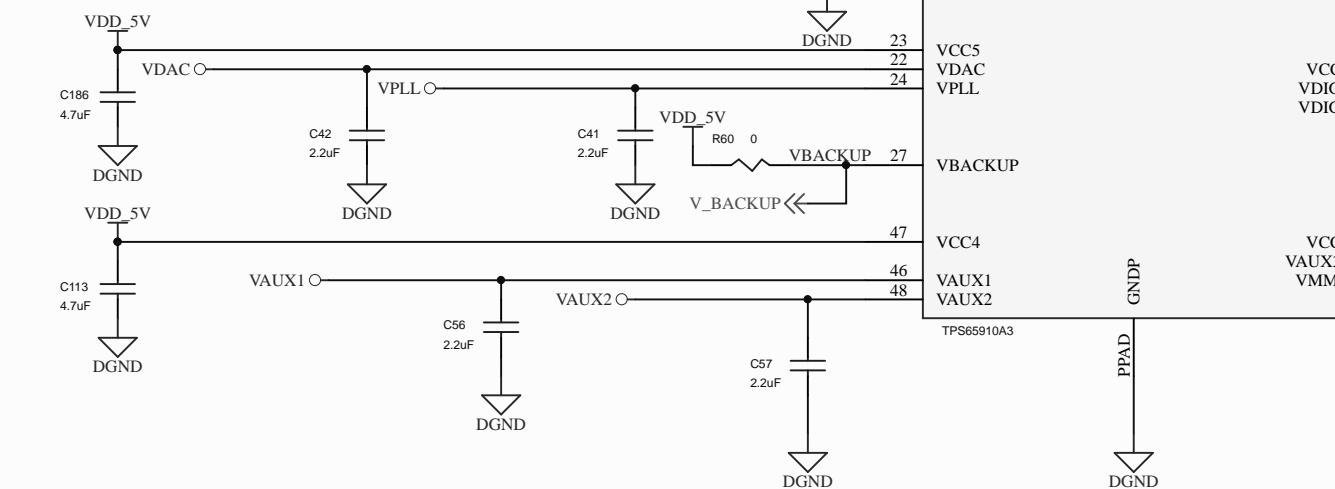
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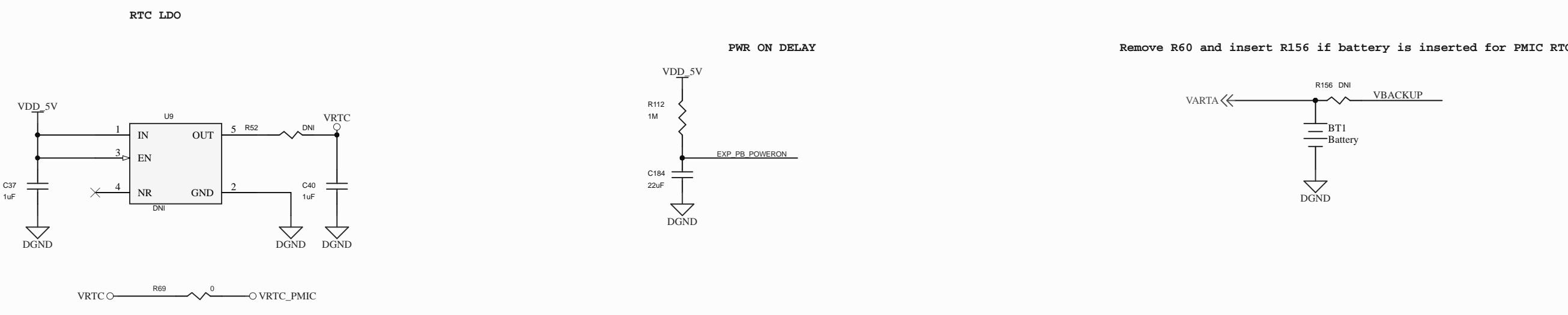
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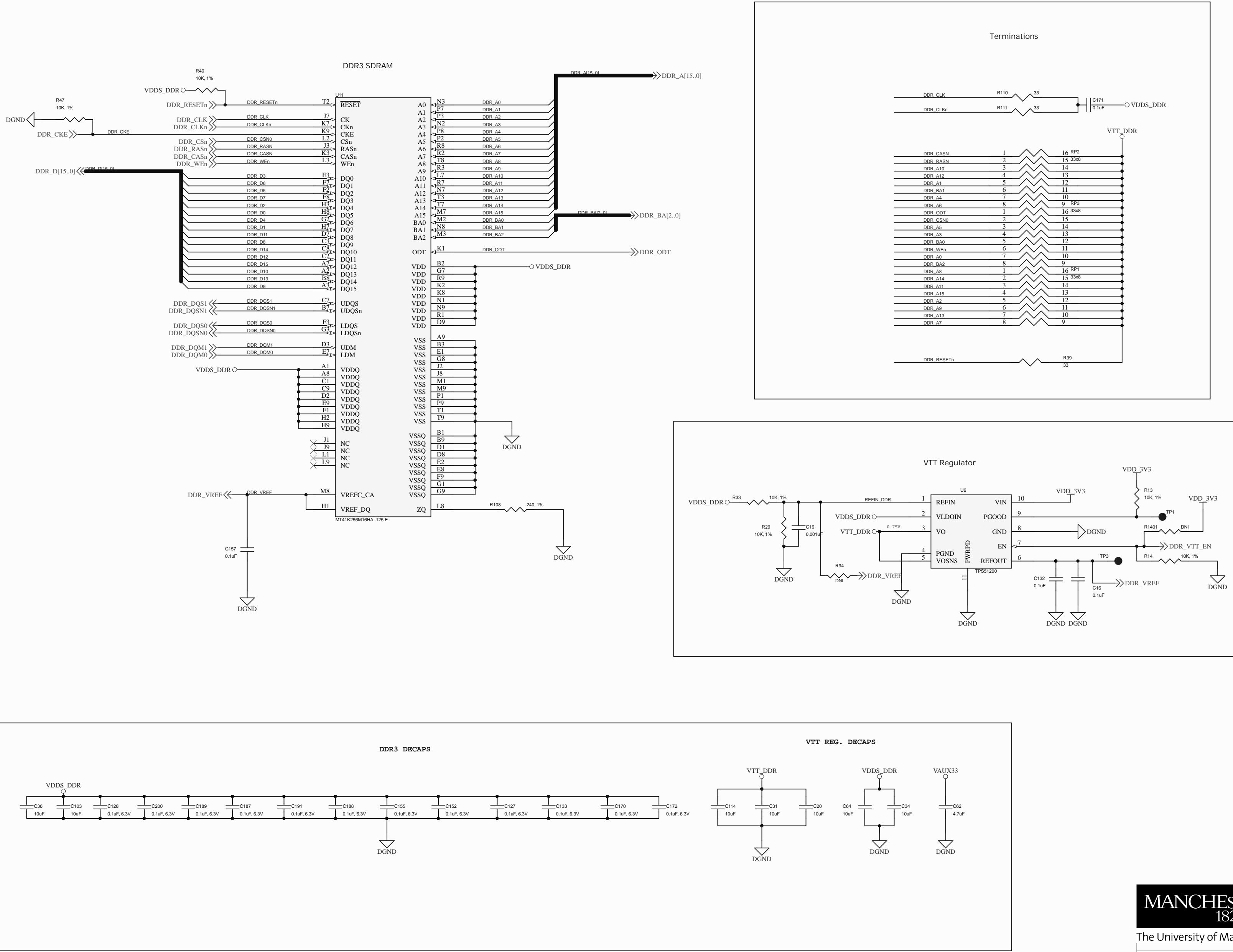


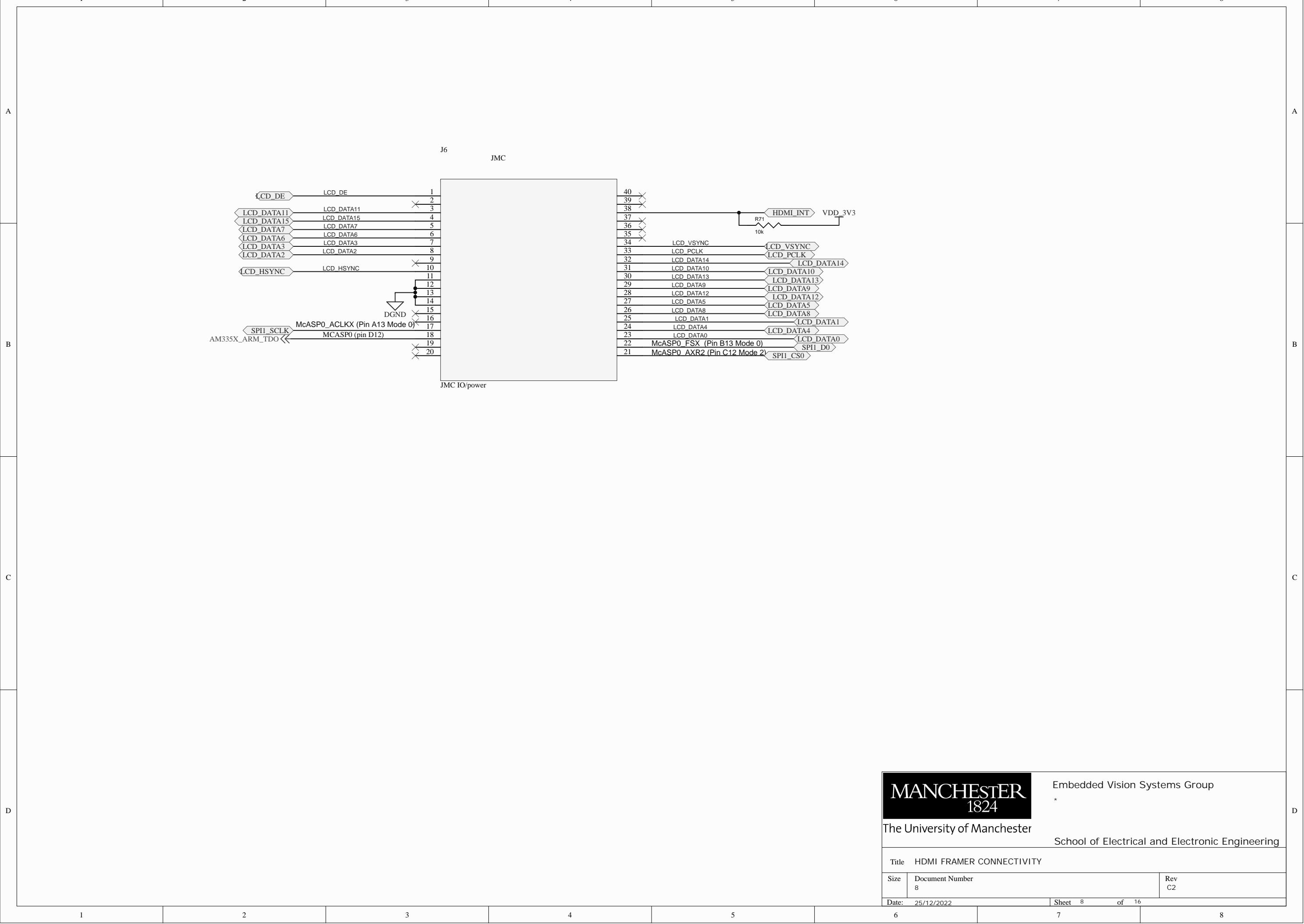
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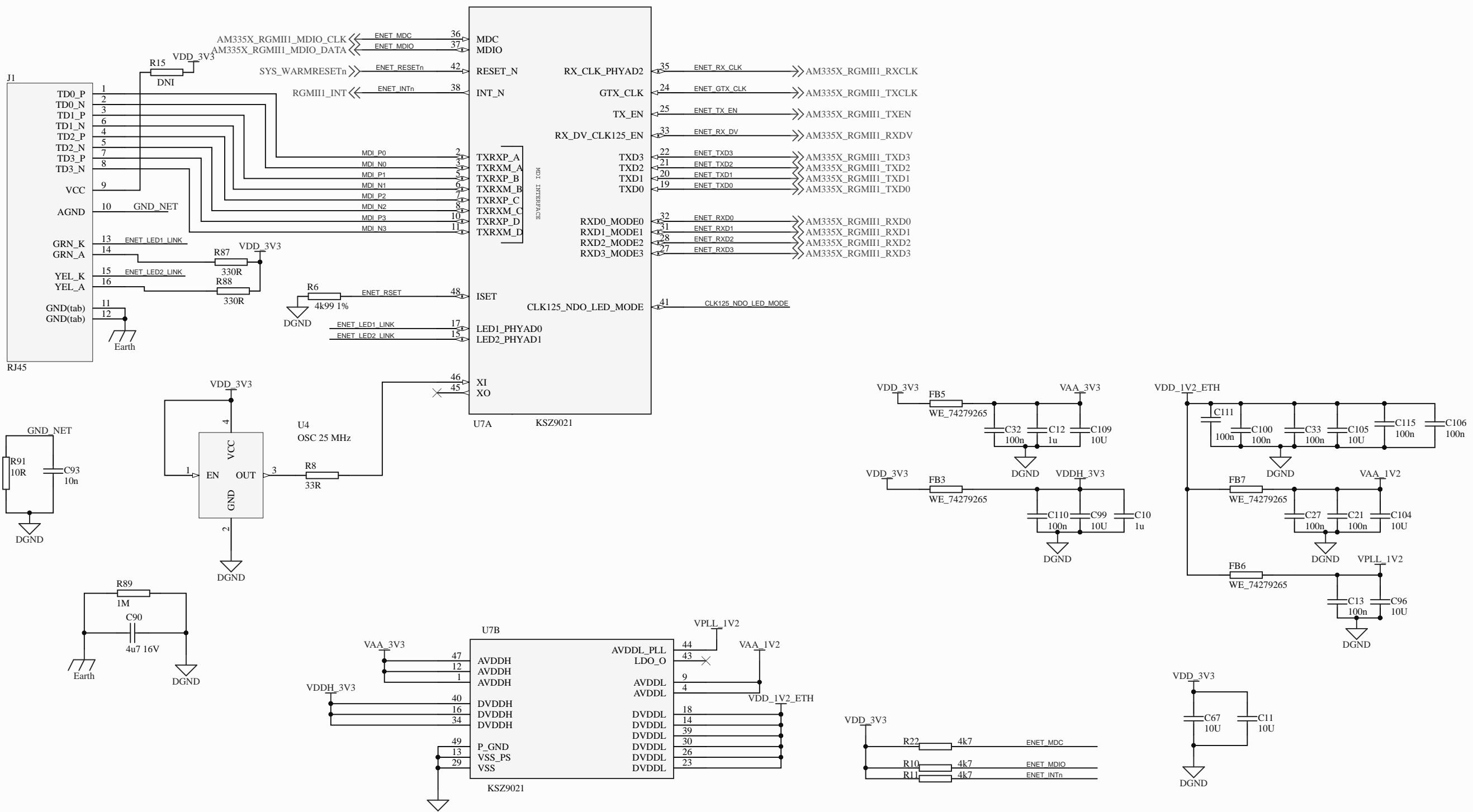


D









Configuration selected:

Single LED mode

RGMII interface advertising 10/100/1000 Full & Half Duplex

PHY ADDR[4..0] = 00001



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Title 10/100/1G PHY

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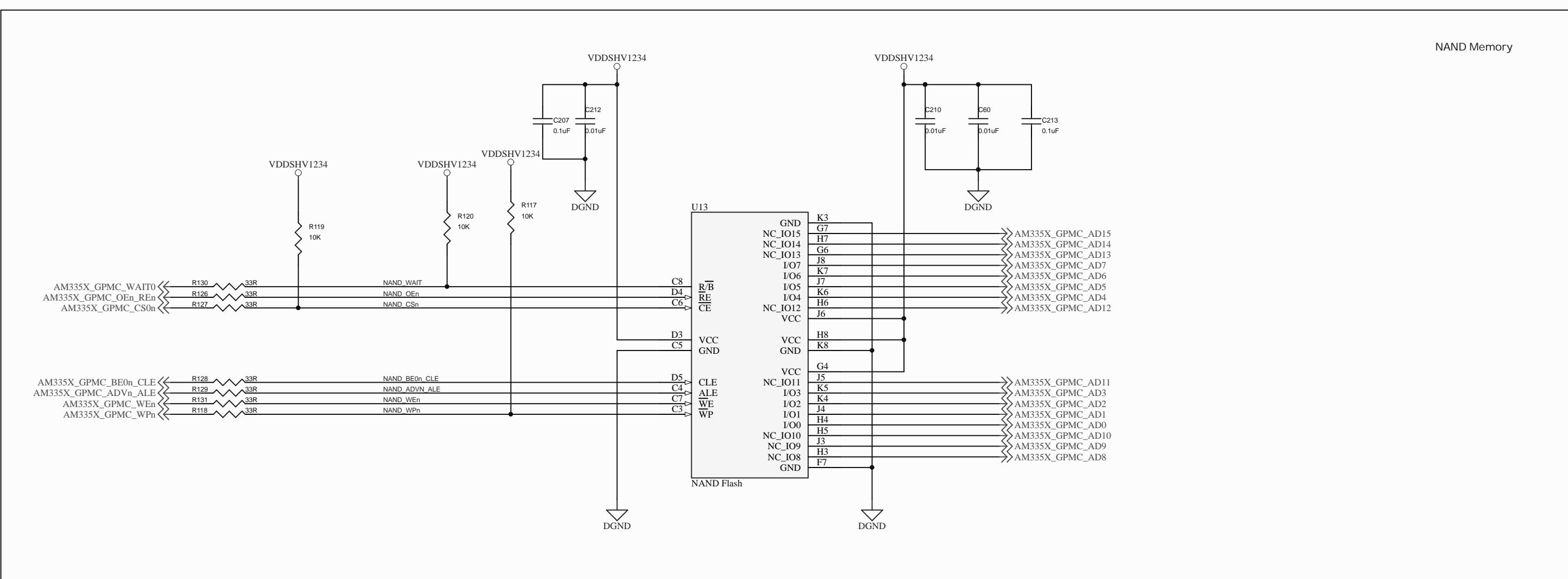
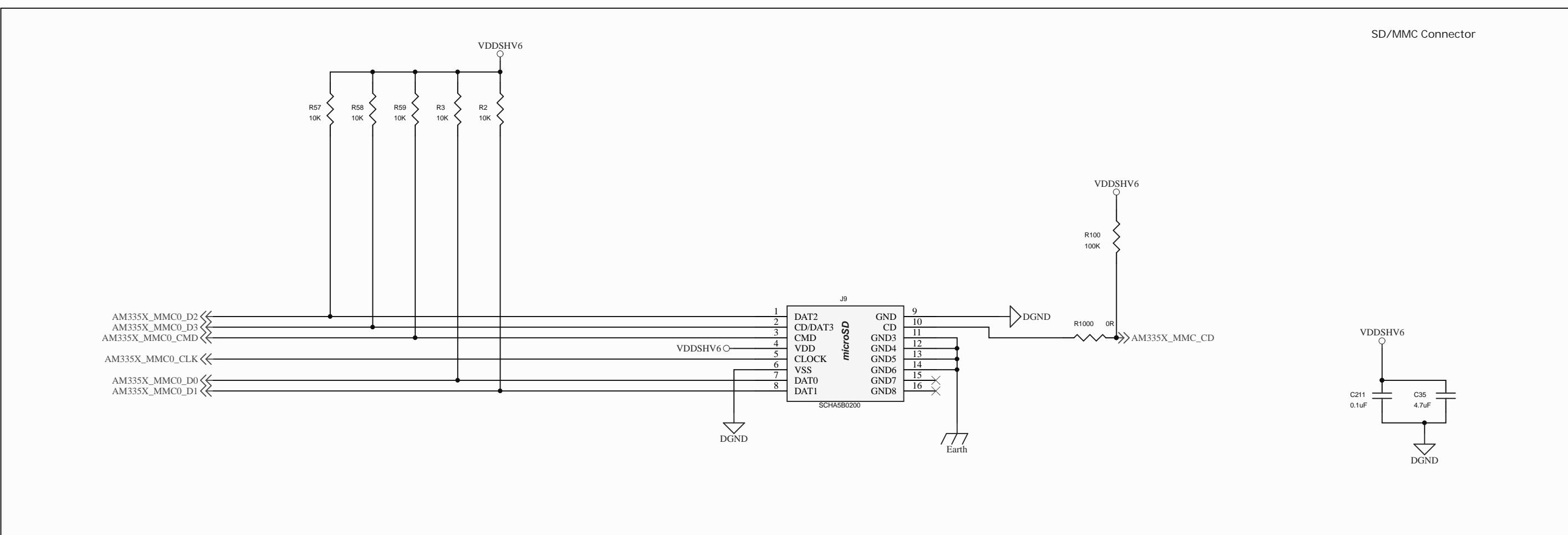
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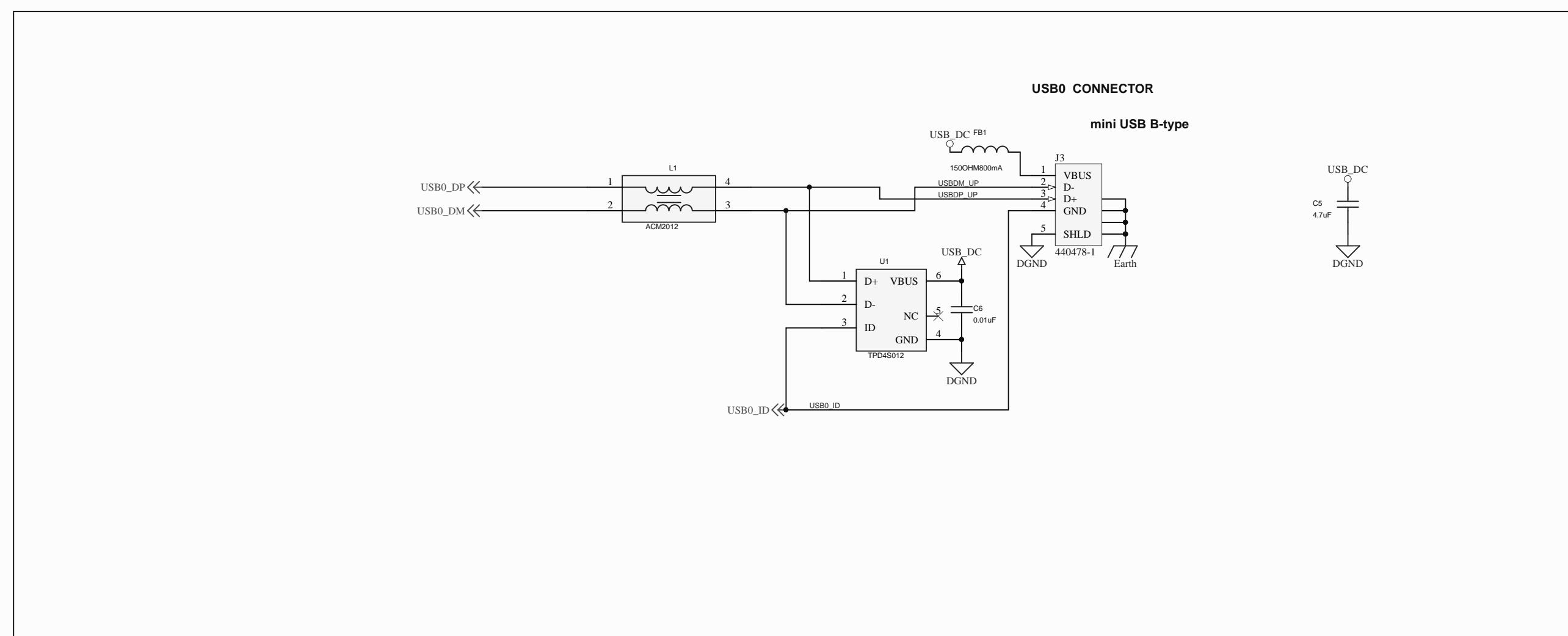
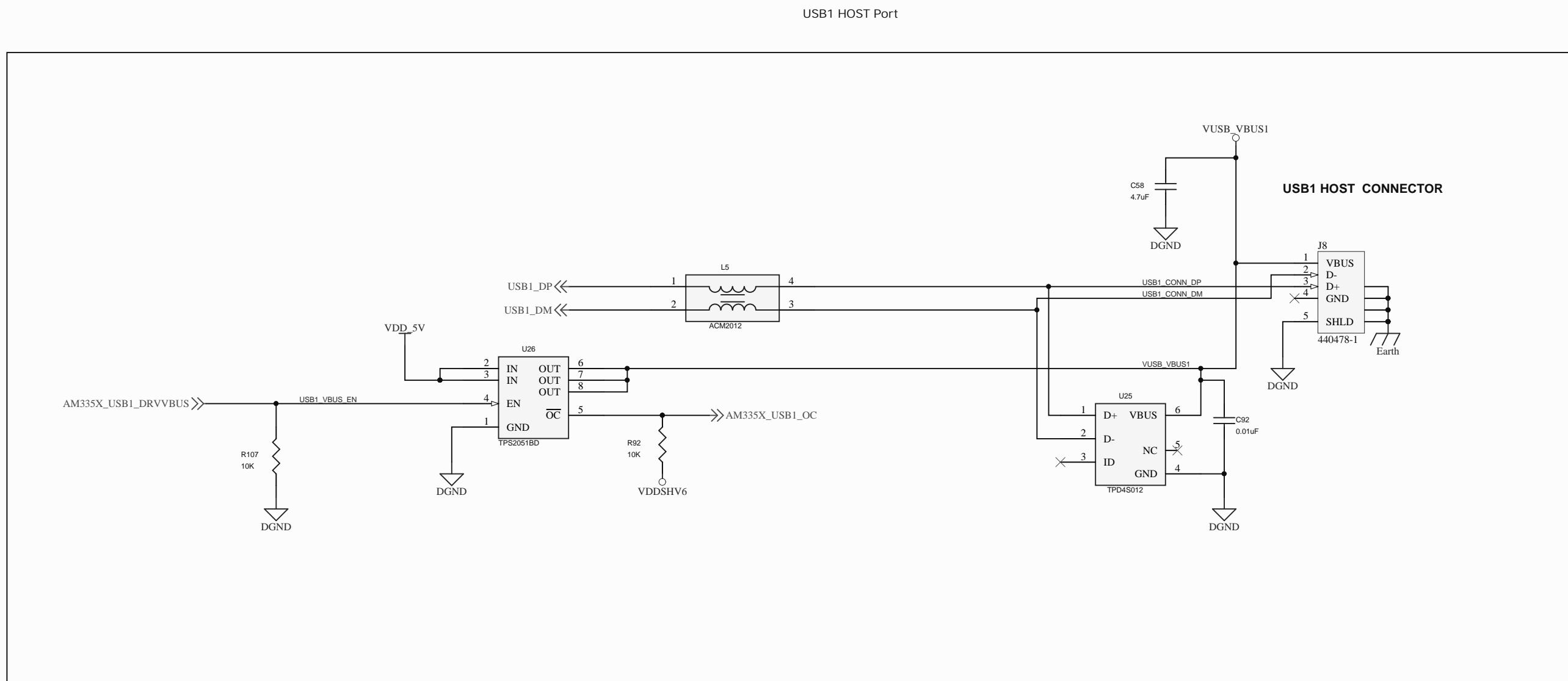
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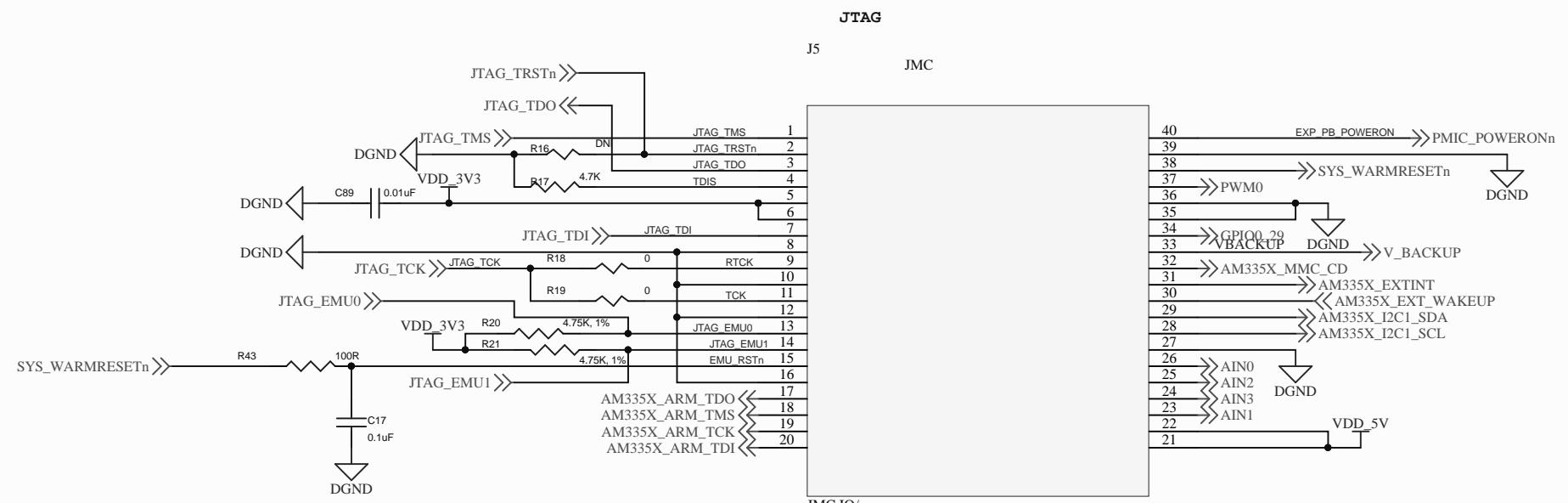
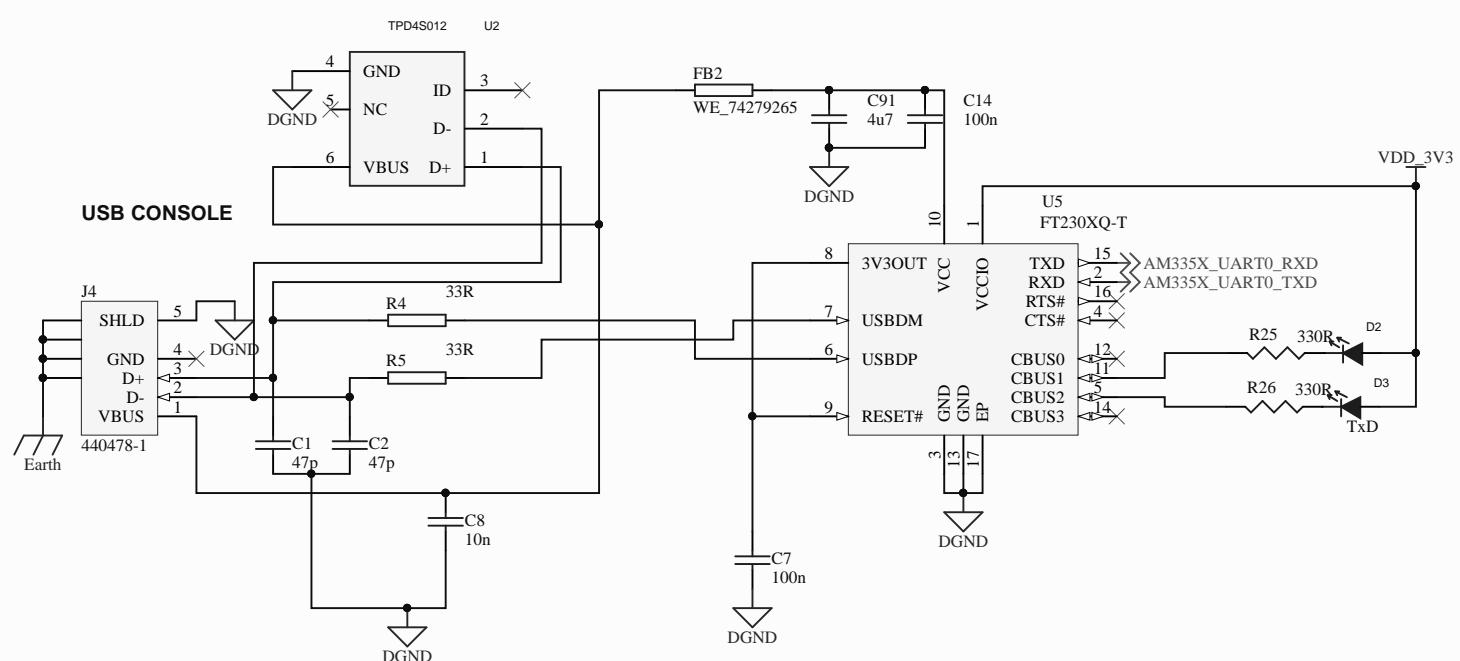
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1 2 3 4 5 6 7 8





USB - UART



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Title UART - USB CONSOLE & JTAG

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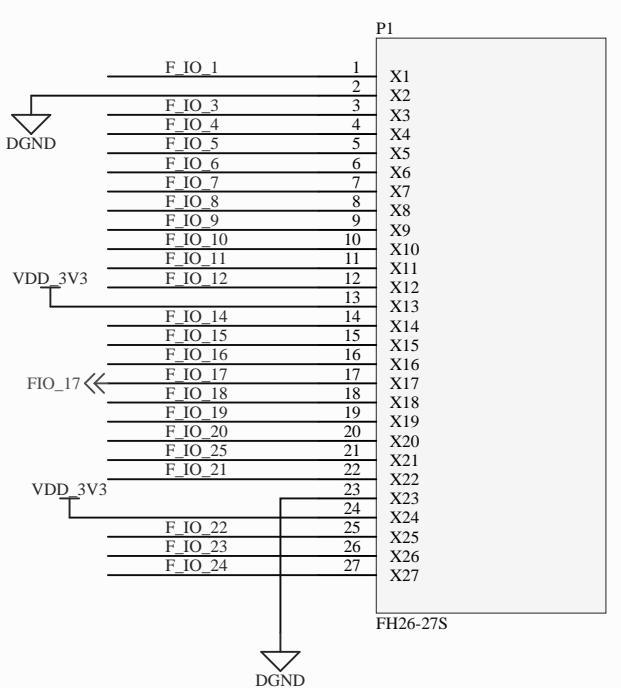
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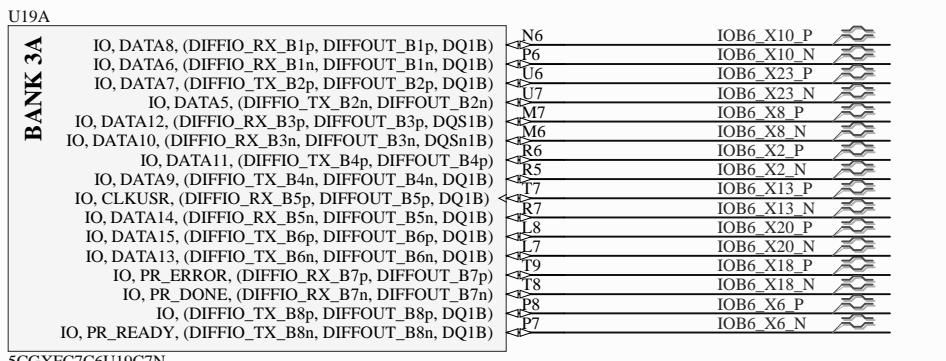
Date: 25/12/2022

1

## External Port To BANK 6 FPGA

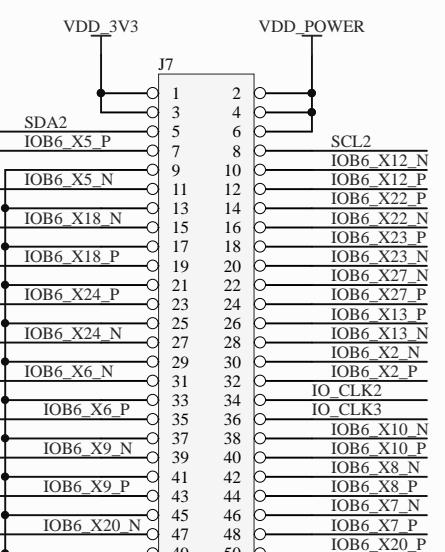


Bank 5:

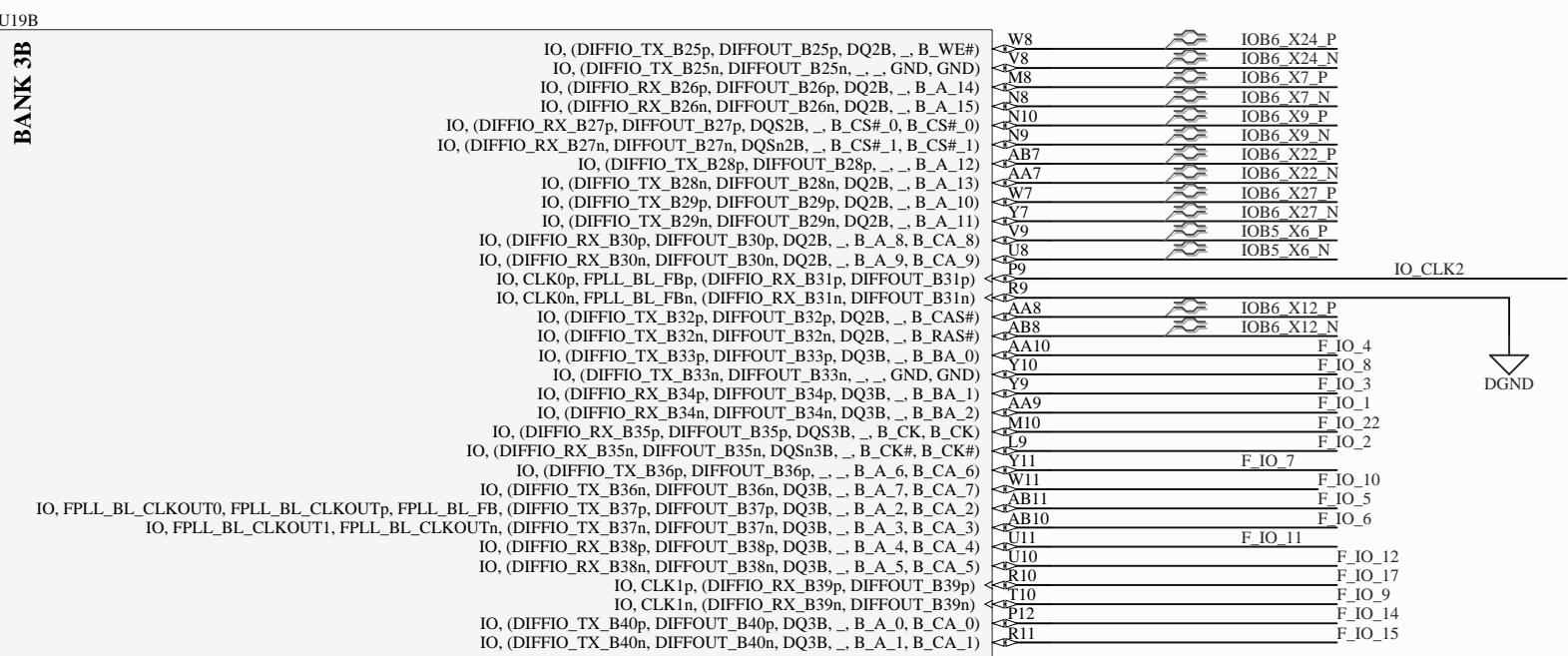


### Sank 3: EXT. BUS

**This 50-pin ERNI connector only has I2C (SCL,SDA)  
ERNI connects to FPGA Bank 6**



U19B

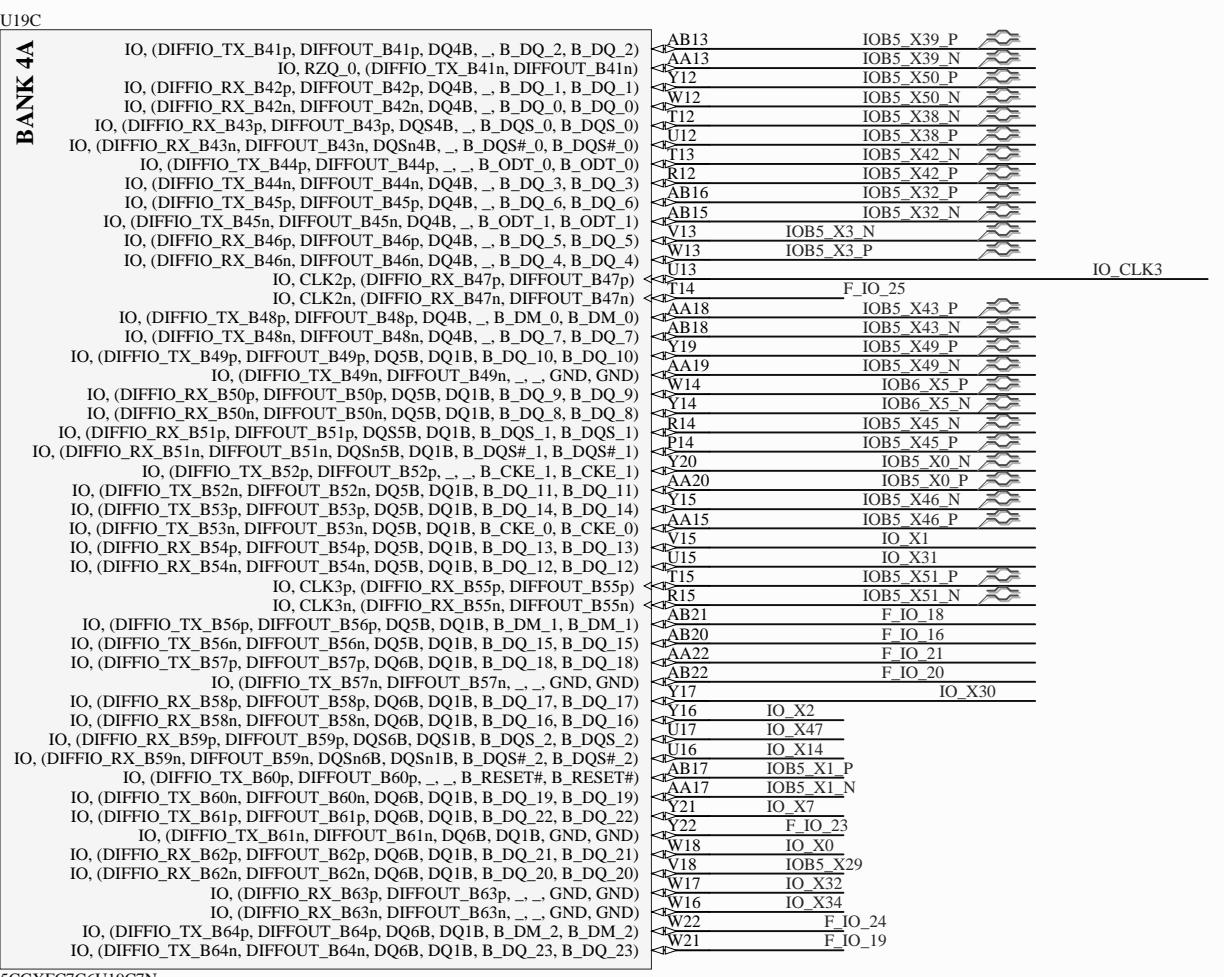


```
>>> REFCLKL1P  
>>> REFCLKL1LN  
>>> GBX_RX_L3p, GBX_REFCLK_L3p  
>>> GBX_RX_L3n, GBX_REFCLK_L3n  
>>> GBX_TX_L3p  
>>> GBX_TX_L3n  
>>> GBX_RX_L4p, GBX_REFCLK_L4p  
>>> GBX_RX_L4n, GBX_REFCLK_L4n  
>>> GBX_TX_L4p  
>>> GBX_TX_L4n  
>>> GBX_RX_L5p, GBX_REFCLK_L5p  
>>> GBX_RX_L5n, GBX_REFCLK_L5n  
>>> GBX_TX_L5p  
>>> GBX_TX_L5n
```

```
U19H  
--> REFCLK0Lp  
--> REFCLK0Ln  
--> GXB_RX_L0p, GXB_REFCLK_L0p  
--> GXB_RX_L0n, GXB_REFCLK_L0n  
--> GXB_TX_L0p  
--> GXB_TX_L0n  
--> GXB_RX_L1p, GXB_REFCLK_L1p  
--> GXB_RX_L1n, GXB_REFCLK_L1n  
--> GXB_TX_L1p  
--> GXB_TX_L1n  
--> GXB_RX_L2p, GXB_REFCLK_L2p  
--> GXB_RX_L2n, GXB_REFCLK_L2n  
--> GXB_TX_L2p  
--> GXB_TX_L2n
```

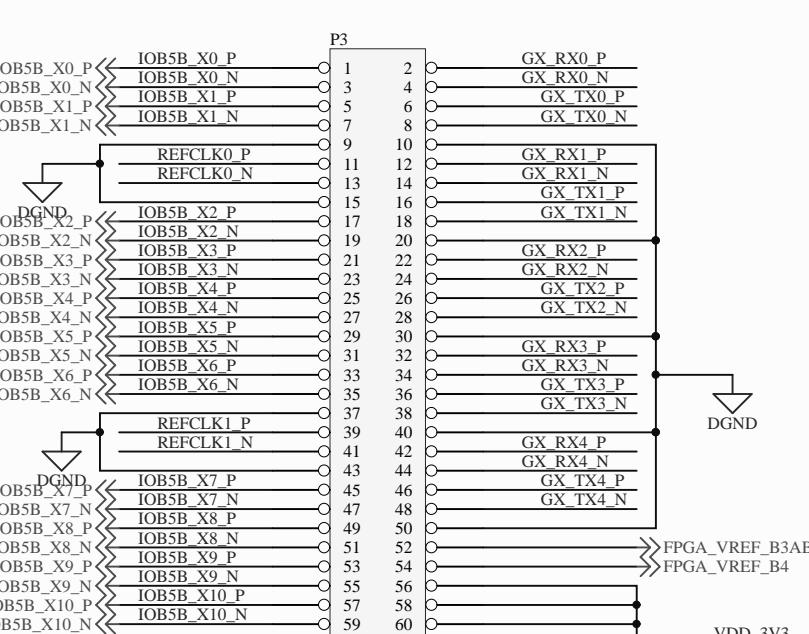
5CGXFC7C6U19C7N

U19C



DGND This connector has both I2C and SPI

5CGXFC7C6U19



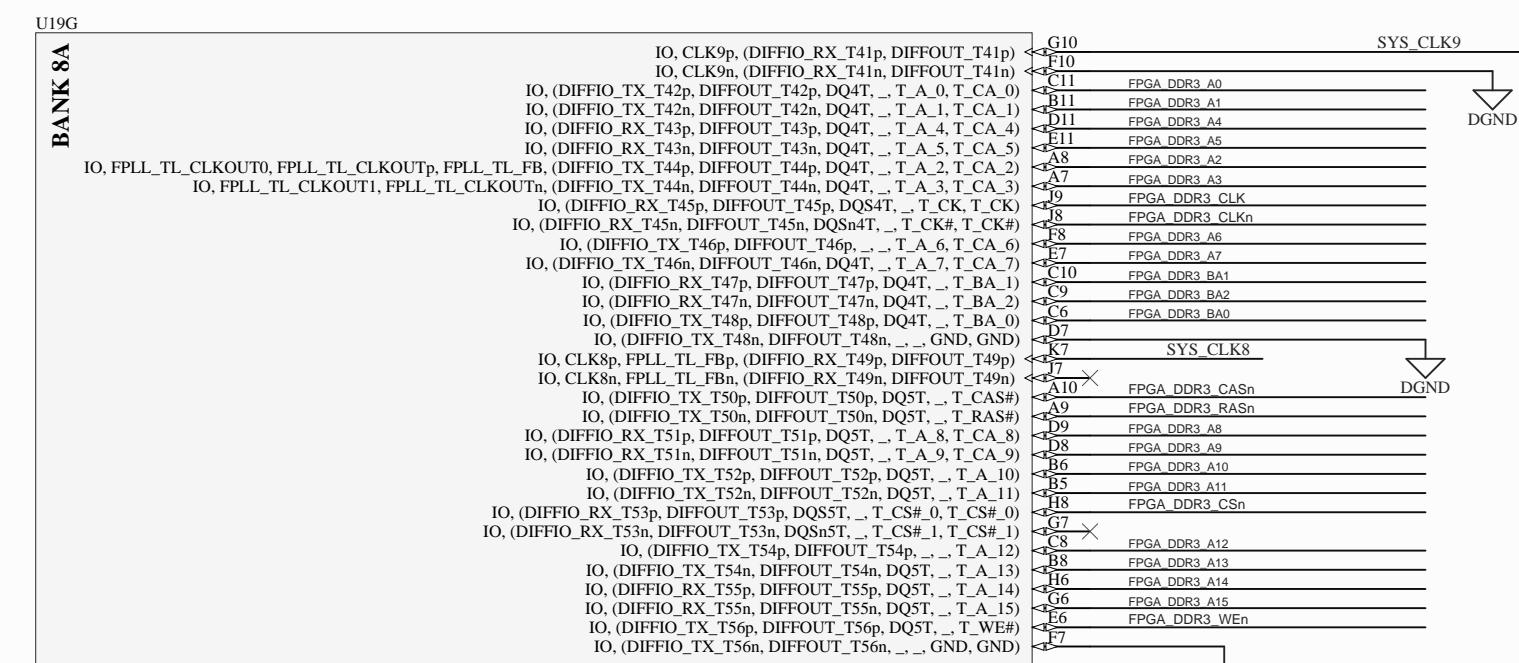
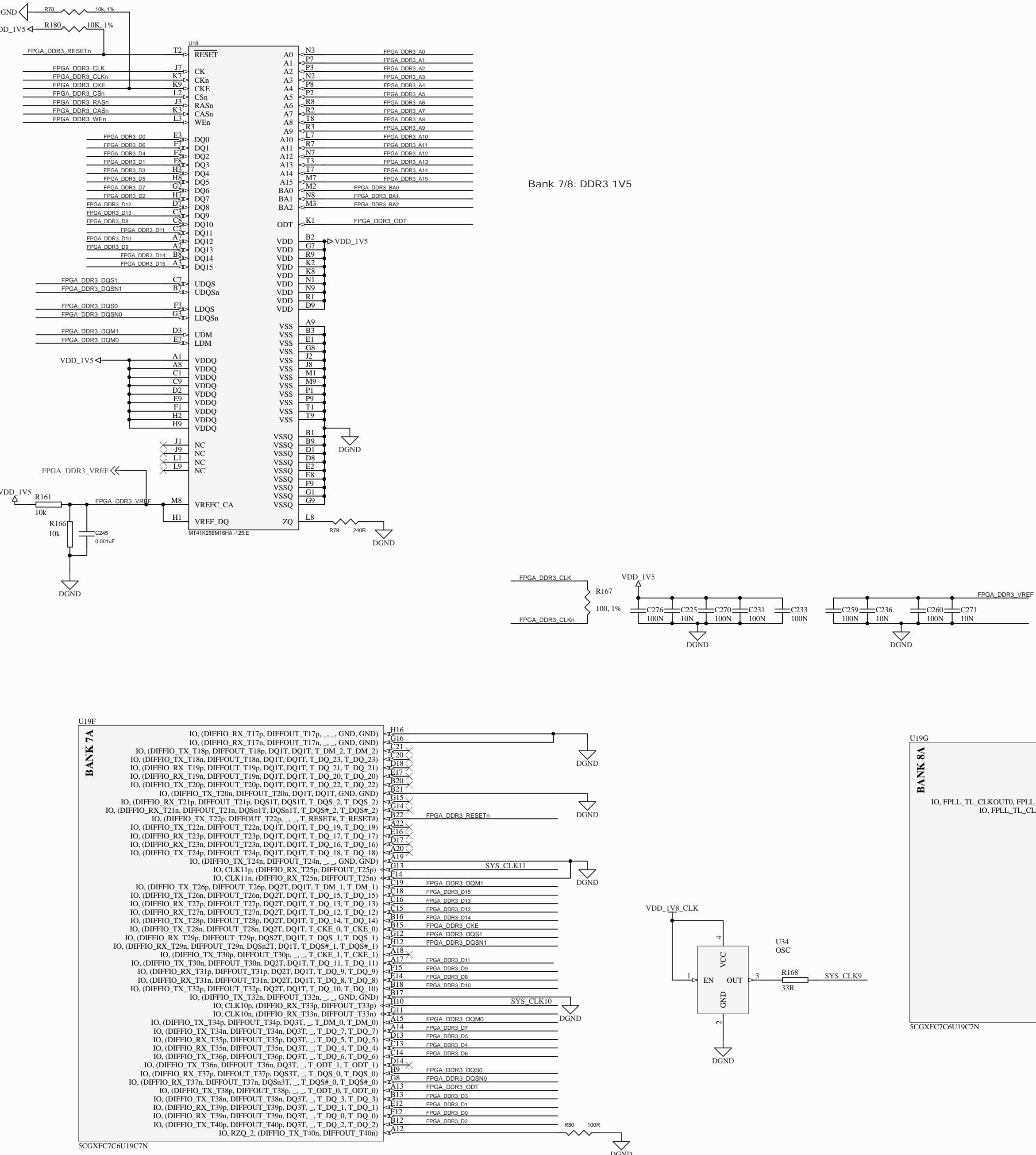
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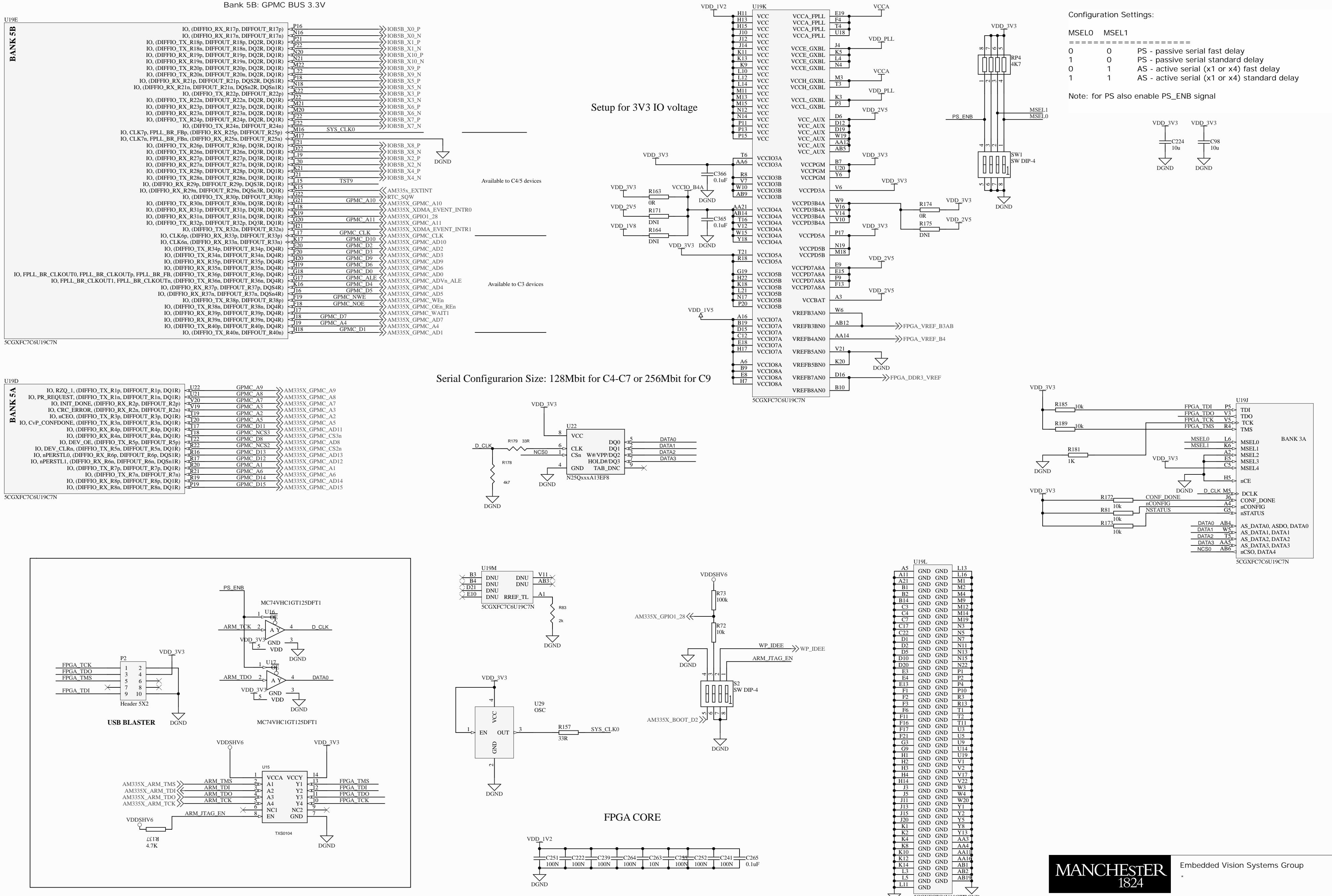
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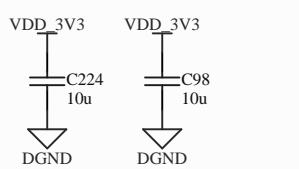


### Configuration Settings:

MSEI 0 MSEI 1

```
=====
0      0      PS - passive serial fast delay
1      0      PS - passive serial standard delay
0      1      AS - active serial (x1 or x4) fast delay
1      1      AS - active serial (x1 or x4) standard delay
```

Note: for PS also enable PS\_ENB signal



## Setup for 3V3 IO voltage

Bank 5B: GPMC BUS 3.3V

**BANK 5B**

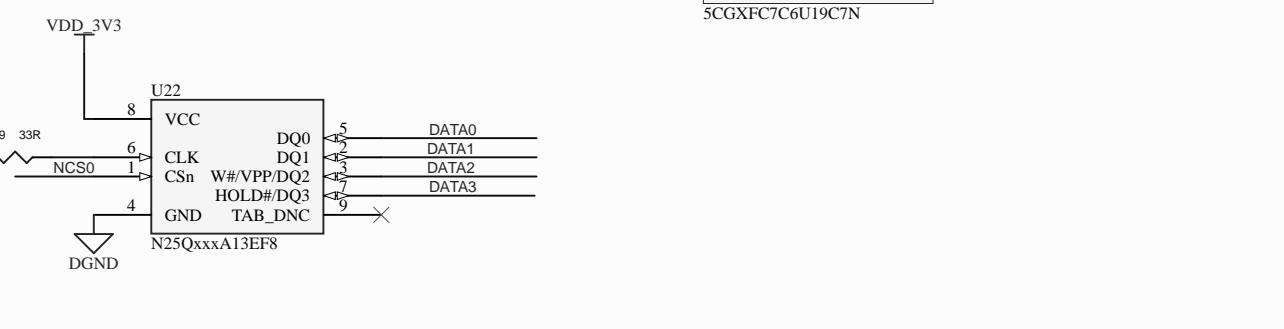
IO, (DIFFIO_RX_R17p, DIFFOUT_R17p)	P16	IOB5B_X0_P
IO, (DIFFIO_RX_R17n, DIFFOUT_R17n)	N16	IOB5B_X0_N
IO, (DIFFIO_TX_R18p, DIFFOUT_R18p, DQ2R, DQ1R)	P21	IOB5B_X1_P
IO, (DIFFIO_RX_R18n, DIFFOUT_R18n, DQ2R, DQ1R)	P22	IOB5B_X1_N
IO, (DIFFIO_RX_R19p, DIFFOUT_R19p, DQ2R, DQ1R)	N20	IOB5B_X10_P
IO, (DIFFIO_RX_R19n, DIFFOUT_R19n, DQ2R, DQ1R)	N21	IOB5B_X10_N
IO, (DIFFIO_TX_R20p, DIFFOUT_R20p, DQ2R, DQ1R)	M22	IOB5B_X9_P
IO, (DIFFIO_RX_R20n, DIFFOUT_R20n, DQ2R, DQ1R)	J22	IOB5B_X9_N
IO, (DIFFIO_RX_R21p, DIFFOUT_R21p, DQS2R, DQS1R)	P18	IOB5B_X5_P
IO, (DIFFIO_RX_R21n, DIFFOUT_R21n, DQSn2R, DQSn1R)	N18	IOB5B_X5_N
IO, (DIFFIO_RX_R22p, DIFFOUT_R22p)	K22	IOB5B_X3_P
IO, (DIFFIO_RX_R22n, DIFFOUT_R22n, DQ2R, DQ1R)	J22	IOB5B_X3_N
IO, (DIFFIO_RX_R23p, DIFFOUT_R23p, DQ2R, DQ1R)	M21	IOB5B_X6_P
IO, (DIFFIO_RX_R23n, DIFFOUT_R23n, DQ2R, DQ1R)	M20	IOB5B_X6_N
IO, (DIFFIO_RX_R24p, DIFFOUT_R24p, DQ2R, DQ1R)	F22	IOB5B_X7_P
IO, (DIFFIO_RX_R24n, DIFFOUT_R24n)	E22	IOB5B_X7_N
IO, CLK7p, FPLL_BR_FBP, (DIFFIO_RX_R25p, DIFFOUT_R25p)	M16	SYS_CLK0
IO, CLK7n, FPLL_BR_FBN, (DIFFIO_RX_R25n, DIFFOUT_R25n)	M17	
IO, (DIFFIO_RX_R26p, DIFFOUT_R26p, DQ3R, DQ1R)	E21	
IO, (DIFFIO_RX_R26n, DIFFOUT_R26n, DQ3R, DQ1R)	D22	IOB5B_X8_P
IO, (DIFFIO_RX_R27p, DIFFOUT_R27p, DQ3R, DQ1R)	J19	IOB5B_X8_N
IO, (DIFFIO_RX_R27n, DIFFOUT_R27n, DQ3R, DQ1R)	L20	IOB5B_X2_N
IO, (DIFFIO_RX_R28p, DIFFOUT_R28p, DQ3R, DQ1R)	K21	IOB5B_X4_P
IO, (DIFFIO_RX_R28n, DIFFOUT_R28n, DQ3R, DQ1R)	J21	IOB5B_X4_N
IO, (DIFFIO_RX_R29p, DIFFOUT_R29p, DQS3R, DQ1R)	J15	TST9
IO, (DIFFIO_RX_R29n, DIFFOUT_R29n, DQSn3R, DQ1R)	K15	
IO, (DIFFIO_RX_R30p, DIFFOUT_R30p)	G22	AM335x_EXTINT
IO, (DIFFIO_RX_R30n, DIFFOUT_R30n, DQ3R, DQ1R)	G21	RTC_SQW
IO, (DIFFIO_RX_R31p, DIFFOUT_R31p, DQ3R, DQ1R)	L18	AM335X_GPMC_A10
IO, (DIFFIO_RX_R31n, DIFFOUT_R31n, DQ3R, DQ1R)	K19	AM335X_XDMA_EVENT_INTR0
IO, (DIFFIO_RX_R32p, DIFFOUT_R32p, DQ3R, DQ1R)	G20	AM335X_GPIO1_28
IO, (DIFFIO_RX_R32n, DIFFOUT_R32n)	H21	AM335X_GPMC_A11
IO, CLK6p, (DIFFIO_RX_R33p, DIFFOUT_R33p)	J17	AM335X_XDMA_EVENT_INTR1
IO, CLK6n, (DIFFIO_RX_R33n, DIFFOUT_R33n)	K17	AM335X_GPMC_CLK
IO, (DIFFIO_RX_R34p, DIFFOUT_R34p, DQ4R)	E20	AM335X_GPMC_AD10
IO, (DIFFIO_RX_R34n, DIFFOUT_R34n, DQ4R)	F20	AM335X_GPMC_D2
IO, (DIFFIO_RX_R35p, DIFFOUT_R35p, DQ4R)	H20	AM335X_GPMC_D3
IO, (DIFFIO_RX_R35n, DIFFOUT_R35n, DQ4R)	H19	AM335X_GPMC_D9
IO, (DIFFIO_RX_R37p, DIFFOUT_R37p, DQS4R)	G18	AM335X_GPMC_D6
IO, (DIFFIO_RX_R37n, DIFFOUT_R37n, DQSn4R)	G17	AM335X_GPMC_D0
IO, (DIFFIO_RX_R38p, DIFFOUT_R38p)	K16	AM335X_GPMC_D4
IO, (DIFFIO_RX_R38n, DIFFOUT_R38n, DQ4R)	J16	AM335X_GPMC_D5
IO, (DIFFIO_RX_R39p, DIFFOUT_R39p, DQ4R)	E19	AM335X_GPMC_NWE
IO, (DIFFIO_RX_R39n, DIFFOUT_R39n, DQ4R)	F18	AM335X_GPMC_NOE
IO, (DIFFIO_RX_R40p, DIFFOUT_R40p, DQ4R)	J17	AM335X_GPMC_OEn_Ren
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	I18	AM335X_GPMC_WAIT1
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	J19	AM335X_GPMC_D7
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	H18	AM335X_GPMC_A4
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	G18	AM335X_GPMC_D1
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	H18	AM335X_GPMC_A1

5CGXFC7C6U19C7N

BANK 5A		U22	GPMC_A9	AM335X_GPMC_A9
IO, RZQ_1, (DIFFIO_TX_R1p, DIFFOUT_R1p, DQ1R)		U21	GPMC_A8	AM335X_GPMC_A8
IO, PR_REQUEST, (DIFFIO_TX_R1n, DIFFOUT_R1n, DQ1R)		V20	GPMC_A7	AM335X_GPMC_A7
IO, INIT_DONE, (DIFFIO_RX_R2p, DIFFOUT_R2p)		V19	GPMC_A3	AM335X_GPMC_A3
IO, CRC_ERROR, (DIFFIO_RX_R2n, DIFFOUT_R2n)		T19	GPMC_A2	AM335X_GPMC_A2
IO, nCEO, (DIFFIO_TX_R3p, DIFFOUT_R3p, DQ1R)		T20	GPMC_A5	AM335X_GPMC_A5
IO, CvP_CONF DONE, (DIFFIO_TX_R3n, DIFFOUT_R3n, DQ1R)		T17	GPMC_D11	AM335X_GPMC_AD11
IO, (DIFFIO_RX_R4p, DIFFOUT_R4p, DQ1R)		T18	GPMC_NCS3	AM335X_GPMC_CS3n
IO, (DIFFIO_RX_R4n, DIFFOUT_R4n, DQ1R)		T22	GPMC_D8	AM335X_GPMC_AD8
IO, DEV_OE, (DIFFIO_TX_R5p, DIFFOUT_R5p)		R22	GPMC_NCS2	AM335X_GPMC_CS2n
IO, DEV_CLRn, (DIFFIO_TX_R5n, DIFFOUT_R5n, DQ1R)		R16	GPMC_D13	AM335X_GPMC_AD13
IO, nPERSTL0, (DIFFIO_RX_R6p, DIFFOUT_R6p, DQS1R)		R17	GPMC_D12	AM335X_GPMC_AD12
IO, nPERSTL1, (DIFFIO_RX_R6n, DIFFOUT_R6n, DQS1R)		R20	GPMC_A1	AM335X_GPMC_A1
IO, (DIFFIO_RX_R7p, DIFFOUT_R7p, DQ1R)		R21	GPMC_A6	AM335X_GPMC_A6
IO, (DIFFIO_TX_R7n, DIFFOUT_R7n)		R19	GPMC_D14	AM335X_GPMC_AD14
IO, (DIFFIO_RX_R8p, DIFFOUT_R8p, DQ1R)		P19	GPMC_D15	AM335X_GPMC_AD15
IO, (DIFFIO_RX_R8n, DIFFOUT_R8n, DQ1R)				

**5CGXFC7C6U19C7N**

Serial Configuration Size: 128Mbit for C4-C7 or 256Mbit for C9



PS\_ENB

MC74VHC1GT125DFT1

FPGA\_TCK  
FPGA\_TDO  
FPGA\_TMS  
FPGA\_TDI

P2

Header 5X2

VDD\_3V3

DGND

USB BLASTER

MC74VHC1GT125DFT1

ARM\_TCK  
ARM\_TDO  
VDD\_3V3  
GND  
VDD

DATA0

MC74VHC1GT125DFT1

VDDSHV6

AM335X\_ARM\_TMS  
AM335X\_ARM\_TDI  
AM335X\_ARM\_TDO  
AM335X\_ARM\_TCK

ARM\_TMS  
ARM\_TDI  
ARM\_TDO  
ARM\_TCK

ARM\_JTAG\_EN

VCCA  
VCCY  
A1  
A2  
A3  
A4  
NC1  
EN  
Y1  
Y2  
Y3  
Y4  
NC2  
GND

4.7K

R137

VDDSHV6

FPGA\_TMS  
FPGA\_TDI  
FPGA\_TDO  
FPGA\_TCK

TXS0104

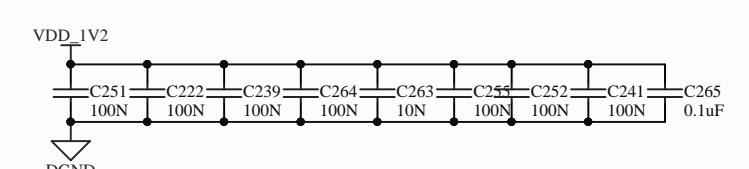
DGND

The diagram illustrates the connection between three main components: U19M, U29, and a DIP-4 switch S2.

- U19M:** A logic device with pins B3, B4, D21, E10, V11, AB3, A1, RREF\_TL, and 5CGXFC7C6U19C7N. Pin A1 is connected to a 2kΩ resistor (R83) which connects to DGND. Pin AB3 is connected to V11.
- U29:** An oscillator component with pins VCC, EN, OUT, and GND. Pin OUT is connected to pin 3 of R157. Pin 1 is connected to VDD\_3V3. Pin 2 is connected to DGND.
- S2:** A DIP-4 switch component with pins 1 through 8. Pin 1 is connected to DGND. Pin 2 is connected to AM335X\_BOOT\_D2. Pin 3 is connected to R72 (10kΩ). Pin 4 is connected to AM335X\_GPIO1\_28. Pin 5 is connected to VDDSHV6. Pin 6 is connected to R73 (100kΩ). Pin 7 is connected to DGND. Pin 8 is connected to WP\_IDEE and ARM\_JTAG\_EN.

U19L	
A5	GND GND
A11	GND GND
A21	GND GND
B1	GND GND
B2	GND GND
B14	GND GND
C3	GND GND
C4	GND GND
C7	GND GND
C17	GND GND
C22	GND GND
D1	GND GND
D2	GND GND
D5	GND GND
D10	GND GND
D20	GND GND
E3	GND GND
E4	GND GND
E13	GND GND
F1	GND GND
F2	GND GND
F3	GND GND
F6	GND GND
F11	GND GND
F16	GND GND
F17	GND GND
F21	GND GND
G3	GND GND
G9	GND GND
H1	GND GND
H2	GND GND
H3	GND GND
H4	GND GND
H14	GND GND
J3	GND GND
J5	GND GND
J11	GND GND
J13	GND GND
J15	GND GND
J20	GND GND
K1	GND GND
K2	GND GND
K4	GND GND
K8	GND GND
K10	GND GND
K12	GND GND
K14	GND GND
L3	GND GND
L5	GND GND
L11	GND GND
L13	L16 M1 M2 M4 M9 M12 M14 M19 N3 N5 N7 N11 N13 N15 N22 P1 P2 P4 P10 R3 R13 T1 T2 T11 U3 U5 U9 U14 U19 V1 V2 V17 V22 W3 W4 W20 Y1 Y2 Y5 Y8 Y13 AA3 AA4 AA11 AA16 AB1 AB2 AB19

EBC A CORE



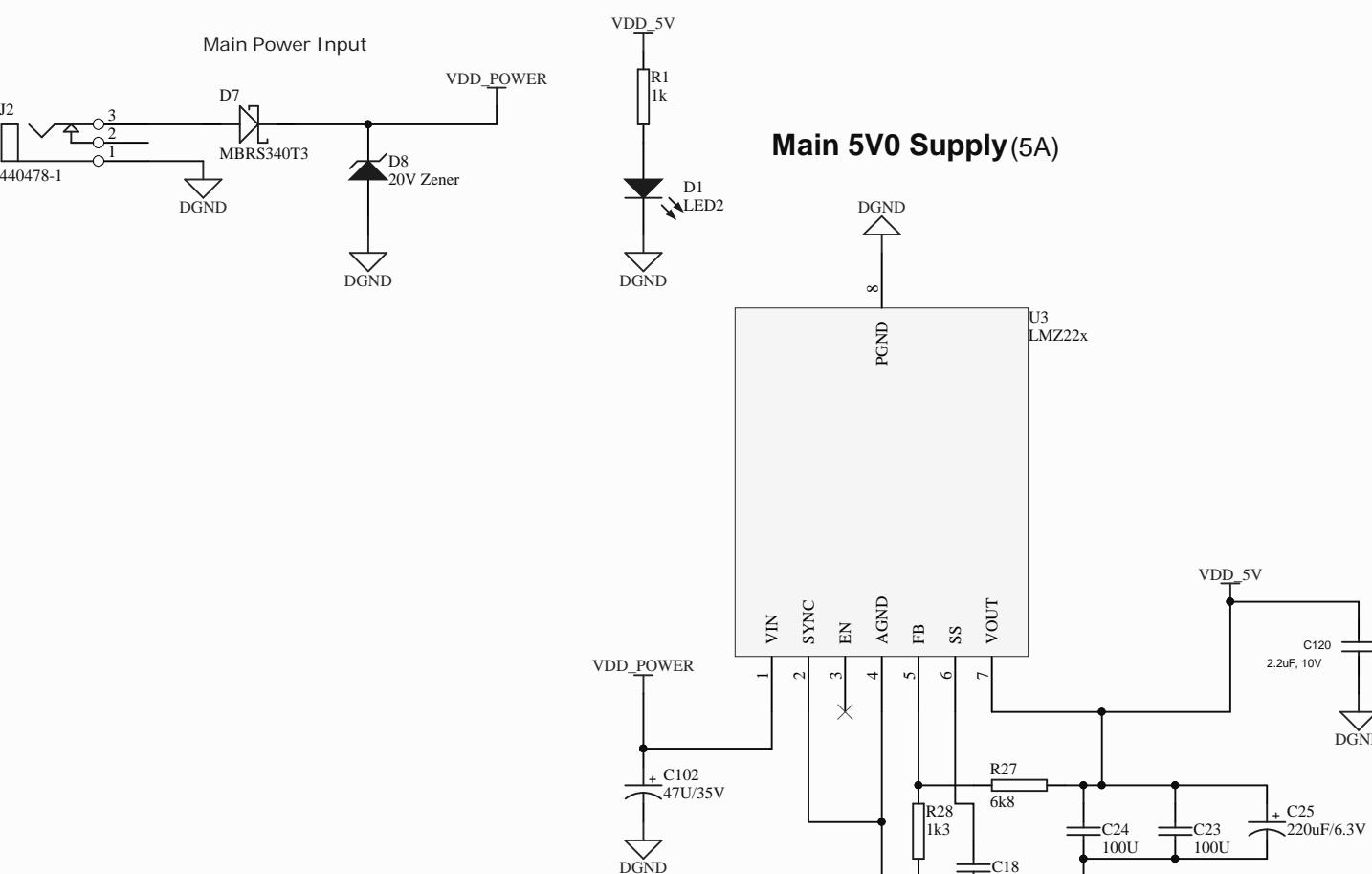
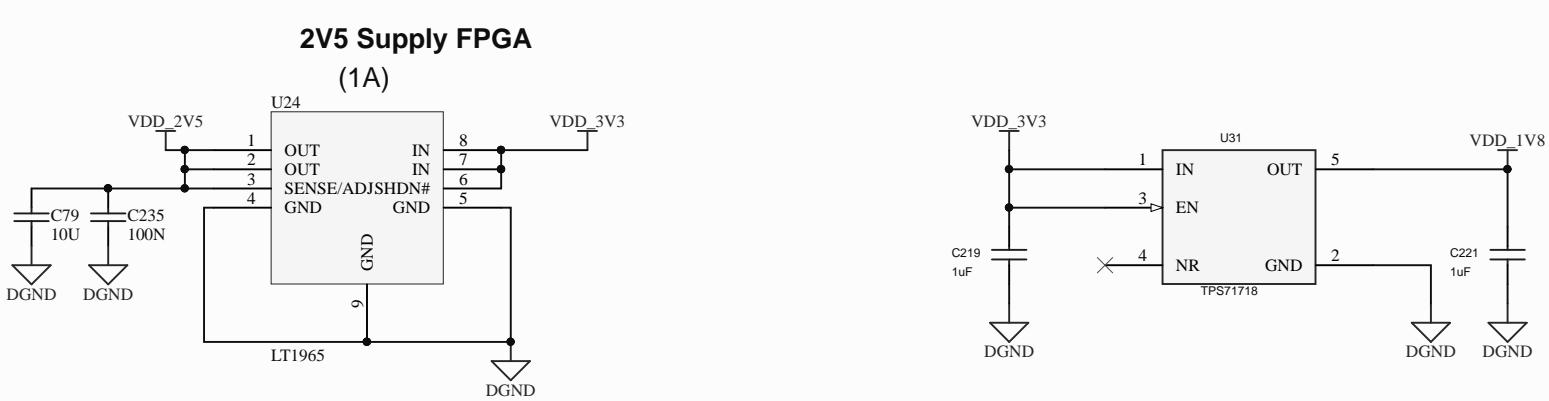
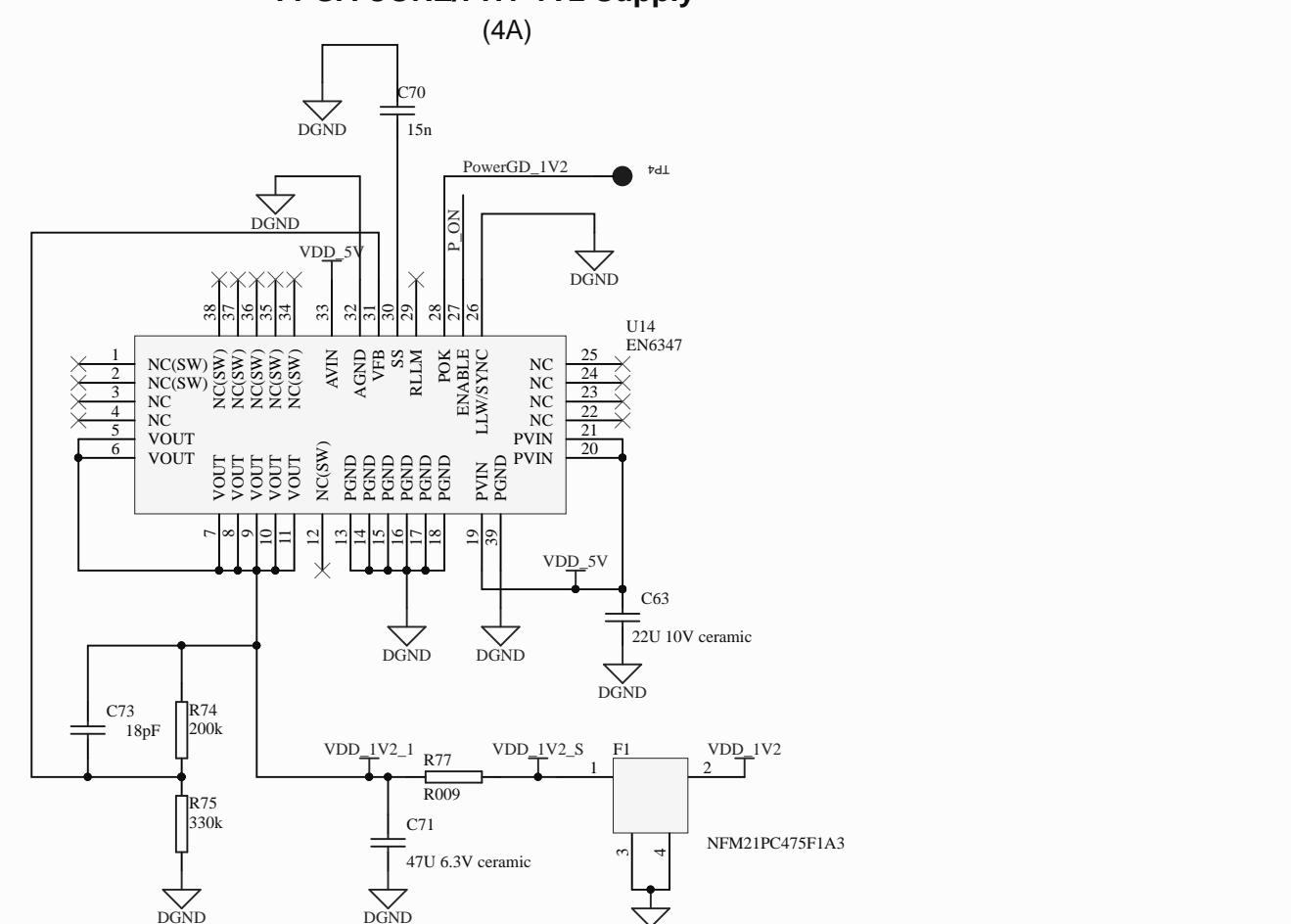
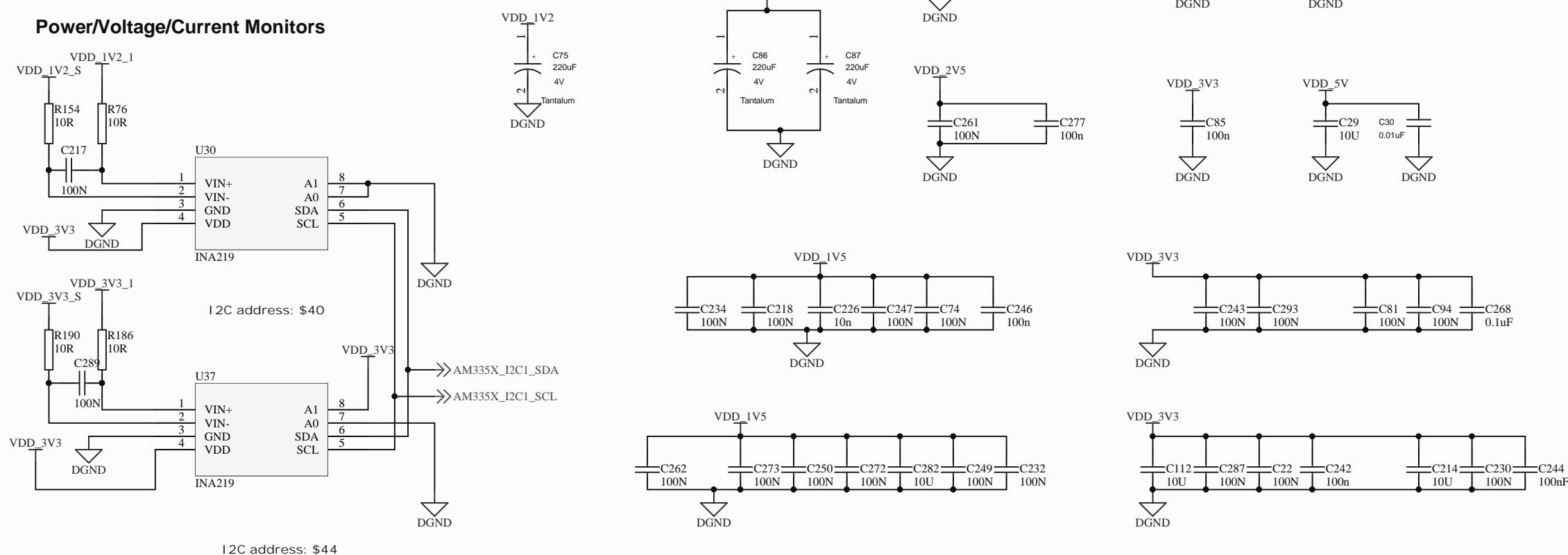
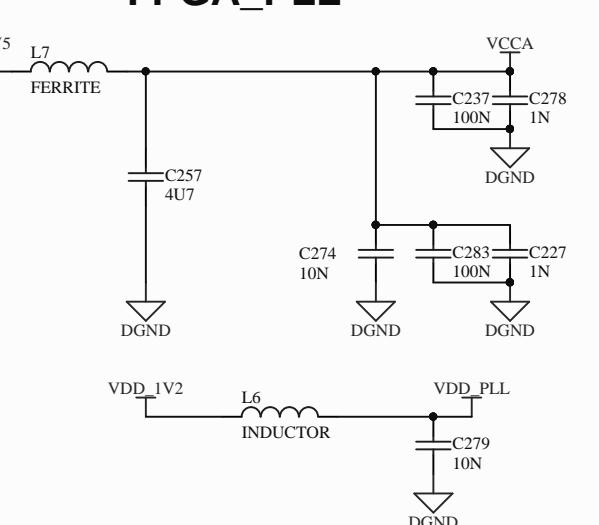
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