11161SM.

COMP 5 – 4 (RC)

T.E. (COMP) (Semester – V) (RC) Examination, May/June 2015
COMPUTER HARDWARE DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any 5** questions, at least **one** question from **each** Module.*
*2) **Assume** suitable **data** necessary.*

MODULE – I

1. a) Explain the difference between structure and behaviour in the digital system context. Illustrate your answer by giving : **6**
   i) A purely structural description
   ii) A purely behaviour description.
   b) Explain the following : **6**
   i) Single address instruction format of RIC
   ii) Shift /Rotate instruction format of RIC.
   c) Construct the logic block diagram of hardware associated with the register AR providing for the accomplishment of either of the transfers : **8**

   $AR \leftarrow \overline{AR}$

   $AR \leftarrow BR$

   Given the proper control signals. Both AR and BR are 4 bit registers.

2. a) Bringout the differences between direct access storage and sequential access storage in terms of hardware designs. **6**
   b) Briefly explain the two address instruction supported by RIC. **6**
   c) Construct a detailed logic block diagram of the hardware realization of both the control and data units specified by the following AHPL description, where a and b are flipflops, x is an input and z is a single output line : **8**
   i) $a \leftarrow x \vee b$;
   ii) $b \leftarrow x$;

   $\rightarrow (a, \overline{a})/(1, 3)$

   iii) $z = 1; b \leftarrow x \oplus b$

   $\rightarrow (1)$.

P.T.O.

MODULE – II

3. a) Write combinational logic unit description for an n - bit ripple carry adder. **6**

   b) Write the sequence of AHPL steps to implement the fetch and address cycles of RIC. **8**

   c) Give flowchart for compiling of data network and briefly explain it. **6**

4. a) Draw the flowchart to implement the fetch sequence of 16 bit instruction. **6**

   b) Determine control unit target source list for the first 11 steps of RIC. **6**

   c) Give the implementation of HLT using DEAD END. Also explain the implementation of HLT by return to step 1. Support your answer with neat diagram. **8**

MODULE – III

5. a) Explain hardwired control unit and microprogrammed control unit with neat block diagrams. **8**

   b) Draw neat block diagram of 64 bit section carry look ahead adder and explain how it speeds up the addition process. **6**

   c) Write the sequence of AHPL steps to implement division of fixed point quantities. **6**

6. a) With neat block diagram explain organization of microprogrammable RIC. **8**

   b) Explain with a neat diagram the hardware organization of floating point coprocessor. **6**

   c) Explain signed multiplication with help of flowchart. **6**

MODULE – IV

7. a) Explain the working of nMOS depletion mode transistor with neat diagram. **6**

   b) Explain the n-well process to CMOS fabrication with neat diagrams. **8**

   c) List the advantages of CMOS inverter and explain its working with necessary equations and diagrams. **6**

8. a) Design CMOS logic gates for the following functions : **8**

      i) $z = \overline{(A \cdot B) + (C \cdot D)}$

      ii) 3 input OR gate.

   b) Obtain current voltage characteristics for various bias condition of a MOSFET channel. **8**

   c) Explain working of a pass transistor. **4**