S.E. (Comp.) (Semester – III) (Revised 2007-08) Examination, May 2009
INTEGRATED ELECTRONICS

Duration : 3 Hours Total Marks : 100

*Instructions : 1) Attempt **any five** choosing at least **one** from **each** module.*
*2) Assume **any** data, **if necessary**.*

MODULE – I

1. a) What are the characteristics of an ideal op-amp ? Explain how the characteristics of a practical op-amp differ from these. 6

   b) Draw the block schematic of an op-amp and briefly describe the operation of each block. 4

   c) Draw the circuit diagram of an op-amp in inverting amplifier configuration and derive the expression for its closed loop gain assuming an ideal op-amp. 6

   d) Write a note on the frequency response of an op-amp. 4

2. a) i) With neat circuit diagram of an instrumentation amplifier derive the expression for its output voltage. 6

   ii) What are the important features of the instrumentation amplifier ? 2

   iii) Discuss any application of this circuit. 2

   b) With a neat circuit diagram describe the operation of a non-inverting op-amp summer with three inputs. 6

   c) Draw the circuit diagram of a basic op-amp comparator circuit. Describe any two applications of this circuit. 4

MODULE – II

3. a) Define and explain the following with respect to a voltage regulator. 4

   i) Load regulation

   ii) Short circuit current limit.

   b) Draw the functional block diagram of voltage regulator IC 723 and its pin configuration. Describe the function of each block. 8

   c) Explain how current limiting is achieved in IC 723 with a neat circuit diagram. 8

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4. a) With the help of a block diagram explain the basic operation of a phase-locked loop. 8

b) Explain what is meant by : 4

i) Capture range and

ii) Lock range of a phase-locked loop.

c) With a neat circuit diagram and waveforms describe the working of an Astable multivibrator that uses the timer IC 555. 8

MODULE – III

5. a) A buffer is used to increase the output drive capability of logic circuit. A "RTL" buffer inverter is shown in fig. 5 (i)

i) Explain the operation of this circuit.

ii) Calculate the fan-out of the circuit assuming $h_{fe} = 30$ and the base current required for saturation for above RTL is about 300 μA. 10

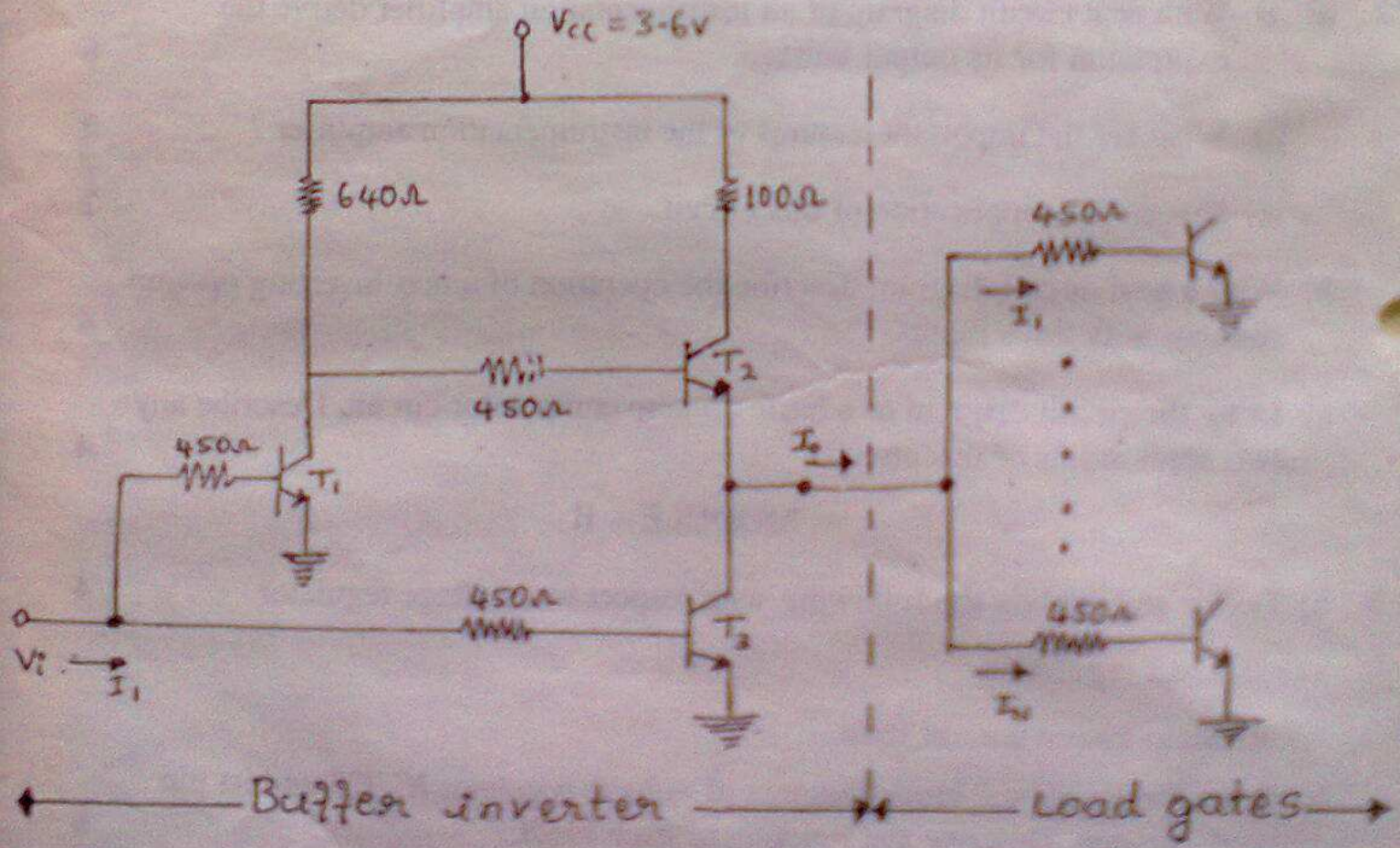

Fig. 5 (i)

b) Explain the following with respect to digital logic circuits.

i) Noise margin

ii) Propagation delay time

iii) Current source logic. 5

c) Explain why DCTL (Direct Coupled Transistor Logic) gate is not popular in IC technology, although it is simpler than RTL (Resistor Transistor Logic) ? 5

6. a) Draw a neat diagram of a 3 input Transistor-Transistor Logic (TTL) "Nand" gate. Explain it's operation. What are the modifications incorporated in the circuit diagram to increase the speed compared to Diode-transistor logic (DTL) circuit ? 10

b) Compare the current spikes in ECL(Emitter Coupled Logic) and TTL (Transistor Transistor Logic) gates. 4

c) Explain with a neat circuit diagram working of a CMOS NAND gate. List some characteristics of a CMOS circuit. 6

MODULE – IV

7. a) Explain the working of successive approximation A/D converter, with a neat diagram. 8

b) An 8-bit ADC output for all 1's is 5.1 volts. Determine it's

i) Resolution

ii) Digital output when the input is 1.28 volts. 4

c) A 5-bit flash comparator ADC has a reference voltage of 15V.

i) How many voltage comparators and resistors will be needed ?

ii) State major advantages and disadvantages of this converter.

iii) What is the increment between fixed voltage applied to the comparator ?

8. a) A 6-bit weighted register D/A converter has input voltage level given by $V_{HIGH} = 10V$ and $V_{LOW} = 0V$. The feedback resistor used is 16 kΩ and the resistor corresponding to LSB bit is 8kΩ.

   i) Calculate all other resistor.

   ii) Calculate output when input is 110111.

   iii) Calculate the gain when all the inputs are high.

   b) Draw the circuit diagram of 4bit R-2R Binary ladder D to A converter and explain how the signal is being converted from D to A. Give logic levels when logic 1 = 10V, logic 0 = 0V, $R_f = 10k\Omega$ and $R_2 = 20k\Omega$ when inputs are

   i) 1101

   ii) 1110

   c) Define the following terms :

   i) Monotonicity

   ii) Settling time

   iii) Linearity error.