COMP 3-5 (RC)

S.E. (Comp.) Sem. – III (RC) Examination, May 2010
LOGIC DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : 1) Answer 5 full questions at least one from each module.
2) Assume any necessary data.

MODULE – I

1. a) A safe has 5 locks V, W, X, Y and Z all of which must be unlocked for the safe to open. The keys to the locks are distributed among 5 executives in the following manner.

Mr. A has keys for locks V and X

Mr. B has keys for locks V and Y

Mr. C has keys for locks W and Y

Mr. D has keys for locks X and Z

Mr. E has keys for locks V and Z. 5

i) Determine the minimal number of executives required to open the safe.

ii) Find all the combinations of executives that can open the safe, write an expression f(A, B, C, D, E) which specifies when the safe can be opened as a function of what executives are present.

iii) Who is the essential executive ?

b) Perform the following : 8

i) $(11.75)_{10}$ to Binary ii) $(8BF4)_{16}$ to octal

iii) $(6327.4051)_8$ to decimal iv) $(675.625)_{10}$ to hexadecimal.

c) Show that Dual of EX-OR is same as its complement. 4

d) Prove the following using Boolean Algebra

$A + \overline{AB} + A\overline{B} = A + B$. 3

P.T.O.

2. a) For the following function find the essential prime implicants and prime implicants using QM method $f(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$.

   Realize the logic circuit using NAND gates only. 8

   b) Represent the decimal number. $(358)_{10}$ in binary form using.

   i) Excess - 3 code ii) Gray code

   iii) Straight binary code iv) Octal code. 4

   c) Perform the following using 2's complement method

   i) 48 – 23 ii) 48 – (– 23)

   iii) – 48 – 23 iv) 23 – 48 8

MODULE – II

3. a) What is a T flipflop ? Explain with the help of a truth table and convert T flipflop to D flipflop. What is 'T' in a T flipflop ? 6

   b) What do you mean by master slave JK flipflop ? Explain why master slave flipflop is called a pulse triggered flipflop. 7

   c) Differentiate between combinational circuit and sequential circuit. Explain working of half subtract or using suitable diagram and truth table. 7

4. a) Design a 2 bit comparator. List all possible combinations and comparison support for your answer with a logic circuit. 5

   b) Design a combination circuit that operates as follows when the control signal enable = 1 m EX-OR gates shall be connected to implement a binary to gray code conversion. For enable = 0 the same EX-OR gates shall execute a gray code to binary conversion. 6

   c) What is the difference between a excitation table and truth table of a flipflop ? Give examples. 5

   d) Implement the following function using a multiplexer

   $F(W, X, Y, Z) = \Sigma m(1, 2, 6, 7, 9, 11, 12, 14, 15)$. 4

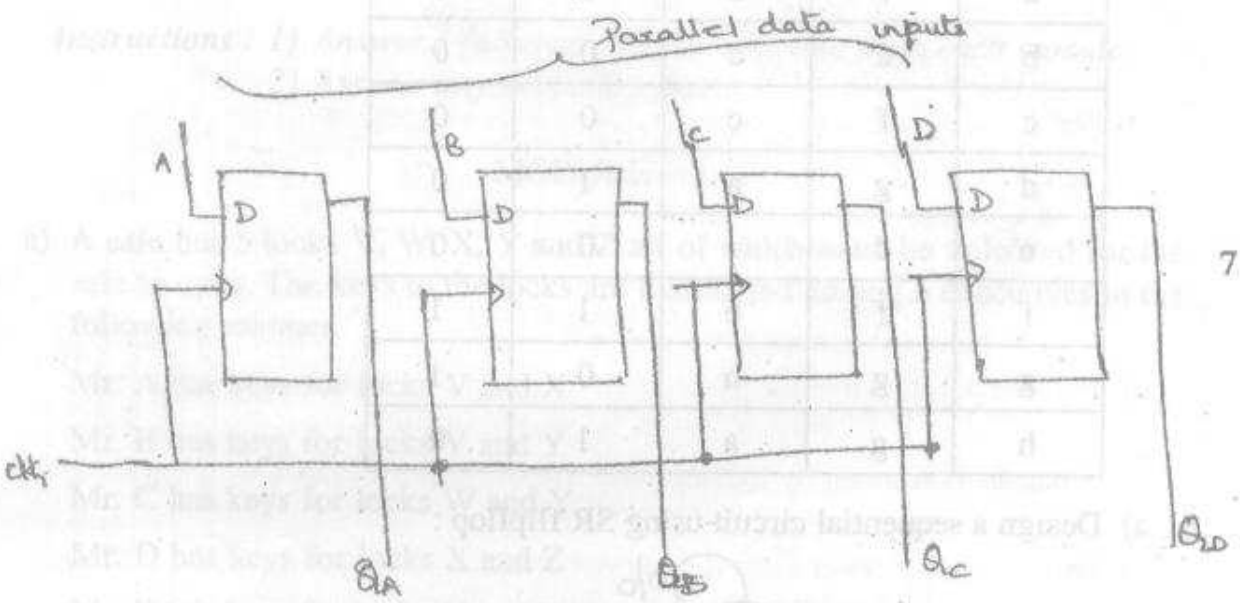
MODULE – III

5. a) What is a Random counter ? Explain the working of 5 bit twisted ring counter with the help of diagrams. 6

   b) Design a 3 bit binary counter which counts according to the gray code use T flipflops. Explain its working. 8

c) The binary number 1101 is serially entered (right most bit first) into a 4 bit parallel out shift register that is initially clear. What are the Q outputs after 2 clock pulses ? 6

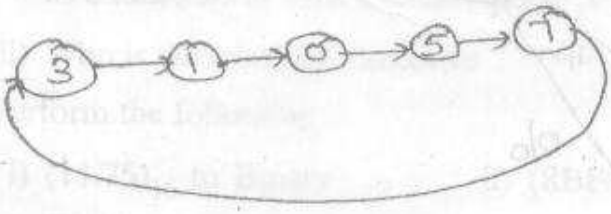
6. a)



7

In figure A = 1, B = 0, C = 0 and D = 1. After 3 clock pulses what are the data outputs.

b) Design a synchronous counter using SR flipflops that goes through the following states. 8



c) State the relative advantages and disadvantages of Asynchronous counters over synchronous counter. 5

MODULE – IV

7. a) Explain the terms state table, state reduction and state assignment with the help of examples. 5

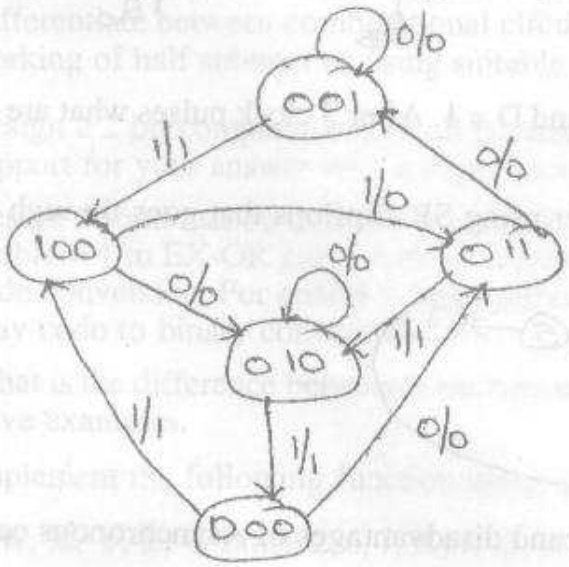
b) Explain the following :

i) Registered PAL's ii) Configurable PAL's. 5

c) For the following state table design a sequential circuit using T flipflops after possible reduction. 10

Present State	Next State		O/P	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	c	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

8. a) Design a sequential circuit using SR flipflop : 8



b) A combinational circuit is defined by the functions
$F_1(A, B, C) = \Sigma(3, 5, 6, 7), F_2(A, B, C) = \Sigma(0, 2, 4, 7)$
Implement the circuit with a PLA having 3 inputs, 4 product terms and 2 outputs. 7

c) List and explain features of

i) 82S200 PLA ii) 82S100 FPLA. 5