SEM- V (E) Regular 5/12/13
Comp Dept.

COMP 5 – 3 (RC)

T.E. (Comp.) (Semester – V) (RC) Examination, Nov./Dec. 2013
MICROPROCESSORS AND MICROCONTROLLERS

Duration : 3 Hours | Total Marks : 100

Instructions : 1) *Answer* ***any five*** *questions by selecting atleast* ***one*** *from* ***each*** *Module.*
2) *Assume appropriate data* ***wherever*** *necessary.*

MODULE – I

1. a) Contents of registers and memory location of 8086 system at a given time are given below :

DS = C000H	AX = 0001H	C0002H = F9H
DI = 0002H	SS = F000H	C0003H = FFH
BX = 0002H	SP = 0010H	

Give contents of affected registers and memory location after execution of each instruction.
i) MOV [DI], BX
ii) MUL BYTEPTR [BX]
iii) ROR BL, 02
iv) PUSH BX. 8

b) Write 8086 ALP to find transpose of matrix. Add proper comments to explain your logic. 6

c) Explain use of the following instruction in 8086, give example for each
i) CMPSB
ii) JNAE
iii) SAR
iv) IDIV. 6

2. a) Can we write the following instructions for 8086. Also state the reason for validity and invalidity : 5
i) Mov CX, AL
ii) Mov Ds, 003AH
iii) Mov BL, [BX]
iv) Mov 434 [SI], DH
v) Mov CS : [BX], DL.

P.T.O.

b) Draw and explain how even and odd addressed words are accessed from memory banks of 8086. 7

c) Write notes on :

i) Procedures

ii) Macros. 8

MODULE – II

3. a) Discuss bit definitions of control and status word of 8087. 8

b) Show each operation with neat diagram :

i) Which 8087 stack register is ST after reset ?

ii) Which 8087 stack register will be ST after one data item is read into 8087 ?

iii) Describe operation that will be done by 8087 FADD ST(2), ST(3) Instruction

iv) How does operation of instruction FADDP ST (2), ST (3) differ from operation of instruction is point (iii) ? 6

c) Write 8087 program to prove the following identity $\sin^2\theta + \cos^2\theta = 1$. Add proper comments to explain the logic. 6

4. a) Explain importance of I/o processor 8089. Support your answer with diagrams. 6

b) With neat diagram explain the coprocessor configuration of 8086. Also state importance of coprocessor. 9

c) Briefly discuss conditions that cause 8086 to perform each of the following types of interrupts Type 0, Type 1, Type 2, Type 3, Type 4. 5

MODULE – III

5. a) With the help of a neat diagram explain synchronous and asynchronous serial transmission with the help of USART. 8

b) Give features of mode 0, mode 1 and mode 2 operation of 8255. 6

c) Draw neat diagram of 8254 timer and explain control word register. 6

6. a) Consider part addresses as follows

Part A = 8000 Part B = 8001 Part C = 8002

Control register = 8003H.

i) Identify mode 0 control word to configure Part A and Part C_L as output Part and Part B and Part C_u as input Part. 2

ii) Write a program to read and display the reading from Part B at Part A and from Part C_L to Part C_u. 4

b) Draw and explain block diagram of 8251. 8

c) Explain two methods of interfacing I/o devices. 6

MODULE – IV

7. a) Interface two 8k* 8 ROM and two 8k* 8 RAM chips with 8086. Select suitable map. 6

b) Draw and explain internal architecture of 80286. 8

c) Explain addressing modes supported by 8051 with example. 6

8. a) With neat figure show how external memory is interfaced with microcontroller. Also explain the importance of $\overline{EA}$ and $\overline{PSEN}$ pins of 8051. 8

b) Define interrupt. List the steps 8051 takes when it is interrupted. 5

c) Describe with figures how 80286 generates physical address when dealing in real and protected mode of operation. 7