COMP– 5-4 (RC)

T.E. (Comp.) (Semester – V) (Revised 2007-08) Examination Nov./Dec. 2009
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

Instructions: *i) Answer **five** full questions, atleast **one full** question from **each** Module.*
*ii) Make suitable assumptions **wherever** necessary.*

MODULE – I

1. a) Explain the difference between structure and behaviour in the digital system context. Illustrate your answer by giving.
   i) a purely structural description.
   ii) a purly behavioral description. **6**

   b) Explain the single address and branch instruction format of RIC. **6**

   c) Construct the logic block diagram of hardware associated with the register AR providing for the accomplishment of either of the transfers.
   $AR \leftarrow \overline{AR}$
   $AR \leftarrow BR$
   given the proper control signal. Both AR and BR are 4 bit registers. **8**

2. a) Suppose that the transfer AR ← AR [2], AR [0:1] is to be accomplished if the control signal CSLI is 1 and AR ← AR [1 : 2], AR [0] is to be accomplished if CSL2 = 1. Construct a logic block diagram of the input network for the register AR that will provide for both these transfers. **8**

   b) Enumerate and describe in brief any four of the basic building blocks used in hardware circuits. **8**

   c) Briefly explain the single address instructions supported by RIC. **4**

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MODULE – II

3. a) Write a combinational logic unit description for a decrementer. When used in a module description the decrementer will be declared DEC [I]. 8

b) Write the AHPL sequence for fetching of 16 bit instructions. 8

c) Given that u = (1, 1, 1, 0) ; V = (1, 0, 0, 1); W = (1, 0, 1).

$$N = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}; x = 5; a = 1.$$

Compute

i) $u \oplus v$ ii) $u \wedge x$

iii) $u \wedge W$ iv) $N \wedge a$

4. a) With the help of a neat flowchart explain the steps involved in the compilation of data network. 4

b) Consider a digital computer with a 32 bit word length and the same registers and bus organisation as in RIC (PC, AC, IX and SP on the BBUS). The set of 32 bit addressed instructions are slightly different. After control has branched away for execution of some addressed instructions (listed in the figure as "don't cares"), the instructions depicted in the below figure, that use AC are to be executed in a single step. The meaning of each mnemonic is the same as in RIC except for MATCH which is the same as XOR except that it has no effect on AC. 8

IR [2 : 3] \ IR [0 : 1]	00	01	11	10
00	SBC	ADC	X	AND
01	SUB	ADD	X	BIT
11	CMP	X	X	XOR
10	X	MVT	X	MATCH

i) Write the AHPL expression for connections to the ABUS in the step that executes the instructions in above figure.

ii) Write an AHPL expression for Cin (Carry-in to the adder) for this execution step.

iii) Write an AHPL expression for connections to the OBUS for this execution step.

iv) Write an AHPL expression for the transfer statement into zff (zero flag) in this execution step.

v) Write an AHPL expression for the transfer statement into vff (Overflow flag) in this execution step. **12**

MODULE – III

5. a) With a neat block diagram explain the organization of microprogrammable RIC. **6**

b) Explain with block diagrams the carry look ahead principle and describe how the full adder unit can be used to build the carry look ahead unit. **8**

c) Explain the hardware organisation of floating point coprocessor. **6**

6. a) Write an AHPL description of the RIC microsequencer and explain. **8**

b) Write the sequence of AHPL steps to implement signed multiplication. **8**

c) Write combinational logic unit description for the propogate and generate section of the full adder circuit. **4**

MODULE – IV

7. a) Explain the structure and energy band diagram of the components that make up the MOS system. 8

b) An enhancement type NMOS transistor with $V_t = 2V$ has its source terminal grounded and a 3v DC source connected to the gate. In what region of operation does the device operate for

i) $V_{dd} = +0.5v$ ii) $V_{dd} = IV$ iii) $V_{dd} = 5V$

If the NMOS device has μ_n Cox = 20 μA/V, w = 100 μm and L = 10 μm. Find the value of the drain current that results in each of the 3 cases. Neglect dependence of I_d on V_{ds} in saturation. 8

c) What is the role of SiO_2 in IC fabrication ? 4

8. a) Design CMOS logic gates for the following functions : 8

i) $z = \overline{A.B.C.D}$

ii) $z = \overline{(A.B) + C \bullet (A + B)}$

b) Explain the working of a MOS Inverter with nMOS depletion type transistor as load. Draw the transfer characteristics. 8

c) What are masks ? How are they used ? 4