[Total No. of Questions : 8]

T.E. (Comp) (Semester - V) Examination, May 2011
COMPUTER HARDWARE DESIGN

Duration : 3 Hours **Total Marks : 100**

Instructions : 1) Answer any 5 questions, at least one question from each module.
2) Assume suitable data necessary.

MODULE - I

Q1) a) Differentiate clearly between 'structure' and 'behaviour' of a digital system. Give description examples to illustrate the difference. **[5]**

b) Describe the internal architecture of the RIC system and explain the single address instruction format. **[7]**

c) Write a RIC assembly language routine to compare two 32-word arrays A and B and find it they are identical or not. **[8]**

Q2) a) Determine the minimal expression for DAR [i] where AR is the destination for the fell transfers. **[8]**

$AR \leftarrow 0, 0, 0, 0$
$AR \leftarrow \overline{AR}$
$AR \leftarrow BR$
$AR \leftarrow 1, 1, 1, 1$

b) Construct the control realization corresponding to the following AHPL sequence:- **[8]**

1. $Z = XVA$
   $\rightarrow (a, a \wedge b, \bar{a} \wedge \bar{b})/(2, 3, 4)$
2. $A \leftarrow X;$
   $\rightarrow (1)$
3. $A \leftarrow X[1:3], X[0]$
   $\rightarrow (4)$
4. $A \leftarrow A[1:3], A[0]$
   $\rightarrow (1)$

c) With a neat block diagram explain the Disk DAS model. **[4]**

MODULE - II

Q3) a) Draw a logic block diagram of all hardware specified by the following module using Flip-flops. Give a combinational logic circuit description. **[10]**

```
MODULE :   EXAMPLE
MEMORY :   A[2]
INPUTS  :  X[2], a
OUTPUTS :  Z
CLUNITS :  FUNC[2] < : LOGIC
1.  A←X
    →(ā)/(1)
2.  A*a←FUNC (A; X);→(1)
END SEQUENCE
    Z = ∧/A
 END
CLUNITS :  LOGIC (B; Y)
INPUTS  :  B[2]; Y[2]
OUTPUTS:   NET OUT [2]
CTERMS :   r, S
BODY
r =  B[0] V Y [0];
S =  B[1] V Y [1];
NETOUT [0] = r ∧ B[1];
NETOUT [1] = S ∨ B[0];
END
```

b) Create a combinational logic circuit for a 6-bit decoder. **[6]**

c) With a neat diagram explain how the AC ← MD ∧ AC operation is executed in RIC. **[4]**

Q4) a) A computer has only 8-bit instructions and data words. If the first 3 bits of an instruction are all 1's, the instruction is to be executed in two event times. Bits 3, 4 and 5 control the first event time and bits 6, 7 the second. If bit 3 is a 0, the 1st event time is a NOP. If bit 3 is a 1 bits 4 and 5 specify rotate or shift. (enter a 0 in the vacated bit position) operations. as follows : **[8]**

Bits 4	5	
0	0	Rotate AC left
0	1	Rotate AC right
1	0	Shift AC left
1	1	Shift AC right

b) With appropriate flowcharts differentiate between the fetch cycles for multiple instructions per word and multiple words per instructions. [4]

c) Use a neat circuit diagram to explain how instruction fetch control is achieved with asynchronous memory. Also provide timing diagrams and control sequence. [8]

MODULE - III

Q5) a) With a neat block diagram explain the architecture and implementation of the microprogrammable RIC. [9]

b) Write the microcoding sequence for implementing 2-address instructions in microprogrammable RIC. [8]

c) Explain the Data path for control memory indexing. [3]

Q6) a) Use a flowchart to explain how floating-point addition and subtraction are carried out. [7]

b) Draw a neat flowchart to explain how signed multiplication is implemented. [8]

c) Draw a basic block diagram of a floating - pt co-processor. [5]

MODULE - IV

Q7) a) Design CMOS logic gates for the following functions. [8]

i) $Z = \overline{(A.B) + (C.D)}$

ii) $Z = \overline{(A + C) \cdot B + (AB)}$

b) Explain clearly the nMOS fabrication process. [8]

c) Describe the functioning of the CMOS inverter circuit. [4]

Q8) a) Obtain the current voltage characteristics for various bias conditions of a MOSFET channel. [8]

b) Explain the working of a pass transistor. [6]

c) With a neat block diagram explain the twin-tub structure and process. [6]

✷✷✷