[Total No. of Questions : 8]

S.E. (Comp.) (Semester - III) (RC) Examination, Nov./Dec. - 2011
INTEGRATED ELECTRONICS

Duration : 3 Hours **Total Marks : 100**

Instructions : *1) Answer any five questions, at least one question from each module.*
2) Make suitable assumptions, wherever necessary.

MODULE - I

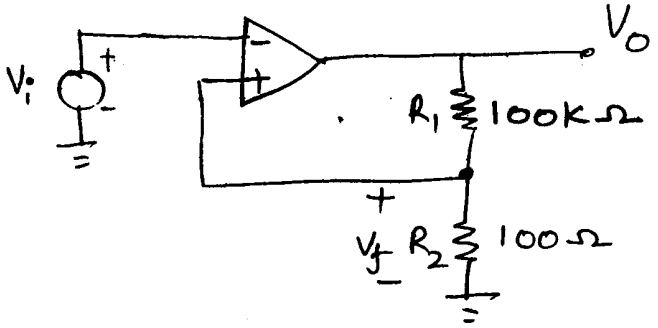
Q1) a) Derive equation for input and output resistance with feedback in voltage series feedback amplifier. **[9]**

b) Draw and explain block diagram of an instrumentation system and name two instrumentation opamp Ics? **[6]**

c) What are the electrical characteristics that op-amp (ideal) should display? **[5]**

Q2) a) What are compensating networks? Why are they required? **[5]**

b)



In the above fig. if $\pm V_{sat} = \pm 13V$, find V_{UT} and V_{LT} if $V_i = 5 \sin wt$, find the wave form of the output voltage. Why schmitt trigger is called as regenerative comparator. **[7]**

c) Derive equation for summing, weighted, Averaging amplifier along with a circuit diagram in inverting configuration. **[8]**

MODULE - II

Q3) a) Explain design of low voltage regulator using IC 723. Draw the circuit and write relevant equations. **[6]**

b) Explain how IC 555 timer can be used as a Astable operation along with a circuit & equation. **[8]**

c) Draw a neat block diagram and explain working of PLL. **[6]**

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Q4) a) Explain how timer 555 can be used as a frequency divider & pulse stretcher. [7]

b) Explain any two applications of PLL. [7]

c) Explain series voltage regulator along with a circuit and give pin configuration of LM 105. [6]

MODULE - III

Q5) a) Explain with a neat diagram the working of 3-input DTL NAND gate. Also draw the circuit for modified DTL gate. [9]

b) Describe the 3-input HTL NAND with fanout of 'N' similar gates and give its advantages. [7]

c) Give a symbol for CMOS transmission gate and along with a circuit its operation. [4]

Q6) a) Explain with a neat diagram the working of 2-input CMOS NOR gate. [6]

b) What are the modifications in corporated TTL, to overcome the limitation of speed compared to DTL. [3]

c) Explain wired-OR connections and fanout in ECL gates. Name two popular ECL families. [7]

d) Name the types in Bipolar and unipolar logic families. [4]

MODULE - IV

Q7) a) Explain A/D converter using voltage to frequency converter, along with schematic and waveforms. [8]

b) Describe 3 bit R-2R ladder D/A network. State its advantages & dis advantages. [8]

c) What is the conversion time of a 10-bit successive approximation type A/D converter using a 1MHz clock and define conversion time of A/D converter. [4]

Q8) a) A 8-bit DAC has a resolution of 20 mV/bit, what is the analog output voltage for the following digital input codes. [6]

i) 11100011 ii) 11111100

b) Give some examples where A/D & D/A converters are used. [6]

c) Explain successive approximation A/D conversion process and along with the effect of offsetting the scale in successive approximation weighing. [8]

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