COMP – 5-4 (RC)

T.E. (Computer) (Semester – V) (RC) Examination, Nov./Dec. 2012
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks :100

***Instructions** : i) Answer **five full** questions, at least **one full** question from **each** Module.*

*ii) Make **necessary** assumptions and state clearly **assumptions** made.*

MODULE – I

1. a) Give the structural and behavioral VHDL description for the full adder circuit. Draw the block diagram and write the truth table. 6

b) Construct a control realization corresponding to the following AHPL sequence.

1) $Z = X \vee A$;
$\rightarrow (a, \bar{a} \wedge b, \bar{a} \wedge \bar{b}) \mid (2, 3, 4)$

2) $A \leftarrow X$;
$\rightarrow (1)$

3) $A \leftarrow X[1:3], X[0]$;
$\rightarrow (4)$

4) $A \leftarrow A[1:3], A[0]$; 6
$\rightarrow (1)$

c) Explain the various addressing modes used in RIC processor. 8

2. a) Enumerate and describe in brief any four of the basic building blocks used in hardware circuits. 6

b) Explain branch instruction format of RIC. 6

c) Suppose that the transfer $AR \leftarrow AR[2], AR[0:1]$ is to be accomplished if the control signal CSL1 is 1 and $AR \leftarrow AR[1:2], AR[0]$ is to be accomplished if CSL2 = 1. Construct a logic block diagram of the input network for the register AR that will provide for both these transfers. 8

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MODULE – II

3. a) Write a combinational logic unit description of n-bit ripple carry adder. 6

b) Explain, how a control unit can be started again after executing a HLT command. 8

c) Explain the different forms of clocked transfer. 6

4. a) With the help of a neat diagram explain the control signals and interconnections involved in OR transfer. Also explain memory read and write operations for the RIC system. 6

b) Write the sequence of AHPL steps to implement the fetch and address cycles of RIC. 8

c) Determine the control unit target source list for the first 11 steps of RIC. 6

MODULE – III

5. a) Explain the following with reference to the Microprogrammable RIC.

i) Format for branch instruction

ii) Flags and special bits. 6

b) Draw a neat block diagram of 64 bit section carry look ahead adder and explain how it speeds up the addition process. 8

c) Draw the flowchart for floating point multiplication. 6

6. a) Write an AHPL description of the RIC microsequencer and explain. 6

b) Write the sequence of AHPL steps to implement division of fixed point quantities. 8

c) Write the combinational logic unit description for the propogate and generate section of the full adder circuit. 6

MODULE – IV

7. a) Derive the current-voltage relationships for various bias conditions for a long channel MOSFET. Plot the characteristics. 8

b) List the advantages of CMOS inverter and explain its working with necessary equations and diagrams. 8

c) What are masks ? List the masks used in nmos fabrication process. 4

8. a) What are the different approaches to CMOS fabrication. Explain the nwell CMOS fabrication process with neat diagrams. 8

b) Design CMOS logic gates for the following functions :

i) $Z = \overline{A.B.C.D}$

ii) $Z = \overline{(A.B) + C.(A+B)}$ 8

c) What is the role of SiO_2 in IC fabrication ? 4