COMP – 3-5 (RC)

S.E. (Comp.) (Semester – III) Examination, Nov./Dec. 2009

LOGIC DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : *1) Answer 5 full questions at least one from **each** Module.*

*2) Assume **any** necessary data.*

Module – I

1. a) Convert the number $AOOA_H$ into

   i) Decimal ii) Octal

   iii) Binary iv) BCD 4

   b) Perform the following operations

   Add $(-17)_{10}$ to $(-21)_{10}$ using 2's complement method. 4

   c) Suppose the Hamming code sequence 1101011 is transmitted and due to error in one position it is received as 1101111. Locate the position of error bit using add parity check. 4

   d) Prepare a K-map for function

   $F = AB + A\overline{C} + C + AD + A\overline{B}C + ABC.$

   Minimize it and realise the minimized equation using Nand gates only. 6

   e) What do you mean by Duality ? Give an example. 2

2. a) Prove the following using Boolean Algebra

   i) $(A + B)(B + C)(C + A) = AB + BC + AC$

   ii) $AB + \overline{A}C = (A + C)(\overline{A} + B)$. 6

   b) Simplify the Boolean expression using Q-M method

   $f(A, B, C, D) = \sum_m (3, 5, 8, 10) + d(1, 4, 6)$. Design/draw logic circuit using NOR gates only. 8

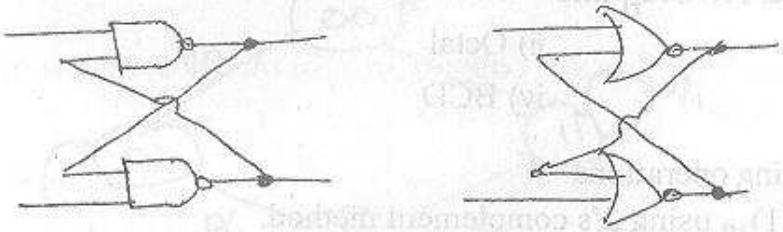
   c) Why gray code is called as a reflected code ? Explain Binary to Gray and Gray to Binary conversion of a 4 bit binary number with suitable examples. 6

P.T.O.

Module – II

3. a) A certain application requires that the absence of input pulses (Constant law) on two input lines can be indicated by a high output. The condition in which both inputs have simultaneous. Positive pulse must also be indicated by a high output. Draw the logic diagram for this circuit.
   Support your answer with a truth table. 5

   b) Explain the working of the following latches. 4



   c) Convert a D flipflop to a JK flipflop. 5

   d) Design a 8 bit adder-subtracter circuit and explain its working with the help of a diagram. 6

4. a) Explain positive and negative edge triggered flipflops. 4

   b) It is necessary to multiply 2 binary numbers, each 2 bits long in order to form their product in binary. Let the 2 numbers be represented by a_0a_1 and b_1b_0.
      i) Determine no. of o/p lines required
      ii) Find the simplified Boolean expression for each output. 6

   c) Implement the following function using a multiplexer
   $F(A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 15)$. 4

   d) Design a circuit for code conversion from excess – 3 to binary coded decimal. Assume 3 bit input. 6

Module – III

5. a) Explain the following :
   i) Ripple counter
   ii) Modulus of a counter and the terminal court
   iii) Lockout of counter. 6

   b) The content of a 4 bit shift register is initially 1101. The register is shifted 6 times to the right with serial input being 101101. What is the content of the register after each shift ? 4

   c) Design a counter using T flipflop that generates the following binary sequence 0, 1, 3, 7, 6, 4 and repeat . 8

   d) Write the different applications of a shift registers. 2

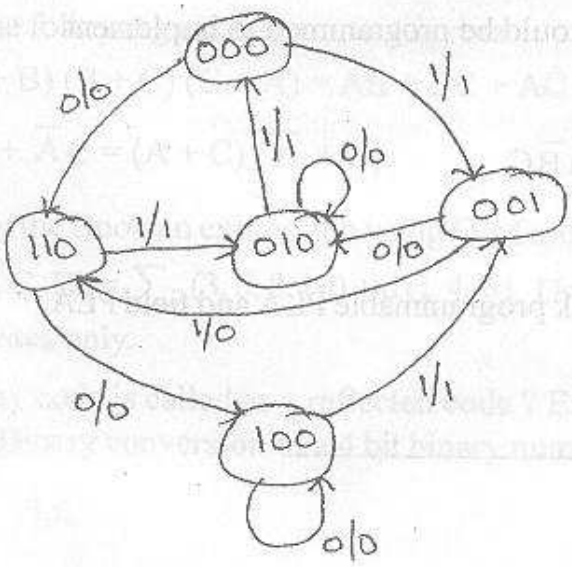
6. a) Design a mod-6 synchronous counter using JK flipflops. 8

   b) Design and explain the working of a 4 bit bidirectional register. 7

   c) Write a count sequence of a 3 bit binary down counter. Design a ripple counter using flipflops for this sequence. 5

Module – IV

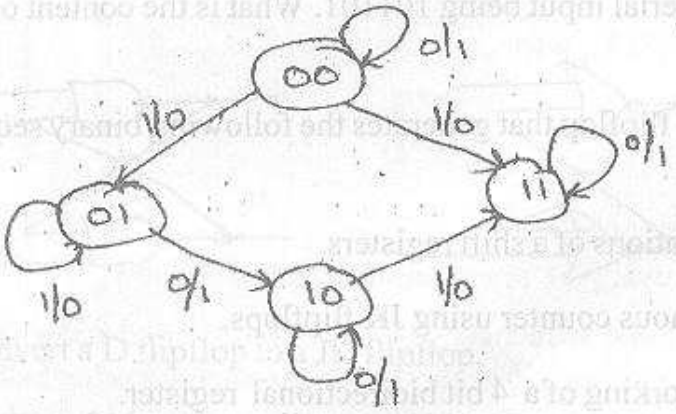
7. a) For the state diagram shown below design the circuit using SR flipflop. 10



b) Design a sequential circuit which tests 3 consecutive bits in a bit stream. If 3 consecutive bits are 1 then the output of the sequential circuit should be active. 6

c) How does PLA differ from a ROM ? 4

8. a) Obtain the state table for the following . 4



b) Design a serial adder that has 2 input lines X_1 and X_2 and 2 output lines sum and carry. The serial adder has 2 states A and B. It remains in state A if no carry is generated and goes to state B when a carry is generated. Draw the state diagram of the adder and design a suitable circuit using D flipflops. 8

c) Show how FPLA circuit would be programmed to implement

$F_1 = A\overline{B}C + AB\overline{C}$

$F_2 = A\overline{BC}BC + \overline{A}BC + A\overline{B}C$

$F_3 = \overline{AB}$ 6

d) Differentiate between Mask programmable PLA and field PLA. 2