[Total No. of Questions : 8]

S.E. (Comp.) (Semester - III) (RC) Examination, Nov./Dec. - 2011
LOGIC DESIGN

Duration : 3 Hours **Total Marks : 100**

Instructions : 1) Answer any five questions; attempt at least one question from each module.
2) Assume suitable data if necessary.
3) Draw neat diagrams if required.
4) Write question numbers legibly while answering.
5) Write description for the questions based on the marks allotted.

MODULE - I

Q1) a) Using Karnaugh Map simplify Boolean expression and give implementation of same using :

i) NAND gates only (SOP form)

ii) NOR gates only (POS form)

$F(A, B, C, D) = \Sigma_m (0, 1, 2, 4, 5, 12, 14) + d(8, 10)$ **[8]**

b) Define (i) Prime Implicant (ii) Essential Prime Implicant
Give example for each. **[4]**

c) The message below coded in 7 bit hamming code is transmitted through noisy channel. Decode message assuming that at most single error occurred in each code word.
1001001,0111001,1110110,0011011 **[8]**

Q2) a) Show 8-bit addition of following decimal numbers into 2's complement representation : **[6]**

i) +125 and +68

ii) +37 and –115

iii) – 43 and –78

b) Reduce following using Quine McClusky method **[8]**
$F(A, B, C, D) = \Sigma_m (0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$.

c) Show that Ex-OR operation is not distributive over AND operation with logic diagrams. **[6]**

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MODULE - II

Q3) a) Derive characteristic equation of SR flipflop and JK flipflop. [6]

b) Implement following logic function using Multiplexer
$F(A, B, C, D) = \Sigma_m (1, 3, 4, 11, 12, 13, 14, 15)$. [4]

c) Draw Block diagram of 4 bit adder-subtractor circuit using full adder and give brief description. [4]

d) Explain how flipflops can be used in [6]
i) Parallel data storage.
ii) Frequency division.

Q4) a) Define Encoder Design 4-bit priority encoder. [8]

b) Design 4 bit BCD to Excess-3 code converter. [8]

c) Explain Advantages of edge triggered flipflop over level triggered flipflop. [4]

MODULE - III

Q5) a) Name and explain in short four basic types of shift registers and draw a block diagram for each. [8]

b) Distinguish between Ring counter and Johnson counter. [6]

c) Show the design of a 4 bit parallel load register with a load line using T flip-flops. [6]

Q6) a) Design mod 6 asynchronous counter using T flip-flops. [6]

b) Design mod 6 self correcting counter whose counting sequence is 0-1-4-6-7-5-0. Use JK flip-flops for realization. [10]

c) Mention differences between ripple and synchronous counter. [4]

MODULE - IV

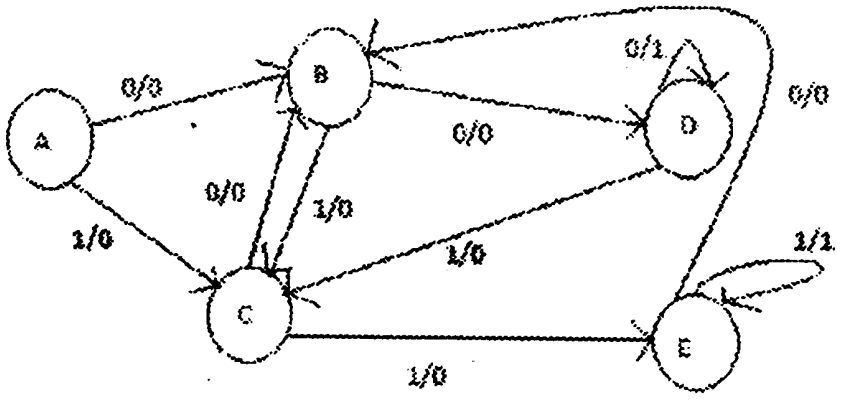
Q7) a) Differentiate between PAL and FPAL. [6]

b) Show how PLA circuit can be programmed to implement sum and carry output of full adder. [6]

c) Show the design of a 2 bit full adder using PLA with AND-OR-NOT construct. Form the programming table of the design. [8]

Q8) a) Design sequential circuit for Serial Binary Adder. **[10]**

b) Design a Sequential circuit for the following state diagram given in the figure below using D flip-flop. **[10]**



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