COMP 3-5 (RC)

S.E. (Comp.) (Semester – III) (RC) Examination, November/December 2010
LOGIC DESIGN

Duration : 3 Hours

Total Marks : 100

Instructions: *i) Answer **five** full questions, atleast **one** full question from **each** Module.*

*ii) Make suitable assumptions **wherever** necessary.*

MODULE – I

1. a) Represent the following decimal numbers in eight bit i) Sign magnitude form ii) Sign 1's complement form and iii) Sign 2's complement form

   i) +27

   ii) – 36. **6**

   b) What is meant by reflected code ? Give an example. **4**

   c) Draw the logic diagram and construct the truth table for the following expression :

   $Y = (AB)\,(\overline{A + B}) + \overline{EF}$ **4**

   d) Obtain the set of prime implicants using the tabular method for the expression

   $\sum m\,(0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$. **6**

2. a) Detect and correct errors, if any in the following even parity Hamming code word 0 1 0 1 1 0 1. **6**

   b) Obtain the minimal POS expression for $\pi M\,(0, 1, 2, 4, 5, 6, 9, 11, 12, 13, 14, 15)$ using K-map and implement it in NOR logic. **8**

   c) Reduce the following Boolean expression $(X + Y + Z)\,(\overline{X} + \overline{Y} + \overline{Z})X$. **4**

   d) How do you obtain the dual of a boolean function ? **2**

P.T.O.

MODULE – II

3. a) When is a carry generated and when is a carry propagated in a carry look ahead adder ? **4**

   b) Construct a 16 to 1 line multiplexer using 2 to 1 line and 4 to 1 line multiplexers. **8**

   c) Convert J-K to S-R flip-flop. **6**

   d) What is meant by toggling ? **2**

4. a) Write the truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the input having the highest index. Determine the minimal sum equations for the outputs. **8**

   b) Explain the operation of edge triggered D flip-flop with a neat diagram. **6**

   c) What is an odd parity generator and an even parity generator ? **6**

MODULE – III

5. a) Design a mod-7 counter with asynchronous inputs for an up operation. Draw the relevant output waveform. **6**

   b) With a neat diagram explain the working of bidirectional shift register. **6**

   c) Design a synchronous counter to produce the following binary sequence. Use JK flip flops.

   1, 3, 5, 7, 1..... **8**

6. a) With neat diagram, explain the working of serial-in-parallel-out shift register. **6**

   b) With neat diagram, explain the operation of ring counter. Also sketch the output waveform. **6**

   c) Design a 3 bit up/down counter which counts up when the control signal M = 1 and counts down when M = 0. **8**

MODULE – IV

7. a) Draw the state diagram, state table and excitation table of D flip flop and J-K flip flop. **8**

   b) A long sequence of pulses enters a 2-input 2-output synchronous sequential circuit which produces an output pulse Z = 1, whenever the sequence 10010 occurs. The overlapping sequences are accepted. Draw the state diagram, select an assignment and show the excitation table. **8**

   c) What are the advantages of programmable logic devices ? **4**

8. a) Design a PAL programmed for the following 3 variable logic function :

   $$X = ABC + \overline{A}C + A\overline{B} + \overline{B}\overline{C}$$ **6**

   b) Design FPLA as a 3 bit gray to binary code converter. **8**

   c) How is FPLA architecture different from the PAL ? **4**

   d) What does PAL 12 L 8 indicate ? **2**