T.E. (Comp.) (Semester – V) (Revised in 2007-08) Examination, Nov./Dec. 2010
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : *i) Answer **five** questions, atleast **one** full question from **each** Module.*
*ii) Make suitable assumptions, **wherever** necessary.*

MODULE – I

1. a) Explain giving examples what is meant by system modelling ? Describe in brief a natural way of modelling a digital system. 6

   b) Explain the following with respect to RIC.

      i) Two address instruction format.

      ii) Shift/rotate instruction format. 6

   c) Construct a control realization corresponding to the following AHPL sequence

      1) $Z = XVA$;

         $\rightarrow (a, \bar{a} \wedge b, \bar{a} \wedge \bar{b})/(2, 3, 4)$

      2) $A \leftarrow X$;

         $\rightarrow (1)$

      3) $A \leftarrow X[1 : 3], X[0]$;

         $\rightarrow (4)$

      4) $A \leftarrow A[1 : 3], A[0]$;

         $\rightarrow (1)$. 8

2. a) Construct a detailed logic network diagram of the digital circuit described by the following AHPL description. Include both the data section and control section and use the one flip flop per control state approach.

   MODULE :

   INPUTS : x ; a

   OUTPUTS : z

   MEMORY : r

1) $\rightarrow (a, \bar{a})/(1, 2)$

2) $r \leftarrow ((x \wedge r\,!\,x) * (a, \bar{a})$

3) $z = r\,;\, r * a \leftarrow x\,;\, \rightarrow (1)$

END. **10**

b) With the help of a neat timing diagram explain read and refresh controls for random access memories. **6**

c) Explain the syntax of a control sequence step in AHPL. What are the different forms of clocked transfers. **4**

MODULE – II

3. a) Write combinational logic unit description of n-bit ripple carry adder. **8**

b) Write the sequence of AHPL steps to implement fetch and address cycles for 32 bit instructions of RIC. **8**

c) Explain how a communication bus is implemented using Tristate Elements. **4**

4. a) Draw a neat block diagram of a single start level generation circuit using D. Flip-flops and explain its operation with neat timing diagram. **8**

b) With a neat diagram explain the basic organization of RIC. **7**

c) Write the sequence of AHPL steps required to implement shift/rotate instruction. **5**

MODULE – III

5. a) Write an AHPL description of the RIC microsequencer and explain. **8**

b) Explain carry look ahead principle with a neat diagram. **6**

c) Draw flowchart for the multiplication of two floating point numbers and explain. **6**

6. a) Explain the following with reference to microprogrammable RIC.

i) Addressing modes

ii) Format for branch instruction. **6**

b) Draw logic diagram of full adder unit and carry look ahead unit. **6**

c) Explain signed multiplication with the help of flowchart. **8**

MODULE – IV

7. a) Derive the current-voltage relationships for various bias conditions for a long channel MOSFET. Plot the characteristics. 8

   b) Explain NMOS fabrication process with neat diagrams. 8

   c) What are masks ? How are they used ? List the masks used in NMOS fabrication process. 4

8. a) Explain the working of a Pass Transistor. 6

   b) Design CMOS logic gates for the following functions :

      i) 3 input OR gate

      ii) $Z = \overline{((A.B.C.) + D)}$. 6

   c) List the advantages of CMOS inverter and explain its working with necessary equations and diagrams. 8