COMP 3-5 (RC)

S.E. (Computer Engineering) (RC) (Semester – III) Examination, May/June 2012
LOGIC DESIGN

Duration: 3 Hours | Total Marks: 100

Instructions : *1) Assume suitable data **if necessary**.*
*2) Answer **any five** questions, attempt at least **one** question from **each** Module.*
*3) Draw **neat** diagrams if **required**.*
*4) Write question numbers **legibly** while answering.*
*5) Write description for the questions based on the marks **allotted**.*

MODULE – I

1. a) If $\overline{A}B + C\overline{D} = 0$ then prove that $AB + \overline{C}(\overline{A} + \overline{D}) = AB + BD + \overline{B}\,\overline{D} + \overline{A}\,\overline{C}D$. **4**

   b) Simplify expression $A\overline{B} + ABC + A(B + A\overline{B})$. **4**

   c) Implement $AB + \overline{C}\,\overline{D}$ with only three NAND gates. Draw logic diagram. Assume inverted input is available. **3**

   d) Using Karnaugh Map simplify Boolean expression and give implementation of same using :
      a) NAND gates only (SOP form)
      b) NOR gates only (POS form)
      $F(A, B, C, D) = \sum_m(0, 1, 2, 4, 5, 12, 14) + d(8, 10)$. **9**

2. a) Obtain the minimal sum of the products for the function
      $F(A, B, C, D) = \sum(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ by Quine-McClusky method. **10**

   b) State and explain the Demargon's theorems which converts a sum into a product and vice versa. Draw the equivalent logic circuits using basic gates. **6**

   c) Given the binary code 1000100100110001. Determine the meaning of this code if the code represents.
      i) ABCD code
      ii) An unsigned integer
      iii) A signed integer in 1's complement
      iv) A signed integer in 2's complement. Show the calculation. **4**

P.T.O.

MODULE – II

3. a) Implement the full adder circuit using NAND gates only. 8

   b) Design 16:1 multiplexer using 4:1 multiplexer. 6

   c) Derive characteristic equation of SR flip-flop and JK flip-flop. 6

4. a) Explain working of parallel adder. What are advantages and disadvantages over serial adder ? 8

   b) Discuss Race Around Condition in JK flip-flop and describe

      i) Master slave JK flip-flop

      ii) Edge Triggered JK flip-flop. 12

MODULE – III

5. a) Design mod 6 self correcting counter whose counting sequence is 0-1-4-6-7-5-0. Use JK flip-flop for realization. 10

   b) Explain the working of a serial-in parallel out shift register with logic diagram and waveforms. 10

6. a) Design synchronous mod-9 counter using T flip-flops. 10

   b) Design a 4 bit rotate shift register with a rotate control input, R. If R assumes a value of 0, then the contents of the register remain the unchanged. If R assumes a value of 1, then the contents of the register are shifted to the right with the contents of the least significant bit shifted into the contents of the most significant bit. Use D flip-flops in your design. 10

MODULE – IV

7. a) A sequential circuit has two flip-flops A and B, two inputs x and y and an output z. The flip-flop input functions and the circuit functions are as follows.

   $J_A = XB + \overline{Y}\,\overline{B}$ $J_B = X\overline{A}...Z = XYA + \overline{X}\,\overline{Y}A$

   $K_A = X\overline{Y}\,\overline{B}$ $K_B = X\overline{Y} + A$

   Obtain Next state equations, logic diagram, state table and state diagram. 10

b) Design a sequential circuit whose next state equations are

$Q_A(t+1) = XQ_AQ_B + Y\overline{Q}_AQ_C + XY$

$Q_B(t+1) = XQ_AQ_C + \overline{Y}.Q_B.Q_C$

$Q_C(t+1) = \overline{X}Q_B + YQ_A.\overline{Q}_B$

Use JK flip-flop. 10

8. a) Differentiate between PAL and FPAL. 4

b) Show how PLA circuit can be programmed to implement sum and carry output of full adder. 6

c) Design sequential circuit for Serial Binary Adder. 10