18-6-15 (M)

COMP – 3-5 (RC)

S.E. (Comp.) (Semester – III) (RC) Examination, May/June 2015
LOGIC DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : 1) *Answer* ***five full*** *questions by selecting atleast* ***one*** *question from* ***each*** *Module.*
2) *Diagrams must be drawn* ***neat*** *and* ***clear*** *with* ***pencil only.***
3) ***Assume*** *missing data if* ***necessary.***

MODULE – I

1. a) Perform the following number conversions : 6
   i) $(630.25)_{10} \rightarrow (A)_2$
   ii) $(A)_2 \rightarrow (B)_8$
   iii) $(B)_8 \rightarrow (C)_{16}$

   b) Reduce the Boolean expression using Boolean algebra. 4

   $\overline{A}B\overline{D} + \overline{A}B\overline{C}D + AB + \overline{A}BCD = B(A + \overline{C})$.

   c) Subtract the following decimal numbers by representing them in 8 bit using 2's complement method. 6
   i) $(-57) - (+33)$
   ii) $(+39) - (-21)$
   iii) $(-17) - (-33)$.

   d) Why NAND and NOR gates are called as universal gates ? Explain using suitable diagrams. 4

2. a) Realize the following Boolean function : 6

   $Y = \overline{A}B + (C + \overline{D})E$

   Using : i) Two input NOR gates only
   ii) Two input NAND gates only.

P.T.O.

b) Represent $(-27)_{10}$ in 8 bit 3

i) Sign magnitude form

ii) Sign 1's complement form

iii) Sign 2's complement form.

c) A secure communication medium is used to transmit data to Bob by Alice. During the communication the data received by Bob was 1100100. Bob was in a dilemma to decide if the data sent was accurate or not. Suggest a secure technique using even numbering concept by which Bob can identify as well as correct the error involved if any. 4

d) Find canonical sop expression of Boolean function 7

$F(A, B, C, D) = ACD + A\bar{C}D + BC + A\bar{B}\bar{C}D + ABD$ and simplify using K-map.

MODULE – II

3. a) Design and explain the working of a 3 bit parallel adder/subtractor circuit. 8

Use a control variable W and a circuit that functions as a full adder when W = 0 and as a full subtractor when W = 1.

b) Realize the Boolean expression using 8 : 1 MUX where B, C, D appear on select lines S2, S1, S0 respectively. 5

$F(A, B, C, D) = \sum m(1, 6, 7, 9, 10, 11, 12)$.

c) Distinguish between combinational circuits and sequential circuits. 5

d) Define code converters. 2

4. a) Explain the circuit diagram, state diagram, present state-next state table, excitation table and characteristic equation of S-R flip-flop. 6

b) Realize J-K flip-flop using D flip-flop. 8

c) Explain level triggered and edge triggered flip-flops with the help of timing diagrams. 6

MODULE – III

5. a) Explain the steps involved in the design of synchronous counters. **6**

   b) What do you mean by glitches or false spikes that appear at the decoding gate output in an asynchronous counter ? Give any two ways by which it can be avoided. **6**

   c) What are the different applications of counters ? **4**

   d) The content of 4 bit shift register is initially 1101. The contents of the register is shifted 4 times to the left with serial input being 101101. What is the content of the register after each shift ? **4**

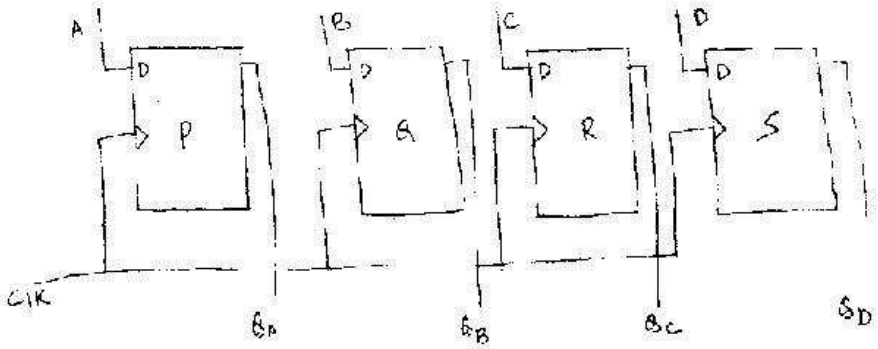
6. a) Design a 3 bit Johnsons counter. Explain its working. **8**

   b) Explain the following registers : **8**

      i) SISO ii) SIPO

      iii) PISO iv) PIPO

   c) Consider the parallel in parallel out register shown below : **4**



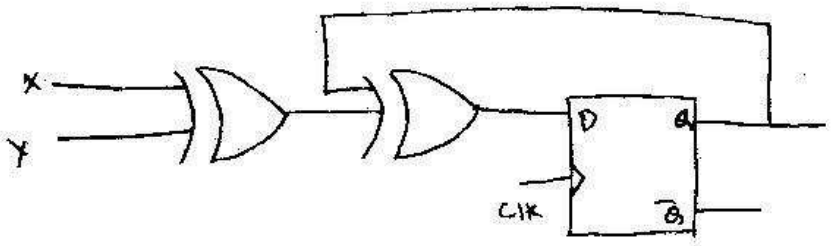
In figure, if A = 1, B = 0, C = 1, D = 1 are the initial contents given to the respective inputs of the flip flop. If a consistent input is given that is A = 0, B = 1, C = 0, D = 1 to the respective flip flop inputs. What will be the data output after the 3rd clock pulse ?

MODULE – IV

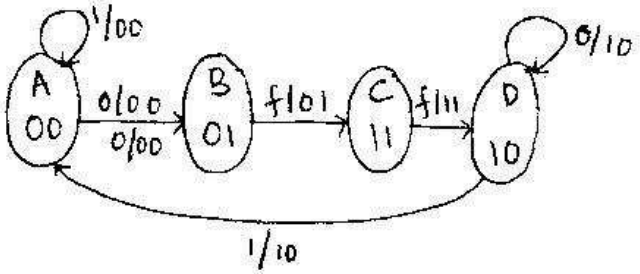
7. a) Compare Moore circuit and Mealy circuit. 6

$K = 1 + 2\mu$

b) Obtain state table, state diagram and state equation for the circuit shown below : 6



c) Design a circuit that will function as prescribed by the state diagram shown below. Use SR flip flops for implementation. 8



8. a) Implement PLA table for the following Boolean functions : 6

$F_1 (A, B, C) = \Sigma_m(0, 1, 6, 7)$

$F_2 (A, B, C) = \Sigma_m(3, 6, 7)$

$F_3 (A, B, C) = \Sigma_m(0, 1, 3, 7)$

b) How is FPLA architecture different from PAL ? 6

c) Explain the following : 6

i) Registered PAL's

ii) Configurable PAL's.

d) What does PAL 12L8 indicate ? 2