COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) Examination, May/June 2012
COMPUTER HARDWARE DESIGN

Duration : 3 Hours | Total Marks : 100

Instruction : *Attempt **any five** questions, by selecting at least **one** question from **each** Module.*

MODULE – I

1. a) What is a system ? Explain the properties of system. 6

   b) Draw and explain single address instruction format and its different addressing modes. Explain each addressing mode with example. 6

   c) Construct the logic block diagram for performing the transfer rotate right $AR \leftarrow AR[1], AR[2], AR[0]$. 8

   Draw the diagram of control levels and control pulses used in Register Transfers and explain how to generate CSP signal from control sequential circuit.

2. a) Determine the minimal expression for DAR[i] where AR must be the destination of following 4 transfers. 8

   $AR \leftarrow 0, 0, 0, 0$

   $AR \leftarrow 1, 1, 1$

   $AR \leftarrow \overline{AR}$

   $AR \leftarrow BR$

   Also draw the logic block diagram.

   b) Explain the concept of inter system busing. With the help of neat diagram, explain the two approaches to inter system bus wiring. 8

   c) Write short notes on the following : 4

   i) Direct access storage

   ii) Read only memory.

P.T.O.

MODULE – II

3. a) Given that U = (1, 1, 1, 0); V = (1, 0, 0, 1); W = (1, 0, 1) **8**

$$N = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{matrix} x = 5 \\ y = 3 \\ z = -1 \end{matrix}$$

Find :

a) $U \oplus V$

b) $\wedge/W$

c) $\oplus/W$

d) N ! W

e) $(4\ T\ 5) \oplus U$

f) $(x < z)$

h) U, V

i) 8TO

b) Explain how a communication bus is implemented using Tristate Elements. **4**

c) Write a combinational logic unit description for a

i) Full-adder

ii) I-input decoder.

4. a) Give the flowchart for compiling of data network and explain. **6**

b) Draw the flowchart for fetch sequence for 16-bit instruction and explain. **6**

c) Give the implementation of HLT using DEAD END. Also explain the implementation of HLT by return to step 1. Support your answer with neat diagram. **8**

MODULE – III

5. a) Write a combinational logic unit description for the propagate and generate section of the full-adder circuit. 5

   b) Write AHPL description of the RIC microsequencer and explain it. 8

   c) With the help of neat diagram explain the organization of microprogrammable RIC. 7

6. a) Discuss the sequence of steps to implement signed multiplication. 8

   b) Explain the hardware organisation of floating point coprocessor. 5

   c) Discuss signed multiplication with the help of flowchart. 7

MODULE – IV

7. a) Discuss the working of CMOS inverter with necessary diagrams. 7

   b) List and explain the steps in IC fabrication. 8

   c) Explain the working of Pass transistor. 5

8. a) Design CMOS logic gates for the following functions 8

      i) 2-input NAND gate

      ii) $Z = \overline{(A \cdot B) + (C \cdot D)}$.

   b) With the help of a neat diagram explain nMOS fabrication process. 8

   c) What are masks ? List the masks used in nMOS fabrication process. 4
