10/12/2013 E

COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) (Revised Course) Examination, Nov./Dec. 2013
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : *i) Answer **five** questions, atleast **one** full question from **each** Module.*
*ii) Make suitable assumptions, **wherever** necessary.*

MODULE – I

1. a) Give the structural and behavioral VHDL description for full subtractor circuit. Draw the block diagram and also write the truth table. 6

   b) Explain :

   i) Single address instruction format of RIC.

   ii) Shift/Rotate instruction format of RIC. 6

   c) Determine a minimal expression for $D_{AR[i]}$ where AR must be the destination of the following four transfers.

   $AR \leftarrow 0, 0, 0$

   $AR \leftarrow 1, 1, 1$

   $AR \leftarrow \overline{AR}$

   $AR \leftarrow BR$

   Also draw the logic block diagram of the associated hardware. 8

2. a) Bring out the differences between direct access storage and sequential access storage in terms of hardware design. 6

   b) Construct logic block diagrams of the data unit realizations of expressions.

   i) $(A \mid B \mid C) * (f, g, h) \leftarrow D$

   ii) $D \leftarrow (A \mid B) * (f, g)$ 8

   c) Explain any two approaches to inter system bus wiring. 6

P.T.O.

MODULE – II

3. a) Write combinational logic unit description for an I bit incrementer. 6

   b) Write the sequence of AHPL steps required to implement shift/rotate instructions of RIC. 6

   c) What is hardware compiler ? With a flow chart explain the steps involved in the compilation of data network. 8

4. a) Explain the different forms of clocked transfers. 5

   b) Write the sequence of AHPL steps to execute the different branch commands of RIC. 8

   c) Explain the start-reset sequence of the control unit. 7

MODULE – III

5. a) Explain hardwired control unit and microprogrammed control unit with neat block diagrams. 8

   b) Draw a neat block diagram of 64 bit section carry look ahead adder and explain how it speeds up the addition process. 6

   c) Write the sequence of AHPL steps to implement division of fixed point quantities. 6

6. a) With a neat block diagram explain the organization of microprogrammable RIC. 8

   b) Write the combinational logic unit description of 16 bit carry look ahead adder given the combinational logic unit description of the carry look ahead unit. 6

   c) Explain with a neat diagram the hardware organization of floating point coprocessor. 6

MODULE – IV

7. a) Explain the working of nMOS depletion mode transistor with neat diagram. 6

   b) Explain the n-well process to CMOS fabrication with neat diagrams. 8

   c) Determine the pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter. 6

8. a) Draw stick diagrams and mask layout for the following : 8

      i) CMOS NAND gate ii) nMOS inverter

   b) Explain the working of MOS inverter with nMOS depletion type transistor as load. Draw the transfer characteristics. 8

   c) Explain the working of a pass transistor. 4