H16116

COMP 4 – 3(RC)

S.E. Computer Engineering (RC) (Semester – IV)
Examination, May/June 2016
COMPUTER ORGANIZATION

Duration : 3 Hours | Total Marks : 100

Instructions: *1)* ***Assume*** *suitable data if necessary.*
2) Answer ***any five*** *questions; attempt at least* ***one*** *question from* ***each*** *Module.*
3) Draw ***neat*** *diagrams if* ***required.***
4) Write question numbers ***legibly*** *while answering.*
5) Write description for the questions based on the marks ***allotted.***

MODULE – I

1. a) Explain the different bus structures supported by desktop systems. **8**

   b) Explain the following parameters with reference to memory system : **6**

   i) access time ii) cycle time
   iii) speed iv) speed
   v) transfer rate vi) cost

   c) With a neat diagram, explain the typical 16Mb DRAM. **6**

2. a). Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. **6**

   i) Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

   ii) Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

iii) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

b) Explain need for RAID technology in computer organization with suitable structures. **8**

c) Explain the various terms related to access of a magnetic disk. Find the average access time that reads or writes to 2048 byte sector. Assume that the disk rotates at 3000rpm; each track of the disk has 16 sectors and the data transfer rate of the disk is 64MB/sec. Assume seek time 12ms. **6**

MODULE – II

3. a) Explain with neat flowchart the process of multiplication of floating point number using computer arithmetic. **8**

b) Divide-122 by 13 in binary twos complement notation, using 12 -bit words. Show the steps clearly. **6**

c) Use the Booth algorithm to multiply-33 (multiplicand) by 29 (multiplier), where each number is represented using 7 bits. **6**

4. a) With a neat flowchart, explain the interrupt I/O processing. **6**

b) With a neat block diagram, explain the structure of the I/O module. **8**

c) Describe mechanisms for identifying device in interrupt I/O processing. **6**

MODULE – III

5. a) Assume a pipeline with four stages : fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO) and execute (EX). Draw a diagram for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies. **4**

b) Discuss the taken/not taken switch techniques used I branch prediction. **8**

c) Describe any three important issues in instruction set design. **8**

6. a) Write the one two and three address instructions that could be used to compute $Y = (A + B*C - D) / (E*F - G*H)$ **6**

b) Explain the interrupt cycle of the instruction cycle. Also show the flow of data during the cycle. **8**

c) Describe the addressing modes supported by x 86 processor with examples. **6**

MODULE – IV

7. a) How does micro programmed control unit function ? Illustrate with neat diagram. **6**

b) What is relationship between instruction and micro operations ? Explain with example. **4**

c) Describe superscalar instruction issue policies. **6**

d) Briefly explain block diagram of tightly coupled multiprocessor. **4**

8. a) What is meaning of each of four states in MESI protocols ? **6**

b) Give advantages and disadvantages of micro programmed control unit. **4**

c) Explain concept of : **6**

i) True data dependency

ii) Procedural dependency

iii) Resource conflict

d) Differentiate between horizontal and vertical microinstruction. **4**