COMP 3 – 6 (RC)

S.E. (Comp) (Semester – III) (RC) Examination, May/June 2015
INTEGRATED ELECTRONICS

Duration : 3 Hours | Total Marks : 100

Instructions : *i) Assume **suitable** data **wherever** required.*
*ii) Answer **any five** questions, selecting atleast **one** from **each** Module.*

MODULE – I

1. a) How do ideal OPAMP characteristics differ from that of practical OPAMP characteristics ? Explain. **5**

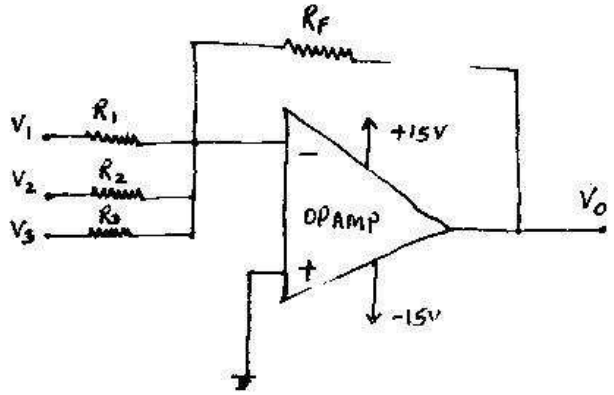
   b) Derive an equation for the closed -loop voltage gain of an OPAMP in a voltage-series feedback amplifier configuration. **8**

   c) Describe the working of Schmitt Trigger with neat diagrams and equations. **7**

2. a) With respect to OPAMP, describe the following terms : **8**
      i) Input offset current
      ii) Gain-Band width product
      iii) CMRR
      iv) Slew rate

   b) Draw and explain the block diagram of a instrumentation system. **6**

   c) i) For the summing amplifier shown below as has following inputs : **6**



P.T.O.

$V_1 = 2V$, $V_2 = 3V$, $V_3 = 4V$ and $R_F = R_1 = R_2 = R_3 = R = 1\ k\Omega$.

Supply voltages are ± 15V. Determine the output voltage.

ii) With neat circuit diagram, state different characteristics of a voltage- follower circuit.

MODULE – II

3. a) Write a short note on voltage regulator IC LM105. 6

b) Explain Monostable multivibrator using timer IC 555. 7

c) With neat block diagram, explain the operating principle of phase-locked loop. 7

4. a) Explain with a neat diagram, how low voltage regulation is achieved using IC723. 6

b) Design an astable multivibrator using 555 timer for a frequency of 1kHz and a duty cycle of 70%. Assume $C = 0.1\ \mu F$. 8

c) Describe the following application of PLL : 6

i) Phase shifter.

MODULE – III

5. a) Name the types in Bipolar and Unipolar logic families. Briefly explain. 6

b) Explain the working of a TTL gate. Draw necessary diagram. 6

c) i) Explain the following characteristics of digital IC 4

I) Speed of operation II) Noise immunity.

ii) Explain CMOS inverter. 4

6. a) Explain the working of a HTL gate. Draw necessary diagram. State its advantages. 8

b) Draw a neat diagram of modified DTL gate and explain its working. 7

c) State some advantages and disadvantages of a RTL gate. 5

MODULE – IV

7. a) Describe 3 bit R-2R ladder D/A converter. State its advantages and disadvantages. **8**

   b) Explain with neat diagrams, A/D converter using voltage-to-frequency conversion. **7**

   c) Explain some specifications of A/D converter. **5**

8. a) Describe Weighted-Resistor D/A converter. State its advantages and disadvantages. **8**

   b) Explain with neat diagrams, dual-slope A/D converter. Why such a converter is used in digital voltmeters ? **7**

   c) Explain some specifications of D/A converter. **5**