COMP 4 – 3 (RC)

S.E. (Comp.) IV Semester Examination, November 2009
(Revised 07-08)
COMPUTER ORGANISATION

Duration : 3 Hours Total Marks : 100

Instructions : *1) Answer **any five** questions, atleast **one from each** module.*
*2) Make suitable assumptions, **wherever** necessary.*
*3) Draw **neat** diagrams **wherever** required.*

Module – I

1. a) Explain the different elements of cache design. 8

   b) What do you mean by multiple bus hierarchy ? Why is it used in computer systems ? Explain any one multiple bus architecture. 8

   c) Enumerate and explain the different cache replacement policies. 4

2. a) A computer system consists of 16 k × 8 cache memory, which uses direct mapping with each line consisting of 8 words. Main memory capacity of the system is 4096 k × 8. 7

   – Show the format of main memory addresses.
   – How many lines are present in cache ?
   – How many bits are there in each word of cache ?

   b) Explain the bus timing and bus data transfer types. 4

   c) What is memory hierarchy ? Why is it required ? 5

   d) Explain the different characteristics of disk systems. 4

Module – II

3. a) For vectored interrupts, why does the I/O module place the vector on the data lines rather than an the address lines ? 2

   b) With the help of a neat flowchart, explain the floating point addition and subtraction. 9

   c) Compare the strengths and weaknesses of sign-magnitude numbers to 2's complement numbers. 4

   d) Explain the functions of I/O Module. 5

P.T.O.

4. a) With the help of a flowchart, explain Booth's algorithm. Perform following multiplication. 7

   $(-18) \times (-7)$

   b) Explain the various design issues in implementing interrupt driven I/O. 6

   c) Draw and explain the block diagram of a DMA controller. 5

   d) Differentiate between synchronous and asynchronous transfer. 2

Module – III

5. a) Explain the various approaches to deal with branches in instruction pipelining. 10

   b) Explain the register organisation of a CPU. 4

   c) What do you mean by compiler based register optimisation in RISC ? 6

6. a) What are the advantages of using large register file over cache and vice versa ? 6

   b) What do you mean by addressing mode ? Explain the various addressing modes in 8086. 6

   c) What are zero-address, single address and two-address instructions ? Explain with the help of an example. 6

   d) Explain data flow during indirect cycle. 2

Module – IV

7. a) Explain the different superscalar instruction issue policies. 4

   b) Differentiate between hardwired and microprogrammed control unit. 6

   c) Explain the 2-address sequencing technique for microinstructions. 6

   d) Explain the functions of multiprocessor operating systems. 4

8. a) Differentiate between hard and soft microinstructions. 3

   b) Explain the organisation of control memory. 4

   c) Explain the h/w approaches to cache coherence problems. 8

   d) What do you mean by microinstructions ? Explain the different microinstructions address generation techniques. 5