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Comp 3 – 6 (RC)

S.E. (Computer) (Semester – III) (RC) Examination, May/June 2013
INTEGRATED ELECTRONICS

Duration : 3 Hours Total Marks : 100

Instruction : *Answer* ***any five*** *questions, selecting at least* ***one*** *question from* ***each*** *Module.*

MODULE – I

1. a) Derive a equation for closed loop voltage gain for voltage-series feedback amplifier. 7

   b) What is a feedback ? List two types of feed back. Which type is used in linear applications ? Give block diagram representation of current series and voltage short feed back. 7

   c) Draw the block diagram of an op-amp and briefly descrieb the operation of each block. 6

2. a) Derive equation for summing, weighted, averaging amplifier along with a circuit diagram in inverting configuration. 8

   b) Draw and explain integrator circuit and draw necessary waveforms. 8

   c) How does negative feedback affect the performance of a inverting amplifier. 4

MODULE – II

3. a) Explain the working and applications of a free running multivibrator. 8

   b) Explain the applications of IC 723 regulator. 8

   c) Define and explain load regulation with respect to a voltage regulator. 4

4. a) Draw the Internal diagram of IC 555 fixed and explain its working. 8

   b) Draw a block diagram and explain the basic operation of a phase-locked loop. 8

   c) Describe in detail any two applications of PLL. 4

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MODULE – III

5. a) Compare the characteristics of the following digital IC logic families : 8

   i) RTL ii) DTL iii) HTL.

   b) Draw the circuit diagram of 2- input TTL NAND gate and explain its operation and state the conditions of the transistors in the circuit for all possible input combinations. 8

   c) Explain why DCTL (Direct Coupled Transistor Logic) gate is not popular in Ic technology, although it is simpler than RTL (Resistor Transistor Logic). 4

6. a) Explain the working of a CMOS Inverter. 7

   b) Calculate : 8

   i) Noise margin

   ii) Fan out

   iii) Power-dissipation of HTL gate.

   Assume $h_{FE} = 40$

   Draw the circuit diagram of HTL gate.

   c) Compare the current spikes in ECL (Emitter Coupled Logic) and TTL (Transistor Transistor Logic) gates. 5

MODULE – IV

7. a) An 8-bit weighted resistor DAC produces an O/P voltage of 2.0 V for an i/p of 00110110. What will be the value of v_{out} for an i/put code. 8

   i) 11000001 ii) 00011100

   b) Explain successive approximation type A/D converter and its advantages. 7

   c) Describe 3 bit R-2R ladder D/A network. State its advantages. 5

8. a) Explain A/D converter using voltage to frequency converter, along with schematic and waveforms. 8

   b) Give examples where A/D and D/A converters are used. 7

   c) Explain the voltage to frequency converter and derive the necessary expressions. 5