17/12/14 regular (m)

COMP 3 – 5 (RC)

S.E. (Comp.) (Semester – III) (RC) Examination, Nov./Dec. 2014
LOGIC DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : 1) *Answer **five full** questions by selecting at least **one** question from **each** Module.*
2) *Diagrams must be drawn **neat** and **clear** with **pencil** only.*
3) ***Assume** missing data **if necessary**.*

MODULE – I

1. a) Perform the following number conversions : 6

   i) $(5678)_{10} \rightarrow$ Excess – 3 code

   ii) $(FABD.74F)_{16} \rightarrow$ Octal

   iii) $(164.34)_8 \rightarrow$ Decimal.

   b) Give the Boolean expression for the following statements : 4

   i) Y is a 1 only if A is a 1 and B is a 1 or if A is a 0 and B is a 0.

   ii) Y is a 1 only if A, B, C are all 1's or if only one of the variables is a 0.

   c) Explain positive logic system and negative logic system with examples. 4

   d) Realize the following expression using NOR gates only 6

   $Y = \overline{A}BC + A\overline{B}C + AB\overline{C}$.

2. a) How do you add two decimal numbers in BCD format if sum is > 9 ? 4

   Perform the following BCD addition :

   128 + 192.

   b) Determine the single error correcting code for the binary data 1011 using even parity. 4

   c) For the Boolean function : 4

   $F(A, B, C) = \overline{A}C + AB + A\overline{B}C$

   i) Find Canonical SOP expression.

   ii) Determine the simplified Boolean expression using K-map.

P.T.O.

d) Find minimal SOP for the Boolean expression

$F(A, B, C, D) = \Sigma m(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$

using tabulation method. 8

MODULE – II

3. a) Design a full adder using Nand gates only. Explain the operation of the circuit with truth tables. 8

b) What is priority Encoder ? 6

c) Implement a full subtractor with two 4 : 1 multiplexers. 2

d) Define magnitude comparator.

4. a) What is 'Race Around Condition' ? Explain any two ways how race around condition can be eliminated. 6

b) Realize J-K flip flop using S-R flip flop. 8

c) Explain the operation of master slave J-K flip flop with suitable diagrams and truth table. 6

MODULE – III

5. a) Design and explain the working of a Asynchronous decade counter using J-flip-flops with its timing diagram. 8

b) Compare synchronous counter and asynchronous counter. Give examples with logic diagrams. 6

c) Design a mod-3 synchronous counter using J-K flip-flop. 6

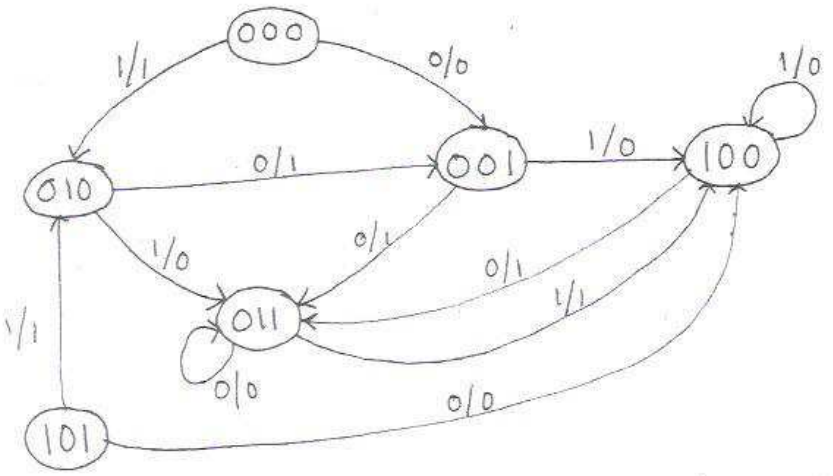
6. a) Explain the operation of a Ring Counter. Also sketch the output waveform. 6

b) Design and explain the working of 4 bit bidirectional shift register with the help of a logic diagram. 8

c) The content of a 4 bit serial in parallel out shift register is 1001. The contents of the register is shifted four times to the right, with serial input being 101101. What is the content of the register after each shift ? 6

MODULE – IV

7. a) For the state diagram shown below. Obtain the state table, reduced state table and reduced state diagram. 8



b) Explain state table, state diagram and state equation in synchronous sequential circuits. 4

c) A long sequence of pulses enters a 2 input 2 output synchronous sequential circuit which is required to produce an output z = 1, whenever the sequence 1111 occurs overlapping sequences are accepted. For example, if the input is 01011111, the required output is 00000011. Design the circuit using D flip-flop. 8

8. a) A combinational circuit is defined by following functions : 8

$F_1(A, B, C) = \Sigma m(3, 5, 6, 7)$

$F_2(A, B, C) = \Sigma m(0, 2, 4, 7)$

Implement the circuit with PLA having three inputs, four product terms and two outputs.

b) Explain the architecture of PLA with the help of a block diagram. 6

c) Design FPLA as a 3 bit gray to binary code converter. 6