COMP 3 – 5(RC)

S.E. (Computer Engineering) (Semester – III) (RC)
Examination, May/June 2013
LOGIC DESIGN

Duration : 3 Hours | Max Marks : 100

Instructions : *1) Assume suitable data **if** necessary.*
*2) Answer **any five** questions, attempt atleast **one** question from **each** Module.*
*3) Draw **neat** diagrams **wherever** required.*
*4) Write question numbers **legibly** while answering.*
*5) Write answers for the questions based on marks allotted. Figures at the **right** inside "()" indicate marks.*

MODULE – I

1. A) Obtain the truth table for the following logic equation :
$Y = (A + BC)(B + C'A)$ **(4)**

B) Represent the decimal number $(249)_{10}$ in binary form using :
i) Excess-3 code
ii) Gray code
iii) Straight Binary code
iv) Octal code. **(8)**

C) Show that Dual of EX-OR is same as its complement. **(4)**

D) Prove the following using Boolean Algebra.
$AB' + A'B + AB = A + B$ **(4)**

2. A) A safe has locks for V, W, X, Y and Z all of which must be unlocked for the safe to open. The keys to the locks are distributed among 5 executives in the following manner :
Mr. A has keys for locks V and X
Mr. B has keys for locks V and Y
Mr. C has keys for locks W and Y
Mr. D has keys for locks X and Z
Mr. E has keys for locks V and Z.
i) Determine the minimal number of executives required to open the safe.
ii) Who is essential executive ?
iii) Find all the combinations of executives that can open the safe ; write an expression f(A, B, C, D, E) which specifies when the safe can be opened as a function of what executives are present. **(6)**

P.T.O.

B) Perform the following :
   i) Convert $(11.75)_{10}$ to binary
   ii) Convert $(8BF4)_{16}$ to octal
   iii) Convert $(6327.4051)_{8}$ to decimal
   iv) Convert $(675.625)_{10}$ to hexadecimal. (8)

C) Perform the following using 2's complement method :
   i) 48 – 23
   ii) 48 – (– 23)
   iii) 23 – 48. (6)

MODULE – II

3. A) Design an Odd Parity Bit Generator using combinational logic design techniques. (6)

   B) Design a combinational logic circuit with 4 inputs A, B, C and D that will produce output '1' only whenever 2 adjacent input variables are 1s. A and D inputs are also to be treated as adjacent. (8)

   C) Design an octal-to-binary encoder i.e. an 8-line to 3-line encoder that accepts 8 input lines and produces a 3-bit output corresponding to the activated input. (6)

4. A) Explain with examples the difference between a latch and a flip flop. (4)

   B) Draw logic diagrams and present truth tables of the following :
      i) Active High S-R latch using NAND gates.
      ii) Active low S-R latch using NAND gates. (6)

   C) Draw the logic diagram of edge triggered S-R flip flop. Also, present its truth table. (4)

   D) Show how you will convert the above S-R flip flop to a D flip flop. (6)

MODULE – III

5. A) Design synchronous mod-9 counter using T flip flops. (10)

   B) Design mod 6 self correcting counter whose counting sequence is 0-1-4-6-7-5-0... Use J-K flip flops for realisation. (10)

6. A) With a neat diagram, explain the working of serial-in-parallel-out shift register. (7)

   B) Design and explain the working of a 3-bit Bidirectional shift register. (8)

   C) The bit sequence 1101 is serially entered (right most bit first) into a 4-bit parallel out shift register that is initially clear. What are the contents of the register after two clock pulses ? (5)

MODULE – IV

7. A) A sequence detector is a sequential machine which produces an output 1, every time the desired sequence is detected and an output 0 at all other times. Draw the state diagram and state table for a sequence detector to detect sequence 1010. (Please note overlapping of input sequence is permitted). **(10)**

B) Reduce the following state table :

Present-State	Next State		O/P	
	X= 0	X = 1	X = 0	X = 1
a	c	b	1	1
b	d	c	0	0
c	g	d	0	1
d	e	f	1	0
e	a	f	1	0
f	g	f	1	0
g	a	f	1	0

i) Present the reduced state diagram.
ii) Present the reduced state table.
iii) For the reduced state table, do the state assignment.
iv) And, draw the transition and output table for the reduced state table. **(10)**

8. A) Show how the FPLA circuit would be programmed to implement :

$F1 = AB'C + ABC'$

$F2 = A(BC)'BC + A'BC + AB'C$

$F3 = (AB)'$ **(8)**

B) Design a PAL programmed for the following 3 variable logic function :

$X = ABC + A'C + AB' + (BC)'$ **(6)**

C) Show how PLA can be programmed to implement 3-bit gray to binary conversion. **(6)**