[Total No. of Questions : 8]

S.E. (Comp.) (Semester - III) Examination, May 2011
LOGIC DESIGN

Duration : 3 Hours **Total Marks : 100**

Instructions : 1) Answer five full questions, atleast one full question from each module.
2) Make suitable assumptions wherever necessary.

MODULE - I

Q1) a) Represent the following decimal numbers in eight bit [6]
i) sign magnitude form
ii) sign 1's complement form and
iii) sign 2's complement form
1) +14
2) –17

b) What are self complementing codes? Write two self complementing codes. [4]

c) Draw the logic diagram and construct the truth table for the following expression
$X = A + B + \overline{CD}$. [4]

d) Obtain the set of prime implicants using the tabular method for the expression [6]
$\Sigma m\,(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$.

Q2) a) Detect and correct errors, if any in the following even parity Hamming code word 1101010. [6]

b) Obtain the minimal SOP expression for Σm (2, 3, 5, 7, 9, 11, 12, 13, 14, 15) using K-map and implement it in NAND logic. [8]

c) Reduce the following Boolean expression [4]
$AB + A(B + C) + \overline{B}(B + D)$

d) From positive to negative logic system, what does an OR gate become and what does an AND gate become? [2]

MODULE - II

Q3) a) How does the look ahead carry adder speed up the addition process? [6]

b) Construct a 16 to 1 line multiplexer using only 2 to 1 line multiplexers. [8]

c) Convert S-R to J-K flip flop. [6]

Q4) a) Using two 2 to 4 line decoders along with any necessary gates, construct a 3 to 8 line decoder. [8]

b) Explain the operation of edge triggered S-R flip flop with a neat diagram. [6]

c) Describe the operations performed by the following logic circuits. [6]

i) Comparator.

ii) Encoder.

MODULE - III

Q5) a) Design an asynchronous decade counter and sketch the output waveform. What is partial decoding? [8]

b) How does synchronous counters differ from asynchronous counters? [4]

c) Design synchronous 2 bit up/down counter. Mention some applications of counters. [8]

Q6) a) What are shift registers? Explain with a diagram parallel-in-serial out shift register. [8]

b) How shift register counter differs from a basic shift register. Explain the operation of Johnson counter for four bits. [7]

c) Explain how shift registers can be used to generate a time delay. [5]

MODULE - IV

Q7) a) Draw the state diagram, state table and excitation table for J-K flip flop. [5]

b) Design a 2-input, 2 output synchronous sequential circuit which produces an output $Z = 1$, whenever any of the following input sequence – 1101, 1011 or 1001 occurs. The circuit resets to the initial state after a 1 output is generated. [7]

c) What are the advantages of programmable logic devices? Give main steps in the synthesis of synchronous sequential circuits. [8]

Q8) a) Show how the PAL circuit is programmed to implement the function. [6]

$F = A\bar{B}\bar{C}D + \bar{A}BCD + \bar{A}BC\bar{D} + AB\bar{C}D$

b) Design a FPLA circuit that can be programmed to implement the difference and carry-out outputs of a full subtractor. [8]

c) Explain the programmable polarity feature of PAL and FPLA devices. [6]

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