10161S M

COMP 4 – 3 (RC)

S.E (Comp.) (Semester – IV) (RC) Examination, May/June 2015
COMPUTER ORGANIZATION

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **five full** questions, at least **one full** question from **each** Module.*
*2) Make **suitable** assumptions **wherever** necessary.*

MODULE – I

1. a) A block associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks each consisting of 128 words.
   i) How many bits are there in main memory address ?
   ii) How many bits are there in each of the TAG, SET and WORD fields ?
   Show proper justification for the values assigned. **6**

   b) Draw the block diagram of 8M × 32 memory using 2M × 8 memory chip. Show all the signals required for the above memory configuration. **6**

   c) Draw a neat diagram and explain the single-bus organization ? Also illustrate the advantages of using multiple bus organization. **8**

2. a) Consider a 8 drive, 500 GB per drive RAID array, what is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5, 6 ? **3**

   b) Explain the operation of Dynamic RAM and compare it static RAM cell. **8**

   c) With neat state diagram, explain instruction cycle, which includes interrupt cycle into consideration. **6**

   d) Explain in briefly, principle of operation of CD-ROM. **3**

MODULE – II

3. a) Explain the broad category of external devices supported for I/O, with block diagram, explain the structure of an external device. **8**

   b) Explain the following device identification techniques in interrupts : **6**
   i) Software Poll
   ii) Daisy chain
   iii) Bus Arbitration.

   c) Use the Booth algorithm to multiply – 23 (multiplicand) by 29 (multiplier), where each number is represented using 6 bits. **6**

P.T.O.

4. a) Explain the characteristics of I/O channels. Support your answer with a neat diagram of I/O channel architecture. **8**

   b) Express the following numbers in IEEE 32 bit floating point format : **4**

      i) – 5

      ii) – 1.5

      iii) 384

      iv) $-\frac{1}{32}$.

   c) Divide 145 by 18 using Restoring division algorithm. Also give the pseudo code for the above algorithm. **8**

MODULE – III

5. a) Write the one, two, three address instructions that could be used to compute

      $Y = (a * b - c)/(d * e - f)$

      Assume that a, b, c, d, e, f and y are memory locations, whose values should not be altered. **8**

   b) Compare the characteristics of CISC and RISC. **6**

   c) Write expressions for time required for a pipe line with K stages to execute n instructions and relative speed up. Explain briefly assumptions made in these expressions. **6**

6. a) Draw and explain data flow diagram for the following : **8**

      i) Fetch cycle

      ii) Indirect cycle

      iii) Interrupt cycle.

   b) Explain RISC pipeline in detail. **6**

   c) What is addressing mode ? Explain at least six addressing mode supported by a typical processor. **6**

MODULE – IV

7. a) Differentiate between :
   i) Instruction level parallelism and machine level parallelism.
   ii) Super scalar and super pipe lined.
   iii) Horizontal and vertical micro instruction. **6**

   b) With the help of a neat diagram how the control unit interacts with other elements of the processor. **8**

   c) Briefly explain hardwired implementation of control unit. **6**

8. a) Explain in briefly. functioning of microprogrammed control unit. **8**

   b) With the help of a neat diagram, discuss the single address microinstructions sequencing technique. **6**

   c) Explain software and hardware cache coherent schemes. **6**