[Total No. of Questions : 8]

S.E. (Comp.) (Semester - IV) Examination, May/June 2011
COMPUTER ORGANIZATION

Duration : 3 Hours **Total Marks : 100**

Instructions : 1) Answer five full questions atleast one full question from each module.
2) Make suitable assumptions wherever necessary.

Module - I

Q1) a) List and briefly define the possible states that define an instruction execution. **[5]**

b) A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2k bytes of RAM, 4k bytes of ROM and 4 interface units each with 4 registers. A memory mapped I/O configuration is used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers. **[8]**

i) How many RAM and ROM chips are needed?

ii) Draw the memory address map for the system.

iii) Give the address range in hexadecimal for RAM, ROM and interface.

c) Describe in words and by means of a block diagram how multiple matched words can be read out from an associative memory. **[7]**

Q2) a) A set associative cache has a block size of four 16 bit words and a set size of 2. the cache can accomodate a total of 4096 words. The main memory size that is cachable is 64K × 32 bits. Design the cache structure and show how the processors addresses are interpreted. **[8]**

b) Compare the multiple bus architecture to a single bus architecture. **[6]**

c) In the context of RAID, what is the distinction between parallel access and independent access. **[6]**

Module - II

Q3) a) Draw the flowchart for Booth's multiplication algorithm and explain. **[7]**

b) Explain programmed I/O data transfer technique. **[7]**

c) Express the following numbers in IEEE 32 bit floating point format **[6]**

i) −5 ii) 384

P.T.O.

Q4) a) Show the contents of registers E, A, Q and SC during the process of division of 10100011 by 1011. Use a dividend of 8 bits. **[8]**

b) What are the major functions of an I/O module? **[6]**

c) What is the benefit of using biased representation for the exponent portion of a floating point number? **[3]**

d) When a device interrupt occurs, how does the processor determine which device issued the interrupt. **[3]**

Module - III

Q5) a) Explain the BIU of 8086. **[4]**

b) Write the one, two and three address instructions that could be used to compute. $Y = (A - B) \div (C + D * E)$ **[6]**

c) What is meant by data dependency? Explain any two methods which can be used to handle data dependency conflicts in a pipeline. **[6]**

d) Compare the characteristics of RISC and CISC. **[4]**

Q6) a) Explain the following instructions of 8086 with examples. **[4]**

i) CWD ii) MOVSB

b) Explain the indirect cycle of the instruction cycle. Also show the flow of data during this cycle. **[6]**

c) Explain the concept of overlapped register windows in RISC. **[6]**

d) What is the difference between arithmetic shift and logical shift? **[4]**

Module - IV

Q7) a) What is the essential characteristic of the superscalar approach to processor design? **[5]**

b) How does the control unit interact with the other elements of the CPU. Explain with a block diagram. **[6]**

c) List and briefly define three types of computer system organization. **[6]**

d) Briefly define : antidependency. **[3]**

Q8) a) What is the distinction between instruction level parallelism and machine parallelism? **[6]**

b) Write the sequence of micro-operations for each of the following cycles. **[6]**

i) Fetch ii) Interrupt.

c) Bring out the differences between software and hardware cache coherent schemes. **[5]**

d) What is the typical sequence in the execution of horizontal microinstruction. **[3]**