



SEM 2 – 5 (RC 07 – 08)

F.E. (Semester – II) Examination, Nov./Dec. 2013

(Revised in 2007-08)

BASIC ELECTRONIC ENGINEERING

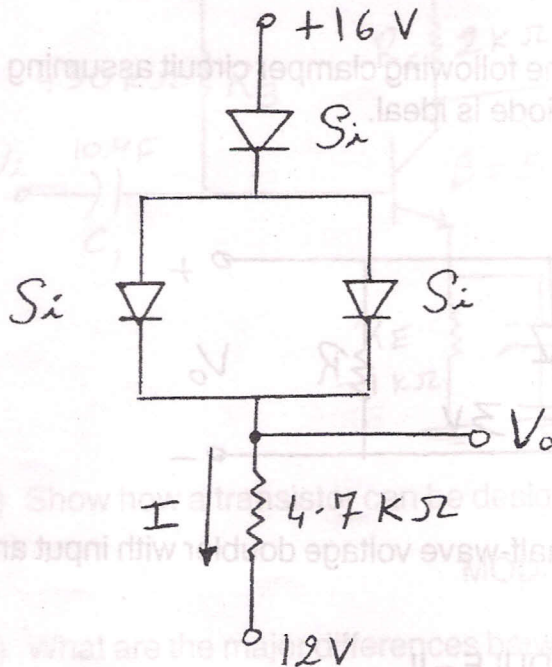
Duration : 3 Hours

Total Marks : 100

- Instructions:**
- 1) Answer **five** questions, choosing at least **one** from **each** Module.
 - 2) **Assume** any additional data, if required.
 - 3) **Graph** papers will be provided on request.

MODULE – I

1. a) Draw a reverse-biased pn junction and explain the following terms : 6
 - i) Potential barrier
 - ii) Reverse saturation current.
- b) Explain the three diode equivalent circuits along with their V-I characteristics. 6
- c) Find V_o and I for the given network. 2

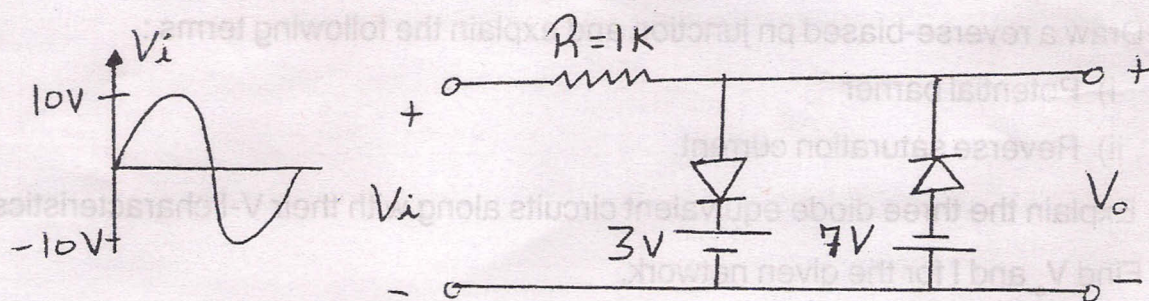


- d) Derive the ripple factor for a center-tapped full wave rectifier. 6

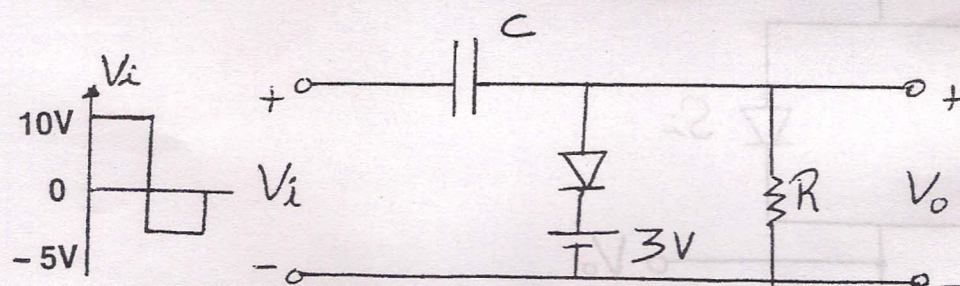
P.T.O.



2. a) A bridge rectifier uses load resistor $R_L = 2k\Omega$. Each diode has a slope resistance $R_f = 10\Omega$. Input voltage V_i in each half cycle has amplitude of 20 Volts and frequency is 50 Hz. Calculate :
- Peak, dc and rms values of load current.
 - dc output voltage.
- b) Why is a filter required in a dc power supply ? Draw the circuit of a C-filter and the output waveform.
- c) Analyze and draw the output waveform for the following biased parallel clipper. Assume ideal diodes.



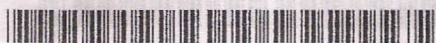
- d) Determine the output waveform for the following clamper circuit assuming RC time constant is very large and diode is ideal.



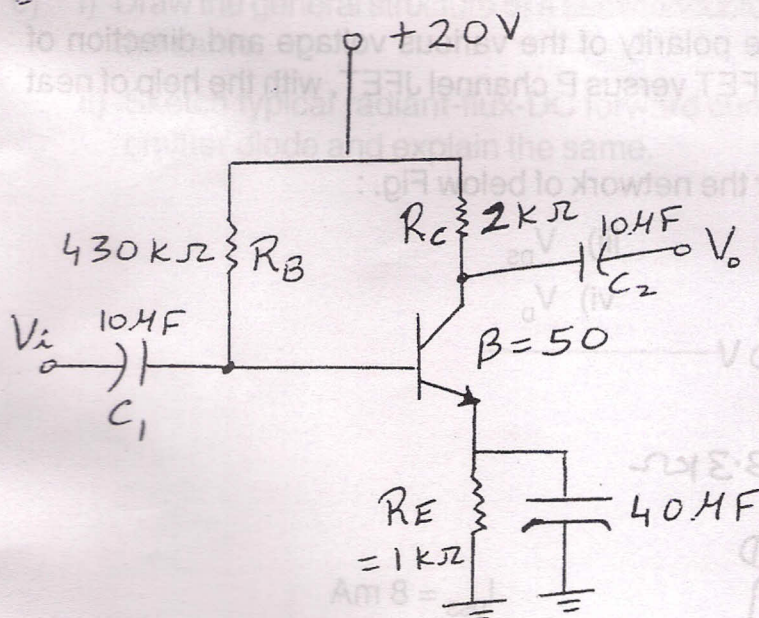
- e) Draw and explain the operation of a half-wave voltage doubler with input and output waveforms.

MODULE – II

3. a) Derive the relationship between the leakage currents in the Common Base (CB) and Common Emitter (CE) transistors.



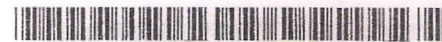
- b) Draw the circuit setup and explain how the static output characteristics of CB (npn) transistor are plotted. 10
- c) Explain how a CE transistor can be used as an amplifier. 6
4. a) i) Explain the parameters to which the collector current of a transistor is sensitive to. 10
- ii) Derive the stability Factor $S(I_{CO})$ for a fixed bias circuit. 8
- b) For the given emitter bias network, determine 8
- a) I_B b) I_C
- c) V_{CE} d) V_C
- e) V_E f) V_B
- g) V_{BC} h) I_{Csat}



- c) Show how a transistor can be designed to operate as a switch. 4

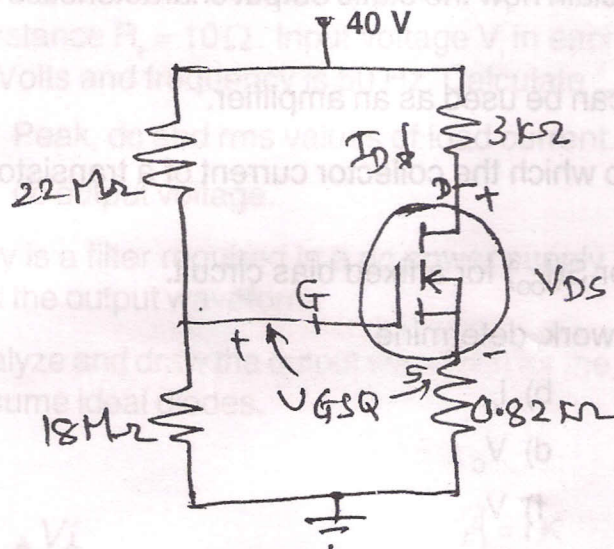
MODULE - III

5. a) What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does I_C react to increasing level of I_B versus change in I_D to increasingly negative value of V_{GS} ? 7



- b) Determine I_{DQ} , V_{GSQ} and V_{DS} for the network of Fig. given below :

7



for 2N4351

$$V_{GS(TH)} = 5V$$

$$I_{D(ON)} = 3mA$$

$$@ V_{GS(ON)} = 10V$$

- c) A p-channel JFET has device parameters of $I_{DSS} = 7.5mA$ and $V_P = 4V$. Sketch the transfer characteristics.

6

6. a) In general comment on the polarity of the various voltage and direction of currents for an n-channel JFET versus P channel JFET, with the help of neat labelled sketches.

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- b) Determine the following for the network of below Fig. :

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i) V_{GSQ}

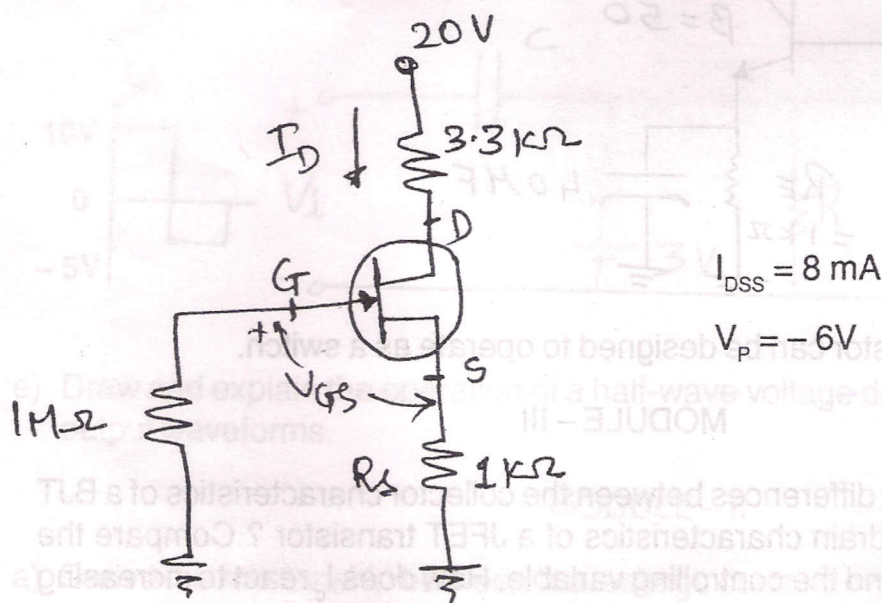
ii) I_{DQ}

iii) V_{DS}

iv) V_S

v) V_G

vi) V_D



- c) Write short note on CMOS Inverter.

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MODULE – IV

7. a) Explain the various steps involved in the fabrication of monolithic ICs. 10
- b) Draw a Wein bridge oscillator and write the expression for the frequency of oscillation. 3
- c) Sketch the typical illumination characteristics of a photodiode and explain the operation of the device. 7
8. a) Sketch the construction of a silicon controlled rectifier. Also, sketch the two-transistor equivalent circuit and show how it is derived from SCR construction. Label all terminals and explain how the device operates. 7
- b) Explain with the help of a block diagram, the trigger operation of a CRO. 7
- c) i) Draw the general structure of a semiconductor IR Emitter Diode and explain the same. 6
- ii) Sketch typical radiant-flux-DC forward current characteristics for an IR emitter diode and explain the same.