COMP 3 – 6 (RC)

S.E. (Computer Engineering) (Semester – III) (RC) Examination, November/December 2015
INTEGRATED ELECTRONICS

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any five** questions, attempt atleast **one** question from **each** Module.*
*2) Draw **neat** diagrams if **required**.*
*3) Assume suitable data if **necessary**.*
*4) Write description for the questions based on the marks **allotted**.*

MODULE – I

1. a) What is the CMRR of an ideal Op-Amp ? 2

   b) Draw and explain block diagram of a instrumentation system and name 2 instrumentation Op-Amp IC's. 7

   c) Draw the block schematic of an Op-Amp and explain the function of each block. 5

   d) Derive output voltage for differentiator with its circuit diagram. 6

2. a) Draw and explain integrator circuit and draw necessary waveforms. What do you mean by 'practical integrator' ? 7

   b) What is a feedback ? List 2 types of feedback. Which type is used in linear applications ? Give block diagram representation of current series and voltage shunt feedback. 6

   c) With the help of relevant circuit diagram, explain the working of Op-Amp inverting amplifier. Derive expression for voltage gain, input and output resistance. 7

P.T.O.

MODULE – II

3. a) Explain what is meant by 4

   a) Capture range

   b) Lock range of a PLL.

   b) Explain the working of timer 555 in monostable mode. Draw the circuit and derive necessary equations. 8

   c) Give pin description of LM 105 with its block diagram. 8

4. a) With a neat diagram and relevant waveforms, explain the working of a free running multivibrator using IC 555. Obtain the expression for the time period. 7

   b) Explain how timer 555 can be used as a frequency divider and pulse stretcher. 7

   c) Design a voltage regulator using IC 723 for the following specifications : 6

   Vo = 5V, Io = 50 mA, Vin = 12 V, Isc = 75 mA, Vsense = 0.65 V.

MODULE – III

5. a) Explain with a neat circuit diagram working of CMOS Nand gate. List some characteristics of CMOS circuit. 6

   b) Explain why DCTL is not popular in IC technology, although it is simpler than RTL. 6

   c) Draw a neat diagram of 3-input HTL Nand gate driving N similar gates. Explain the working operation of the circuit. Describe its various characteristics, which are related to its better performance. 8

6. a) Explain the working of 2 input DTL Nand gate and draw the circuit for 3 input modified DTL gate. 6

   b) Draw the circuit diagram of 2 input TTL Nand gate and explain its operation clearly stating the conditions of the transistors in the circuit for all possible input combinations. 8

   c) List the characteristics of CMOS and name the types in bipolar and unipolar logic families. 6

MODULE – IV

7. a) Discuss the advantages and disadvantages of R-2R ladder over binary weighted resistor DAC. 5

   b) Explain the voltage to frequency converter and derive the necessary expressions. 5

   c) Draw the circuit diagram of weighted-resistor D/A converter and give uses of A/D and D/A converters. 8

   d) State the advantages of Dual Slope A/D converter. 2

8. a) A D/A converter has a full scale analog output of 10 V and accepts 6 binary bits as input. Find the voltage corresponding to each analog step. 4

   b) Draw the circuit of an 8 bit R-2R Binary ladder. Explain its working as a digital to analog converter. If the logic levels are given by 5 V and 0 V for logic one and logic zero respectively, calculate the output voltage when the input is 00100000 ? 10

   c) Define the following terms : 6

      i) Monotonicity

      ii) Settling time

      iii) Linearity error.
