9.6.14 Repeat 14

COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) (Revised Course) Examination, May/June 2014
COMPUTER HARDWARE DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : *i) Answer **five** questions, at least **one full** question from **each** Module.*
*ii) Make suitable assumptions, **wherever** necessary.*

MODULE – I

1. a) Give the behavioural VHDL description of a D flip flop. **6**

   b) Explain :

      i) Two address instruction format of RIC.

      ii) Branch instruction format of RIC. **6**

   c) Suppose that the transfer AR ← AR [2], AR [0 : 1] is to be accomplished if the control signal CSL1 is 1 and AR ← AR [1 : 2], AR [0] is to be accomplished if CSL2 = 1. Construct a logic block diagram of the input network for the register AR that will provide for both these transfers. **8**

2. a) Construct a detailed logic network diagram of the digital circuit described by the following AHPL description. Include both the data section and the control section and use the one flip flop per control state approach.

   MODULE : ABC

   INPUTS : x ; a

   OUTPUTS : z

   MEMORY : r

   1) $\rightarrow (a, \bar{a})/(1, 2)$

   2) $r \leftarrow ((x \wedge r \,!\, x) \cdot (a, \bar{a})$

   3) $z = r ; r \cdot a \leftarrow x$;

      $\rightarrow (1)$

   END. **8**

P.T.O.

b) Describe in brief any three of the basic building blocks used in hardware circuits. 6

c) Write the sequence of AHPL steps to describe a system that receives a vector X and makes it available as an output after a delay, subject to the control of input signals a and b. If a = b = 0, the vector is not transferred. If a = 0 and b = 1, the vector is transferred without modification. If a = 1, the vector is first rotated, one place right if b = 0, two places right if b = 1. 6

MODULE – II

3. a) Write combinational logic unit description of n-bit ripple carry adder. 6

b) Draw and explain the flowchart to implement the fetch sequence of 16 bit instructions. 6

c) Tabulate the transfer connection list for the control unit resulting from the following AHPL control sequence.

1) $A \leftarrow INC(A)$

2) $\rightarrow (A[0] \wedge A[1] \wedge A[2])/(1)$

3) NO DELAY

$\rightarrow (A[3] \vee A[4])/(6)$

4) NO DELAY

$B \leftarrow \overline{A}$

5) $B \leftarrow (INC(B)\ !\ 8\ T\ 0) * (x, \overline{x})$;

$\rightarrow (B[0])/(5)$

6) $B \leftarrow \overline{B}$;

$\rightarrow (1)$. 8

4. a) Explain the different forms of connection statements in RIC. 6

b) Suppose an addressing mode, specified by IR [5 : 7] = 111, and calling for indexing, before indirect addressing is added to RIC. Modify steps 1 through 11 of the RIC control sequence accordingly. 8

c) Using the format of the branch instruction, code the 32 bit branch instruction that would be generated by the assembler for each of the following. Each number preceeded by $ is a relative address in hexadecimal.

i) BLE $ 9

ii) BGE $ 00FF

iii) BGT $ 2. **6**

MODULE – III

5. a) Explain the following with reference to the microprogrammable RIC.

i) Format of Branch instructions.

ii) Format of transfer instructions. **8**

b) Explain the carry look ahead principle with a neat logic diagram. **6**

c) Explain signed multiplication with the help of flowchart. **6**

6. a) Write an AHPL description of the RIC microsequencer and explain. **6**

b) Write the AHPL description of a 64 bit carry look ahead adder. **8**

c) Explain the hardware organization of floating point coprocessor with a neat diagram. **6**

MODULE – IV

7. a) Explain n-well process to CMOS fabrication with neat diagrams. **8**

b) Explain the working of nMOS enhancement mode transistor with neat diagram. **6**

c) Determine the pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors. **6**

8. a) Design CMOS logic gates for the following functions.

i) $Z = \overline{A.B.C.D}$

ii) three input OR gate. **8**

b) Derive the current voltage relationships for various bias conditions for a long channel MOSFET. Plot the characteristics. **8**

c) Define MOS transistor transconductance and output conductance. **4**