9/12/14 Repeat (RM) Comp

COMP 4 – 3 (RC)

S.E. (Computer) (Semester – IV) (RC) Examination, Nov./Dec. 2014
COMPUTER ORGANIZATION

Duration : 3 Hours

Total Marks : 100

Instructions : *1) Answer **any five** questions, at least **one** from **each** Module.*
*2) Make **suitable** assumptions, **wherever** necessary.*

MODULE – I

1. a) Explain top level view of computer components with the help of a neat diagram. 5
   b) Explain Direct Cache Mapping with an example. 6
   c) Write a short note on types of optical memories available. 5
   d) Differentiate between SRAM and DRAM with respect to speed, size and cost. 4

2. a) A two way set associative cache memory uses lines of 4 words each. The cache can accommodate a total of 3072 words. The main memory capacity of the system is 256 × 32. Find out how many bits are required in each field of main memory address ? 8
   b) Explain cache read operation. 5
   c) What is an instruction cycle ? Explain instruction cycle state diagram with interrupts. 7

MODULE – II

3. a) Why is I/O Module required to connect the peripheral devices to CPU ? 4
   b) Explain DMA data transfer technique with neat diagram. 8
   c) What is the benefit of using biased representation for the exponent portion of floating point number ? 4
   d) Express the following numbers in IEEE 32 – bit floating point format. 4
      i) –3.5
      ii) 1/32

P.T.O.

4. a) Draw the flowchart for division of signed magnitude numbers (restoration method) and explain it. 7

   b) Explain Interrupt Driven I/O with the help of flowchart. 7

   c) Perform the multiplication of (–4) × (6) using Booth's Algorithm. 6

MODULE – III

5. a) Explain the following terms : 6

      i) Resource Hazards

      ii) Data Transfer Instructions

   b) Explain the register organization in the processor. 6

   c) Write an 8086 program to find sum of even and odd numbers in an array. 4

   d) Explain the following addressing modes of 8086 : 4

      i) Direct

      ii) Indirect

6. a) Explain the concept of overlapping register window with the help of a diagram. 6

   b) What is instruction pipelining ? Explain with help of neat diagram a 6 stage pipeline. 6

   c) What are maskable and non-maskable interrupts ? 3

   d) What is graph coloring ? How is it used in compiler based register optimization in RISC ? 5

MODULE – IV

7. a) Explain the MESI protocol for multiprocessors. 8

   b) Explain how a control unit interacts with other elements of CPU with the help of neat block diagram. 6

   c) Explain the following terms : 6

      i) True data dependency

      ii) Output dependency

      iii) Instruction level parallelism.

8. a) With the help of neat timing diagram explain the following approaches : 10

   i) Superscalar

   ii) Super pipelined

   b) State and explain limitations of parallelism. 4

   c) Differentiate the following with respect to micro instructions : 6

   i) Direct v/s Indirect Encoding

   ii) Hard v/s Soft micro programming

   iii) Vertical v/s Horizontal micro instructions.