$i = I_s\left(e^{\frac{\eta V}{kT}} - 1\right)$

SEM 2 – 5 (RC 07-08)

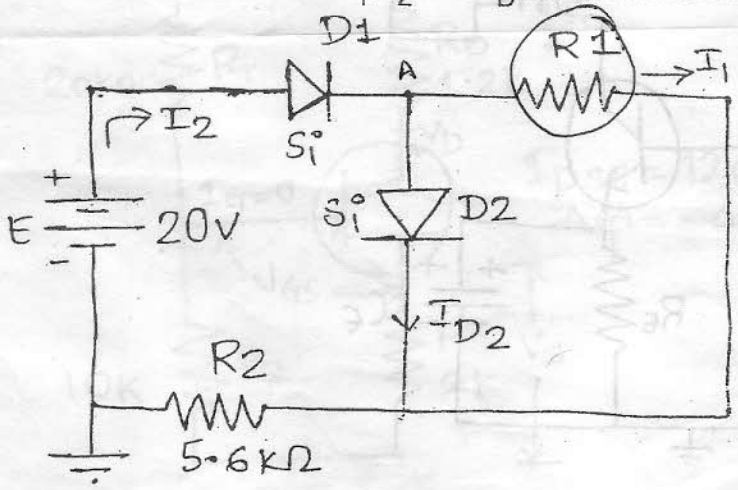
F.E. (Semester – II) Examination, November/December 2012
(Revised Course 2007-2008)
BASIC ELECTRONIC ENGINEERING

Duration : 3 Hours Total Marks : 100

Instructions : 1) *Answer* ***five*** *questions, choosing at least* ***one*** *from* ***each*** *Module.*
2) ***Assume*** *any additional data, if required.*

MODULE – I

1. a) Explain with circuit diagram the details of drawing the load line and finding the Q-point of operation on the diode characteristics 7
   b) Sketch a curve showing how the dynamic resistance of a silicon diode varies with the voltage across the diode, from 0V to 1V, without using the actual values for resistance. Indicate the cut-in voltage and explain its significance in determining diode resistance. 5
   c) In the reverse bias region the saturation current of a silicon diode is about 0.1 μ A (T = 20° C). Determine its approximate value if the temperature is increased to 40° C. 5
   d) The barrier potential developed across an open circuited PN junction aids the flow of minority carriers. Explain how this flow of charge is counter balanced. 3
2. a) Explain why it is necessary to use a voltage regulator circuit in the power supply. 6
   b) Show that the maximum rectification efficiency of a half wave rectifier is 40.6%. 6
   c) A zener diode is specified as having a breakdown voltage of 9.1 V with a maximum power dissipation of 364 mW. What is the maximum current the diode can handle ? 2
   d) Determine the currents I_1, I_2 and I_D for the network of figure below : 6



P.T.O.

MODULE – II

3. a) Using the two diode analogy explain why the base emitter junction has to be forward biased to provide collector current. If the base emitter junction is open, what current will flow and how is this designated ? 4

   b) Consider the transistor in the CB connection with zero emitter current. What is the designation used to describe the collector current under this condition and what effect would a reduction in temperature have on this current ? 4

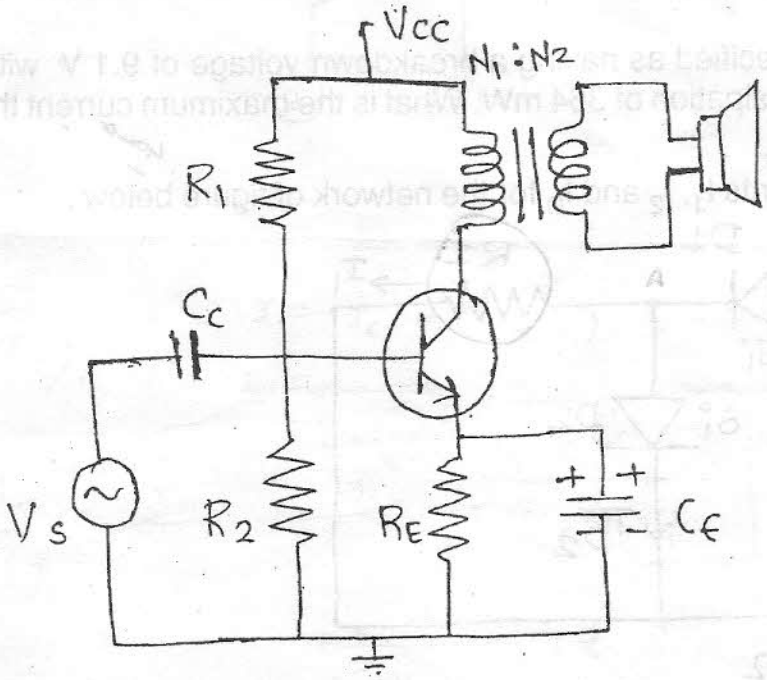
   c) What is the 'Early Effect' ? What does it account for in the transistor's characteristic curves ? 4

   d) Sketch typical CE input characteristics for an NPN transistor. Label all variables. Outline the procedure of calculating the input dynamic resistance of the transistor at a given point from these curves. 8

4. a) Explain graphically why operating point is not selected near the saturation region of transistor characteristics in a good voltage amplifier used for faithful amplification. 5

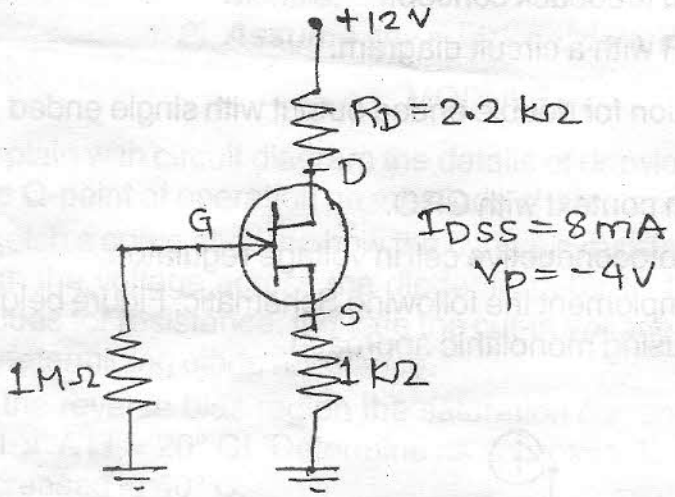
   b) What is the drawback of emitter bias ? What modification should be made if an emitter bias resistor is added to an unstabilized amplifier ? 8

   c) To set up a 100 mA of emitter current in the power amplifier circuit of figure shown below, calculate the value of resistor RE. Also calculate V_{CE}. The dc resistance of the primary of the output transformer is 20 Ω . Given that $R_1 = 200\ \Omega$, $R_2 = 100\ \Omega$, $R_c = 20\ \Omega$, $V_{CC} = 15$ V and $I_C = 0.1$ A. 7

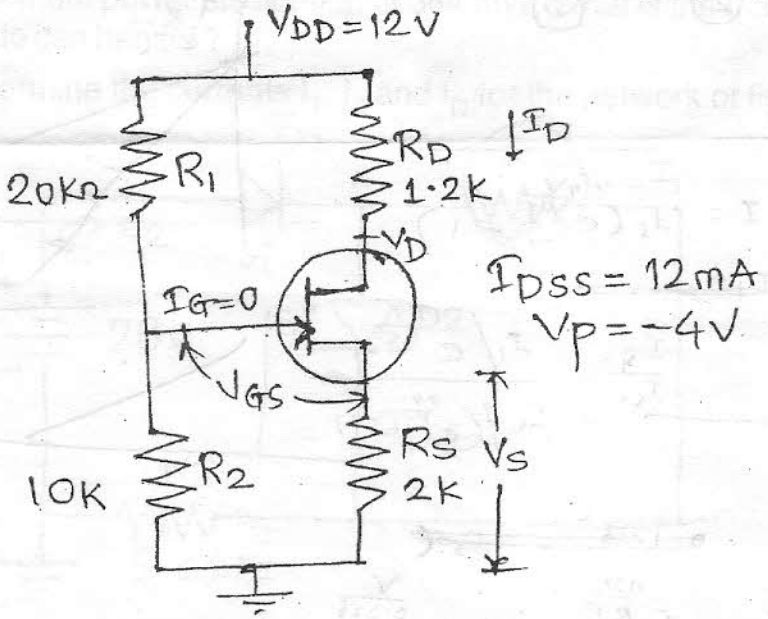


MODULE – III

5. a) Why FET is called as a voltage operated device ? 2
   b) Sketch a typical transfer characteristics for an n channel JFET and show how the transconductance gm can be derived from the transfer characteristics. 6
   c) Explain with the help of diagram the basic CMOS operation. 5
   d) For the circuit shown in the fig. below, calculate V_{GSQ}, I_{DQ}, V_{DS}, V_S and V_D. 7



6. a) i) What is meant by FET's 'Channel Ohmic Region' ?
   ii) Is the variation of drain resistance with gate voltage linear ?
   iii) What value of drain to source voltage should be used to obtain the effects in the channel Ohmic region ? 6
   b) Explain the voltage divider biasing arrangement for an n-channel enhancement MOSFET. 7
   c) For the circuit shown in figure below, calculate I_D, V_{GS}, V_G, V_{DS} and V_S. 7



MODULE IV

7. a) What are the relative advantages and disadvantages of an LCD display as compared to LED display ? 4

   b) A 1 cm by 2 cm, solar cell has a conversion efficiency of 9%. Determine the maximum power rating of the device. 3

   c) Explain with block diagram, a feedback concept. 6

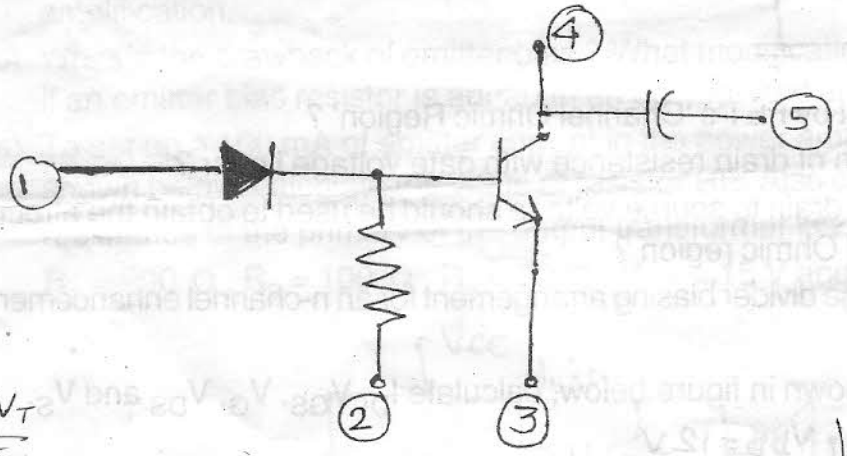
   d) Explain the operation of SCR with a circuit diagram. 7

8. a) Describe the OPAMP operation for double ended output with single ended input . 6

   b) Define the term 'triggering' in context with CRO. 2

   c) Explain the application of photoconductive cell in voltage regulator. 5

   d) Design the monolithic IC to implement the following Schematic. Figure below shows the circuit to be built using monolithic approach. 7



$\frac{\eta V_T}{I}$

$\frac{T_R}{k I_S}$

$\frac{T_R}{k(T_0 + I_S)}$.

$I = I_S\left(e^{\frac{\eta V}{RT}} - 1\right)$

$I + I_S$

$\frac{I_1}{I_2} = \frac{I_{S1}}{I_{S2}}$

$\frac{I_1 / e^{\frac{\eta V}{RT}} - 1}{I_2 / \left(e^{\frac{\eta V}{RT_2}} - 1\right)}$

$\frac{I}{I_S} - 1 = \frac{I + I_S}{I_S} = e^{\frac{\eta V}{RT}} = e^{\frac{V}{0.026}}$

$\frac{I_1}{I_S}$ =