[Total No. of Questions : 8]

T.E. (Comp.) (Semester - V) (RC) Examination, Nov./Dec. - 2011

COMPUTER HARDWARE DESIGN

Duration : 3 Hours **Total Marks : 100**

Instructions : 1) Answer any five questions. Atleast one from question each module.

2) Assume suitable data, necessary.

MODULE - I

Q1) a) Draw and explain shift/rotate instruction format. Also draw and explain seven distinct shift/rotate operations. **[10]**

b) Write short notes on the following: **[4]**

i) Logic elements.

ii) Speed, Delay and tanout in logic circuits.

c) Consider AR register of 4-bits. Assume only one control signal is 1 at a time. **[6]**

AR = set when CSL 1 = 1

AR = cleared when CSL 2 = 1

AR ← BR when CSL 3 = 1

Draw the logic block diagram for the above problem.

Q2) a) Construct the logic block diagram of hardware associated with register AR providing for the accomplishment of either of the transfers. **[8]**

$AR \leftarrow \overline{AR}$

$AR \leftarrow BR$

Given the proper signal. Both AR and BR are 4-bit registors.

b) Explain the concept of Inter System Busing. With the help of neat diagram, explain the two approaches to intersystem bus wiring. **[8]**

c) Write short notes on the following: **[4]**

i) Sequential Access storage.

ii) Direct Access storage.

P.T.O.

MODULE - II

Q3) a) Write combinational logic unit description of n-bit ripple carry adder. [8]

b) Explain how a communication bus is implemented using wired NOR logic. [4]

c) Given that U = (1, 1, 1, 0); V = (1, 0, 0, 1) W = (1, 0, 1) [8]

$$N = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}; \quad x = 5; \quad a = 1$$

find i) $U \oplus V$ ii) $U \wedge x$

iii) $\oplus / W$ iv) U ! V

v) U, V vi) (x < a)

vii) $\oplus$ // N viii) 8 T 1

Q4) a) Draw the flow chart for the fetch sequence for 16-bit instructions and explain. [6]

b) Write the AHPL steps for fetch and Address cycles in the design of control unit for RIC. [8]

c) Give the flowchart for compiling of data network and explain. [6]

MODULE - III

Q5) a) Explain the following with reference to microprogrammable RIC [6]

i) Addressing modes

ii) Format for Transfer microinstruction

b) Draw and explain the flowchart for the multiplication of two floating point numbers. [7]

c) Write an AHPL description of the RIC microsequencer and explain. [7]

Q6) a) With a neat diagram explain carry look a-head principle. [7]

b) With the help of flowchart explain signed multiplication. [8]

c) Write a note on Microcoding. [5]

MODULE - IV

Q7) a) Derive the current -voltage relationships for the various bias conditions for a long channel MOSFET. Plot the characteristics. **[8]**

b) With neat diagram explain nMOS fabrication process. **[8]**

c) What is the role of SiO_2 in IC fabrication. **[4]**

Q8) a) What are masks? How are they used? list the masks used in NMOS fabrication. **[6]**

b) Design CMOS logic gates for **[8]**

i) 3 - input OR gate

ii) $Z = \overline{A \cdot B \cdot C \cdot D}$

c) Explain the nMOS and CMOS design styles. **[6]**

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