COMP 4 – 3 (RC)

S.E. (Computers) (Semester – IV) Examination, Nov./Dec. 2012
COMPUTER ORGANIZATION (RC)

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any five** questions selecting at least **one** question from **each** Module.*
*2) Make necessary assumptions **if required**.*
*3) **Draw** diagrams **wherever** necessary.*

MODULE – I

1. a) Draw and explain the steps involved in instruction cycle state diagram. 7
   b) Explain the construction of magnetic disk with help of diagram. 6
   c) What is cache mapping ? Why is it required ? Explain set associative cache mapping with an example. 7

2. a) A computer uses RAM chips of 1024 × 1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes ? 8
   Explain in words how chips are connected to address bus ? Support your answer with memory address map and interconnection diagram.
   b) List and discuss features of various semiconductor memories w.r.t. category, erasure, write mechanism and volatility. 8
   c) What is a bus ? Explain the structure of a bus. 4

MODULE – II

3. a) Why is I/O module required to connect peripheral devices to CPU ? Draw a block diagram to describe the I/O module structure. 8
   b) Distinguish between Isolated I/O and memory mapped I/O. 4
   c) Express the following numbers in IEEE 32 bit floating pt format. 4
      i) 0.5 ii) – 5.0
   d) What is sign extension rule for 2's complement numbers and how can you form an integer in 2's complement representation ? 4

4. a) Draw and explain Booth's algorithm for multiplication of signed two's complement number. Given x = 4 and y = – 6 ; compute the product p = x • y with Booth's algorithm. 8

P.T.O.

b) What is interrupt driver I/O ? Why is it preferred over programmed I/O ? Explain in detail. 8

c) List and explain functions of DMA. 4

MODULE – III

5. a) Write one, two and three address instructions that could compute : $y = (A + B) * (C + D) + E$. 6

b) List the important characteristics of RISC machines. 4

c) Explain the interrupt cycle of the instruction cycle. Also show the flow of data during this cycle. 6

d) Explain RISC pipelining. 4

6. a) Draw and explain the dataflow diagrams for the following cycles. 6
   i) Fetch cycle
   ii) Indirect cycle.

b) Explain the register organization of CPU. 5

c) Why are transfer of control operations required in an instruction set ? Explain. 5

d) What do you mean by compiler based register optimization in RISC ? Explain. 4

MODULE – IV

7. a) What is the overall function of a Processor's control unit ? 6

b) List and briefly explain the different types of computer system organization. 8

c) What is the essential characteristics of the superscalar approach to processor design ? 6

8. a) Define Micro-operations. Explain the following with the help of micro-operations : 8
   i) Fetch cycle
   ii) Indirect cycle
   iii) Interrupt cycle.

b) What is the meaning of each of the four states in the MESI protocol ? 6

c) Differentiate and w.r.t. micro instructions : 6
   i) Direct v/s indirect encoding
   ii) Vertical v/s Horizontal micro instructions
   iii) Hard v/s soft micro programming.