COMP 3 – 5 (RC)

S.E. (Comp.) (Semester – III) (RC) Examination, November/December 2015
LOGIC DESIGN

Duration : 3 Hours | Total Marks : 100

Instruction : *Answer **any five** questions by selecting atleast **one** from **each** Module.*

MODULE – I

1. a) Perform the following number conversion. **6**
   i) $(101011101)_2 \rightarrow$ grey
   ii) $(247.75)_{10} \rightarrow$ hexadecimal
   iii) $(3A \,.\, 2F)_{16} \rightarrow$ Decimal.

   b) Prove the following using Boolean algebraic theorems. **5**
   $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = AB + BC + CA$

   c) Draw the logic diagram and construct the truth table for the following expression **4**
   $X = A + B + \overline{CD}$.

   d) What are self complementing codes ? Write two self complementing codes. **5**

2. a) Realize the expression. **4**
   $(A + C)(A + \overline{D})(A + B + \overline{C})$
   Using NOR gates only (2 inputs).

   b) Determine the single error correcting code for the binary data 1011 using even parity. **5**

   c) For positive to negative logic system, what does an OR gate become and what does an AND gate become. **4**

   d) Obtain the minimal sum of the product for the function
   $F(A, B, C, D) = \sum(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ by Quine Mcclusky method. **7**

MODULE – II

3. a) What are combinational circuits ? Explain working of a full subtracter using suitable diagram, k-map and truth tables. **7**

   b) Construct a 16 to 1 line multiplexer using only 2 to 1 line multiplexers. **7**

   c) What master slave JK flip flop ? Explain why master slave flip flop is called a pulse triggered flip flop. **6**

P.T.O.

4. a) Explain working of parallel adder. What are advantages and disadvantages over serial adder. 7

b) Design a 2 bit comparator. List all possible combinations and comparison support for your answer with a logic circuit. 6

c) What is the difference between an excitation table and truth table of a flipflop ? Give example. 4

d) Explain the advantages of edge triggered flip flop over level triggered flipflop. 3

MODULE – III

5. a) Explain the working of a serial in parallel out shift register with logic diagram and waveforms. 8

b) Compare synchronous counter and asynchronous counter. Give examples with logic diagrams. 6

c) With a neat diagram, explain the operation of a ling counter. Also sketch output waveform. 6

6. a) Explain how counter can be used as frequency divider. 6

b) Design a 3 bit up/down counter which counts VP when the control signal m = 1 and counts down when m = 0. 7

c) Design a mod-7 counter with asynchronous inputs for an up operation. Draw the output waveforms. 7

MODULE – IV

7. a) Explain the steps involved in design procedure for synchronous sequential circuits. 7

b) A sequential circuit has 3 D-flip flops A, B, C and one input X. It is described by following flip flop input function 8

$DA = (BC' + B'C)X + (BC + B'C')X'$

$DB = A$

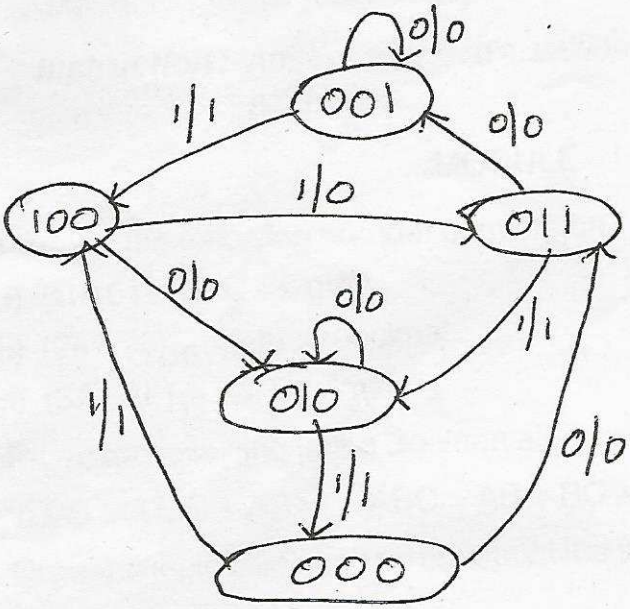
$DC = B$

i) Derive the state table for the circuit.

ii) Draw two state diagram one for X = 0 and other for X = 1.

c) Differentiate between PAL and FPAL. 5

8. a) Design a sequential circuit using SR flip flop. 8



b) What are finite state machines ? Explain state table, state diagram and excitation table of R-S flip flop. 6

c) Explain the architecture of PLA with the help of a block diagram. 6