

## T.E. (Comp.) Sem. – V (RC) Examination, May 2010 COMPUTER HARDWARE DESIGN

Duration: 3 Hours

Total Marks: 100

Instructions: i) Answer five questions, atleast one full question from each Module.

ii) Make suitable assumptions, wherever necessary.

## IOV bentw guizu belieu MODULE - I officialism more a work maly of the

 a) The design of a complex system such as a digital computer can be viewed at many different levels. Justify the statement with the characteristics of typical components recognized at each level.

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b) Explain the following instruction formats of RIC:

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- i) Two address instruction format
- ii) Shift/rotate instruction format.
- c) Determine a minimal expression for DAR [i] where AR must be the destination of the following four transfers.

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 $AR \leftarrow 0.0.0$ 

 $AR \leftarrow 1,1,1$ 

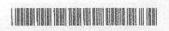
 $AR \leftarrow \overline{AR}$ 

 $AR \leftarrow BR$ 

 a) Construct a detailed logic block diagram of the hardware realization of both the control and data units specified by the following AHPL description, where a and b are flipflops, x is an input and z a single output line.

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- 1)  $a \leftarrow x \lor b$ ;
- (a)  $b \leftarrow x$ ; which will instruction of square FHA to compare and shift (decreases  $\rightarrow$  (a,  $\overline{a}$ ) | (1,3) property of resignment introduction of the first terms of the square of the s
  - 3)  $z = 1; b \leftarrow x \oplus b;$  $\rightarrow (1)$



b		Bring out the differences between direct access storage and sequential access storage in terms of hardware design.	6
c	:)	Briefly explain the two address instructions supported by RIC.	6
) Lya		MODULE-II	
3. a	1)	Write combinational logic unit description of an I bit incrementer.	8
ł	0)	Write the sequence of AHPL steps required to implement shift/rotate instruction.	8
(	2)	Explain how a communication bus is implemented using wired NOR logic.	4
4. 8	a)	Explain, how the control unit can be started again after executing a HLT command.	8
1	b)	Suppose a machine with exactly the same instruction set as RIC is to be designed and named RIC 16. RIC 16 will differ in that the memory data bus will consist of only 16 bits and the 24 bit address will address individual 16 bit words. Operands will usually consist of two consecutive words in memory. Jumps and branches to any 16 bit word are allowed in RIC 16. Rewrite the first 22 steps of the RIC control sequence transforming it into a sequence for RIC 16.	12
		MODULE - III a regular a production of the contract of the con	
5.	a)	Explain the following with reference to the microprogrammable RIC.  i) Instruction Format	6
		ii) Addressing modes	
	b)	Write AHPL description of a 64 bit carry look ahead adder.	8
	c)	With the help of a flowchart explain how floating point addition and subtraction is carried out.	6
6.	a)	With a neat block diagram explain the organization of microprogrammable RIC	. 8
	b)	Write the sequence of AHPL steps to implement division of fixed point quantitie	s. 8
	c)	Write combinational logic unit description for the propagate and generate section of the full adder circuit.	4



## MODULE-IV

7.	a)	Enumerate the steps in IC Fabrication.	8
	b)	Explain the working of a MOS Inverter with nMOS depletion type transistor as load. Draw the transfer characteristics.	8
	c)	What are masks? How are they used? List the masks used in nMOS fabrication process.	4
8.	. a)	List the advantages of CMOS Inverter.	3
	b)	Explain the structure and operation of the MOS transistor. Derive the expression for drain current.	1(
	c)	Explain the working of a Pass Transistor.	7

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