COMP 3 – 6 (RC)

S.E. (Comp.) (Sem. III) (RC) Examination, May 2010
INTEGRATED ELECTRONICS

Duration: 3 Hours Total Marks: 100

Instructions : 1) Answer 5 questions by selecting atleast one from each Module.
2) Answers to subquestions of a question should be written in continuation of each other.
3) Make suitable assumptions wherever necessary.

MODULE – 1

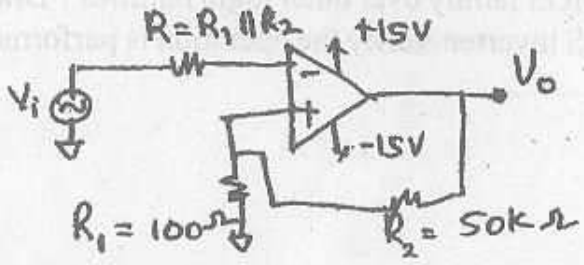
1. a) Define the following electrical parameters input offset voltage, input resistance CMRR and slew rate. 6

   b) What is a feedback ? List two types of feed back ? Which type is used in linear applications ? Give block diagram representation of current series and voltage shunt feedback. 6

   c) Draw the circuit diagram of an opamp configured in the inverting mode as a summing scaling and averaging amplifier. Derive an expression for the O/P. 8

2. a) With the help of a neat diagram, explain how opamp can be used as differentiator. Show the output wave forms for square and sine wave inputs and draw the frequency response. 8

   b) For the Schmitt trigger circuit shown below, find the upper and lower Trigger points if $R_1 = 100\Omega$, $R_2 = 50K\Omega$ and the supply voltages are +15V and – 15V. 4



   c) Draw and explain block diagram of a instrumentation system and name the IC number of its. 8

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MODULE – 2

3. a) Explain how IC 555 can be used as a astable multivibrator and obtain the expression for the frequency. 8

   b) Design a low voltage regulator for the following specifications. $V_0 = 5V$, $I_m = 50mA$, $V_{in} = 15V$, $T_A = 25°C$, $V_{sense} = 0.65V$. 4

   c) Explain the working of PLL and give one application with explanation. 8

4. a) Give pin description of LM105 with its block diagram. 8

   b) Explain the applications of mono stable multivibrator (any 2). Why it is called as one shot multivibrator ? 8

   c) Give basic principle of series voltage regulator. 4

MODULE – 3

5. a) Draw the circuit diagram to show how DCTL gates can be connected to perform the logic operation AND and NOT. 4

   b) Explain the following with respect to digital logic circuit.

      1) Noise margin
      2) Propagation time delay
      3) Current source logic. 5

   c) Draw the circuit diagram of 2 – input TTL NAND gate and explain its operation clearly stating the conditions of the transistors in the circuit for all possible input combinations. 8

   d) Compare the current spikes in ECL and TTL gates. 3

6. a) What are the advantages of CMOS family over other logic families ? Draw and explain the working of a CMOS inverter. Verify the operation is performed for all input combinations. 6

   b) Calculate :

      1) Noise margin
      2) Fanout
      3) Power-dissipation of HTL gate.

      Assume $h_{FE} = 40$

      Draw the circuit diagram of HTL gate. 6

c) Compare the following logic families :
   1) DTL
   2) HTL
   3) TTL
   4) ECL. **8**

MODULE – 4

7. a) Explain analog to digital converter using voltage to time conversion with suitable diagram. Mention its advantage and disadvantage. **8**

   b) Explain successive approximation type A/D converter and its advantages. **6**

   c) A D/A converter has a full scale analog output voltage of 10V and accepts six binary bits as input and find the voltage corresponding to each analog step. Explain in detail. **6**

8. a) A dual slope A/D converter has a resolution of 12 bits. If the clock rate is 100Hz, what is the maximum rate at which samples can be converted ? **4**

   b) Draw the circuit diagram and graph of output versus input of following converter
      1) Binary weighted resistor network
      2) R-2R resistor network.

      explain the working of R-2R DAC. **10**

   c) Define the following terms : **6**
      1) Monotonicity
      2) Settling time
      3) Linearity error.