COMP – 3-5 (RC 07-08)

S.E. (Comp) Semester – III (Revised 2007-2008) Examination, May 2009

LOGIC DESIGN

Duration : 3 Hours

Total Marks : 100

Instructions : 1) Answer five full questions, atleast one from each Module.

2) Make suitable assumptions, wherever necessary.

MODULE – I

1. a) Find the complement of the following boolean function and reduce it to a minimum number of literals $\overline{B}D + \overline{A}B\overline{C} + ACD + \overline{A}BC$. 4

b) For the following function find all of the prime implicants using Quine McCluskey procedure $f(p, q, r, s) = \Sigma m(1, 3, 7, 9, 12, 14, 15)$ 6

c) Represent the decimal number 9830 in

i) BCD

ii) Excess-3 code 4

d) Prove that

i) $AB + \overline{AC} + A\overline{B}C(AB + C) = 1$

ii) $AB + A(B + C) + B(B + C) = B + AC$ 6

2. a) Determine the single error correcting code for the information code 10110 for odd parity. 6

b) Find the minimum sum of products expression for the following function using K map $f(w, x, y, z) = \Sigma m(0, 1, 5, 8, 12, 14, 15) + \Sigma d(2, 7, 11)$. 6

c) Convert the following hexadecimal numbers to decimal

i) A08F . EA

ii) 2EB7 4

d) Realize EX-OR operation using only NOR gates. 4

P.T.O.

MODULE – II

3. a) Design the circuit of a 3 bit parity generator and the circuit of a 4 bit parity checker using an odd parity bit. 8

   b) What is meant by excitation table of a flip flop ? 2

   c) Construct a 16 to 1 line multiplexer using 2 to 1 line and 4 to 1 line multiplexers. 6

   d) Explain the operation of edge triggered S-R flip flop. 4

4. a) Draw the logic diagram of a 2 to 4 line decoder with only NOR gates. Include an enable input. 6

   b) What are the various methods used for triggering flip flop ? 4

   c) Realize the following boolean expression using an 8 to 1 line MUX, where w, x and y appear on select lines S_2, S_1 and S_0 respectively
   $f(w, x, y, z) = \Sigma m\,(2, 5, 6, 7, 9, 12, 13, 15)$. 6

   d) Convert J-K flip flop to S-R flip flop. 4

MODULE – III

5. a) Design a decade counter to count in excess 3 code sequence. Use minimum number of J-K flip flop.

   b) Discuss briefly different types of shift registers. 8

   c) How many clock periods are required to shift a 8 bit number in to 8 bit register ? Also show the waveform. 4

6. a) Design a 3 bit synchronous counter using S-R flip flops. 6

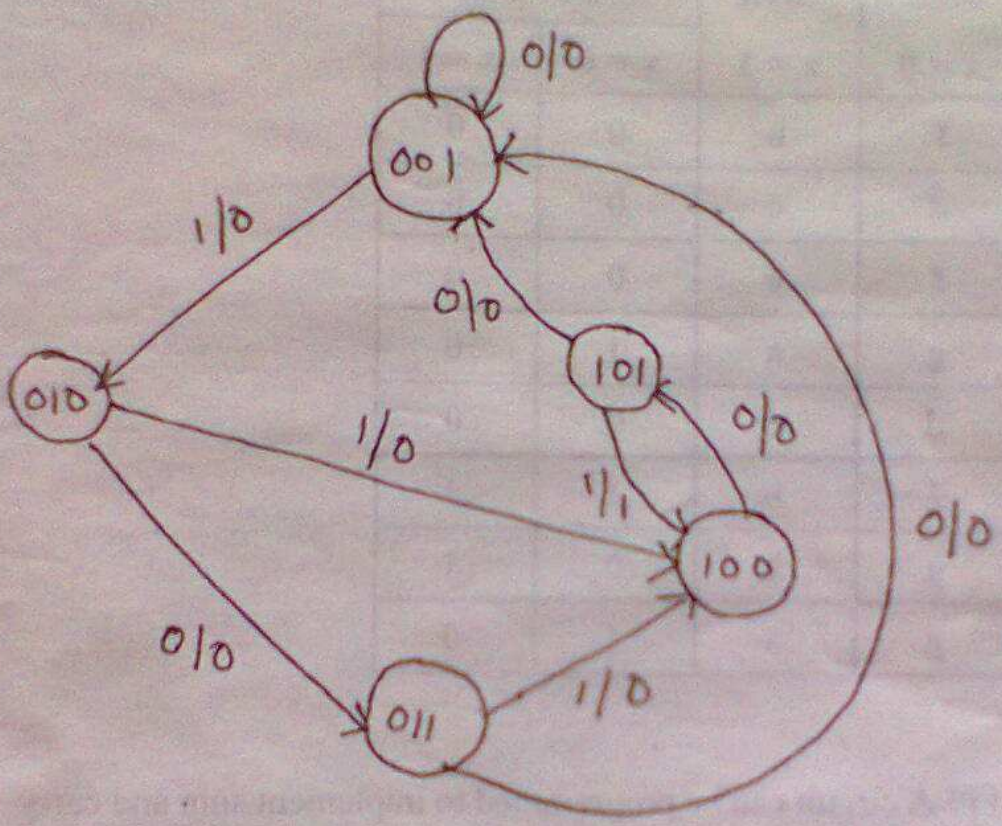
   b) Explain how counter can be used as frequency divider. 4

   c) Give some applications of shift registers. 4

   d) Explain the operation of a twisted ring counter and give its state diagram. 6

MODULE – IV

7. a) Design a sequential circuit for the following state diagram using R-S flip flops. 8



b) A sequential circuit has 3 D-flip flops A, B, C and one input x. It is described by following flip flop input function. 8

$DA = (BC' + B'C)x + (BC + B'C')x'$

$DB = A$

$DC = B$

i) Derive the state table for the circuit.

ii) Draw two state diagram one for x = 0 and other for x = 1.

c) Differentiate between PAL and FAPL. 4

8. a) Reduce the number of states in the following state table and tabulate reduced state table. 6

Present State	Next State		Out put	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	b	0	1
h	g	a	1	0

b) Show how FPLA circuit can be programmed to implement sum and carry output of a full adder. 6

c) What are advantages of

i) State diagram.

ii) State table. 2

d) Design a 3-bit counter which counts in the following sequence
0 – 2 – 5 – 3 – 4 – 0 → 2 6