17 - 6 - 2015

SEM 2-5 (RC 07-08)

F.E. (Semester – II) Examination, May/June 2015
(Revised in 2007-08)
BASIC ELECTRONICS ENGINEERING

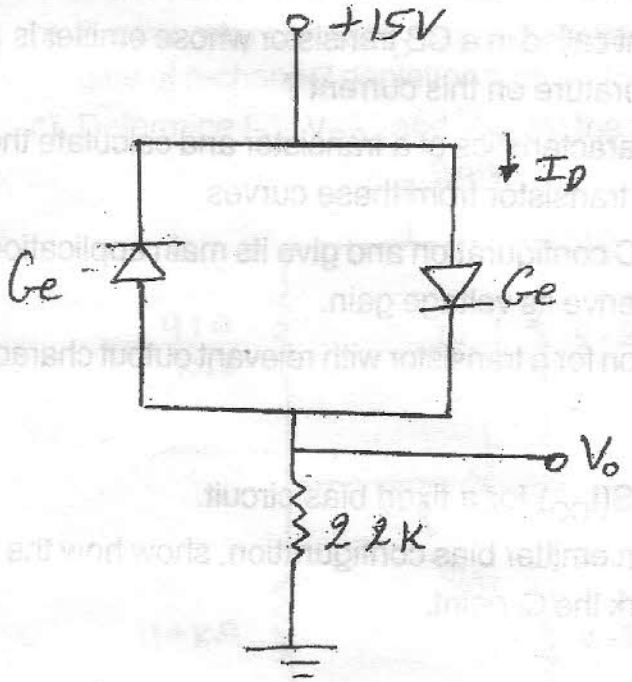
Duration : 3 Hours Total Marks : 100

Instructions : *1) Answer **any five** questions selecting atleast **one** from each Module.*
*2) Make **suitable** assumptions, **if** required.*

MODULE – I

1. a) Draw a reverse biased pn junction and explain the following terms :
   i) Knee voltage ii) PIV of a diode. **8**
   b) Draw the simplified equivalent circuit of a diode and its V-I characteristics. **2**
   c) Define and explain static and average resistances of a diode with the help of diagram. **4**
   d) Differentiate between Zener and Avalanche breakdowns. **6**

2. a) Find V_0 and I for the given circuit.



2

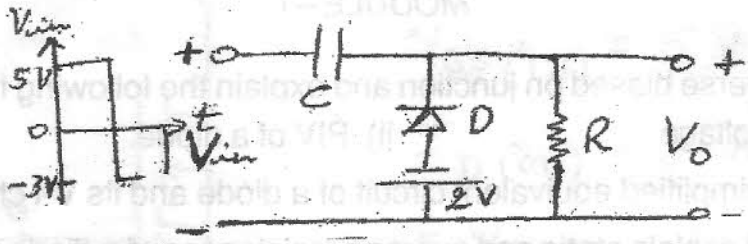
P.T.O.

b) Derive the TnF for a bridge rectifier and compare its value with that of a centre-tapped full wave rectifier. 5

c) Draw the circuit of C-filter (using fullwave rectifier) with the input and output waveforms. 2

d) A zener diode is specified as having a breakdown voltage of 9.1 V with a maximum power dissipation of 364 mW. What is the maximum current the diode can handle ? 2

e) Determine the output waveform for the following clamper circuit assuming ideal diode and large RC time constant. 5



f) Explain the operation of a full wave voltage doubler. 4

MODULE – II

3. a) Distinguish between the emitter, base and collector regions of a transistor. 3

b) What is the collector current called in a CB transistor whose emitter is open ? What is the effect of temperature on this current ? 2

c) Sketch typical CE input characteristics of a transistor and calculate the input dynamic resistance of the transistor from these curves. 4

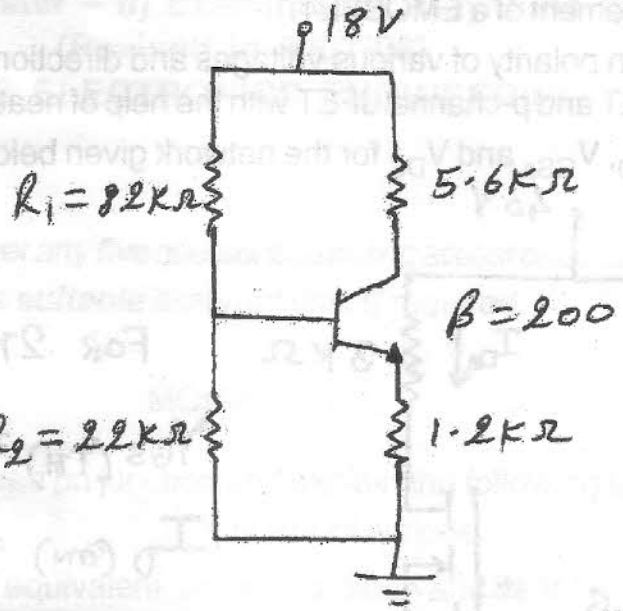
d) Draw a pnp transistor in CC configuration and give its main application. Also draw a CB amplifier and derive its voltage gain. 5

e) Explain the limits of operation for a transistor with relevant output characteristic sketch. 6

4. a) Derive the stability factor $S(I_{CO})$ for a fixed bias circuit. 4

b) By analyzing a transistor in emitter bias configuration, show how the load line can be drawn and mark the Q-point. 6

c) Determine the Q-point I_{CQ} and V_{CEQ} for the voltage divider configuration shown using the appropriate technique. 6



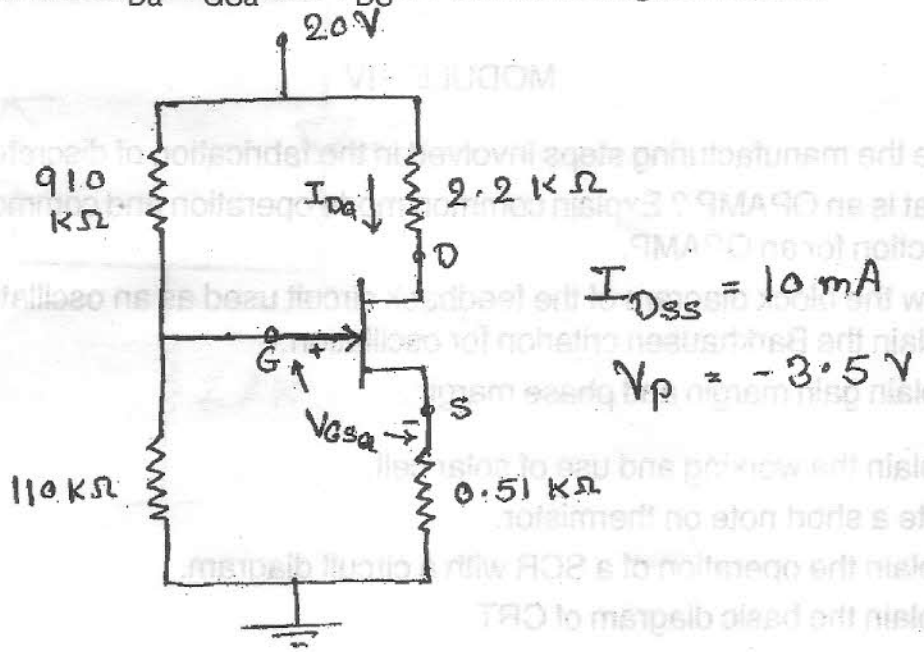
d) Show how a transistor can be designed as a switch. 4

MODULE – III

5. a) Draw and explain drain to source characteristics of n-channel JFET. Explain how can the transfer characteristics curves be obtained from output characteristics. 6

b) Explain why current I_D exceeds beyond I_{DSS} if positive voltage is applied at gate of n-channel depletion type MOSFET. 6

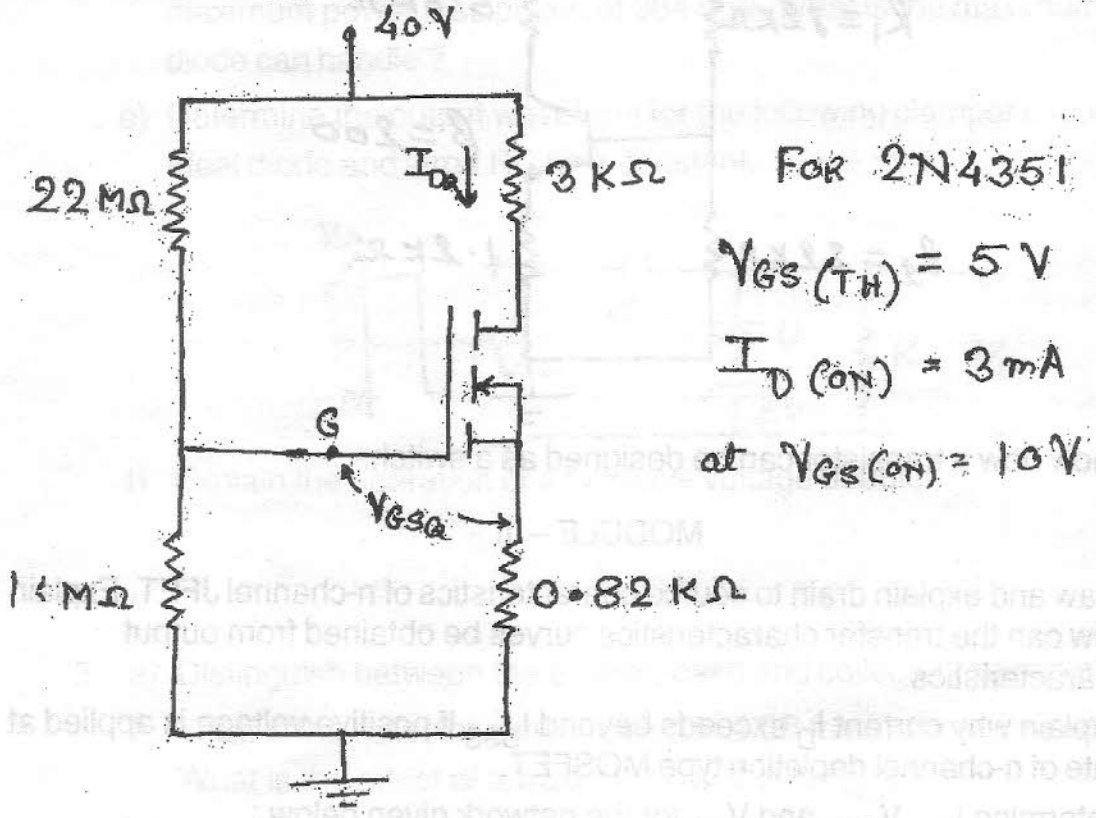
c) Determine I_{Da}, V_{GSa} and V_{DS} for the network given below : 8



6. a) With the help of a neat diagram and set of equations explain the feedback biasing arrangement of a EMOSFET. 6

   b) Write a note on polarity of various voltages and direction of current for n-channel JFET and p-channel JFET with the help of neat labelled sketches. 6

   c) Determine I_{DQ}, V_{GSa} and V_{DS} for the network given below : 8



MODULE – IV

7. a) Give the manufacturing steps involved in the fabrication of discrete diode. 5

   b) What is an OPAMP ? Explain common mode operation and common mode rejection for an OPAMP. 6

   c) Draw the block diagram of the feedback circuit used as an oscillator and explain the Barkhausen criterion for oscillation. 5

   d) Explain gain margin and phase margin. 4

8. a) Explain the working and use of solar cell. 5

   b) Write a short note on thermistor. 6

   c) Explain the operation of a SCR with a circuit diagram. 5

   d) Explain the basic diagram of CRT. 4