06-06-15 (M)

COMP 5 – 3 (RC)

T.E. Computer Engineering (RC) (Semester – V)
Examination, May/June 2015
MICROPROCESSORS AND MICROCONTROLLERS

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any five** questions, attempt atleast **one** question from **each** module.*
*2) Draw neat diagrams **if required**.*
*3) Assume suitable data **if necessary**.*
*4) Write description for the questions based on the marks **allowed**.*

MODULE – 1

1. a) Can we write the following instruction for 8086. Also state the reason for validity and invalidity. **6**
   i) MOV CX, AL
   ii) MOV DS, 003 AH
   iii) MOV BL, [BX]
   iv) MOV 434 [SI], DH
   v) MOV CS : [BX], DL
   vi) MOV DS, 437 AH.

   b) Explain any 3 addressing modes of 8086 processor with an example each. **6**

   c) Write notes on : **8**
   i) Procedures
   ii) Macros.

2. a) With a neat block diagram, explain the internal architecture of 8086 microprocessor. **8**

   b) Explain the use of the following instruction in 8086. Give example for each :
   i) SAR
   ii) LES
   iii) AAM
   iv) SAHF. **4**

P.T.O.

c) Write 8086 ALP using macros to swap two numbers. Add proper comments in the program. 6

d) What is the difference between SAR and SHR instruction ? 2

MODULE – II

3. a) Discuss bit definitions of control and status word of 8087. 8

b) Convert $(225.125)_{10}$ into short real, long real and temporary real representation used by the 8087. 4

c) What is I/O processor 8089 ? Describe the need of that processor in 8086 architecture. Explain with outline diagram. 8

4. a) Explain the architecture of the 8087 floating math co-processor with a neat diagram. Highlight the host processor-coprocessor interface. 12

b) Write 8087 program to prove the following identity $\text{Sin}^2\theta + \text{Cos}^2\theta = 1$. Add proper comments to explain the logic. 8

MODULE – III

5. a) Draw the interfacing diagram between 8086 CPU and 8255 with 8 LEDs and 8 SPDT switches. Also write a program in 8086 assembly language to read the switch status and display it on the LEDs. Add proper comments in the program. 7

b) Explain with neat block diagram the internal architecture of 8254 timer. 7

c) Explain the different modes of operation of 8255. 6

6. a) Discuss the organization and architecture of 8255 programmable peripheral interface IC with a functional block diagram. 10

b) Draw the block diagram of 8251 and explain in brief, how synchronous communication is different from asynchronous communication. 10

MODULE – IV

7. a) With the help of neat diagram explain interrupt enable register of 8051. **6**

   b) Explain addressing modes supported by 8051 with example. **6**

   c) It is required to interface two chips of 32 K x 80 ROM and four chips of 32 K x 8 RAM with 8086, according to the following memory map : **8**

   ROM 1 and 2 : F0000H – FFFFFH

   RAM 1 and 2 : D0000H – DFFFFH

   RAM 3 and 4 : E0000H – EFFFFH

8. a) Explain the following addressing modes of 8051. **8**

   i) Immediate

   ii) Register

   iii) Direct

   iv) Register indirect.

   b) Describe TCON and TMOD function registers. **6**

   c) Draw and explain all bits of flag register of 80286. **6**