10/12/14 Regular (T.E.) Comp

COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) (RC) Examination, Nov./Dec. 2014
COMPUTER HARDWARE DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : *i) Answer **5** questions atleast **one** question from **each** Module.*
*ii) Make **necessary** assumption.*

MODULE – I

1. a) Consider AR register of 4 bits. Assume only one control signal is 1 at a time. 6
AR = set When CSL 1 = 1
AR = Cleared when CSL 2 = 1
AR ← BR when CSL 3 = 1
Draw the logic block diagram for the above problem.

   b) Explain the following with respect to RIC : 6
      i) Two address instruction format
      ii) Shift/Rotate instruction format.

   c) Construct a control realization corresponding to the following AHPL sequence. 8

      i) $Z = X \vee A;$
      $\rightarrow (a, \bar{a} \wedge b, \bar{a} \wedge \bar{b})/(2,3,4)$

      ii) $A \leftarrow X;$
      $\rightarrow (1)$

      iii) $A \leftarrow X[1:3], X[0]$
      $\rightarrow (4)$

      iv) $A \leftarrow A[1:3], A[0]$
      $\rightarrow (1)$

2. a) Suppose that the transfer AR ← AR[2], AR [0 :1] is to be accomplished if the control signal CSL 1 is 1 and AR ← AR[1: 2], AR [0] is to be accomplished if CSL 2 = 1. Construct a logic block diagram of the input network for the register AR that will provide for both these transfers. 8

   b) Explain the concept of inter system b using with the help of neat diagram, explain the two approaches to inter system bus wiring. 6

   c) Describe the internal architecture of RIC system and explain the single address instruction format. 6

P.T.O.

MODULE – II

3. a) Given that u = (1, 1, 1, 0) v = (1, 0, 0, 1) w = (1, 0, 1)

$$N = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad x = 5,\ y = 3,\ z = -1.$$ 8

Find :

i) $u \oplus v$

ii) $\wedge / w$

iii) $(4T5) \oplus v$

iv) $(x < z)$

v) 8 T O

vi) N ! W

vii) v / / N

viii) u, v

b) Write a combinational logic unit description for a

i) Full Adder

ii) I-input decoder. 8

c) With neat diagram explain how the AC ← MD ∧ AC operation is executed in RIC. 4

4. a) Give flow chart for compiling of data network and explain. 6

b) Draw flow chart for fetch sequence for 16 bit instruction and explain. 6

c) Give the implementation of HLT using DEAD END. Also explain implementation of HLT by return to step 1. Support your answer with neat diagram. 8

MODULE – III

5. a) Explain the following with reference to the microprogrammable RIC. 8

i) Format of Branch instructions

ii) Format of transfer instructions.

b) Explain the carry look ahead principal with a neat logic diagram. 6

c) Draw flow chart for following point multiplication. 6

6. a) Write AHPL description of RIC sequences and explain. 6

   b) Write combinational logic unit description for the propagate and generate section of the full adder circuit. 6

   c) Write the sequence of AHPL steps to implement division of fixed point quantities. 8

MODULE – IV

7. a) Derive current voltage relationship for various bias condition for a long channel MOSFET. Plot characteristics. 8

   b) What are masks ? List masks used in nMOS fabrication process. 4

   c) What are the different approaches to CMOS fabrication. Explain the nwell CMOS fabrication process with neat diagrams. 8

8. a) Design CMOS logic gate for following function :

      i) $Z = \overline{A.B.C.D}$

      ii) $Z = (A \cdot B) + (C \cdot D)$. 8

   b) With the help of neat diagram explain nMOS fabrication process. 8

   c) Explain the working of pass transistor. 4