comp 28/11/16 Regular

COMP 5 – 4 (RC)

T.E. (Computer Engineering) (Semester – V) (RC) Examination, November/December 2016
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : *1) Answer **any five** questions, **atleast one full** question from **each** Module.*
*2) Draw **neat** diagrams **if required**.*
*3) Make suitable assumptions, **wherever** necessary.*

MODULE – I

1. a) Give the structural and behavioural VHDL description for full subtractor circuit. Draw the block diagram and also write the truth table. **6**

   b) Decode the following for the RIC machine : **6**

      i) 0101 01 0000 10 0001 where 0101 stands for ADD

      ii) 0010 01 0000 00 1111 where 0010 stands for MVT.

   c) Explain the various addressing modes used in RIC processor. **8**

2. a) The design of a complex system such as a digital computer can be viewed at many different levels. Justify the statement with the characteristics of typical components recognized at each level. **6**

   b) Explain the concept of inter system busing. With the help of a neat diagram, explain the two approaches to inter system bus wiring. **6**

   c) Suppose that the transfer AR ← AR [2], AR [0 : 1] is to be accomplished if the control signal CSL1 = 1 and AR ← AR [1 : 2], AR [0] is to be accomplished if the control signal CSL2 = 1. Construct a logic block diagram of the input network for the register AR that will provide for both these transfers. **8**

MODULE – II

3. a) Write the sequence of AHPL steps to execute the different branch commands of RIC. **8**

   b) With a neat diagram explain how the AC ← MD ∧ AC operation is executed in RIC. **4**

   c) Write a combinational logic unit description for a : **8**

      i) Full Adder ii) 1-input decoder.

P.T.O.

4. a) With the help of a neat flowchart explain the steps involved in the compilation of data network. 6

   b) With the help of a neat diagram explain the control signals and interconnections involved in the AND transfer. Also explain memory read and write operations for the RIC system. 6

   c) Write the sequence of AHPL steps required to implement shift/rotate instruction. 8

MODULE – III

5. a) Discuss the sequence of steps to implement signed multiplication. 7

   b) Write the micro coding sequence for implementing 2-address instructions in micro programmable RIC. 7

   c) Explain the carry look ahead principle with a neat logic diagram. 6

6. a) With the help of a flowchart explain how floating point addition and subtraction is carried out. 8

   b) Explain the following with reference to micro programmable RIC : 6

      i) Addressing modes ii) Format for transfer microinstruction.

   c) Write combinational logic unit description for propagate and generate section of the full adder circuit. 6

MODULE – IV

7. a) Draw stick diagrams and mask layout for the following : 8

      i) nMOS inverter ii) CMOS NAND gate.

   b) With the help of neat diagram explain nMOS fabrication process. 8

   c) Define MOS transistor transconductance and output conductance. 4

8. a) Explain the nMOS and CMOS design styles. 6

   b) Determine the pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter. 6

   c) Design CMOS logic gate for following function : 8

      i) $Z = \overline{(A.B) + C.(A + B)}$ ii) $Z = (A.B) + (C.D)$.