COMP 3 – 6 (RC)

S.E. (Comp.) (Semester – III) Examination, Nov./Dec. 2009

(Revised 2007-08)

INTEGRATED ELECTRONICS

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer 5 questions by selecting atleast one from each Module.*

2) Answers to sub-questions of a question should be written in continuation of each other.

3) Make suitable assumptions wherever necessary.

MODULE – I

1. a) Draw the circuit diagram for an op amp configured as voltage series feedback amplifier. Derive an expression for : 10

   1) Voltage gain 2) Input resistance

   3) O/p resistance 4) Total output offset voltage

   5) Bandwidth with feedback.

   b) Explain how op amp cab be used as a square wave converter and what is difference between basic comparator and Schmitt trigger. 6

   c) Explain voltage follower. Why it is called as non inverting buffer ? 4

2. a) Derive output voltage for differentiator, with its circuit diagram. 6

   b) Explain the working of an instrumentation amplifier and discuss its applications. 5

   c) What is a freq response ? Explain the need for compensating networks in op-amps. 6

   d) How opamp can be used as a average amplifier. 3

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MODULE – II

3. a) With a neat diagram and relevant waveforms, explain the working of an free running multivibrator using 555 timer. Obtain the expression for the time period. 8

b) Design a regulator using IC 723 to meet the following specification : $V_o = 5V, I_o = 100$ mA, $V_{in} = 15 \pm 20\%$, $I_{sc} = 150$ mA, $V_{sense} = 0.7V$. 4

c) What is a phase locked loop ? With the help of diagram explain the building blocks of PLL and obtain the necessary expression for free running frequency of V_{co}, lock range and capture range. 8

4. a) Explain the working of series voltage regulator. 6

b) Give the pin description and block diagram explanation for IC 723. 8

c) Explain how 555 timer can be used as a one shot multivibrator. List the applications. 6

MODULE – III

5. a) Draw a neat, diagram of a 3-input TTL. Explain its operation. What are the modifications incorporated in the circuit diagram to increase the speed compared to DTL circuit ? 10

b) An RTL gate has the following specifications I_{in} (max) = 400 μA I_o(min) = 2 mA. Leakage current of each resistor = 100 μA. Considering that each gate has 4 inputs and that all gates have the same characteristics. What fan out can a gate accommodate ? 4

c) Compare the following logic families : 6

1) CMOS 2) HTL 3) ECL

6. a) Explain why DCTL gate is not popular in IC technology although it is simpler than RTL. 5

b) Explain with a neat diagram working of a CMOS inverter gate. List some characteristics of a CMOS circuit. 8

c) Draw the circuit diagram of a basic schottky TTL Nand gate and explain its operation. How does the use of schottky diode in TTL circuit reduce the transistor turn-off time to negligible proportion. 7

MODULE – IV

7. a) Discuss the advantage and disadvantage of R-2R ladder over binary weighted resistor DAC. 5

   b) With a neat circuit diagram of 4 bit R-2R binary ladder D/A converter and explain how the signal is being converted from digital to analog. Give logic levels when logic 1 = 5V, logic 0 = 0V, R_f = 10 K, R_2 = 20 K. When input are 1) 1101 2) 1110. 6

   c) Define the following specification with suitable example : 9

   1) Linearity error 2) Accuracy
   3) Resolution 4) Settling time
   5) Monotonicity

8. a) Explain with a neat diagram Dual-slope A/D converter. 6

   b) With suitable diagram, explain voltage to frequency converter for ADC. 6

   c) Explain successive approximation type ADC. List the advantages. 8
