COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) (Revised Course) Examination, Nov./Dec. 2015
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

Instructions : *i) Answer **five** questions, atleast **one full** question from **each** Module.*
*ii) Make **suitable** assumptions, **wherever** necessary.*

MODULE – I

1. a) Explain the single address and branch instruction format of RIC. **6**

   b) Consider AR register of 3 bits. Assume only one control signal is 1 at a time : **8**

   AR = Set when CSL 1 = 1

   AR = Cleared when CSL 2 = 1

   AR $\leftarrow$ BR when CSL 3 = 1

   Draw the logic block diagram for the above problem.

   c) With the help of neat diagram, explain the two approaches to intersystem bus wiring. **6**

2. a) Write short notes on :
      1) Direct access storage
      2) Sequential access storage. **6**

   b) Construct a control realization for the following AHPL steps : **6**

      1) $z = x \vee A$;

         $\rightarrow (a, \bar{a} \wedge b, \bar{a} \wedge \bar{b})/(2, 3, 4)$

      2) $A \leftarrow X$;

         $\rightarrow (1)$

      3) $A \leftarrow X[1:3], X[0]$;

         $\rightarrow (4)$

      4) $A \leftarrow A[1:3], A[0]$;

         $\rightarrow (1)$

   c) Describe in brief any four building blocks used in hardware circuit. **8**

P.T.O.

MODULE – II

3. a) Write combinational logic unit description of an I bit incrementer. 8

   b) Draw the flow chart for fetch sequence of a 16 bit instruction and explain. 8

   c) Given that u = (1, 1, 1, 0) ; v = (1, 0, 0, 1) ; w = (1, 0, 1)

$$N = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix}, \quad x = 4 , \quad a = 2$$

   Compute : 4

   i) $u \oplus v$

   ii) v / N

   iii) $x < a$

   iv) u, v.

4. a) With the help of a neat flowchart explain the steps involved in the compilation of data network. 7

   b) Write the AHPL steps for fetch and Address Cycles in the design of control unit for RIC. 8

   c) Write the sequence of AHPL steps required to implement shift/Rotate instruction. 5

MODULE – III

5. a) With a neat block diagram explain the organization of microprogrammable RIC. 6

   b) Write combinational logic unit description for the generate and propagate section of full Adder circuit. 8

   c) Explain the hardware organization of floating point coprocessor. 6

6. a) With a neat diagram explain carry look ahead principle. 7

   b) Draw the flow chart for signed multiplication. 7

   c) Explain the following with reference to micro programmable RIC : 6

      1) Addressing modes

      2) Format for transfer Micro instruction.

MODULE – IV

7. a) What are masks ? List the masks used in NMOS fabrication process. 6

   b) Explain the working of a MOS inverter with NMOS depletion type transistor as load. Draw the transfer characteristics. 8

   c) Explain the structure and operation of the MOS transistor. 6

8. a) Explain the steps in IC fabrication. 8

   b) Differentiate between enhancement and depletion a type MOSFET. 4

   c) Design CMOS logic gates for : 8

      1) $F = \overline{(A \cdot B) + (C \cdot D)}$

      2) $F = (A \cdot B \cdot C) + D$.