28/5/13

COMP 5-4 (RC)

T.E. (Computer) (Sem. – V) (RC) Examination, May/June 2013
COMPUTER HARDWARE DESIGN

Duration : 3 Hours Total Marks : 100

***Instructions** : i) Answer **five full** questions, at least **one full** question from **each** Module.*
*ii) Make **necessary** assumptions and state **clearly** assumptions made.*

MODULE – I

1. a) Explain the difference between structure and behaviour in the digital system context. Illustrate your answer by giving 6
   i) a purely structural description
   ii) a purely behavioural description.

   b) Construct the logic block diagram of hardware associated with the register AR providing for the accomplishment of either of the transfers

   $AR \leftarrow \overline{AR}$

   $AR \leftarrow BR$

   given the proper control signal. Both AR and BR are 4 bit registers. 8

   c) Explain any two approaches to inter-system bus wiring. 6

2. a) Explain the single address instruction format for RIC. 5

   b) Decode the following for the RIC machine :
   i) 0101 01 0000 10 0001 where 0101 stands for ADD
   ii) 0010 01 0000 00 1111 where 0010 stands for MVT. 6

   c) Construct a detailed logic block diagram of the hardware realization of both the control and data units specified by the following AHPL description, where a and b are flip flops, x is an input, and z a single output line.

   1) $a \leftarrow x \vee b$;
   2) $b \leftarrow x$;
      $\rightarrow (a, \bar{a}) \mid (1, 3)$
   3) $z = 1$; $b \leftarrow x \oplus b$;
      $\rightarrow (1)$ 9

P.T.O.

MODULE – II

3. a) Write a combinational logic unit description for a decrementer. When used in a module description, the decrementer will be declared DEC [I]. 6

   b) Let M be a memory consisting of 1024 eighteen bit words with a 10 bit memory address register AR. Write an AHPL control sequence that will compute V | ∧ | M in an economical sequential manner. 8

   c) Draw the flowchart to implement the fetch sequence of 16 bit instructions.

4. a) With the help of a neat diagram explain the control signals and interconnections involved in the AND transfer. Also explain memory read and write operations for the RIC system. 6

   b) Write the sequence of AHPL steps to implement the fetch and address cycles of RIC. 8

   c) With the help of a neat flowchart explain the steps involved in the compilation of data network. 6

MODULE – III

5. a) With a neat block diagram explain the organization of a microprogrammable RIC. 6

   b) Explain the Carry Look Ahead principle and describe how the full adder unit can be used to build the carry look ahead unit. 6

   c) With the help of a flowchart explain how floating point addition and subtraction is carried out. 8

6. a) Write an AHPL description of the RIC microsequencer and explain. 6

   b) Write the sequence of AHPL steps to implement signed multiplication. 8

   c) Write the combinational logic unit description for the propagate and generate section of the full adder circuit. 6

MODULE – IV

7. a) Explain the structure and operation of the MOS transistor. Derive the expression for the drain current. 8

   b) Explain the working of a pass transistor. 6

   c) Differentiate between enhancement and depletion type MOSFET. 6

8. a) Explain NMOS fabrication process with neat diagrams. 8

   b) Explain the working of a MOS inverter with NMOS depletion type transistor as load. Draw the transfer characteristics. 8

   c) Draw the stick diagram and mask layout for CMOS nor gate. 4