COMP 3 – 5 (RC)

S.E. (Comp.) (Semester – III) (RC) Examination, May/June 2014
LOGIC DESIGN

Duration: 3 Hours | Total Marks: 100

Instructions : *1) Answer **five full** questions by selecting atleast **one** question from **each** Module.*
*2) Diagrams must be drawn **neat** and **clear** with pencil only.*
*3) Assume data **if necessary**.*

MODULE – I

1. a) Perform the following number conversions : **6**
   i) $(11.75)_{10}$ to binary
   ii) $(8BF4)_{16}$ to octal
   iii) $(6327.4051)_8$ to decimal.

   b) Prove the following using Boolean algebraic theorems. **4**
   $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = AB + BC + CA$

   c) For the following Boolean equation. **6**
   $Z = \overline{(\overline{C + D})} + \overline{A}\,C\,\overline{D} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C\,D + A\,C\,\overline{D}$
   i) Simplify the expression to a minimum number of literals using Boolean algebra. Verify the answer using a k-map.
   ii) Draw the logic circuit corresponding to this reduced form.

   d) Represent the following decimal numbers in eight bit **4**
   i) Sign magnitude form
   ii) Sign 1's complement form
   iii) Sign 2's complement form
   1) +27 2) –36

2. a) The Hamming code sequence as received contains error in one position 1101111. Locate the position of error bit using odd parity check. **4**

   b) Realize the expression **6**
   $(A + C)(A + \overline{D})(A + B + \overline{C})$
   using NOR gates only (only 2 inputs).

   c) Minimize the logic function using QM method.
   $f(A, B, C, D) = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$. **7**

   d) Why 2421 code is called as self complementing code ? Explain with help of example. **3**

P.T.O.

MODULE – II

3. a) What are combinational circuits ? Explain working of a full subtractor using suitable diagrams, k-map and truth tables. **7**

   b) Realize the following Boolean expression using a multiplexer with a circuit diagram. **5**

   $f(w, x, y, z) = \sum m(2, 5, 6, 7, 9, 12, 13, 15)$

   c) It is necessary to multiply two binary numbers each two bits long inorder to form their product in binary. Let the two numbers be represented by $a_0\ a_1$ and $b_1\ b_0$. **8**

   i) Determine the number of output lines required.

   ii) Find the simplified Boolean expression for each output.

4. a) Explain the working of following latches. **6**

   b) Realize a J-K flip flop using D flip flop. Show the conversion procedure. **8**

   c) What is race around condition ? Explain any two ways how race around condition can be eliminated. **6**

MODULE – III

5. a) Explain the following : **6**

   i) up/down counter

   ii) Modulus of a counter

   iii) Lock out of a counter.

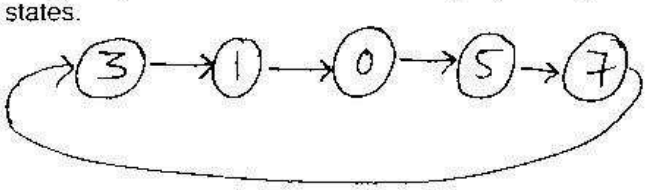
   b) The content of a 4 bit shift register is initially 1101. The register is shifted 6 times to right with serial input being 101101. What is the content of the register after each shift. **6**

   c) Design a asynchronous decade counter, sketch the output waveform. Make use of J-K flip flops. **8**

6. a) With the help of neat logic circuit and a neat waveform, explain the working of a 3 bit ring counter. What is the modulus of this counter ? 6

   b) Design a 3 bit synchronous up/down counter which counts up when the control signal is M = 1 and count down when M = 0. 6

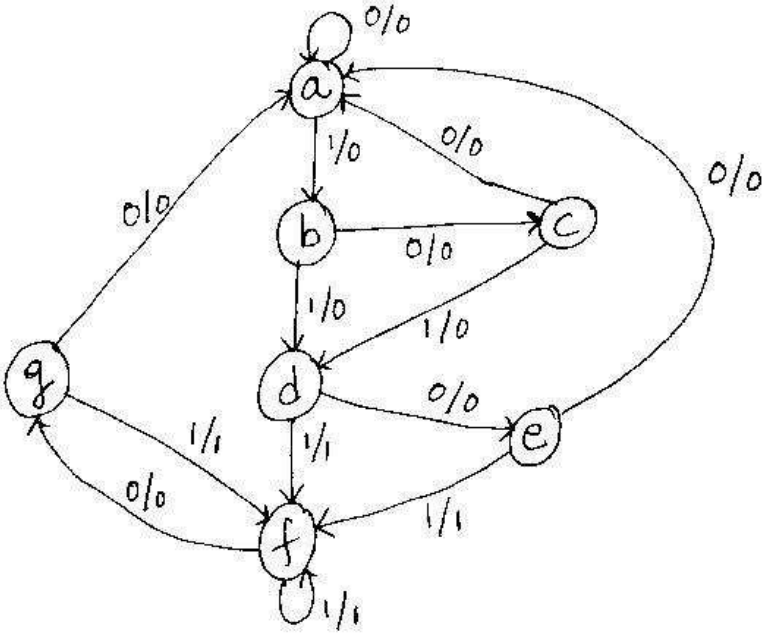
   c) Design a synchronous counter with S-R flip flops that goes through the following states. 8



MODULE – IV

7. a) Explain the steps involved in design procedure for synchronous sequential circuits. 5

   b) For the state diagram shown below obtain the state table and the reduced state diagram with the state table. 8



   c) Show how the PAL circuit is programmed for the following combinational circuit with functions. 7

   $F_1 = AB + AC$

   $F_2 = AC - BC$

8. a) A synchronous sequential machine has a single control input x and the clock and two outputs A and B on consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if x = 1, if at any time x = 0 it holds to the present state. Draw the state diagram and implement the circuit using T flip-flops. **8**

b) What are finite state machines ? Explain state table, state diagram and excitation table of R-S flip flop. **6**

c) A combinational circuit is defined by the following functions

$F_1(A, B, C) = \sum m(3, 5, 6, 7)$

$F_2(A, B, C) = \sum m(0, 2, 4, 7)$

Implement the circuit with a PLA having three inputs, four product terms and two outputs. **6**