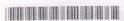
9/12/2013 M.

COMP 4 - 3 (RC)

S.E. (Comp.) (Sem. – IV) (RC) Examination, Nov./Dec. 2013 COMPUTER ORGANIZATION

Duration: 3 Hours Total Marks: 100 Instruction: Answer any five questions, by selecting at least one question from each Module. Module - I 1. a) List and explain the elements of bus design. 10 b) With diagrams explain the different RAID levels. 10 2. a) Draw an explain the instruction cycle state diagram. b) What is a 'Cache Mapping' ? Why is it required ? Explain set Associative Cache Mapping with an example. c) What is a bus? Explain its structure. 4 Module - II 3. a) Explain the functions of I/O Module. 5 b) Why is I/O Module required to connect peripheral devices to CPU? Draw a block diagram and explain the I/O Module structure. c) Explain simple interrupt processing with a neat diagram. 7 4. a) Explain characteristics of I/O channel. Support your answer with a neat diagram of I/O channel architecture. 8 b) Express the following numbers in IEEE 32-bit floating point format. i) - 2.5ii) 1/32 c) With the help of a flowchart, explain Booth's algorithm. Perform the following multiplication (-4) * (-5).



Module - III

5.	a)	With the help of a neat diagram explain the data flow during:	
		i) Fetch cycle	
		ii) Interrupt cycle.	6
	b)	Explain the concept of overlapped register windows in RISC.	6
	c)	With the help of a timing diagram explain the instruction pipeline operation. Assume that instruction 2 is a conditional branch to instruction 15. Until the instruction 2 is executed there is no way of knowing that the next instruction to be executed is instruction 15.	6
	d)	Discuss any two design issues of instruction set design.	2
6.	a)	Explain the following 8086 instructions:	
		i) CMPSB	
		ii) MULBX	
		iii) ADD AX, 0098H	
		iv) Loop label.	4
	b)	Explain RISC pipelining in detail.	6
	c)	If the last operation performed on a computer with an 8-bit word was an addition in which two operands were 00000010 and 00000011. What would be the values of the following flags?	
	5.	i) Carry mangata teams now prosessors rooms of sequential deaths.	
		ii) Zero	
		iii) Overflow	
		iv) Sign. mol trisoprity of tides. Baselink restricts gravelled em #assign 3. (d.	4
	d)	Discuss the various transfer of control instructions.	6
		Module – IV	
7.	a)	With the help of a timing diagram explain the following approaches:	
		i) Superscalar	
		ii) Super pipelined.	5

	b)	What is the relationship between instructions and micro-operations?	2
	c)	Write the sequence of micro-operations for the instruction $1SZ x$. The above instruction increments the contents of register x and skips the next instruction if x is zero.	3
	d)	How does a micro-programmed control unit function? Illustrate with a neat diagram.	6
	e)	Explain the two address sequencing technique.	4
3.	a)	Define the following w.r.t. parallelism :	
		i) Procedural dependency	
		ii) Anti dependency.	5
	b)	How does the control unit interact with the other elements of the CPU. Explain with a block diagram.	5
	c)	Explain the MESI protocol for multi processors.	6
	d)	Differentiate between:	
		i) Hardwired and microprogrammed control unit.	
		ii) Horizontal and vertical microinstructions.	4