616116.

COMP 5 – 4 (RC)

T.E. (Comp.) (Semester – V) (Revised Course)
Examination, May/June 2016
COMPUTER HARDWARE DESIGN

Duration : 3 Hours | Total Marks : 100

Instructions : *i) Answer **five** questions, atleast **one full** question from **each** Module.*
*ii) Make suitable assumptions, **wherever** necessary.*

MODULE – I

1. a) Give the behavioural VHDL description for the half adder circuit. **5**

   b) Describe the internal architecture of RIC system and explain two address instruction format. **8**

   c) Construct a detailed logic block diagram of the hardware realization of both control unit and data units of following AHPL sequence : **7**

   1) $a \leftarrow x \vee b$;

   2) $b \leftarrow x$;
   $\rightarrow (a, \overline{a}) / (1, 3)$

   3) $z = 1, b \leftarrow x \oplus b$;
   $\rightarrow (1)$

2. a) What do you mean by system ? Explain the properties of the system. **6**

   b) Construct the logic block diagram of hardware associated with register AR providing for accomplishment of either of the transfers. **6**

   $AR \leftarrow \overline{AR}$

   $AR \leftarrow BR$

   Give the proper control signals. Both AR and BR are 4 bit registers.

   c) Draw and explain shift/rotate instruction format. Also draw and explain seven distinct shift/rotate operations. **8**

MODULE – II

3. a) Given that U = (1, 1, 1, 0); V = (1, 0, 0, 1), W = (1, 0, 1) $N = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$ x = 5,

y = 3, z = – 1

Find :

i) $\wedge/W$ ii) N ! W

iii) 8T (2 ↑ x) iv) (4T5) $\oplus$ U

v) $\oplus$ // N vi) V/ N

vii) U $\wedge$ x viii) U, V **8**

b) Write combinational logic unit description of n bit ripple carry adder. **8**

c) Explain how a communication bus is implemented using Tristate Elements. **4**

4. a) Give the implementation of HLT using DEADEND. Also explain the implementation of HLT by return to step 1. Support your answer with neat diagram. **6**

b) With a neat diagram explain the basic organization of RIC. **6**

c) Suppose an address mode specified by IR [5 : 7] = 111 and calling for indexing, before indirect addressing is added to RIC. Modify steps 1 through 11 of the RIC control sequence accordingly. **8**

MODULE – III

5. a) Explain the following with reference to microprogrammable RIC. **6**

1) Format for branch instruction.

2) Flags and special bits.

b) Draw and explain the flowchart for floating point multiplication. **8**

c) Write short note on Microcoding. **6**

MODULE – IV

7. a) Derive the current-voltage relationship for the various bias conditions for a long channel MOSFET. Plot the characteristics. **7**

   b) Explain the working of pass transistor. **5**

   c) Design CMOS logic gates for

      1) $Z = \overline{A.B.C.D.}$

      2) 2 input OR gate **8**

8. a) Explain the n well CMOS fabrication process with neat diagrams. **8**

   b) Explain the nMOS design styles. **6**

   c) Discuss working of CMOS inverter with necessary diagrams. Also list the advantages. **6**