COMP – 4-3(RC)

S.E. (Comp.) Semester – IV (Revised 07 – 08) Examination, May/June 2009

COMPUTER ORGANIZATION

Duration : 3 Hours

Total Marks : 100

*Instructions : 1) Answer **any five** questions, at least **one** from each Module.*
*2) Make **suitable** assumptions **wherever** necessary.*
*3) Draw **neat** diagrams **wherever** required.*

Module – 1

1. a) What is memory hierarchy ? Explain with the help of a diagram. Justify the need for memory hierarchy. 6

   b) Differentiate between the following : 4

      i) Sequential access and direct access

      ii) SRAM and DRAM.

   c) A set-associative cache consists of 256 lines divided into 4-slot sets. Main memory consists of 16 k blocks of 128 words each. 7

      i) Show the format of main memory addresses.

      ii) How many sets are present in the cache ?

   d) What is associative memory ? Explain its operation. 3

2. a) A computer uses RAM chips of 512×4 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 2k bytes. Draw the memory address map and the interconnection diagram. 8

   b) What are the advantages of unified cache over split cache and that of split cache over unified cache ? 4

   c) Differentiate between constant angular velocity and constant linear velocity. 2

   d) With the help of a neat diagram, explain Mezzanine Architecture. What are its advantages over traditional bus architecture ? 6

P.T.O.

Module – II

3. a) Represent the following numbers in IEEE 32-bit floating point format. 4

   i) – 1/32 ii) 1234

   b) What are the advantages of biased representation over sign-magnitude representation ? 2

   c) With the help of a flowchart, explain Booth's algorithm. Show step by step procedure how –21×12 are multiplied using Booth's algorithm. 8

   d) Differentiate between the following :

   i) Vectored and non-vectored interrupts

   ii) I/O channel and I/O processor

   iii) Memory mapped I/O and Isolated I/O. 6

4. a) With the help of a block diagram, explain the functions of an I/O module. 8

   b) What are the design issues in implementing interrupt driven I/O. Explain. 6

   c) With the help of a neat flowchart, explain division of signed magnitude numbers. Perform the following division –50/11. 6

Module – III

5. a) Explain the graph colouring problem. Explain its application in RISC machines. 6

   b) Explain RISC pipelining in detail. 8

   c) Write the one-addr, two-addr and 3 – address instructions that could be used to compute 6

   $X = (A + B * C) (D - E/F)$

6. a) With the help of a diagram, explain data flow during 6

   i) Fetch cycle ii) Indirect cycle.

b) Explain the 6-stage instruction pipeline, with the help of a flowchart and timing diagram. 6

c) What do you mean by addressing mode ? Explain the following addressing modes with ex. 8

i) Based indexed

ii) Direct

iii) Immediate.

Module – IV

7. a) Explain the MESI protocol for multiprocessors. 8

b) Explain the features, advantages and disadvantages of following interconnection structures. 12

i) Time shared bus

ii) Crossbar switch

iii) Switching network.

8. a) Differentiate between : 6

i) Instruction level parallelism and machine level parallelism.

ii) Superscalar and superpipelined.

iii) Horizontal and vertical microinstruction..

b) With the help of a diagram, explain single address sequencing technique for micro instructions. 6

c) Explain the micro operations for execute stage of a add R1, x instruction, which adds contents of X memory location to R1 and stores result in R1. 2

d) With the help of a diagram, explain Hardwired control unit. 6