COMP 4 – 3 (RC)

S.E. (Comp.) (Semester – IV) Examination, May/June 2010
COMPUTER ORGANIZATION

Duration : 3 Hours Max. Marks : 100

Instructions : *1) Answer **any five** questions, at least **one** from **each** Module.*
*2) Make **suitable** assumptions, **wherever** necessary.*

MODULE – I

1. a) With diagrams, describe the different RAID levels. 12
   b) How does the control unit interact with other elements of the CPU ? Explain with a block diagram. 8
2. a) Discuss the features of RAM, ROM, PROM, EPROM, EEPROM and flash memory. 12
   b) Compare direct mapping, set associative and associative mapping techniques. 6
   c) What are micro-instructions ? 2

MODULE – II

3. a) Show the contents of the registers during the process of division of 10100011 by 0011. (Use the dividend of 8 bits) 10
   b) Describe the step by step process of DMA transfer. 8
   c) What are interrupts ? List the different types of interrupts. 2
4. a) Explain the different ways in which computer buses can be used to communicate with memory and I/O. 6
   b) Describe the working of programmed I/O with a flowchart. 6
   c) With a flowchart, describe Booth's algorithm. 8

MODULE – III

5. a) Explain six stage CPU instruction pipeline with the help of a diagram. 8
   b) What do you mean by compiler based register optimization in RISC ? 5
   c) Explain characteristics of RISC architecture. 5
   d) Write a note on transfer of control instructions. 2

P.T.O.

6. a) Explain the following 8086 addressing modes with the help of an example : 6
   i) Immediate addressing.
   ii) Direct addressing.
   iii) Register addressing.
   b) Draw and explain instruction cycle, state diagram with interrupt. 6
   c) Write a note on instruction set design. 2
   d) Write a 8086 program to compute factorial of a number. 6

MODULE – IV

7. a) Explain the micro-operations for a fetch cycle. 5
   b) Describe Superscalar Instruction Issue Policies. 5
   c) Write short notes on : 10
   i) Symmetric multiprocessors.
   ii) Cache coherence protocols.

8. a) State and explain limitations of parallelism. 6
   b) Write a note on multiprocessor operating system design considerations. 6
   c) Explain branch control logic, variable format micro-instruction sequencing technique. 6
   d) Explain direct and indirect encoding of micro-instruction. 2