Sem - III m R-gulan 23/12/13
comp Part

COMP 3 – 6 (RC)

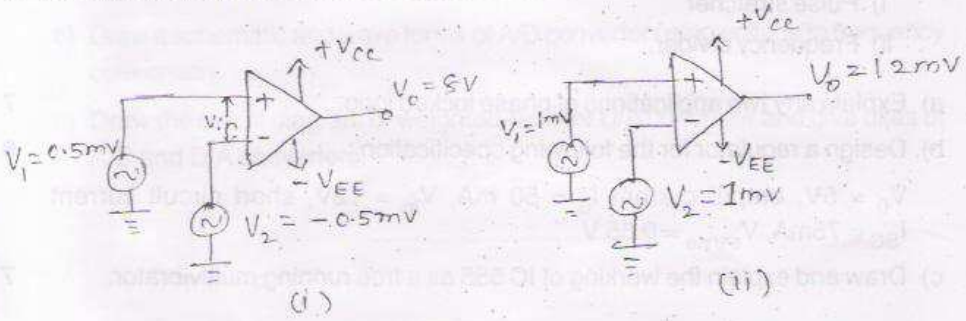
S.E. (Computer) (Semester – III) (RC) Examination, Nov./Dec. 2013
INTEGRATED ELECTRONICS

Duration : 3 Hours Total Marks : 100

Instructions : *1) Attempt **any five**, choosing at least **one** from **each** Module.*
*2) Assume **any** data, **if necessary**.*

MODULE – 1

1. a) Calculate the CMRR for the circuit measurement shown in fig. 5

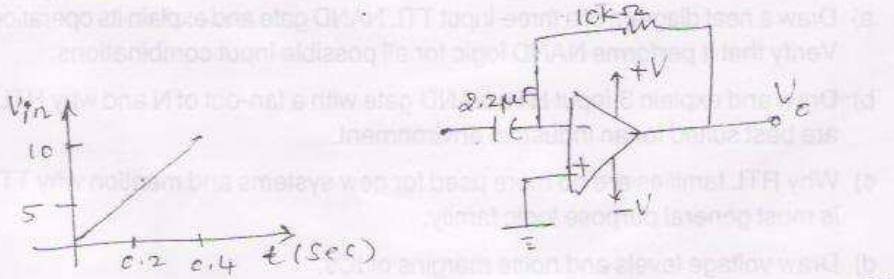


b) Explain the working of a zero crossing detector. 5

c) With a neat circuit diagram describe the operation of a non-inverting op-amp summer and averager with three inputs. 6

d) Draw the block schematic of an op-amp and describe the operation of each block. 4

2. a) For the differentiator circuit shown in fig. determine the output voltage, if the input goes from 0 V to 10 V in 0.4 seconds. Assume the input voltage changes at constant rate. 4



P.T.O.

b) Draw the circuit diagram and explain the working of an op-amp configured in the inverting mode as a summing, scaling and averaging amplifier. 8

c) Draw and explain the working of a Schmitt trigger. 8

MODULE – 2

3. a) Describe the operating principle of PLL. 6

b) Give pin description of LM 105 with its block diagram. 6

c) Write a short note on 8

i) Pulse stretcher

ii) Frequency divider.

4. a) Explain any two applications of phase locked loop. 7

b) Design a regulator for the following specification : 6

V_0 = 5V, output current I_0 = 50 mA, V_{in} = 12V, short circuit current I_{SC} = 75mA, V_{sense} = 0.65 V.

c) Draw and explain the working of IC 555 as a free running multivibrator. 7

MODULE – 3

5. a) List the characteristics of CMOS and name the types in bipolar and unipolar logic families. 6

b) Explain the working of two input DTL NAND gate and draw the circuit for three input modified DTL gate. 8

c) Mention the fastest logic family and give its disadvantages along with a symbol for a 3-input OR/NOR gate. 6

6. a) Draw a neat diagram of a three-input TTL NAND gate and explain its operation. Verify that it performs NAND logic for all possible input combinations. 8

b) Draw and explain 3-input HTL NAND gate with a fan-out of N and why HTL are best suited for an industrial environment. 6

c) Why RTL families are no more used for new systems and mention why TTL is most general purpose logic family. 4

d) Draw voltage levels and noise margins of ICs. 2

MODULE – 4

7. a) Explain the specifications of D/A converters. 8

   b) Describe 3-bit binary Ladder D/A network. State its advantages and disadvantages. 7

   c) An 8-bit successive approximation A/D converter has a resolution of 20 mV. If the analog input voltage is 1.085 V, find its digital output in binary form. 5

8. a) Illustrate how output of counter in dual-slop A/D converter is proportional to the analog voltage. 6

   b) Draw a schematic and wave forms of A/D converter using voltage to frequency conversion. 6

   c) Draw the circuit diagram of weighted-resistor D/A converter and give uses of A/D and D/A converters. 8