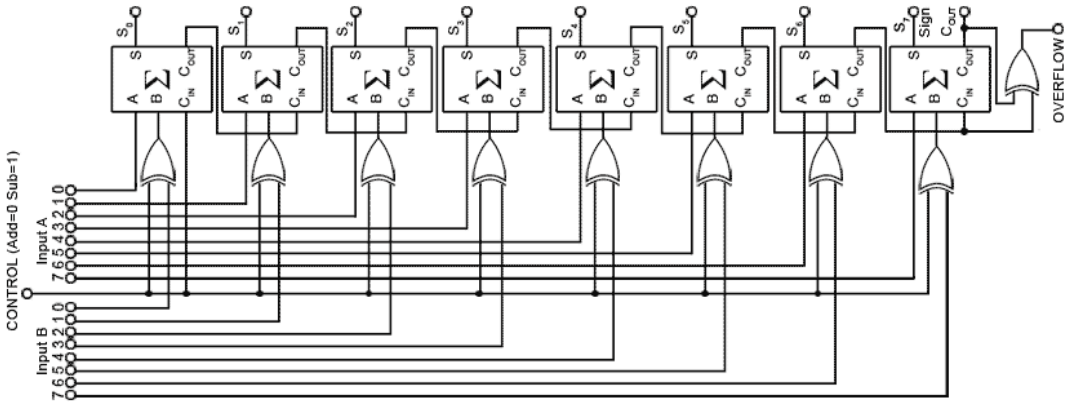
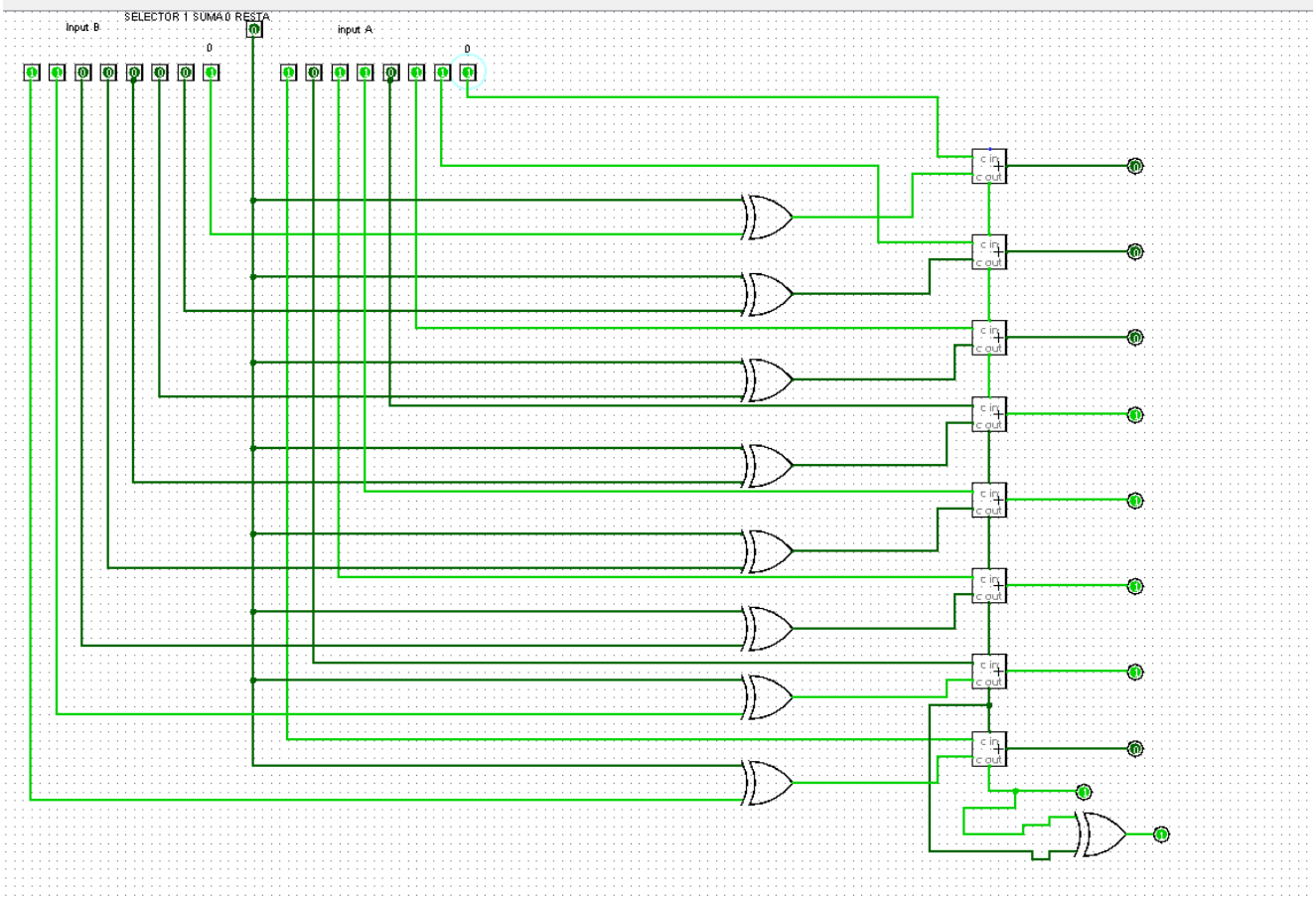
Diseñe en VHDL un sumador/restador de 8 bits en complementos a 2. Instanciando 8 suma dores completos con el mismo diseño usado en la práctica anterior usando la arquitectura Data-flow.

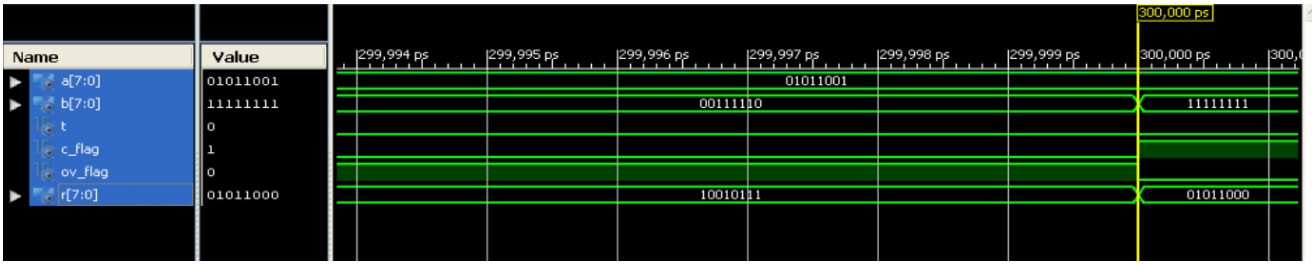


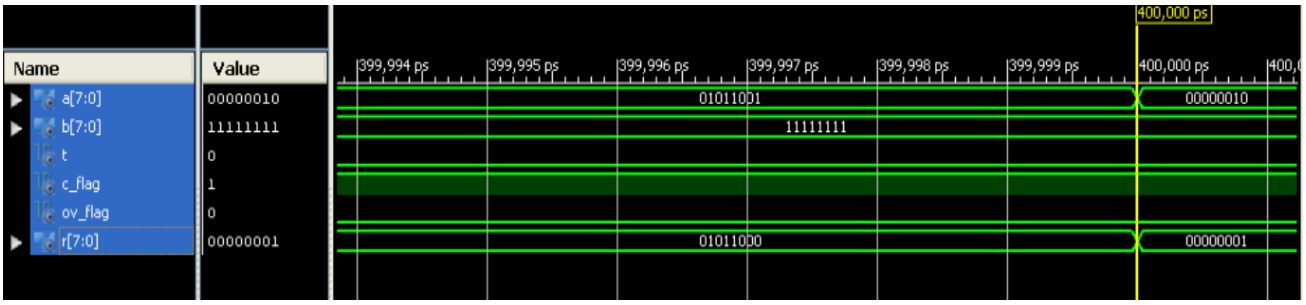


SIMULACION

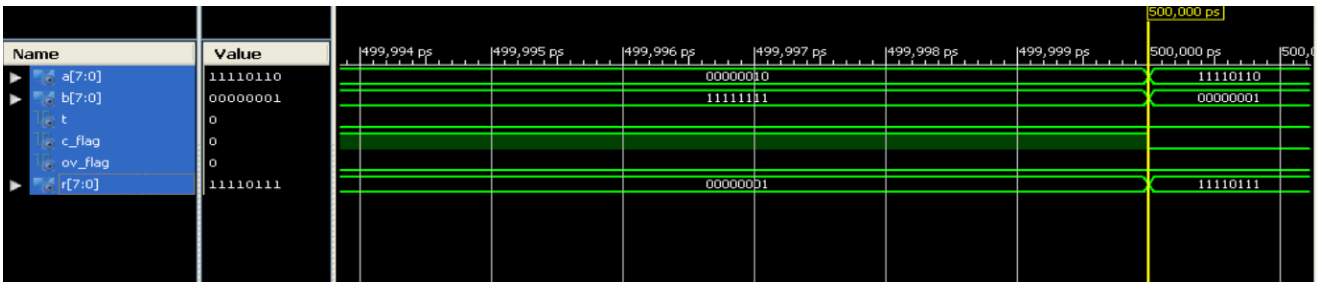
SUMA DE DOS NUMEROS POSITIVOS

SUMA DE NUMERO POSITIVO / NEGATIVO

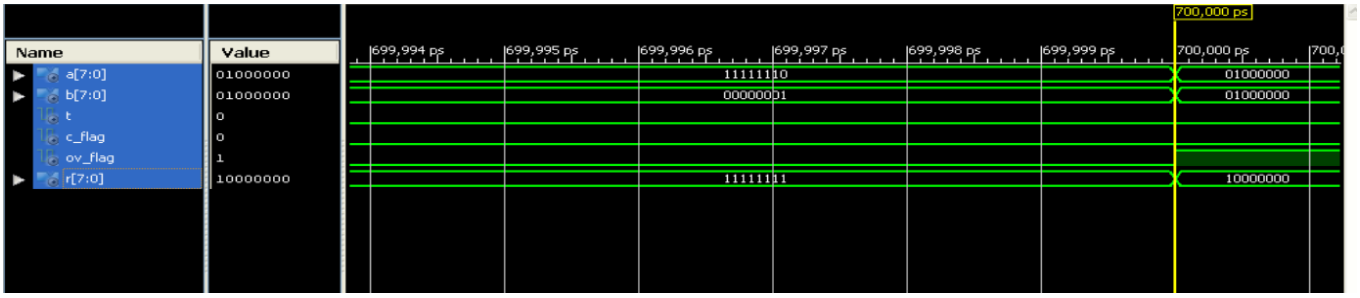


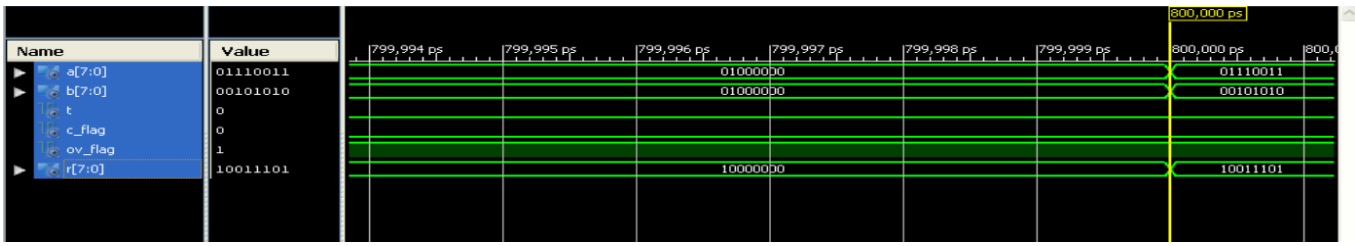


SUMA NUMERO NEGATIVO/POSITIVO

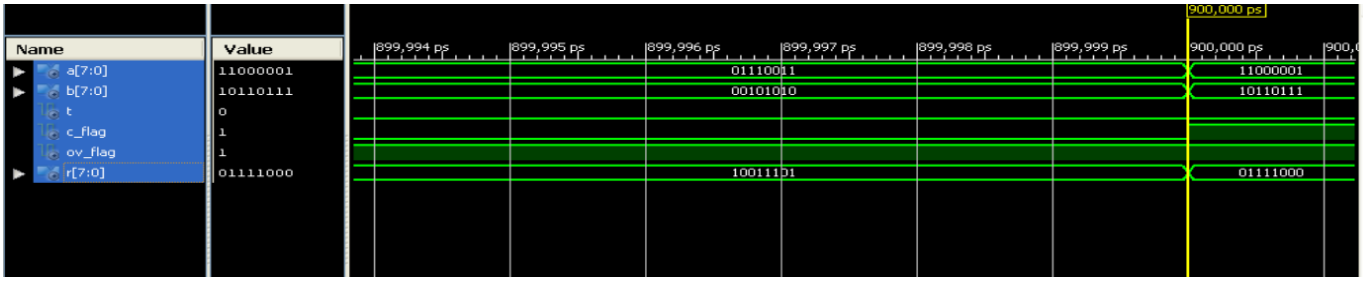


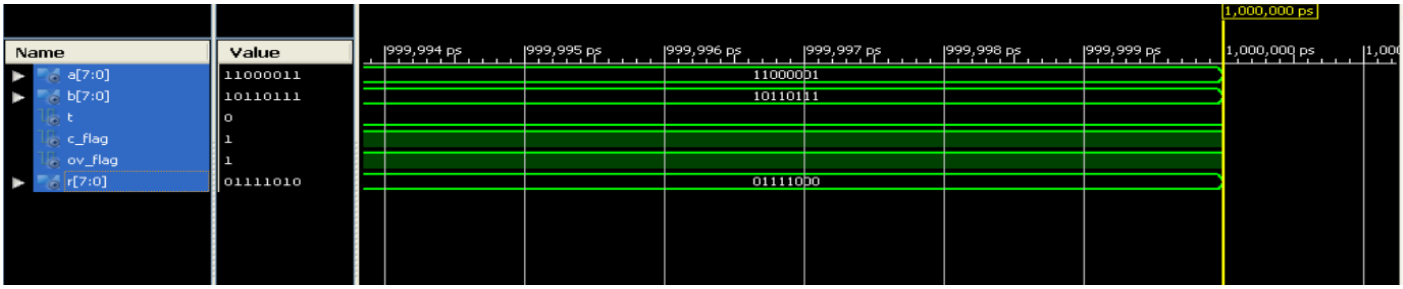
--OVERFLOW SUMA



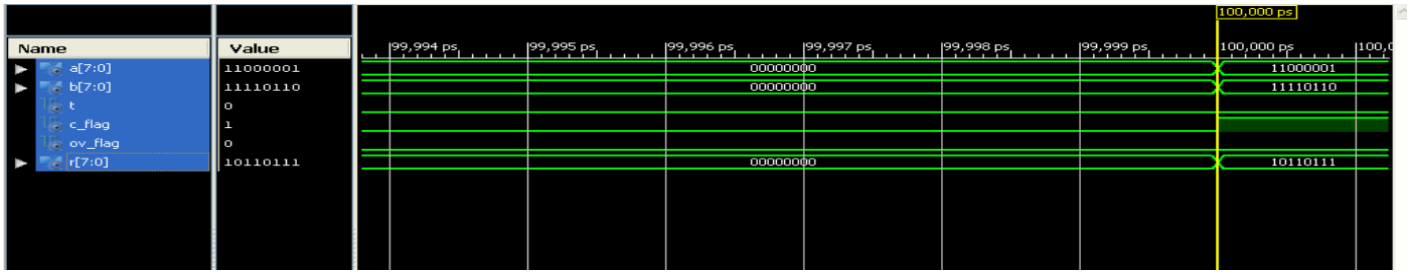


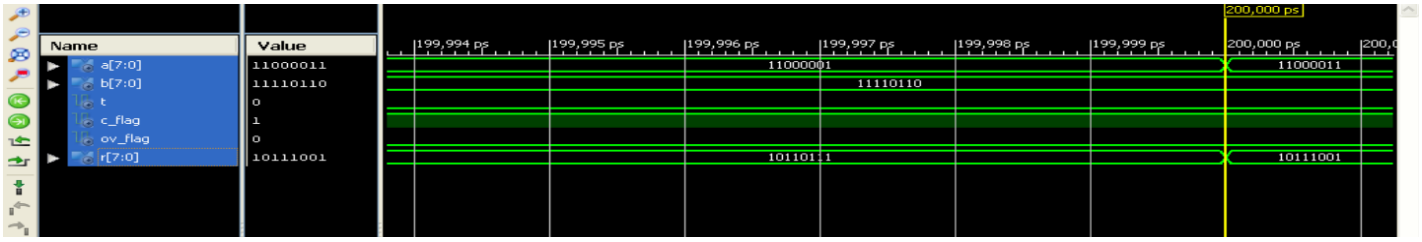
--OVERFLOW NEGATIVES





CARRY OUT SUMA





CARRY OUT RESTA