11-bit Column-Parallel Single-Slope ADC With First-Step Half-Reference Ramping Scheme for High-Speed CMOS Image Sensors

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***Abstract*— A first-step half-reference ramping (FHR) readout scheme is presented in this study for high frame rate CMOS image sensors (CISs). The proposed readout scheme enhances the conversion speed of a single-slope (SS) analog-to-digital converter (ADC) by applying a binary-weighted searching algorithm at the first A/D conversion attempt. By effectively reducing the reference signal range, the proposed FHR readout scheme can reduce the number of A/D conversion steps in the SS ADC while maintaining the ADC performance. Furthermore, the proposed scheme is reversible to operate the conventional SS ADC algorithm, thus it preserves the structural advantages of the SS ADC. The proposed FHR scheme becomes more effective as the bit-depth of the ADC increases. A prototype CIS with a column-parallel 11-bit SS ADC was fabricated in a 0.11-μm 1P4M CIS process with a 2.9-μm pixel pitch. A maximum frame rate of 570 frames/s was achieved with a 1024 × 240 pixel resolution, corresponding to a 140.08 Mp/s pixel rate. Total power consumption was 57.2 mW under 2.8 V for pixel readout and 1.8 V for readout circuitry. When compared with the conventional 11-bit SS ADC, the proposed FHR scheme shortens the total A/D conversion time by 38.4%. The prototype CIS demonstrated the figure of merits (FoM) of 0.84 e^-·nJ and 0.41 e^-·nJ/step.**

***Index Terms*— CMOS image sensor (CIS), column-parallel readout, first-step half-reference ramping (FHR) readout scheme, high-speed single-slope (SS) analog-to-digital converter.**

I. Introduction

In RECENT years, digital imagers built into mobile devices have been developed in large numbers that feature high pixel resolution, high bit-depth, high speed, and low-power performance [1]–[3]. Accordingly, the consumer demand for various applications demonstrating higher pixel rate [4] performance has increased. Because mobile devices are battery-powered, low power consumption is still a major stipulation.

Various analog-to-digital converters (ADCs) for CMOS image sensors (CISs) [5]–[9] have been studied for realizing the aforementioned features, and each type of ADC is uniquely advantageous. Nevertheless, the single-slope (SS) ADCs are the most widely employed in CIS applications, because they can be implemented with a narrow column pitch using a simple column circuit, which consists of a comparator and a counter. Thereby, SS ADCs consume relatively less power than that consumed by other ADCs. Furthermore, SS ADCs demonstrate a higher uniformity between the columns, resulting in lesser column fixed-pattern noise (CFPN) [3]. However, despite all their advantages, SS ADCs present the disadvantage of low conversion speed owing to their operational algorithm. Each N-bit A/D conversion of an SS ADC requires 2^N clock periods, which is significantly longer than the N clock period in case of both successive-approximation register (SAR) ADCs [10] and cyclic ADCs [11] (here, N represents the ADC resolution). This is a major impediment limiting the readout speed of CIS, which makes increasing the bit-depth with high pixel resolution difficult.

For enhancing the conversion speed of an N-bit SS ADC requiring 2^N conversion steps, various approaches involving two-step (TS)-based SS ADCs requiring $(2^C + 2^F)$ conversion steps have been studied in [12]–[16]; where C and F represent the number of coarse bits and fine bits, respectively ($N = C + F$). According to these approaches, the results of coarse conversion are obtained using column memories. One such TS-based SS ADC is the multiple-ramp single slope (MRSS) ADC [12], which stores the results of coarse conversion in the column digital memory. The MRSS ADC exhibits a significantly enhanced conversion speed relative to that of the SS ADC. However, there are two drawbacks presented in this case. First, the MRSS scheme occupies a larger area and consumes high power because of the multiple ramp generators and its ramp signal paths corresponding to the number of coarse steps. Second, a ramp slope mismatch can cause linearity degradation. In a different study, another type of TS-based SS ADC was presented [13], namely, the TS SS ADC, which utilizes holding capacitors as the analog memory to sample the coarse steps. This scheme involves TS conversion using only two ramp generators of the coarse and fine steps. However, the disadvantage is that its resolution is limited because of a gain error mismatch between the coarse and fine conversions. Both the MRSS ADC and TS SS ADC present linearity problems owing to the use of several ramp slopes.

In this regard, alleviating the aforementioned inherent limitations of the SS algorithms would require a meticulous analysis of the characteristics of other high-speed ADCs,

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such as the SAR algorithm. Because SS ADCs are based on unary searching algorithms for A/D conversion, they require $2N - 1$) conversion steps for obtaining the most significant bit (MSB). The reason for this is that when an A/D conversion is initialized, a ramp slope generator provides a reference signal to all column SS ADCs. By contrast, SAR ADCs are based on binary-weighted searching algorithms, and they obtain the MSB in the first A/D conversion attempt. In this case, during an A/D conversion, the column SAR ADC holds residues of each A/D conversion result via its own reference generator. In this manner, with respect to the conversion speed, the SAR ADC demonstrates a significant advantage over SS ADCs owing to these interesting characteristics. Therefore, incorporating the SAR algorithm to the conventional SS architecture would prove highly beneficial.

In this study, the first-step half-reference ramping (FHR)-SS readout scheme is proposed for high frame-rate commercial CISs to alleviate the inherent speed limitation of SS algorithm. The proposed readout scheme can effectively reduce the number of A/D conversion steps to obtain the MSB by adopting a binary-weighted searching algorithm in the first A/D conversion attempt. The proposed scheme is applicable to conventional SS ADC architecture and still preserves its structural advantages.

The remainder of this article is organized as follows. Section II discusses the operational principle of the proposed readout scheme and its error collection process. Section III describes the prototype CIS and circuit implementation details. Section IV presents the experimental results regarding the prototype chip, and Section V presents the concluding remarks.

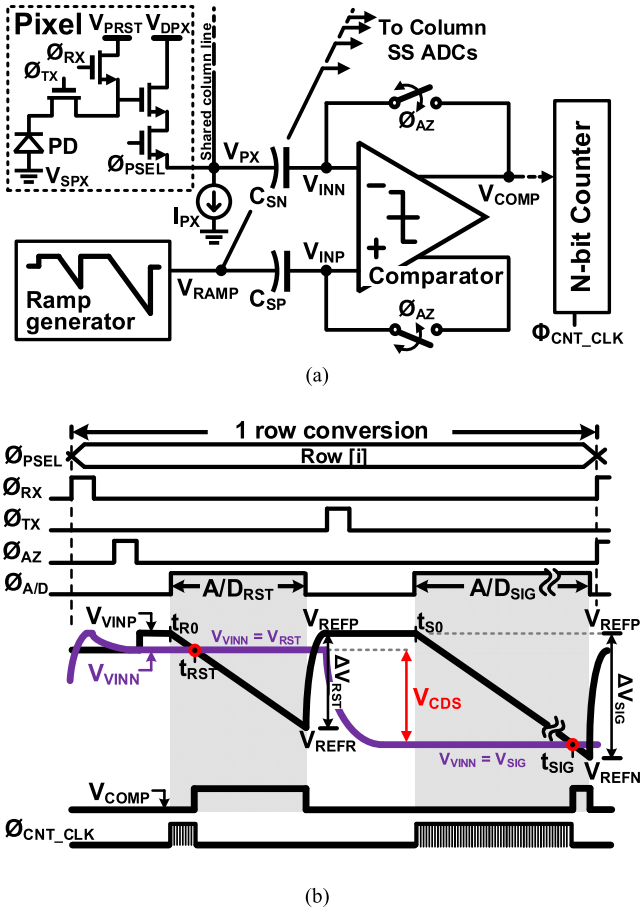


Fig. 1. (a) Simplified conventional column-parallel SS ADC and (b) its operational timing diagram and waveform.

II. Proposed Readout Scheme

A. Conventional SS ADC

Fig. 1(a) shows a conventional column-parallel SS ADC [3]. Each column consists of a comparator with two sampling capacitors (C_{SN} and C_{SP}), switches (Φ_{AZ}s), an N-bit counter, and a ramp generator that is shared by all column SS ADCs. Each column SS ADC is ac-coupled by a reference signal (V_{RAMP}) from the ramp generator and an input signal (V_{PX}) from the pixel. Fig. 1(b) depicts the operational timing diagram and waveform of the conventional SS ADC with dual correlated double sampling (dual CDS) [17]. Dual CDS, which is performed in both analog and digital domains, is widely used because of its high noise suppression capability. The pixel is selected by Φ_{PSEL}, and V_{PX} becomes the pixel reset voltage (V_{RST}) and the pixel signal voltage (V_{SIG}) according to the pixel control signals of Φ_{RX} and Φ_{TX}, respectively. When Φ_{AZ} is ON, V_{INN} and V_{INP} have the same voltage levels ($= V_{REFP}$), and C_{SN} and C_{SP} sample V_{REFP}-V_{RST} and V_{REFP}-V_{RAMP}, respectively; then, $\Phi_{A/D}$ is triggered. During the A/D$_{RST}$ period, SS A/D conversion is performed for initial state sampling in the digital domain: V_{RAMP} starts to decrease at t_{R0}, and a comparator simultaneously compares V_{INP} with V_{INN}. If V_{INP} exceeds V_{INN} at t_{RST}, the output of the comparator (V_{COMP}) changes, which in turn causes the latch to store the counter value as the result of the A/D$_{RST}$ (D$_{RST}$) conversion. After Φ_{TX} is triggered, analog CDS is performed at the V_{INN} node, which yields a value of $V_{REFP} - V_{CDS}$, where V_{CDS} is the photodiode voltage, and $V_{CDS} = V_{RST} - V_{SIG}$. During the A/D$_{SIG}$ period, SS A/D conversion is performed once again, whereby the result of A/D$_{SIG}$ (D$_{SIG}$) is produced. Here, the ramp signal spans the full scale from V_{REFP} to V_{REFN} ($= \Delta V_{SIG}$), including the range of ΔV_{RST}. Upon subtraction of D$_{RST}$ from D$_{SIG}$, only the digital code of the photodiode voltage (D$_{CDS}$) can be obtained. In this manner, further suppression of the noise and offset error is achieved in the digital domain, but it should be noted that this increases the A/D conversion time owing to the presence of the two conversion periods of A/D$_{RST}$ and A/D$_{SIG}$. To improve the conversion speed of the SS ADC combined with dual CDS, this study focuses on A/D$_{SIG}$ period.

B. Operational Principle of Proposed ADC

Fig. 2 shows a simplified schematic of the proposed single-column SS ADC. It consists of two comparators with sampling capacitors (C_{SN}, C_{SP}, and C_{SO}), switches (Φ_{CM} and Φ_{AZ}s), an N-bit counter with a 1-bit memory for MSB and ($N - 1$) bit local counter, a NAND for enabling column circuits, and a simple digital control logic. The ramp generator implemented using a current digital-to-analog converter (I-DAC) is shared by every column. The proposed SS ADC structure is based on the conventional SS ADC structure; the only difference

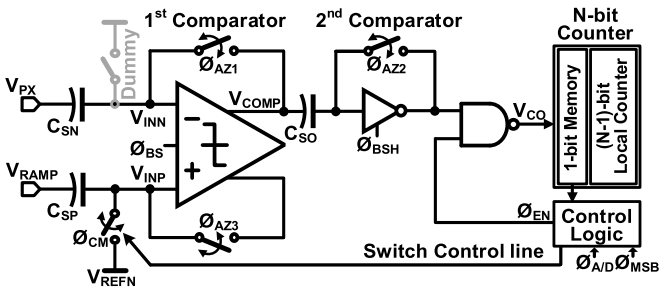


Fig. 2. Simplified schematic of the proposed single-column SS ADC.

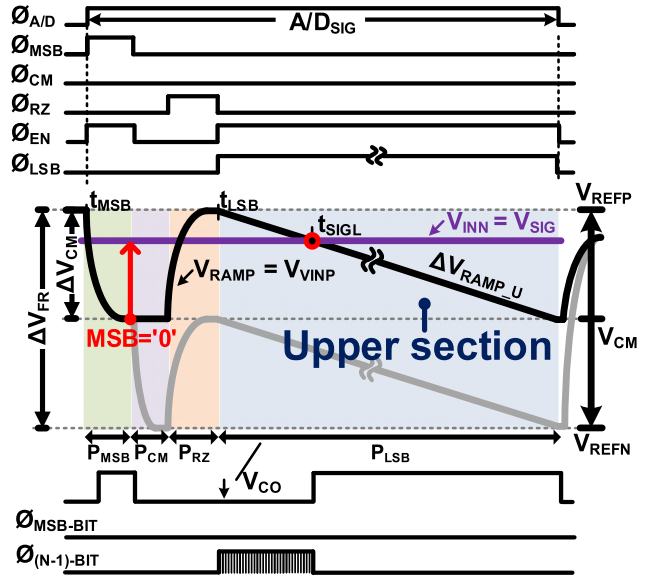
between them is with regard to the additional switch (Φ_{CM}) and the control line from the control logic. Thus, the proposed ADC has a structural advantage, which makes it reversible to the conventional one.

The objective of the proposed FHR scheme is to improve the conversion speed of the SS ADC by applying a binary-weighted searching algorithm in the first A/D conversion attempt itself. After the MSB is resolved, the full reference scale (V_{FS}) is divided into two subsections: the upper section (where MSB = 0) and the lower section (where MSB = 1). According to the results of MSB conversion, unary-weighted searching (the same procedure as in SS A/D conversion) is then performed for the rest of the least significant bits (LSBs) within the selected subsection. Thus, the actual number of conversion steps for obtaining the MSB is effectively reduced relative to that of the conventional SS ADC approaches.

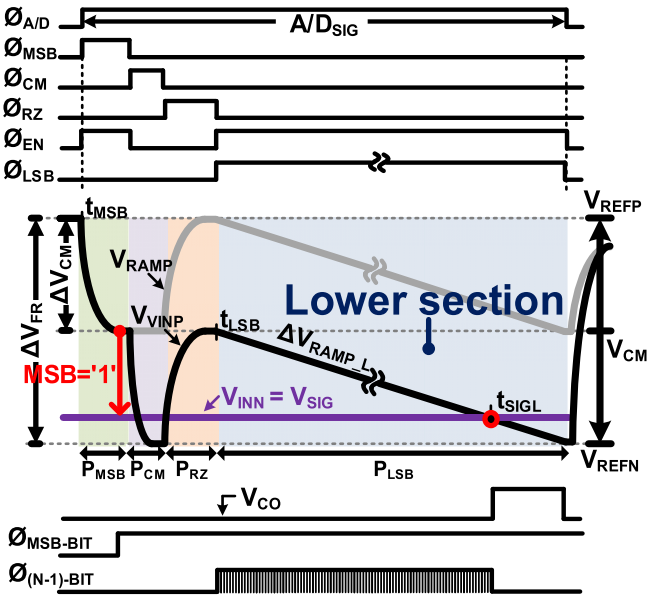
For providing a clear explanation of the proposed scheme, the waveforms of the proposed SS ADC are illustrated in Fig. 3, wherein two different cases of A/D_{SIG} are depicted as examples. Let us assume that the common level of both V_{INP} and V_{RAMP} is the same as that in an ideal design. The proposed readout scheme is implemented via four phases with P_{MSB}, P_{CM}, P_{RZ}, and P_{LSB} during the A/D conversion period. The ramp generator generates two ramp signals of the MSB step ($\Delta V_{FS}/2$) at P_{MSB}, P_{CM}, and P_{RZ}, and the LSB step ($\Delta V_{FS}/2^N$) at P_{LSB}. The proposed readout scheme commences by performing comparison with half of the full reference (V_{CM}) and V_{INN} (= V_{SIG}). When Φ_{MSB} is active (during P_{MSB}), the ramp signal (V_{RAMP}) spans from V_{REFP} to V_{CM} (= ΔV_{CM}) and is ac-coupled to the V_{INP} node. The proposed scheme operates in two cases.

1) After the comparison of V_{INP} with V_{INN}, if $V_{INP} < V_{INN}$ [Fig. 3(a)], the final output of the comparator (V_{CO}) changes to "logic high," and its conversion result (D_{MSB}) "0" is stored in the 1-bit memory of the N-bit counter. Subsequently, Φ_{RZ} becomes active (during P_{RZ}), and V_{RAMP} returns to V_{RFEP} (ΔV_{CM}), resulting in $V_{INP} = V_{RFEP}$. At Φ_{LSB} (during P_{LSB}), similar to the process occurring via the conventional SS algorithm, the A/D conversion is performed with the LSB step for obtaining the remaining bits in the upper section ($V_{INP} = V_{REFP} - \Delta V_{RAMP\_U}$). Here, the range of ΔV_{RAMP_U} is from V_{REFP} to V_{CM} of the full reference scale. Its conversion results (D_{LSB}s) are stored in the latch of the ($N-1$)-bit local counter. The full digital code (D_{FULL}) can be obtained by merging D_{MSB} with D_{LSB}s according to their code weights.

2) After the comparison of V_{INP} with V_{INN}, if $V_{INP} > V_{INN}$ [Fig. 3(b)], a D_{MSB} of "1" is stored, and the additional switch (Φ_{CM}) is on (during P_{CM}). Then, the V_{INP} node is reset as V_{REFN} of the full reference. When Φ_{RZ} is active (during P_{RZ}) and when V_{RAMP} returns to V_{RFEP} (ΔV_{CM}), V_{INP} becomes V_{CM} of the full scale. At Φ_{LSB} (during P_{LSB}), the SS A/D conversion is performed in the lower section ($V_{INP} = V_{CM} - \Delta V_{RAMP\_L}$). Here, the range of ΔV_{RAMP_L} is from V_{CM} to V_{REFN} of the full reference.



(a)



(b)

Fig. 3. Operational waveform of the proposed SS ADC during A/DSIG in two cases. (a) Upper section and (b) lower section in the full reference.

When compared with other TS-based SS ADCs, from the commercial perspective, the proposed SS ADC with the

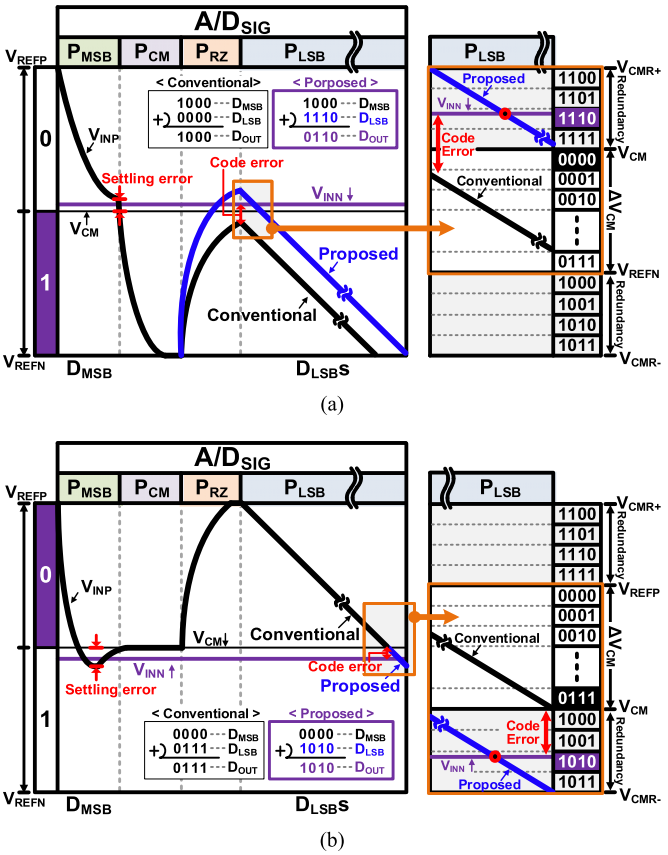


Fig. 4. Error correction of the proposed readout scheme for (a) and (b) different two cases.

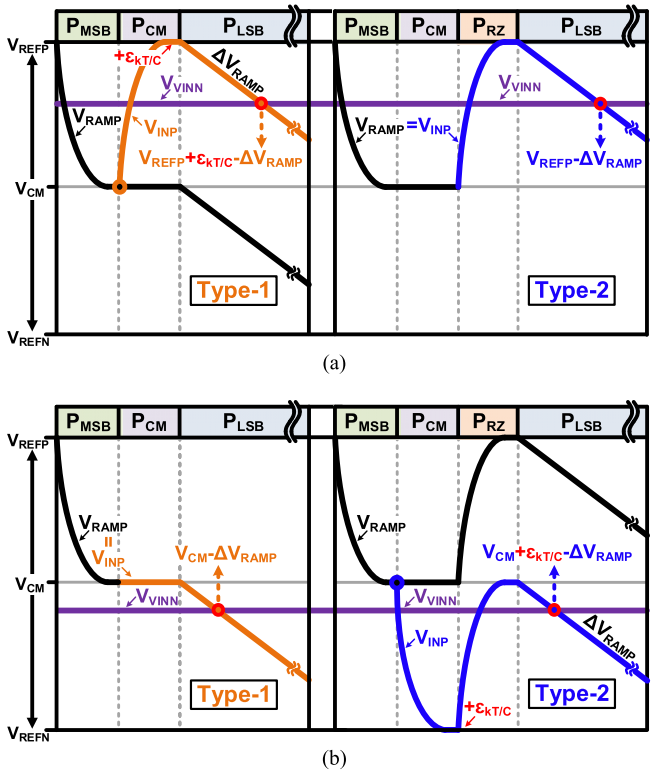


Fig. 5. (a) and (b) Two operation types of the proposed readout scheme.

proposed FHR readout scheme presents several advantages. First, because the proposed readout scheme becomes more effective as the ADC resolution increases, the proposed ADC architecture is suitable for high-performance CISs. Second, the proposed scheme operates only in two cases with the upper and lower sections in the full reference, enabling the application of error correction for nonlinearities more effectively than in other TS-based SS ADCs (this is discussed in detail in the following section). Finally, the proposed ADC architecture is easily reversible to the conventional SS A/D conversion algorithm. Considering its compatibility with the existing system environment, similarity with the conventional architecture could be the proposed method's main commercial advantage. It is worth noting that the proposed SS ADC is based on the conventional architecture with an additional switch.

C. Error Correction

A parasitic capacitor at the V_{INP} node could cause a difference in the ramp slope between the upper and lower sections of the full reference during P_{LSB}. In the proposed readout scheme, this does not influence the linearity of the proposed ADC, and it can merely be considered as an offset error. The primary source of nonlinearity in the proposed readout scheme is, however, a settling error of the ramp slope during P_{MSB}. For a clear explanation thereof, the waveforms of a 4-bit SS ADC are illustrated in Fig. 4 for two different cases. Let us assume that there exists insufficient time to settle ΔV_{CM} during P_{MSB} [black line in Fig. 4(a) and (b)]. In Fig. 4(a), although V_{INN} is larger than V_{CM}, the result of D_3 (D_{MSB}) is obtained as "1." In the case of the proposed readout algorithm, if the result of P_{MSB} (D_3) is "1," the following SS A/D conversion in P_{LSB} is performed in the lower section of the full reference. In that case, the result of "000" is obtained regarding the remaining LSBs (D_{2-0}) because there exists no zero-crossing. To resolve this problem, the ramping range of V_{RAMP} is extended to cover the over-range of ΔV_{CM} (from V_{CMR+} to V_{REFN}, represented by the blue line). After the ramping range is expanded, the results of D_{2-0} are obtained as "1110." Consequently, the error-collected 4-bit full code is achieved via addition of D_3 and D_{2-0} according to their code weights, which results in D_{FULL} = "0110." In Fig. 4(b), although V_{INN} is lower than V_{CM}, the result of D_3 is obtained as "0" (represented by the dark line). In this case, the following SS A/D conversion is performed in the higher section, resulting in D_{2-0} = "111." For correcting the digital code error [similar to that in Fig. 4(a)], the ramping range of V_{RAMP} is extended to cover the over-ΔV_{CM} range (from V_{REFP} to V_{CMR-}, represented by the blue line). Consequently, the results of D_{2-0} are obtained as "1010"; via addition of D_3 and D_{2-0} according to their code weights, the 4-bit full code is obtained as D_{FULL} = "1010." Therefore, by expanding the ramping range of ΔV_{CM} from V_{CMR+} to V_{CMR-},the error correction in the proposed readout scheme is performed. In addition, by reflecting on the redundancy for error correction, the ramping range of A/D_{RST} becomes from V_{CMR+} to V_{REFR} for correlation with A/D_{SIG}. In this design, by considering the comparator's input range, 32 steps are inserted in P_{LSB} for error correction.

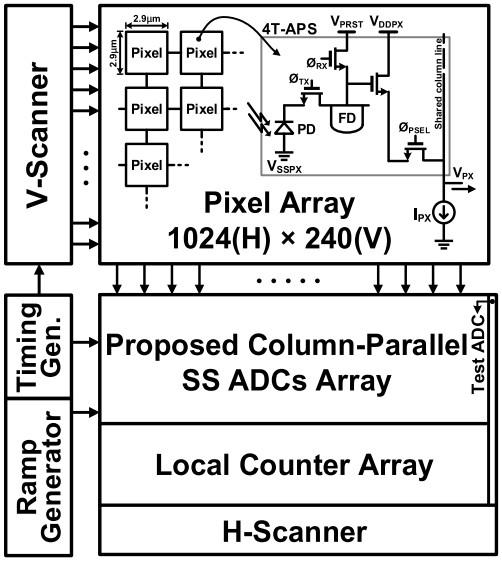


Fig. 6. Overall block diagram of the prototype CIS.

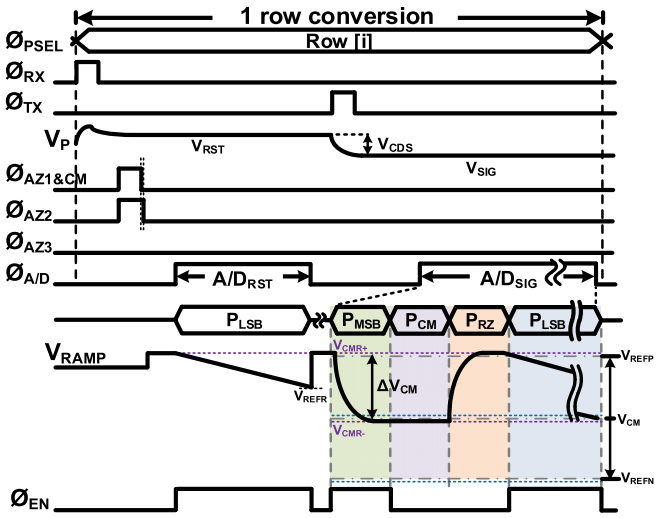


Fig. 7. Operational timing diagram of the prototype CIS.

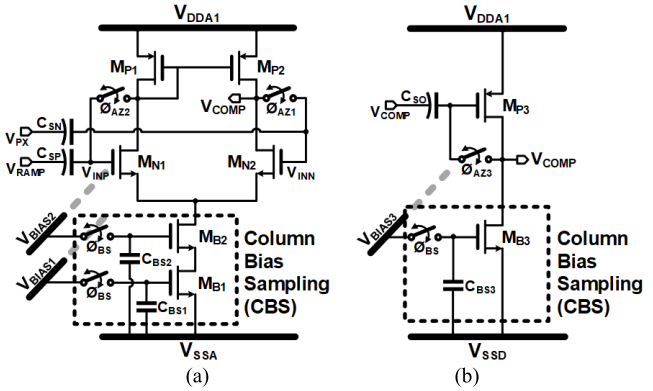


Fig. 8. Simplified schematics of (a) first stage and (b) second stage comparator.

D. Study of Proposed Scheme

The proposed FHR readout scheme can be implemented in two operation types, depending on the manner in which the V_{INP} node is reset (Fig. 2). Fig. 5 illustrates the two operation types of the proposed scheme: in type-1, the V_{INP} node is reset to V_{REFP}, and in type-2 (as proposed in this work), the V_{INP} node is reset to V_{REFN}. If $V_{INN} > V_{RAMP}$ at P_{MSB}, in type-1, the V_{INP} node is reset to V_{REFP} through S_{CM} (Φ_{CM}) (Fig. 2), which causes kT/C noise (i.e., $\varepsilon_{kT/C}$) at P_{CM}. In this way, $\varepsilon_{kT/C}$ is not eliminated by the dual CDS operation, resulting in dark scene images (oriented to low-illumination conditions) being contaminated. On the contrary, in type-2, when $V_{INN} < V_{RAMP}$ at P_{MSB}, the V_{INP} node is reset to V_{REFN} through $S_{CM}(\Phi_{CM})$ at P_{RZ}. In this part of the input range, the photon shot noise is the dominant noise source; thus, the ADC exhibits considerably better noise performance than that required [12], [18]. Considering the noise performance of the ADC, this work adopts the type-2 operation.

III. Prototype CIS Architecture and Implementation

Fig. 6 shows the block diagram of the prototype CMOS imager with the proposed FHR SS ADC. It has a 1024 × 240 array of 2.9-μm-pitch 4T-APS pixels, V-scanner, ramp generator, timing controller, H-scanner, and column-parallel SS ADCs with local counters operating on the proposed FHR scheme. For evaluation of the performance of a single column ADC, a test ADC is added in the column readout array.

A simplified operational timing diagram is illustrated in Fig. 7. The prototype CIS has a clock frequency of 215 MHz for 570 frames/s, corresponding to 140.08 megapixels/second (Mp/s). The horizontal readout time is approximately 7.3 μs; of which approximately 2.3 μs are for pixel readout operation and approximately 5 μs for ADC operation with dual data rate (DDR) counting. The resolution of the ADC is 11 bit, and its MSB bit is resolved in the first A/D conversion attempt via the proposed scheme. The range of A/D_{RST} is 712 steps for power efficiency at the analog gain ×16 condition; therefore, the range of A/D_{SIG} is 1412 steps ((712 steps for A/D_{RST}+ 2048 steps for V_{SIG})/2 + 32 steps for redundancy). Because the ramp generator has a fixed bandwidth in a 1-row time, sufficient time to settle ΔV_{CM} for MSB conversion is therefore required to ensure high image quality, allocating additional 16 clocks. Note that the nonlinearity of the proposed ADC could be caused by insufficient time during the MSB-first conversion. Compared with the conventional SS ADC with 11-bit resolution, the proposed readout scheme can reduce the required A/D conversion time by 38.4%.

A simplified schematic of the comparator with a two-stage topology [19] is shown in Fig. 8. It consists of a simple single-ended differential amplifier [Fig. 8(a)] and a common source amplifier [Fig. 8(b)]. Each amplifier has an autozeroing switch Φ_{AZ1} and Φ_{AZ2}, which control the reset operation of the first and second stage comparators, respectively. Referring to Fig. 7, note that Φ_{AZ1} and Φ_{AZ2} have a different operational timing. To reduce the effects of charge injection and clock feedthrough, Φ_{AZ2} is OFF later than Φ_{AZ1}. The ground of the

comparators is separated into V_{SSA} and V_{SSD} using a deep n-well to reduce the susceptibility to ground noise. In the column-parallel structure, many global lines are present for column ADCs, such as biasing lines, reference lines, and control lines. These lines could cause coupling noises between adjacent columns, resulting in the "horizontal stripes" noise. Therefore, it is essential for them to be shielded (i.e., shielding), so that the CMOS imager maintains the image quality in dark illumination conditions. However, as the column pitch continuously shrinks to a few micrometers [20], it is difficult to achieve shielding via only layout patterning techniques. Therefore, to further improve the shielding effects, the column bias sampling (CBS) technique [19], [21] is adopted for the comparators of each column. Because the CBS technique samples its own bias voltage in C_{BS} before the A/D conversion begins, each column can be isolated from any fluctuation with respect to adjacent columns during the A/D conversion. The CBS technique is widely utilized for reducing the coupling noise in the column-parallel readout structure [22], [23]. The comparator noise in the first stage is the main noise source. Thus, in the post-simulation level [24], the noise requirement of the first-stage comparator is targeted to be under 1/4 LSB in the full reference scale. Here, the input transconductance and the 3-dB bandwidth of the first-stage comparator are set to approximately 29 μS and 397 kHz, respectively.

As another noise problem, the floating diffusion (FD) node of the 4T-APS is affected by each switching operation of Φ_{RX} and Φ_{TX}, which causes different fluctuations (i.e., coupling noise) at the V_{PX} node. Moreover, when the pixel output is changed from $V_{SIG(N-1)}$ to $V_{RST(N)}$ during row-to-row readout (i.e., rolling shutter readout), a V_{SIG}-dependent settling error is generated. Note that the pixel current source (I_{PX}) becomes OFF-state for the duration in which Φ_{PSEL} is OFF. In this case, with insufficient time to settle the pixel output, both variations are not mitigated via dual CDS, which results in random noise (RN). Accordingly, to mitigate these problems, this work adopts the additional current bleeding path with the proposed pixel readout timing, as shown in Fig. 9. With the current bleeding path through M_{PC} and M_{SB}, the pixel output node contains a certain voltage level when Φ_{PSEL} is OFF ($= \overline{\Phi_{PSEL}}$), which reduces the pixel output fluctuation.

According to the proposed readout scheme, the ramp generator output (V_{RAMP}) transits half of the full reference scale (ΔV_{CM}) for MSB conversion (similar to that in SAR ADC), from P_{MSB} to P_{RZ}. Therefore, it requires sufficient time to settle each conversion step, which causes a speed bottleneck as the pixel resolution increases. As an effective technique to reduce the settling time, digital calibration is proposed to compensate for the settling error (ε_{MSB}) caused because of insufficient time to readout the MSB bit (here, ε_{MSB} can be considered as an offset error dependent on the conversion time). Fig. 10 shows a simplified schematic of the ramp signal generator. The structure of the ramp generator is based on a conventional current-steering DAC (I-DAC). It is composed of 11 segments of I-DAC, and each segment includes 256 unit current cells (I-Cells). In addition, the settling error calibrator is added to compensate for ε_{MSB} during MSB conversion by allocating additional 128 I-Cell pairs, which are composed of

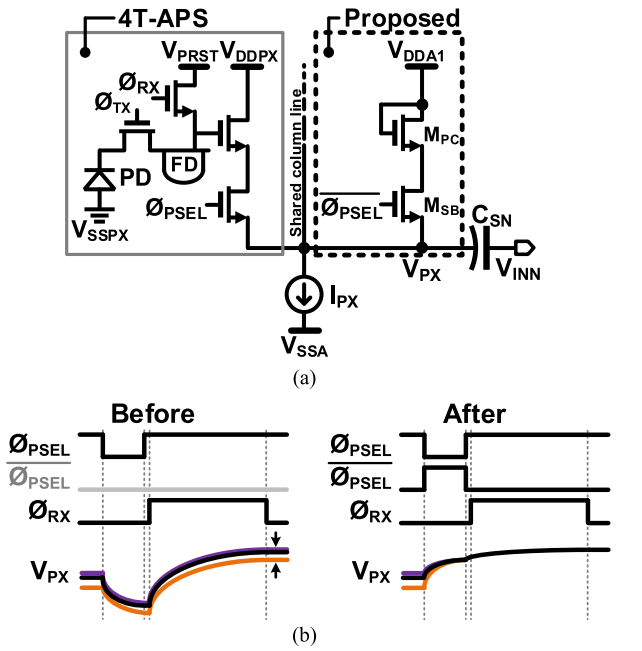


Fig. 9. (a) Additional current path in the pixel output and (b) proposed pixel readout timing.

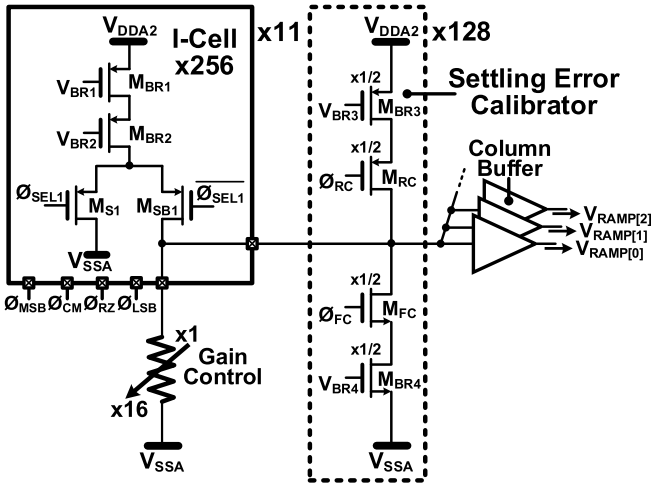


Fig. 10. Simplified schematic of the ramp signal generator with the settling error calibrator.

M_{BR3} and M_{RC} for expanding the range of ΔV_{RAMP} as well as M_{BR4} and M_{FC} to reduce the range of ΔV_{RAMP} with 0.5 LSB steps. Here, Φ_{RC} and Φ_{FC} are used for enabling/disabling the settling error calibrator. In the initial frame, settling error adjustment is performed as mentioned in [25] and [26], whereby an offset cancellation effect similar to that in conventional digital calibration is produced. In this work, the settling error calibration was processed in TSs: digital calibration and error correction. The ramp signal generator output is fed into each column through the column buffer, and it isolates any fluctuations induced by the column comparator. Note that the offset distribution of the column buffer is eliminated by the dual CDS operation.

IV. Experimental Results

The prototype chip was implemented with a 0.11-μm CIS process. A microphotograph of the prototype CMOS imager

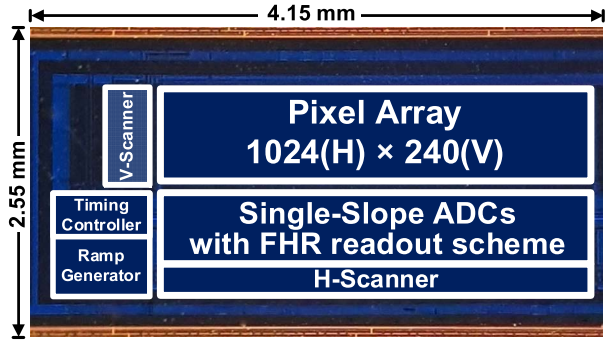


Fig. 11. Chip microphotograph.

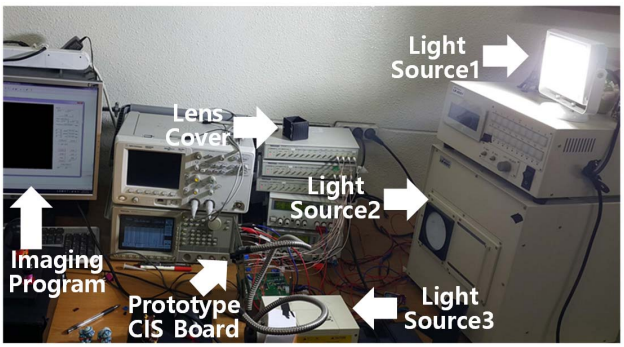


Fig. 12. CIS test environment.

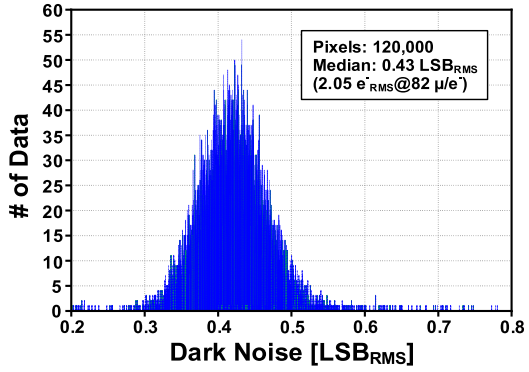


Fig. 13. Noise histogram for 120 000 pixels in dark room conditions.

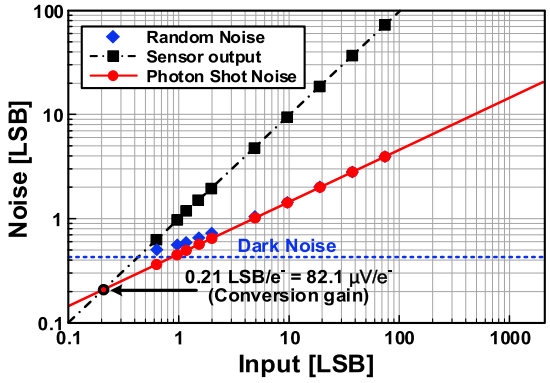


Fig. 14. Measured photon transfer curve.

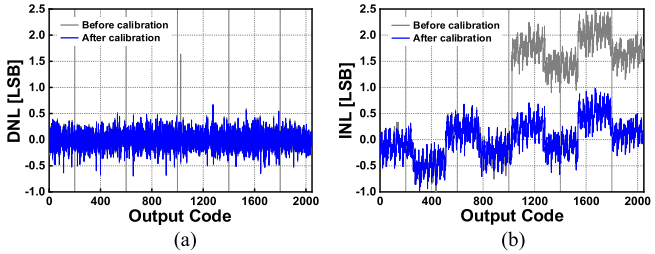


Fig. 15. Measured linearity of the ADC. (a) DNL. (b) INL.

and the CIS test environment are shown in Figs. 11 and 12, respectively. A 1024 × 240 array of 2.9-μm-pitch 4T-APS pixels and the column-parallel SS ADCs operating on the proposed FHR scheme were implemented in a chip of size 4.15 × 2.55 mm^2 with control logic circuitry, including I/O pads. Each column ADC occupied an area of 2.9 × 650 μm^2. The prototype CIS demonstrates a maximum pixel data rate of 140.08 Mp/s, corresponding to 570 frames/s at half of the Wide Super VGA resolution (1024 × 240). The total capacitance of C_{SN} and C_{SP} is 1.53 pF, and that of C_{SO} is 0.58 pF with a 6.2-fF unit capacitor wherein a metal–insulator–metal (MiM) capacitor is employed.

The measured noise histogram obtained from 120 000 pixels and the measured photon transfer curve in response to incident illumination are shown in Figs. 13 and 14, respectively. 1 LSB corresponds to 390.6 μV with 0.8-V full scale reference at an 11-bit ADC resolution. Here, 100 frames were captured in dark room conditions to obtain the noise standard deviation. The median RN under dark conditions can be represented with a root mean squared (rms) noise value of 168 μV_{rms} at the analog gain of 1, which corresponds to 2.05 e^-_{rms} with a pixel conversion gain of 82 μV/e$^-$. Consequently, an ADC dynamic range [15] of 73.6 dB was obtained. Note that the measurements were performed at room temperature using an IR-cut filter.

Fig. 15 shows the measured maximum differential nonlinearity (DNL) and integral nonlinearity (INL) profiles of the proposed SS ADC upon application of the proposed digital calibration. The measured maximum DNL and INL were 1.65 and 2.49 LSB without application of the proposed digital calibration, and 0.69 and 1.01 LSB with application of the proposed digital calibration, respectively. The INL results show a bimodal behavior of 1/8 periodic change in the full range, which arises from the structure of the ramp signal generator.

The ADC output in the dark condition is measured according to the readout channel number, as shown in Fig. 16. The average ADC temporal noise value is 0.23 LSB_{rms}, which corresponds to 88.56 μV_{rms}.

Regarding the length of the A/D conversion process, Fig. 17 shows the number of conversion clocks involved in the conventional and proposed SS ADC cases depending on the resolution. When compared with the conventional SS readout scheme, the proposed readout scheme can effectively reduce the number of conversion clocks in A/D_{RST} by almost half, which corresponds to approximately 38.4% of the total

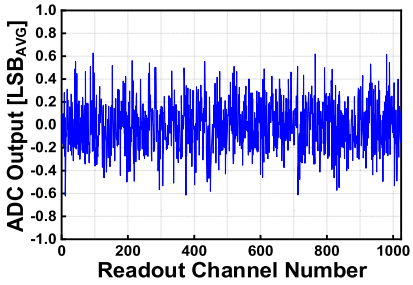


Fig. 16. Measured ADC output under dark condition.

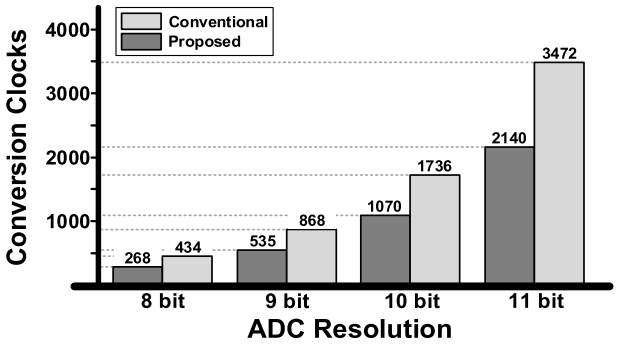


Fig. 17. Comparison of the numbers of conversion clocks in the conventional and proposed SS ADC.

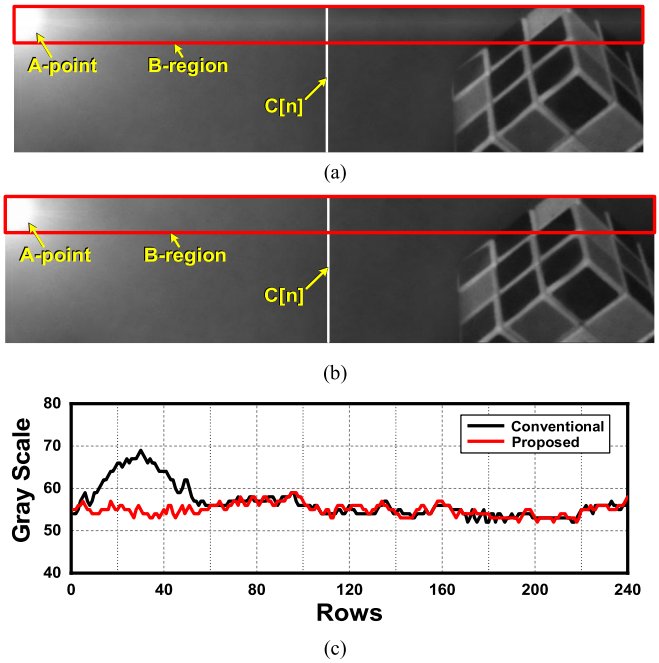


Fig. 18. Captured image with digital gain of 4. (a) Without the CBS technique. (b) With the CBS technique. (c) Gray scale along with C[n].

conversion clocks for 11-bit resolution. To perform a fair comparison, it assumes that the conventional SS readout scheme has the same number of conversion clocks for A/D$_{SIG}$ as the proposed readout scheme. This result is significant and demonstrates that the proposed readout scheme becomes more effective as the bit depth of the ADC increases. Although the reduction ratio of the total conversion clocks is the same (38%) as the ADC resolution increases, the number of absolute saving conversion clocks increases. As compared to the conventional scheme, the proposed scheme reduces the horizontal readout time by 29.8% that results in the high frame rate by the same amount.

Fig. 18 shows the captured image obtained with digital gain of 4 by the prototype CIS. A bright light source of intensity greater than 10 000 lux was focused on the upper left side (A-point in Fig. 18). The coupling noise induced by global lines of column-parallel ADCs appeared as horizontal stripes [B-region in Fig. 18(a)]. Because horizontal stripes are further visible at dark illumination conditions, the image quality appears to be worse. However, this problem can be alleviated upon adoption of the CBS technique whereby the coupling effect was reduced via isolation and shielding of the adjacent columns [Fig. 18(b)], as discussed earlier. The values of the pixels along the *C*th-column(C[n]) are shown in Fig. 18(c) for both cases of Fig. 18(a) and (b). After the CBS technique was applied, the horizontal stripes were reduced by lesser than 1 LSB of the 11-bit resolution, along with maintenance of the original image quality.

The measured performances of the prototype chip are summarized in Table I. The total power consumption was 57.2 mW with 2.8 V for the pixel array and 1.8 V for the readout

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Technology	0.11 μm 1P4M CIS Process
Total area	4.15 × 2.55 mm
Supply voltages	2.8 V (Pixel), 1.8 V (Circuit)
Power consumption	57.2 mW
Number of pixels	1024 (H) × 240 (V)
Pixel type	4-TR (Pinned Photodiode)
Pixel size	2.9 μm × 2.9 μm
Sensitivity	2.4 V/lx·s
Conversion gain	82 μV/e$^-$
Random noise	2.05 e$^-_{rms}$
Column FPN	0.81 LSB$_{rms}$
Dynamic range	73.6 dB
ADC resolution	11-bits
DNL / INL	0.69 LSB / 1.01 LSB
ADC noise	1.08 e$^-_{rms}$
Frame rate	570 fps
Data rate	140.08 Mp/s

circuitry. The time consumed for the readout of one row was 7 μs. A test SS ADC with 11-bit resolution was demonstrated to run at a conversion rate of 410 kS/s.

Table II presents a comparison of the performances of the proposed CIS and recently reported works. To perform a fair CIS performance evaluation, various figure of merits (FoM) were calculated with their own specifications and attained performances, as in [32] and [33]; FoM$_1$ and FoM$_2$ are used for representing the performance of CMOS imagers, FoM$_3$,

TABLE II
PERFORMANCE COMPARISON

	JSSC'16 [4]	TED'16 [27]	ISSCC'17 [28]	ISSCC'18 [29]	ISSCC'19 [30]	Sensors'20 [16]	TCAS-I'20 [23]	JSSC'20 [31]	This work
Process (μm)	0.18	0.09	0.13	0.09	0.11	0.09	0.11	0.11	0.11
Supply voltage (V)	2.8/1.8	2.8/1.2	-	1.8/1.0	3.3/1.5	2.8/1.5	3.3/1.5	2.8/2.2/1.5	2.8/1.8
Pixel type	4T APS	4T APS	4T APS	4T APS	4T APS	4T APS	4T APS	4T APS	4T APS
Pixel pitch (μm)	4.4	2.24	3.4	1.5	4	5.6	6.5	4	2.9
Pixel resolution	160 x 120	1936 x 840	2592 x 2054	2560 x 1536	640 x 480	960 x 720	128 x 128	640 x 640	1024 x 240
Frame rate (fps)	1000	60	120	60	500	35	228	44	570
ADC type	SAR	SAR/SS	SS	SS	SS	TS SS	SS	SS	FHR SS
ADC resolution (bit)	10	12	10	10	10	12	10	10	11
ADC dynamic range (dB)	60	62	73.1	67	-	66.7	68.9	67	73.6
Pixel rate (Mp/s)	19.2	97.6	638.88	235.93	154	24.2	3.74	18.02	140.08
Random noise (μV_{rms})	670 (11 e^-_{rms})	527 ([1]6.43 e^-_{rms})	148 ([1]1.8 e^-_{rms})	100 (1.8 e^-_{rms})	160 (1.95 e^-_{rms})	472 ([1]5.76 e^-_{rms})	411 ([1]5.01 e^-_{rms})	476 (6.1 e^-_{rms})	168 (2.05 e^-_{rms})
Power consumption (mW)	1.5	[2]81.8	450	95	76	28	40	2.1	57.2
[3]FoM_1 [e^-·nJ]	0.86	5.39	1.26	0.72	0.96	6.66	53.58	0.71	0.84
[4]FoM_2 [e^-·pJ/step]	0.84	1.36	1.24	0.71	0.94	1.63	52.33	0.69	0.41
[5]FoM_3 [e^-/MHz]	91.67	127.58	7.3	19.53	8.13	229	171.7	216.6	14.99
[6]FoM_4 [e^-/MHz/step]	89.52	31.15	7.13	19.07	7.93	55.8	167.6	211.5	7.32

1) For fair comparison, conversion gain is assumed by 82 μV/e^-
2) Power consumption = [ADC power in the readout channel] x [The number of readout channels] + [ADC peripheral circuit power]
3) FoM_1 = [Noise] x [Power consumption] / [The number of pixels] / [Frame rate]
4) FoM_2 = [Noise] x [Power consumption] / [The number of pixels] / [Frame rate] / 2^[ADC resolution]
5) FoM_3 = [Noise] / [The number of vertical pixels] / [Frame rate]
6) FoM_4 = [Noise] / [The number of vertical pixels] / [Frame rate] / 2^[ADC resolution]

and FoM_4 are used for representing the performance of readout ADCs. For the chosen pixel array format, those FoMs reflect the performance change as the pixel rate increases. For various FoMs, the prototype CIS demonstrates state-of-the-art level performances: FoM_1 of 0.84 e^-·nJ, FoM_2 of 0.41 e^-·pJ/step, FoM_3 of 14.99 e^-/MHz, and FoM_4 of 7.32 e^-/MHz/step. Regarding FoM_2, this work shows the competitive performance compared to other works.

V. CONCLUSION

This work introduced a high-speed low-power SS ADC that operates on the proposed FHR scheme. The proposed scheme alleviates the structural limitation of conventional SS ADCs by performing binary-weighted searching algorithm in the first A/D conversion attempt. This study demonstrated speed enhancement by the proposed scheme amounting to 38.4% for 11-bit SS ADC design; additionally, its effectiveness was shown to increase as the ADC resolution increases. Moreover, the proposed ADC architecture was proven to be easily reversible to operate as the conventional SS algorithm, and it can thus be utilized in various applications as per requirement. Therefore, it is an effective technique for improving the conversion speed to realize high frame rate CISs.

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