An Efficient and Implementation-friendly Method for More Smart ADC Design with Dynamical Energy Optimization in Edge Computing

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Abstract—As precision adaptive computing has already been widely studied for more efficeint Neural Networks (NNs), Analog-to-Digital Converters (ADCs), which dominate the power consumption of traditional sensing systems, can also be smartly designed for more intelligent edge computing. In this work, we propose a method combining adaptive precision and fine-grained power management strategies for more smart ADC design with dynamical energy optimization. We present two case study ADC designs and demonstrate the effectiveness of the proposed method in detail. Results show that almost a half of the ADCs' power consumption can be reduced in the low precision mode, while the cost of extra control circuits is rather small. As this method is easy to resonate with multiple downstream algorithms, it will be promising for ultra-efficient edge computing in the future.

Index Terms—ADC, precision adaptive, power management, energy-efficient, edge computing

I. Introduction

With the development of the Internet-of-Things (IoT), edge devices like mobile phones, smart watches, and other portable products have been playing an important role in people's daily lives for collecting and processing data in site and in time. On the other hand, Neural Networks have shown broad prospects for sensing applications, such as computer vision, speech recognition, and robotics. Therefore, deploying NNs on edge devices is an emerging trend which leads to many efforts of research.

To integrate large and computationally intensive NN models on edge devices of which the power supply and computing resources are quite limited, improving the systems' energy efficiency is critical. While compression and optimization of NN models have been extensively studied [xxxx], Analog-to-Digital Converters, which dominate the power consumption of traditional sensing systems, have been generally treated as black boxes.

However, as more and more intelligent algorithms are able to process data of varying precision for different tasks[xxxx], opportunities have been offered for us to achieve better energy efficiency by taking algorithm-aware adjustments inside the ADCs. Considering the precision (i.e. the quantization bits) is at the heart of an ADC's energy constraints, making it dynamically adaptive will be promising.

In certain applications, such as image processing, the camera's resolution has already been considered to be dynamically adaptive for efficient multi-task analysis [xxxx], where the precision of ADCs has not been considered as a variable. Besides, there are efforts trying to relieve the design specifications of ADCs by applying low-precision analog computing firstly close to the sensor [xxxx]. But high-precision ADCs and NN processors are still there for complex tasks. Therefore, dynamical energy optimization inside ADCs remains competitive.

Motivated by these facts, we mainly makes the following contributions in this paper:

1) A method combining adaptive precision and power gating is proposed for more smart ADC design with dynamicall energy optimization. With the fine-grained power management strategies, which have rarely been studied before, we successfully reduce the ADCs' power consumptionin to nearly half in the low-precision mode.

2) Two case study ADC designs are presented. The first one is column-parallel Single-Slope (SS) ADCs and the second is column-parallel SAR/SS ADCs. We analyze the power distribution of the ADCs in detail and demonstrate the effectiveness of the proposed method with specific simulating results. Both of the two designs can be applied in the CMOS Image Sensors (CISs) and are suitable for different design specifications.

3) As the evaluation results are easy to extend and the extra

control logic is implementation-friendly, we argue for the universality of the proposed method for ADCs of not only different architectures but also varying application scenarios.

The remainder of this paper is organized as follows. Sect. II presents the architecture overview of the two case study ADC designs. Sect. III describes the adaptive precision and power gating strategies for the two case study ADC designs, specifically. Sect. IV reports the evaluation results and Sect. V develops discussions. Finally, Sect. VI concludes this paper.

II. ARCHITECTURE OVERVIEW

A. Architecture of the SS ADCs

The overall architecture of the SS ADCs is presented in Fig. 1. The main modules include column-parallel Correlated Double Sampling (CDS) circuits, comparators, and a column-shared ramp generator. Fig. 2 shows the basic operational waveform of the SS ADCs. When the ramp signal exceeds the output of a CDS circuit in a certain column, the corresponding comparator will be flipped and latch the time information Δt in the 8-bit registers in that column as conversion results. And Such conversions across all columns will be done as soon as the ramp signal reaches V_{refh}.
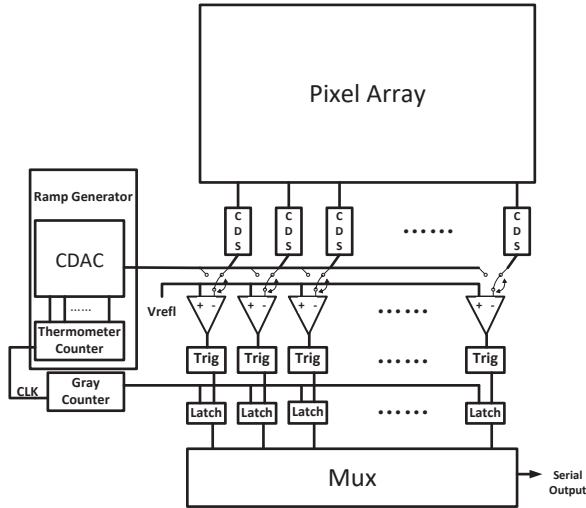

Fig. 1. Overall Architecture of the SS ADCs.

As the structure of the three main modules are described more specifically as follows, details of the three waves in Fig. 2 are also revealed.

1) CDS Circuits: CDS circuits are the interface between the pixel array and the ADCs, responsible for subtracting the pixels' signal voltages from reference voltages and amplifying the difference by a certain coefficient. The difference (i.e. ΔV in Fig. 2) is physically attached to the exposure time of the pixels, and the subtraction will help cancel the noises caused by the varying reference voltages.
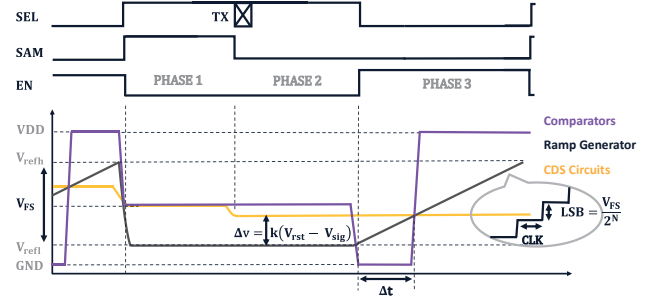

Fig. 2. Operational waveform of the SS ADCs.

Switched-capacitor operational amplifiers are commonly used in CDS circuits as presented in Fig. 3. According to the law of charge conservation, the output voltage of the CDS circuits (in PHASE2 of Fig. 2) can be calculated as (1). It is noticed that the Input Offset Cancelation (IOS) is realized, which is necessary because the amplifiers in different columns may have different offset voltage.
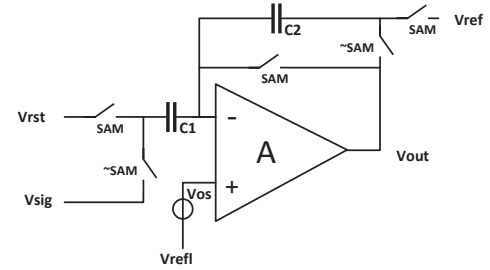

Fig. 3. the Structure of the CDS Circuits.

$$V_{out} = \left[V_{ref} + \frac{C_1}{C_2} * (V_{rst} - V_{sig}) \right] * \frac{\beta A}{1 + \beta A}$$
$$+ (V_{refl} + V_{os}) * \frac{A}{1 + A} * \frac{1}{\beta A} \qquad (1)$$
$$where \quad \beta = \frac{C_2}{C_1 + C_2}$$

2) the Ramp Generater: As presented in Fig. 4, the ramp generator consists of a thermometer counter and a Capacitor Digital-to-Analog Converter (CDAC). While the capacitors in CDAC are being switched one by one from V_{refl} to V_{vefh}, the output voltage of the ramp generator will be as (2) according to the law of charge conservation. In this equation, N means the number of switched capacitors and M means the total number of capacitors of the same size (for the 8-bit precision, the total number will be 255). Therefore, as in PHASE3 of Fig. 2, the ramp signal will be like stages from V_{refl} to V_{refh}, of which the range is consistent with the output of CDS circuits. And the height of every stage is actually the Least Significant Bit (LSB) converted by the ADCs.

The three buffers in Fig. 4 make sure that the reference voltages and ramp signal have enough driving capability, and

the output buffer will be in the largest size because it has to drive hundreds of column-parallel comparators.
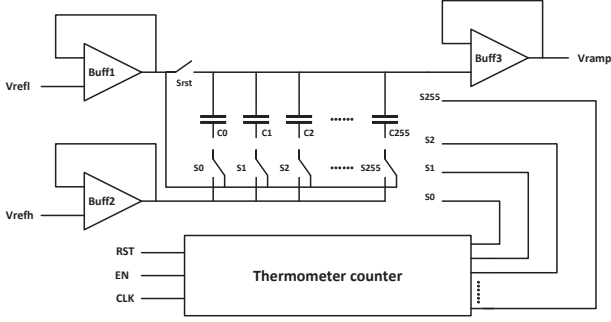

Fig. 4. the Structure of the Ramp Generator.

$$V_{ramp} = V_{refl} + \frac{N}{M} * (V_{refh} - V_{refl}) \qquad (2)$$

3) Comparators: The comparators work for comparing the CDS circuits' output and the ramp signal. In the SS ADCs, two-stage open-loop comparators can be applied as presented in Fig. 5. Again according to the law of charge conservation, the comparators' output (in PHASE3 of Fig. 2) can be calculated as (3). The comparison will be dominated by $V_{ramp} - V_{cds}$ as long as the amplifiers' open-loop gain is large enough and the IOS is realized. Besides, the comparators' speed depends on the amplifiers' bandwidth and slew rate.
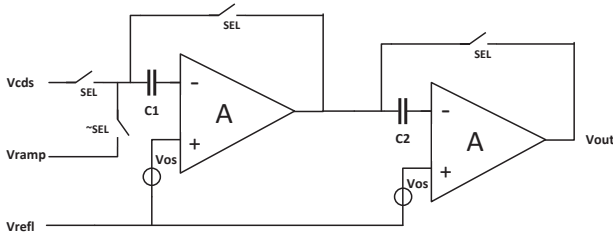

Fig. 5. the Structure of the Comparators in the SS ADCs.

$$V_{out} = A^2(V_{ramp} - V_{cds})$$
$$+ (V_{refl} + V_{os}) * \frac{A}{1 + A} \qquad (3)$$

B. Architecture of the SAR/SS ADCs

The overall architecture of the SAR/SS ADCs is almost the same as the SS ADCs, and the only difference is that the comparators are now replaced with low-precision (4bit) SAR sub-ADCs as presented in Fig. 6, where the ramp signal is connected to one of the unity capacitors.

While generating the upper 4-bit results, the SAR/SS ADCs will change V_X in Fig. 6 according to SAR logic. That means

after 4 comparisons with the reference voltage, V_X will be as (4), where $D_U[i]$ is the i th bit of the upper 4 bits. Then, the ramp generator will start working and make V_X increase gradually as (5), where the range of the V_{ramp} is from gnd to $Vref$ (rather than V_{refl} to V_{refh} as in the SS ADCs) to avoid too small LSB, and $D_L[i]$ is the i th bit of the lower 6 bits. Therefore, when the $V_{X.2}$ reaches V_{ref}, the corresponding V_{cds} will be as (6), showing that the pixels' $(V_{rst} - V_{sig})$ can be represented by the 10-bit conversion results, exactly.

The related operational waveform is presented in Fig. 7. It is obvious that the upper 4-bit results (as the second last item of (6)) are generated from the SAR logic and the lower 6-bit results (as the last item of (6)) is counted according to the time between the ramp signal's start and the comparators' last flip.
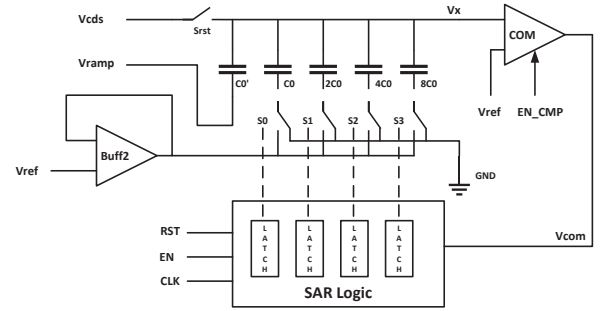

Fig. 6. the Structure of the SAR Sub-ADCs in the SAR/SS ADCs.

$$V_{X.1} = V_{cds} + \sum_{i=1}^{4} \frac{V_{ref}}{2^i} * D_U[i] \qquad (4)$$

$$V_{X.2} = V_{X.1} + \frac{V_{ramp}}{2^4}$$
$$where \; V_{ramp} = \frac{V_{ref}}{2^6 - 1} * \sum_{i=1}^{6} 2^{6-i} * D_L[i] \qquad (5)$$

$$V_{cds} = k * (V_{rst} - V_{sig})$$
$$\approx V_{ref} - \sum_{i=1}^{4} \frac{V_{ref}}{2^i} * D_U[i] - \sum_{i=1}^{6} \frac{V_{ref}}{2^{4+i}} * D_L[i] \qquad (6)$$

As for the comparators inside the low-precision SAR sub-ADCs, the strong-arm with pre-amp structure is applied, as presented in Fig. 8. Such comparators are suitable for multiple comparisons because high speed is easy to achieve. Besides, the pre-amps' offset voltages can be canceled effectively through the Output Offset Cancelation (OOS) technique [x].

The total number of clocks for conversion in the SAR/SS ADCs are 68 $(4 + 2^6)$, which is much less than the SS ADCs where 1024 clocks (for 10 bits) are required. However, the SAR/SS ADCs have traded off area for less conversion clocks. Therefore, for different design specifications, different arcitecture can be chosen.

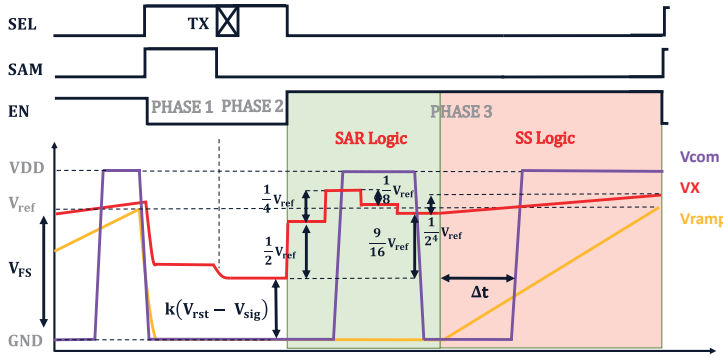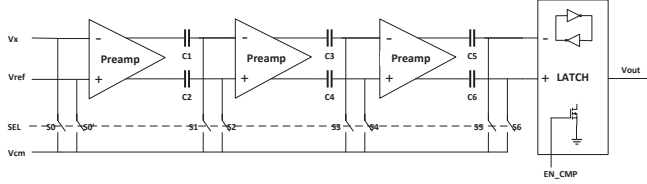Fig. 7. the Structure of the SAR Sub-ADCs in the SAR/SS ADCs.

Fig. 8. the Structure of the Comparators in the SAR Sub-ADCs.

III. ADAPTIVE PRECISION AND POWER GATING STRATEGIES

A. Power Gating Implementation

The power gating can be implemented simply by adding PMOS-transistor switches between the functional blocks and the supply voltage [x]. When the switches are turned off, the corresponding blocks' current paths will be cut off, thus the energy is saved. It is obvious that the more currents are under control, the more effective the power gating is. However, to avoid unacceptable IR drop, the total size of the switches will be large, thus inverters should be inserted between the control signal and the switches' gates for adequate driving capability. Besides, the functional blocks' recovery speed from power off should be taken into consideration, because the slower the speed is, the less time the blocks can be power gated.

B. Strategy for the SS ADCs

As evaluated in Sect. IV, the SS ADCs' power consumption is mainly taken up by the column-parallel comparators, bias circuits, and the output buffer of the ramp generator. Considering that all bias circuits are settled down only once (tens of microseconds after the whole system's power up) and then other circuits can be settled down quickly by the distributed bias circuits, we just apply power gating to the comparators and the output buffer.

The related waveform are presented in Fig. 9. In the low-precision mode, the thermometer counter should have been extended to support switching the capacitors in CDAC 16 by 16 rather than one by one, thus the ramp signal will reach V_{refh} in 16 clocks (for 4 bits) rather than 256 clocks (for

8 bits). After the 16 clocks, the comparators and the output buffer can be power gated for a long time with the output signals drop gradually.
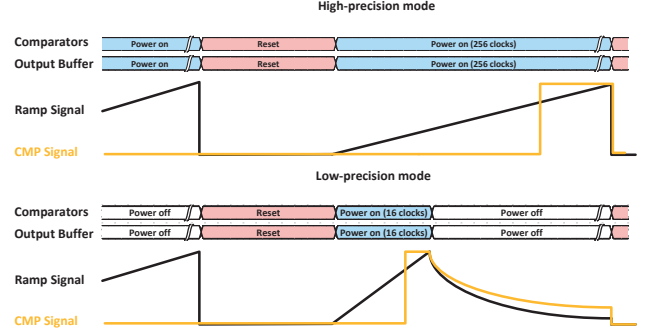

Fig. 9. Power Gating and Adaptive Precision Strategies for the SS ADCs.

C. Strategy for the SAR/SS ADCs

As evaluated in Sect. IV, the SAR/SS ADCs' power consumption is mainly taken up by the column-parallel buffers of SAR logic and comparators, which can be power gated with adaptive precision as presented in Fig. 10. It shows that in the low-precision mode, the ramp signal is generated as usaual but the comparators will be power off then, leaving the 4-bit results converted completely by the SAR logic.

Compared with the SS ADCs, the thermometer counter in the SAR/SS ADCs does not need to support two modes for adaptive precision. Besides, the start signal of the ramp generator and the power off signal of the comparators can be the same. As for the proportion between the power gating time and the conversion time, 64/68 is achieved in the SAR/SS ADCs, which is similar to the number 240/256 in the SS ADCs.
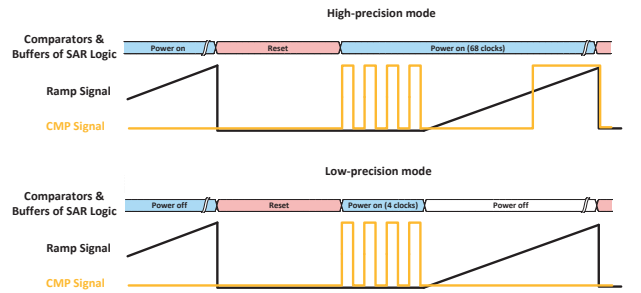

Fig. 10. Power Gating and Adaptive Precision Strategies for the SAR/SS ADCs.

IV. EVALUATION RESULTS

This section provides quantitative results of the two case study ADC designs' fundamental characteristics and energy-saving performance. The statistical data is obtained from simulation in Virtuoso's AMS Environment. Although some

digital modules are in behavior level written by Verilog, we argue that the power consumption of this parts can be ignored because these digital modules do not have static current paths.

A. Evaluation of the SS ADCs

The fundamental characteristics of the SS ADCs are summarized in Table I. Assuming a 512×512 pixel array, the frame rate will be xx fps. The SNDR of SS ADCs is xx dB/ xx dB, which means the ENOB is 3.x bits/ 7.x bits. The power consumption of the SS ADCs is measured and divided by columns, it shows that compared to xx uW/column in the high-precision mode, only xx uW/column is needed in the low-precision mode, reduced by almost a half. A more specific energy analysis is presented in Fig. 11. As we can see, most parts of the power consumption are taken up by the column-parallel comparators and output buffer of the ramp generator, both of which can be power gated effectively in the low-precision mode. The related quantity results is presented in Fig. 12, where the peripheral circuits include a bandgap and voltage divider, some level-shift circuits and global buffers.

TABLE I
PERFORMANCE OF THE SS ADCs

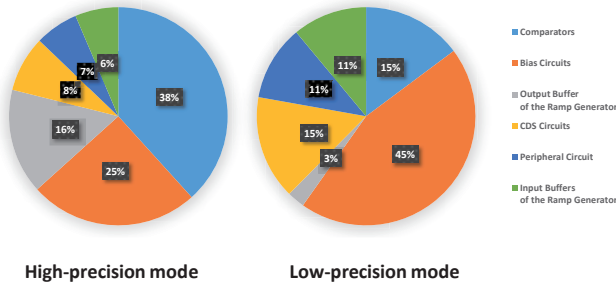| Prameter	Value
Process	65nm
Supply voltage	2.5V/1.2V
Clock Frequency	25 MHz
Architecture	SS
Quantization bits	4/8
Conversion time (us)	2.4 us/12 us
Number of parallel columns	512
Throughput (samples per second)	42.7MSPS
Power (per column)	40.8 uW/76.2 uW
SNDR	
Fom	

Fig. 11. Power Saving Results of the SS ADCs.

B. Evaluation of the SAR/SS ADCs

The fundamental characteristics of the SAR/SS ADCs are summarized in Table II. While the throughput is set similar to the SS ADCs, a lower clock frequency is required. The SNDR is xx dB/ xx dB and the ENOB is 3.x bits/ 9.x bits, consistent with the design specifications. The power
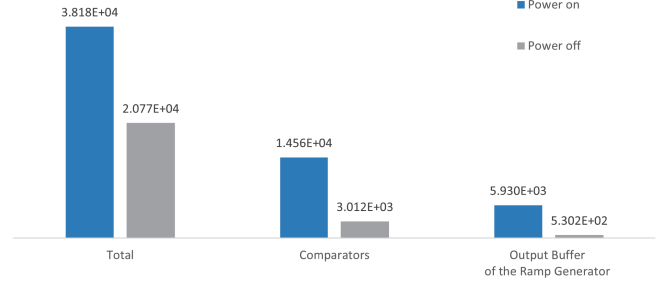

Fig. 12. Power Saving Results of the SS ADCs.

consumption is xx uW/column in the high-precision mode and xx uW/column in the low-precision mode, respectively. According to the energy analysis presented in Fig. 13, most parts of the SAR/SS ADCs' power consumption are taken up by the column-parallel comparators and buffers of SAR logic. And in the low-precision mode, this parts' energy can also be reduced to nearly half. The related quantity results is presented in Fig. 14.

TABLE II
PERFORMANCE OF THE SAR/SS ADCs

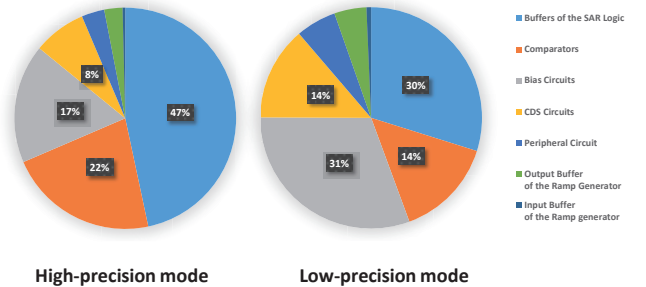| Prameter	Value
Process	65nm
Supply voltage	2.5V/1.2V
Clock Frequency	25 MHz
Architecture	SS
Quantization bits	4/8
Conversion time (us)	2.4 us/12 us
Number of parallel columns	512
Throughput (samples per second)	42.7MSPS
Power (per column)	40.8 uW/76.2 uW
SNDR	
Fom	

Fig. 13. Power Saving Results of the SAR/SS ADCs.

V. DISCUSSIONS

With precision adaptive and power gating strategies, both the SS ADCs and SAR/SS ADCs can save energy dynamically and significantly.
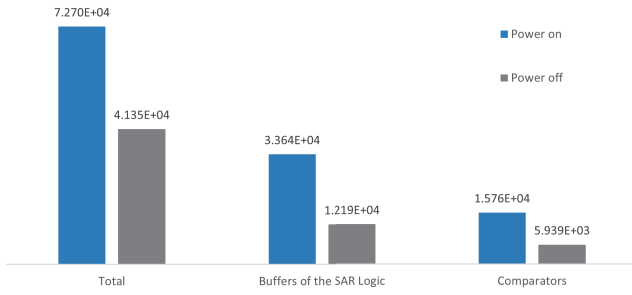
Fig. 14. Power Saving Results of the SAR/SS ADCs.

In comparison, the SAR/SS ADCs can support higher quantization bits and require fewer extra control circuits for the adaptive precision, while SS ADCs inherently require less area and can effectively applied in the 4/8-bit situation. Therefore, according to specific design specifications, different structures can be chosen.

For other different precision configurations (e.g. 2/8 adaptive precision) and number of parallel collumns, the corresponding power consumption and energy-saving performance can also be estimated with extending the evaluation results in Sect. IV.

VI. CONCLUSIONS

In this work, a method combining adaptive precision and power gating is proposed for more smart ADC design with dynamicall energy optimization. According to the evaluation results of two CIS-applied ADC designs, almost a half of the ADCs' power consumption can be reduced in the low precision mode, while the cost of extra control circuits is rather small.

The method in this paper is universal and has prospects to be combined with varying downstream intelligent algorithms for efficient multi-tasks analysis. As such an integrated system will be more promising for edge computing in the future, more works on the co-design of ADCs and algorithms remain to be developed.

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