A 6-to-10-Bit 0.5 V-to-0.9 V Reconfigurable 2 MS/s Power Scalable SAR ADC in 0.18 μm CMOS

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***Abstract*—An asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) for sensor applications is presented. High linear and power efficient switching scheme is proposed. The proposed low leakage latched dynamic cell in SAR logic and wide range configurable delay element extend the flexibility of speed and resolution tradeoff. The ADC fabricated in 0.18 μm CMOS process covers 6–10 bit resolution and 0.5 V–0.9 V power supply range. At 10 bit mode and 0.5 V operation, the proposed SAR ADC achieves 56.36 dB SNDR and 67.96 dB SFDR with sampling rate up to 2 MS/s, corresponding to a figure-of-merit of 20.6 fJ/conversion-step. The proposed ADC core occupies an active area of about $300 \times 700\ \mu m^2$.**

***Index Terms*—Low power, power scalable, resolution reconfigurable, SAR ADC.**

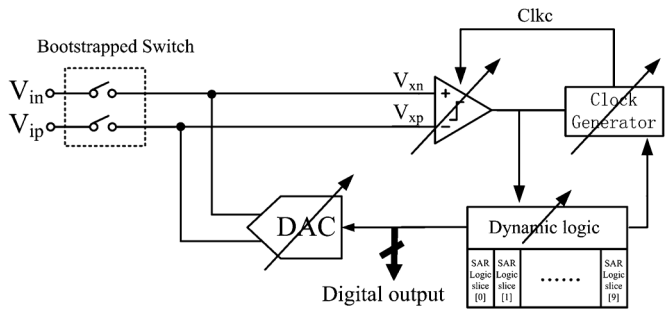

Fig. 1. Block diagram of proposed flexible asynchronous SAR ADC.

I. Introduction

THE miniaturization of electronics has enabled the development of wireless sensor networks which consist of many distributed nodes, each equipped with sensors and low power circuits to acquire, process, and transmit the signal of interest. The analog-to-digital converter (ADC) is responsible for interfacing the physical world to the digital signal processing unit. For most energy constrained systems, it benefits to adapt the ADC performance to the signal of interest to avoid power consumed on unnecessary accuracy or bandwidth. In this context, an energy-efficient and reconfigurable SAR ADC is indispensable. Among various types of ADC architectures, the successive approximation register (SAR) ADC is suited for low power and low voltage design due to its simplicity and easiness to be integrated with other blocks.

Recently, SAR ADCs are intensively studied. Several reported SAR ADCs have achieved exceptional energy efficiency [1]–[4]. Ref[1] present a 8-bit 500 KS/s with an energy-saving bottom-plate switching scheme. However, compared to top-plate switching scheme, a bottom-plate one doubles the capacitors of DAC array which cost area and power. Reference [2] presented low voltage reconfigure SAR ADC. However, the resolution-reconfigurable segmented DAC is vulnerable without calibration since a segmented DAC is highly sensitive to parasitics. In addition, the core area of the ADC is not competitive either. SAR ADC with flexible resolution and speed has been proposed in [3]. However, it lacks the ability to operate at supplies below 1 V. A modified version of [3] was proposed in [4] which achieved extraordinary power-efficiency. However, the leakage issue in the asynchronous dynamic logic remains to be solved.

A capacitor splitting scheme is power-efficient compared to 2-Step Switching and Charge Sharing (CS) one [5]. Inspired by this fact, we present a novel capacitor splitting switching scheme with configurable resolution. Switching energy and static nonlinearity based on the V_{cm}-based and proposed switching schemes are analyzed in detail. Behavioral model for the supply noise rejection is developed to verify the effectiveness of the analysis. The leakage issue in dynamic logic is subtly eliminated thanks to the proposed dynamic logic cell. Based on these techniques, an energy efficient resolution configurable asynchronous SAR ADC in 0.18μm 1P6M CMOS process is presented.

In the following sections, Section II presents the SAR ADC architecture and describes techniques used to achieve resolution reconfiguration. Section III presents prototype measurement results, and Section IV concludes the paper.

II. Architecture Description

This section describes the details of the proposed SAR ADC architecture. Low power asymmetric switching scheme is proposed. Power consumption, linearity performance and power supply noise sensitivity of the DAC circuits are discussed. Several techniques are presented to extend the flexibility of speed and resolution tradeoff. Fig. 1 shows the architecture of the SAR ADC. Differential architecture is chosen to improve power supply and common mode rejection. The input voltage is sampled on the capacitor arrays inside the DAC. The asynchronous clock generators clock for the dynamic comparator based on self-synchronization. Thus, only a sample-rate clock instead of an oversampled clock is required. The dynamic SAR control logic resolves the bits of the output code.

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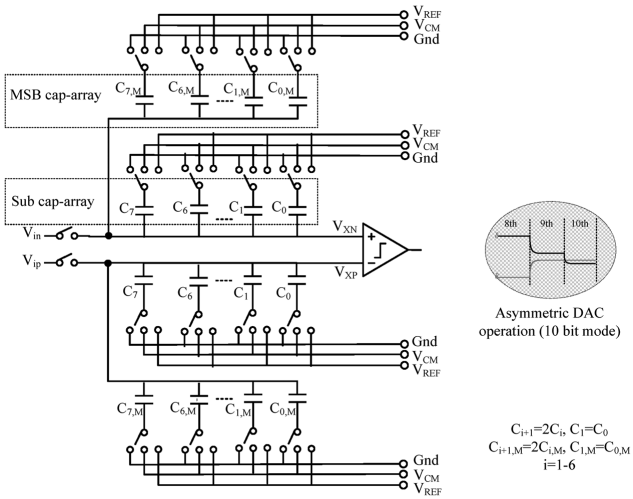

Fig. 2. Capacitive DAC architecture.

A. Capacitive DAC With Asymmetric Switching Scheme

Fig. 2 shows the proposed switching scheme. The MSB capacitor has been splitted into an identical copy (MSB cap-array, $C_{0,M} - C_{7,M}$) of the rest of the array (Sub cap-array, $C_0 - C_7$). In the conversion phase, once the MSB comparison is finished, different reference voltages will be chosen for the differential capacitor arrays according to the value of MSB. If $V_{XP} < V_{XN}(MSB = 1)$, the bottom-plates of the MSB cap-array capacitors on the V_{XP} side are charged to V_{ref} and the MSB cap-array on the V_{XN} side are switched to ground. Thus, V_{XP} is level-shifted up by $1/4V_{ref}$ and V_{XN} is level-shifted down by $1/4V_{ref}$. Then the comparator does the comparison again. In the case of MSB $= 1$ and 2nd-MSB $= 1$, the largest capacitor of the main sub-array on the V_{XN} side is switched from V_{cm} to Gnd, and the largest capacitor of the main sub-array on the V_{XP} side is switched from V_{cm} to V_{ref}. In the case of $MSB = 1$ and 2nd-MSB $= 0$, the largest capacitors of the MSB sub-array on both sides are reconnected to V_{cm}, and the largest capacitors of the main sub-array on both sides remain unchanged. The ADC repeats the procedure until the bottom plate of C_1 is switched and the 2nd-LSB is decided. The asymmetric DAC operation is performed in the decision of LSB. In 10 bit mode, for example, one of the complementary C_0 is switched to set one of the references according to the SAR logic. However, C_0 on the other side maintains connected to V_{cm} in all of the conversion phases. The asymmetric switching scheme halves total capacitance of the DAC and saves power consumption.

B. Energy Efficiency and Resolution Reconfigurability

Assuming that the output codes are uniformly distributed, and the unit capacitors are assumed to be identical to each other for uniform matching. Behavioral simulations of differential 10-bit SAR ADC based on previously published switching schemes [6]–[9] and the proposed scheme were preformed and analyzed in MATLAB. The switching energy at each output code for the switching schemes is plotted in Fig. 3(a). The energy of Switch-Back scheme is higher than our proposed scheme at the middle range of codes, and is lower when converting the high/low codes. However, since the common mode voltage of the output voltage of DAC in Switch-Back scheme changes in every bit conversion, it could have dramatic influence on the offset of comparator. Fig. 3(b) shows the average switching energy versus resolution for each of the switching schemes, demonstrating that the proposed switching scheme remains energy efficient down to 7 bits.

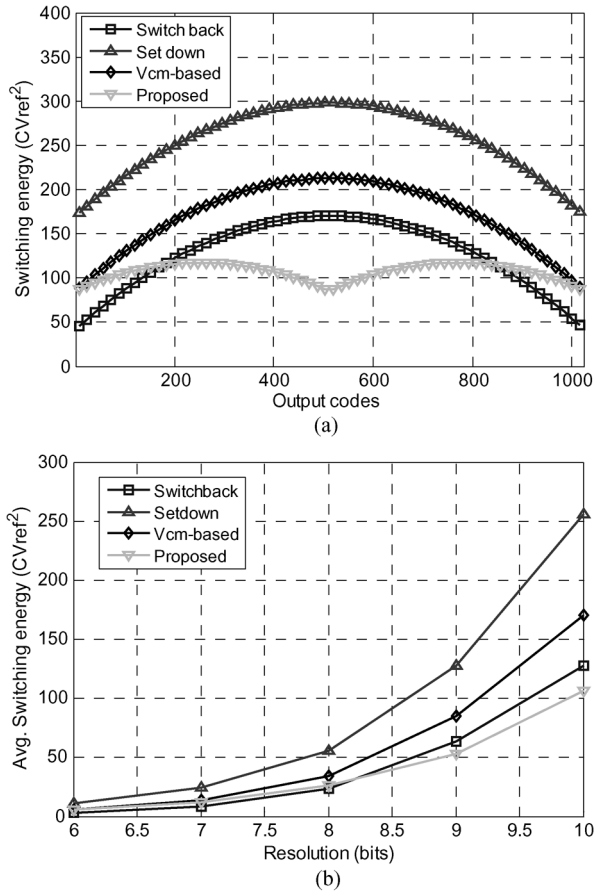

Fig. 3. Energy efficiency of switching scheme. (a) Comparison of switching energy versus output code for a 10-bit ADC. (b) Average switching energy versus resolution.

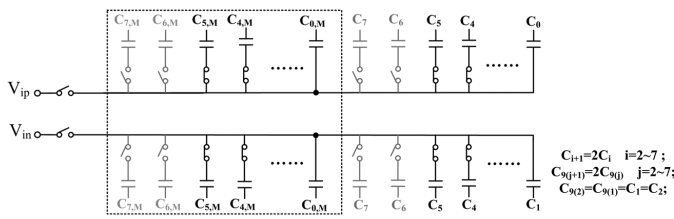

Fig. 4. Reconfigurable DAC example in 8-bit mode.

The DAC is configurable according to the selected resolution to achieve high energy efficiency. The capacitors are selected to be disabled and disconnected from the capacitor array for lower resolution settings while the kT/C noise floor is kept suppressed far below quantization noise. The 8-bit modes DAC example is shown in Fig. 4. Note that the asymmetric DAC operation still fits well when the resolution is reduced. The proposed scheme exhibits smaller voltage glitches at the top-plates since only smaller fraction of the capacitor array is charged and discharged during bit cycling iteration.

C. Linearity Consideration

Besides minimizing the switching energy of the capacitor array through architectural optimizations, the unit capacitance

C_0 should be sized for sufficient matching at each level of resolution. In most cases, mismatch is dominant over thermal noise. In the following discussion, each of the capacitors in the DAC is modeled as the sum of the nominal capacitance value and the error term.

$$C_i = 2^{i-1}C_u + \delta_i (i = 1 \sim N-1)$$
$$C_1 = C_0 \quad (1)$$

Assume the error distributions of unit capacitors are independent and identically distributed (i.i.d.) Gaussian random variables, and have a variance of

$$E\left[\delta_i^2\right] = 2^{i-1}\sigma_u^2 \quad (2)$$

where σ is the standard deviation of the unit capacitor.

To calculate a given digital input X with its corresponding DAC output $V_{DAC}(X)$, the array is considered initially discharged. The analog output of the N bit capacitive DAC can be expressed as

$$V_{DAC}(X) = \frac{\sum_{i=1}^{N-1}(2^{i-1}C_u + \delta_i)S_i + (C_u + \delta_0)S_0}{2^{N-1}C_u + \sum_{i=0}^{N-1}\delta_i} \quad (3)$$

where the DAC digital input $X = [S_i \cdots S_0]$, with S_i equal to 1, 1/2 or 0 representing the DAC connecting to V_{ref}, V_{CM} or Gnd for bit i. The error term $\sum_{i=0}^{N-1}\delta_i$ in the denominator of (3) will be neglected for this discussion because the mean of $\sum_{i=0}^{N-1}\delta_i$ should statistically equal to 0. Subtracting the nominal value yields:

$$INL(X) = \frac{V_{DACP,real}(X) - V_{DACP,ideal}(X)}{LSB} \quad (4)$$

And DNL can be expressed as:

$$DNL(X) = INL(X) - INL(X-1) \quad (5)$$

Since MSB is determined mismatch-independently, the maximum INL is expected to occur at the $V_{FS}/4$ or $3V_{FS}/4$:

$$INL_{\max,proposed} = INL\left(\frac{V_{FS}}{4}\right) = \frac{\sum_{i=0}^{N-3}\delta_i + \sum_{i=0}^{N-3}\delta_{i,b}}{2^{N-1}C_u}\frac{V_{CM}}{LSB} \quad (6)$$

with variance

$$E\left[\delta^2_{\max,INL,proposed}\right] = \frac{2^{N-2}\sigma_u^2}{2^{2N-2}C_u^2}\frac{V_{CM}^2}{LSB^2} = \frac{1}{4}\frac{2^N\sigma_u^2}{C_u^2} \quad (7)$$

The variance of DNL can be expressed as

$$E\left[\delta^2_{\max,DNL,proposed}\right] = E\left[\left(\frac{\delta_{N-2}+\delta_{N-2,b}-\sum_{i=0}^{N-3}\delta_i - \sum_{i=0}^{N-3}\delta_{i,b}}{2^{N-1}C_u}\frac{V_{CM}}{LSB}\right)^2\right] = \frac{1}{2}\frac{2^N\sigma_u^2}{C_u^2} \quad (8)$$

Linearity performance comparison of some published switching schemes is shown in Table I. As can be seen from the comparison, the proposed scheme exhibits outstanding linearity performance.

TABLE I
LINEARITY COMPARISON

Switching scheme	$E\left[\delta^2_{\max,DNL}\right]$	$E\left[\delta^2_{\max,DNL}\right]$
Conventional	$\frac{2^N\sigma_u^2}{C_u^2}$	$\frac{2^N\sigma_u^2}{C_u^2}$
Set down	$\frac{2^N\sigma_u^2}{C_u^2}$	$\frac{2^N\sigma_u^2}{C_u^2}$
V_{cm}-based	$\frac{2^N\sigma_u^2}{C_u^2}$	$\frac{2^N\sigma_u^2}{C_u^2}$
Proposed	$\frac{2^{N-2}\sigma_u^2}{C_u^2}$	$\frac{2^{N-1}\sigma_u^2}{C_u^2}$

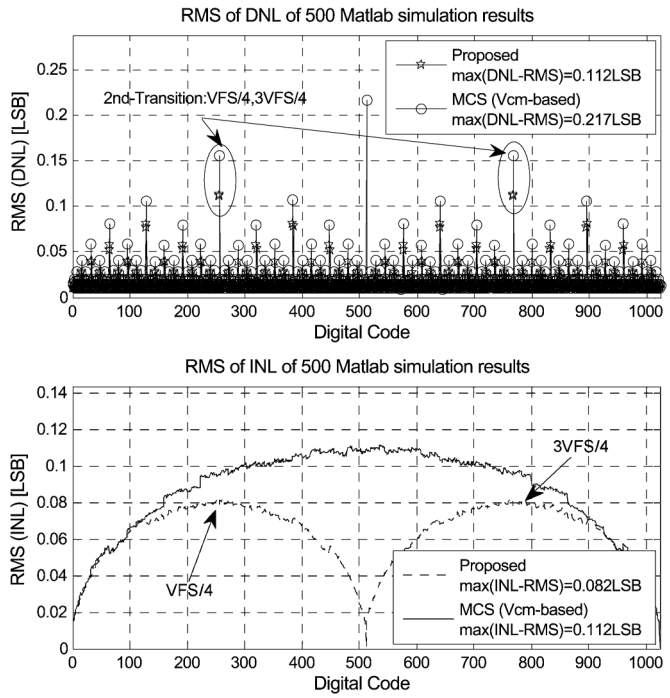

Fig. 5. Behavioral simulation of conversion linearity.

To verify previous analysis, behavioral simulations were performed to model the conversion linearity of the proposed switching scheme. The random mismatch of capacitors is the only error source considered. The values of the unit capacitors are taken to be Gaussian random variables with standard deviation of 1%. Fig. 5 shows the DNL and INL of 500-point Monte-Carlo runs. As expected, the worst INL for the proposed switching procedure occurs at $V_{FS}/4$ and $3V_{FS}/4$.

The mathematical analysis and behavioral simulations of the DNL error caused by device mismatch show that the proposed switching scheme allows implementation of smaller unit capacitor. Note that the proposed switching scheme offers better layout matching since the MSB is split into identical copy of the rest of the capacitor array which turns out that the proposed switching scheme offers much better linearity performance.

D. Sensitivity to Power Supply Noise and Common Mode Voltage Generator

In SAR ADC design, power supply voltage is usually utilized as a voltage reference. The analog circuit will be normally biased by a dedicated linear voltage regulator or low dropout regulator (LDO) to isolate the noisy digital signals. Meanwhile, the frequently switching activity may introduce transient overshoot

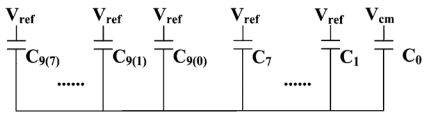

Fig. 6. Simplified supply network of DAC.

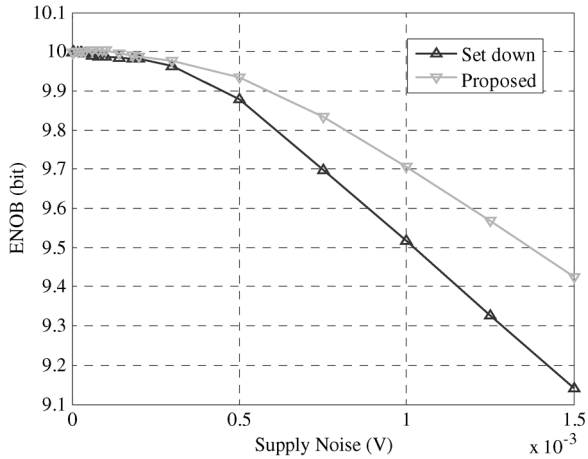

Fig. 7. Behavioral simulation of ENOB versus supply noise in 10 bit SAR ADC.

or ringing and decrease overall performance. It is crucial to analyze the influence of the reference on ADC performance.

Since most SAR ADC operates in differential model [8], we assume that common mode voltage reference does not exhibit noise. Therefore, only supply variation is considered. The most critical case is when the bottom plates of DAC capacitors are connected to V_{dd}. Fig. 6 shows the DAC of proposed switching scheme with power references in the worst case.

The differential output of DAC can be expressed as

$$V_{out} = \frac{2^{n-1}-1}{2^{n-1}}(V_{dd}+\Delta) \tag{9}$$

where Δ is the variation of the reference. The error generated from the supply noise can be quantified by

$$V_{error} = \frac{2^{n-1}-1}{2^{n-1}} \cdot \Delta \tag{10}$$

which is usually required to be smaller than 1/4LSB.

A behavioral simulation is performed in MATLAB as shown in Fig. 7. The proposed switching scheme achieves over 9.4 bit ENOB within 1.5 mV. The difference between the two switching scheme expands with the increase of supply noise. The Set down scheme [7] achieves 9.14 bit at 1.5 mV supply noise while the proposed switching scheme achieves ENOB above 9.4 bit. To exclude the influence of supply noise, special care is normally taken in PCB routing.

In addition to V_{ref} and Gnd, another reference voltage V_{cm} is needed in this design. Fig. 8 shows the common mode voltage reference generator. An OTA is added to Class-AB super source follower to ensure sufficient transconductance of the buffer for the voltage to recover during switching. Note that the supply voltage of the reference generator does not scale according to the scaling of SAR core supply.

E. Asynchronous Processing

The sequential operation nature of SAR ADCs has been limitation on the high-speed applications, because a synchronous approach relies on a clock to divide the conversion phase into

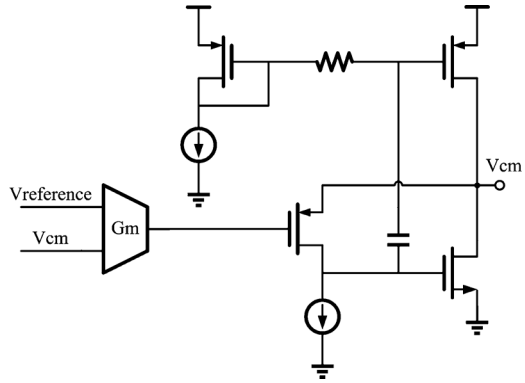

Fig. 8. Common mode voltage generator.

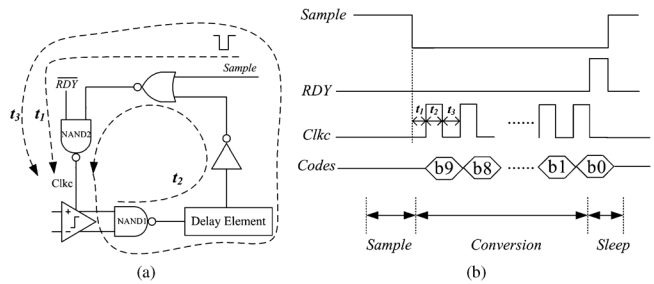

Fig. 9. Clock generator architecture and timing diagram. (a) Clock generator. (b) Timing diagram.

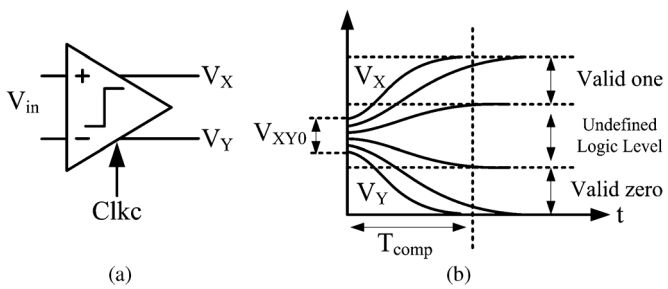

Fig. 10. Outputs of a typical clocked comparator.

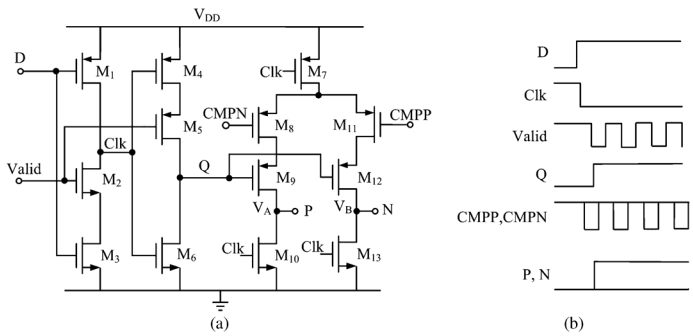

Fig. 11. Conventional dynamic logic. (a) Schematic of conventional dynamic logic. (b) Timing diagram of conventional dynamic logic.

equally timed slots as the conversion proceeds from MSB to LSB. Moreover, synchronous approach requires complicated external clocks to be fed into the chip, making it complicated in designing and measuring a configurable ADC. The circuit schematic of asynchronous clock generator is shown in Fig. 9(a). During the *Sample* is high, $Clkc$ stays low. The outputs of comparator are reset to V_{dd}. Once *Sample* comes to low, it takes t_1 for $Clkc$ to pull up and the comparator starts to compare two input signals. The outputs of the comparator set up and NAND1 generates a high level signal. After it takes t_2, $Clkc$

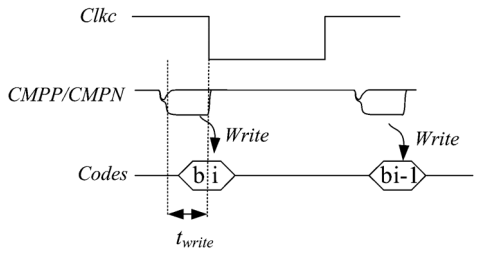

Fig. 12. Control logic operation.

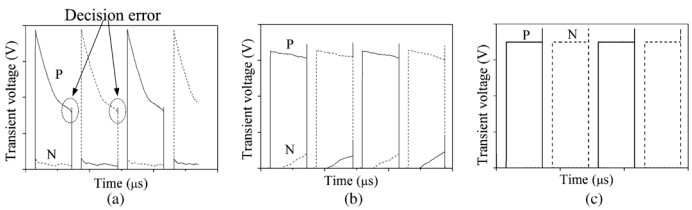

Fig. 13. Simulation results of transient P and N voltage levels. (a) Transient P and N voltage levels of conventional logic in short channel MOSFET. (b) Transient P and N voltage levels of conventional logic in long channel MOSFET. (c) Transient P and N voltage levels of proposed dynamic logic.

is pulled down to Gnd to preset the comparator for the next comparison cycle. Once the outputs of comparator are pulled up to V_{dd}, NAND1 generates a high level signal and triggers the comparator which represents t_3 represented in Fig. 9(b). The clock generator repeats this operation until the SAR logic generates a low level voltage RDY indicating that the conversion is completed. Since t_2, t_3 vary with the proceeding of conversion, therefore, the asynchronous conversion efficiently utilizes the fast comparison cycles for large comparator inputs. The asynchronous processing requires only a low-speed sample-rate clock instead of an oversampled clock, thereby saving power in the clock structure and simplifying the required scalability in the data rate [10].

Comparators typically incorporate a regenerative feedback with clocking so as to provide fast amplification in a certain time period. As illustrated in Fig. 10, $Clkc$ is applied at $t = 0$, and the outputs, V_x and V_y, regeneratively depart from an initial difference of V_{xy0}. For an excessively small V_{xy0}, the outputs fail to reach valid logical levels within the allotted time, T_{comp}, possibly causing metastability errors in the subsequent stages [11]. It is better to strobe the comparator slightly before the input tracking phase ends, allowing a longer comparison time t_2 and hence a lower metastability error rate.

In our work, the comparator is designed fast enough for the 2 MS/s ADC chip. Meanwhile, the "*Delay element*" in Fig. 9(a) is programmable with 3 digital control signals in the asynchronous timing. Therefore, the speed of the comparator could be adjusted to reduce the metastability error rate.

F. SAR Control Logic

The conventional static logic gate based SAR controller uses two DFFs for each conversion bit which is relatively complex and increases power and area. Dynamic logic is utilized in low power design. Fig. 11(a) shows the schematic of the conventional dynamic logic [4], [10], [11]. At first, D is low and nodes P and N are reset to low. Then D turns to high and Clk is pulled down to ground. When the comparator outputs $CMPP$

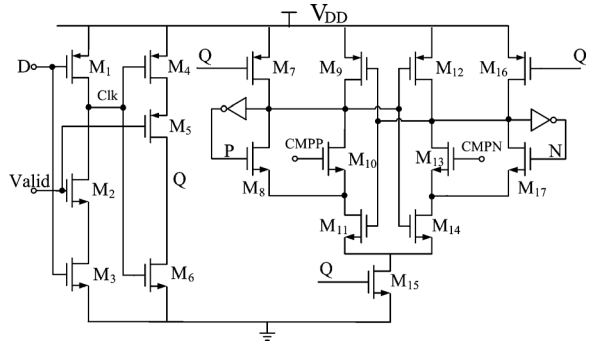

Fig. 14. Proposed dynamic latched logic.

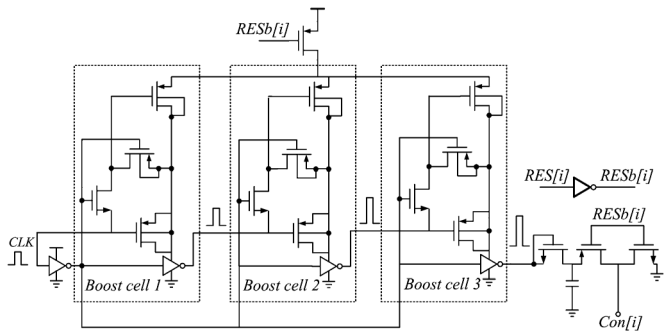

Fig. 15. Voltage boost cells for resolution switches.

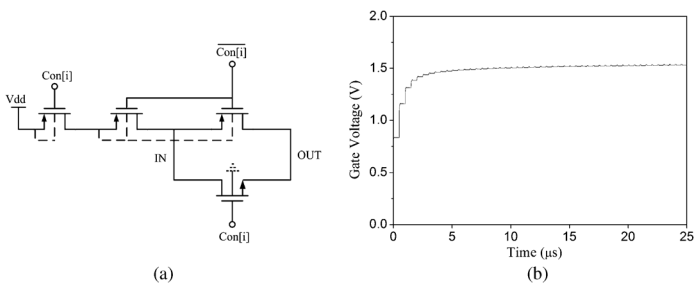

Fig. 16. Resolution switch and the gate voltage of the switch. (a) Resolution switch. (b) Gate voltage of resolution switch.

and $CMPN$ are ready, the results are stored by P and N. Meanwhile Q turns to high to indicate that the bit cycle is completed. The timing diagram is shown in Fig. 11(b).

However, the conventional dynamic logic requires critical timing control, therefore, it is not suitable for wide frequency design. As shown in Fig. 12, the dynamic logic should be sufficient fast to write the outputs of the comparator. Otherwise, $CMPP$ and $CMPN$ would be reset to V_{dd} when $Clkc$ is pulled down. In conventional dynamic logic, M_8 and M_{11} are responsible for pulling node P or node N to high. In low voltage operation, the transistors operate in sub-threshold region, the currents flowing in M_8 and M_{11} are probably not large enough to pull one of the output nodes to high fast enough. Especially when the input voltage difference of comparator is small, and it takes the comparator relatively long time resolve, thus leaving a short time for logic to write.

Moreover, nodes P and N are floating in the conversion phase. Therefore, they suffer drastically from leakage current in the long bit cycle due to the low sampling rate. This could cause decision errors in P and N. In low sampling rate design, the long bit conversion period offers node P and N enough time to drop below V_{Th}, resulting in decision errors as it is illustrated Fig. 13(a). V_{Th} is the threshold voltage of the following buffer.

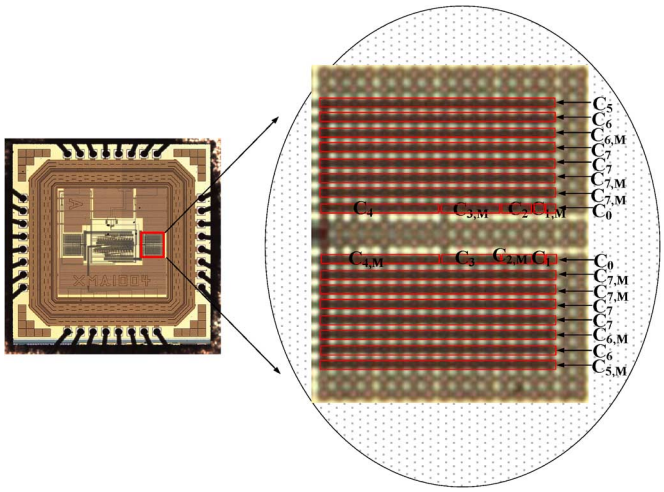

Fig. 17. Die microphotograph of the fabricated SAR ADC.

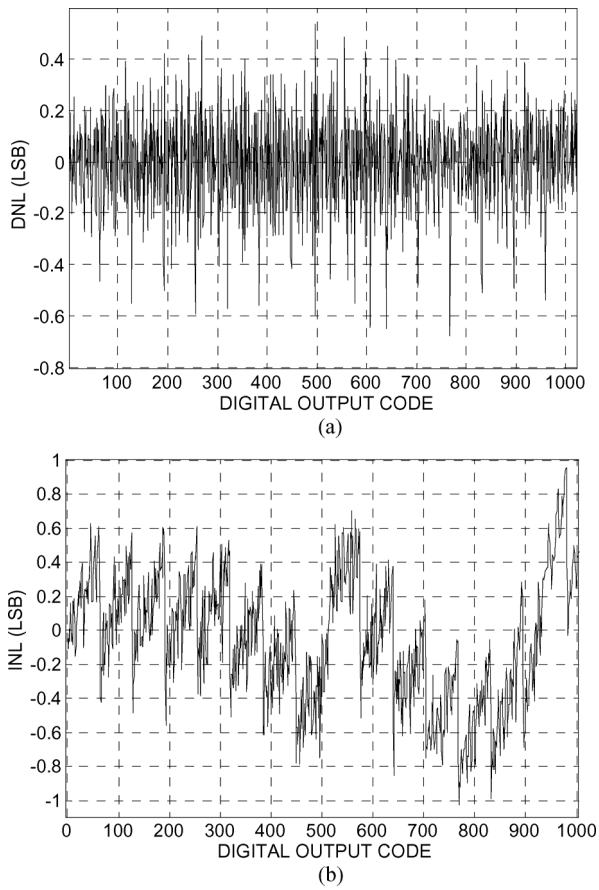

Fig. 18. Measured static performance at sampling rate of 2 MS/s in 10 bit mode. (a) Measured DNL. (b) Measured INL.

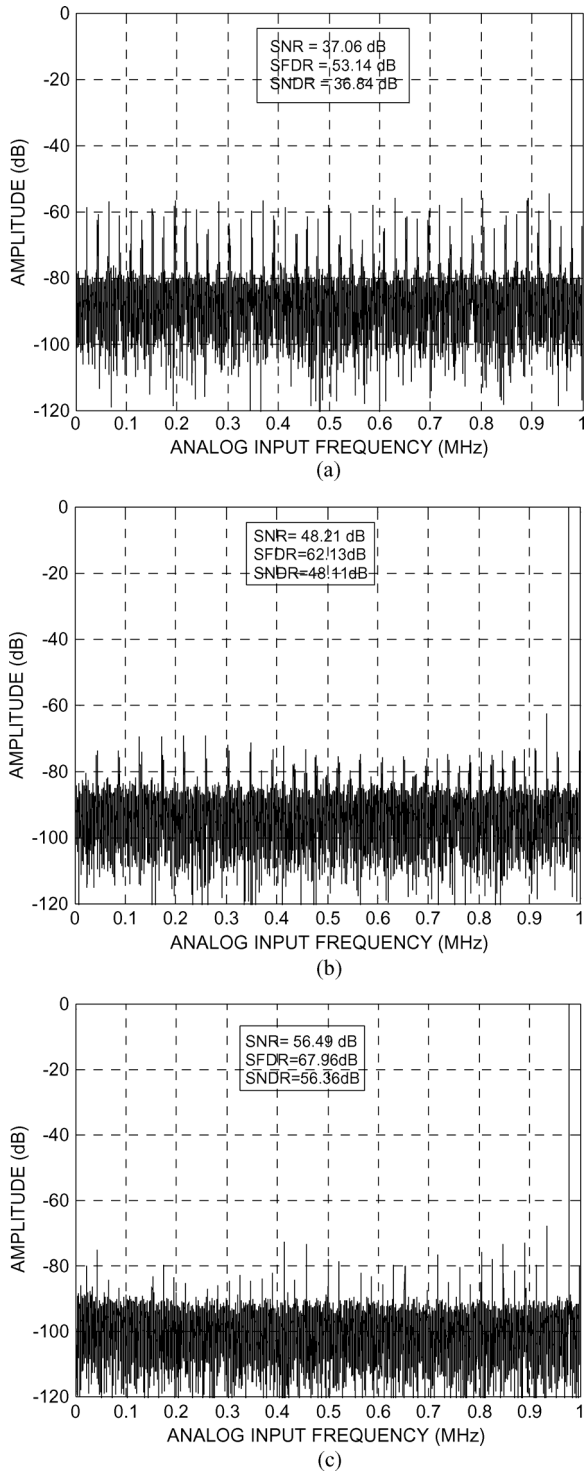

Fig. 19. Measured 32768-point Frequency FFT. (a) FFT in 6 bit, 2 MS/s. (b) FFT in 8 bit, 2 MS/s. (c) FFT in 10 bit, 2 MS/s.

In order to decrease the leakage current, a possible approach is to double or triple the channel length. As shown in Fig. 13(b), the voltage level drop is decreased due to the utilization of long channel devices in M_{10} and M_{13}. However, the decision error is still not eliminated since the pulse widths of P and N vary in according to the regeneration speed of the comparator.

A novel dynamic latched logic cell is proposed to eliminate decision error caused by leakage current as shown in Fig. 14. At first, D and Q are low, M_7 and M_{16} are turned on, node P and N are reset to low. Meanwhile, M_{15} is off, cutting off the current of the circuit to save power. When D turns to high, Clk is pulled down to ground. Once it comes falling edge of *Valid*, Q turns to high. Afterwards, either M_{10} or M_{13} is turned on and the back-to-back inverters formed by M_9, M_{11}, M_{12}, M_{14} start positive regeneration and update one of the latch outputs once the comparator outputs are ready. Afterwards, P and N are latched by M_8 or M_{17} regardless of any changes of $CMPP$ or $CMPN$. The delay time of a latch depends in a logarithmic manner on the initial output voltage difference between $CMPP$ and $CMPN$ resulting in better performance in speed than the conventional

TABLE II
PERFORMANCE COMPARISON

Article Title	[1]	[2]		[3]				This work		
Technology	0.18μm	65nm		90nm				0.18μm		
Supply (V)	1.0	0.4V-1V		1.1				0.5V-0.9V		
Resolution (bit)	8	8	10	7	8	9	10	6	8	10
Sampling rate(Hz)	500K	20K		4M				2M	2M	2M
SNDR (dB)	46.92	47.0	55.0	43.72	48.90	54.13	58.35	36.84	48.11	56.36
Power (μW) (Reference power excluded)	7.75	0.146	0.206	8.22	9.00	13.57	17.44	10.39	15.98	22.12
FoM(fJ/conv.-step)	86	40.0	22.4	16.4	9.9	8.2	6.5	91.5	38.4	20.6

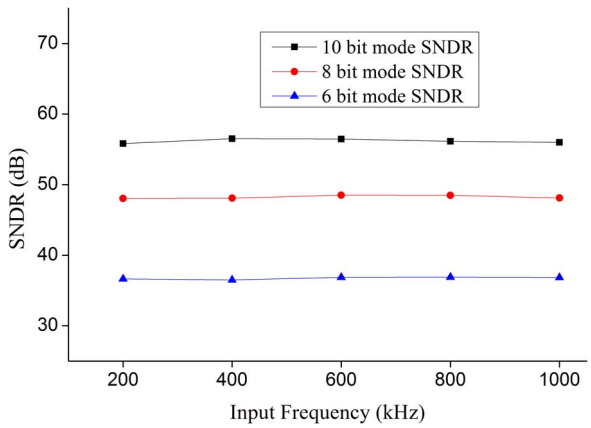

Fig. 20. Measured SNDR versus input frequency at 0.5 V 2 MS/s.

one. With decision error issue eliminated, the latched logic is suitable for wide frequency design. As shown in Fig. 13(c), the voltage level of P and N hold virtually constant in the conversion phase.

G. Resolution Switch

As resolution is scaled in the proposed ADC, both the noise and linearity requirements are relaxed, providing an opportunity to use voltage scaling to optimize energy-efficiency. However, at low supply voltage level, the switch may introduce distortion and limit the bandwidth. Therefore, it is important to balance distortion with scaled supply voltage in order to improve energy efficiency. The resolution scaling in the D/A converter is implemented by switching the resolution switch. Fig. 15 shows the schematic of Boost cell which is used to generate the control voltage of the resolution switch. The high-level is boosted by the clock boosting circuit to reduce the on-resistance of the switch. When RES[i] is high, the *boost cells* are active. When RES[i] is low, the *boost cells* are disabled to save power. The boost cells could be configured according to the supply voltage. When the supply voltage is 0.5 V, three *boost cells* are activated to boost the voltage up to around 1.5 V. When the ADC is operating at 0.7 V, two *boost cells* are enabled to boost the voltage up to 1.4 V. When 0.9 V supply voltage is applied, only one *boost cell* is working, and the boost voltage level is about 1.3 V.

Fig. 16(a) shows the gate voltage of the resolution switch in 0.5 V supply mode. The gate voltage is boosted fast enough up to about 1.5 V and maintain virtually constant afterwards. The transmission gate using bulk-switching of the PMOS transistor is hence chosen as a resolution switch to achieve better linearity as shown in Fig. 16(b). When Con is high, the bulk of the PMOS transistor is connected to source, resulting in lower threshold voltage and subsequently lower on-resistance. When Con is low, the bulk is switched to V_{dd} to increase off-resistance.

III. MEASUREMENT RESULTS

Fig. 17 shows the die microphotograph of the proposed ADC. It has been fabricated in 0.18μm standard CMOS technology and the active area occupies about 300μm* 700μm. The covered core supply ranges from 0.5 V to 0.9 V. The unit capacitance was set to be 15.5 fF in this work which is the minimum MIM capacitance defined by this process. The capacitor array follows partial common-centroid configuration as shown in Fig. 17. The capacitors $(\mathrm{C_7}-\mathrm{C_5}, \mathrm{C_{7,M}}-\mathrm{C_{5,M}})$ follow exact common-centroid layout strategy to minimize the error from the non-uniform oxide growth in the MIM capacitors. The smaller capacitors $(\mathrm{C_4}-\mathrm{C_1}, \mathrm{C_{4,M}}-\mathrm{C_{1,M}})$ were placed in the same form as $\mathrm{C_5}(\mathrm{C_{5,M}})$ to achieve better matching and binary parasitic capacitances resulting in better linearity performance. Besides, $\mathrm{C_4}-\mathrm{C_1}$, $\mathrm{C_{4,M}}-\mathrm{C_{1,M}}$ were arranged in an interleaved manner for better matching.

Histogram test was conducted to measure the linearity of the proposed SAR ADC. A full swing, differential sinusoidal input signal was applied when the proposed SAR ADC is operating in 10 bit 2 MS/s mode. Fig. 18 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) based on code density measurement. The peak DNL error is $+0.54/-0.61$ LSB, and the peak INL error is $+0.9$ LSB/-1.0 LSB.

The dynamic performance of the proposed SAR ADC was measured using tone testing. Fig. 19 shows the fast Fourier transform (FFT) of the SAR ADC in 6 bit, 8 bit, 10 bit modes with near Nyquist inputs at 2 MS/s ($V_{dd} = 0.5$ V). The SNDR in 6 bit, 8 bit, and 10 bit mode are 36.84 dB, 48.11 dB, and 56.36 dB, respectively.

Fig. 20 shows the measured SNDR of the proposed SAR ADC with respect to the input frequency. The measured results show a consistent ENOB performance with input frequency ranging from static to Nyquist-rate in each mode. Hence, the effective resolution bandwidth (ERBW) is higher than the Nyquist bandwidth.

Table II summarizes the performance of the proposed SAR ADC, and shows the performance comparison between our work and previous reported low power ADCs [1]–[3]. Here, the figure-of-merit (FoM) used to evaluate the power efficiency is configured as

$$FOM = \frac{Power}{\min\{f_s, 2 \times ERBW\} \times 2^{ENOB}} \tag{11}$$

where f_s represents the sampling rate. Power efficiencies from 20.6 to 91.5 fJ/conversion-step are achieved which is competitive with current state-of-art ADCs.

IV. Conclusion

In this paper, an asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) for sensor applications is presented. High linear configurable switching scheme is proposed. The SAR ADC is fabricated in 0.18μm CMOS process, supporting 6 to 10 bit resolution and 0.5 V–0.9 V power supply range. The measured results show that at 10 bit 2 MS/s mode, the proposed SAR ADC achieves an ENOB of 9.07 bit, this leads to energy efficiency of 20.6 fJ/conv.-step.

References

[1] Y.-K. Chang, "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 228–231.

[2] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10-bit 0.4-to-1 V power scalable SAR ADC for sensor applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1453–1464, Jun. 2013.

[3] P. Harpe, Y. Zhang, G. Dolmans, and K. Philips, "A 7-to-10 b 0-to-4 MS/s flexible SAR ADC with 6.5-to-16 fJ/conversion-step," *Proc. IEEE ISSCC*, pp. 472–474, Feb. 2012.

[4] P. Harpe, "A 0.7 V 7-to-10 bit 0-to-2 MS/s flexible SAR ADC for ultra low-power wireless sensor nodes," *Proc. ESSCIRC*, pp. 373–376, Sep. 2012.

[5] B. P. Ginsburg, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *Proc. IEEE ISCAS*, vol. 1, pp. 184–187, May 2005.

[6] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "10-bit 30-MS/s SAR ADC Using a Switchback Switching Method," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 3, pp. 584–588, Mar. 2013.

[7] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[8] Y. Zhu, C.-H. Chan, U.-F. Chio, and S.-W. Sin, "Split-SAR ADCs: Improved linearity with power and speed optimization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 372–383, Feb. 2014.

[9] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electron. Lett.*, vol. 46, no. 9, pp. 620–621, Apr. 2010.

[10] P. J. A. Harpe, C. Zhou, and Y. Bi, "A 26 μW 8 bit 10 MS/s Asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, 2011.

[11] P. Harpe and X. Huang *et al.*, "A 0.37 μW 4 bit 1 MS/s SAR ADC for ultra-low energy radios," in *Proc. IEEE Int. Symp. VLSI Design, Autom., Test (VLSI-DAT)*, Hsinchu, Taiwan, 2011, pp. 1–4.

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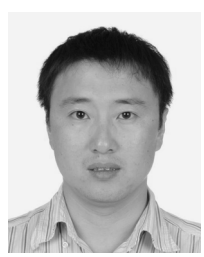

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