An Area-Efficient and Low-Power 12-b SAR/Single-Slope ADC Without Calibration Method for CMOS Image Sensors

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***Abstract*— This paper presents an area-efficient and low-power 12-b successive approximation register/single-slope analog-to-digital converter (SAR/SS ADC) for CMOS image sensor (CIS) applications. The number of unit capacitors of the proposed SAR/SS ADC is reduced to 1/64th of that of a conventional 12-b SAR ADC using only a 6-b capacitor digital-to-analog converter (DAC) and the power consumption is reduced by sharing analog circuits between the SAR ADC and the SS ADC. In addition, the proposed ADC properly operates without using any calibration method as it is designed to be robust to inaccuracies in analog circuits by connecting the ramp signal to the bottom plate of the unit capacitor in the capacitor DAC. A 1936 × 840 pixel 60 frames/s CIS with the proposed SAR/SS ADCs was fabricated using a 90-nm CMOS process, and each readout channel with the proposed SAR/SS ADC occupies an area of 2.24 μm × 998 μm and consumes a power of 30 μW. The measurement results show that the SAR/SS ADC has a differential nonlinearity of −0.45/+0.84 LSB and an integral nonlinearity of −1.5/+0.74 LSB. In addition, the developed CIS has a temporal noise of 2.7 LSB_{rms} and a column fixed pattern noise of 0.07 LSB.**

***Index Terms*— CMOS image sensor (CIS), column-parallel readout, hybrid analog-to-digital converter (ADC), single-slope (SS) ADC, successive approximation ADC.**

I. Introduction

RECENTLY, single-slope analog-to-digital converters (SS ADCs) have been widely used for CMOS image sensor (CIS) applications due to their small area and high linearity [1], but takes a long A/D conversion time for high resolution. For alternative solutions to the SS ADC, several ADCs such as $\Delta\Sigma$ ADCs, cyclic ADCs, and successive approximation register (SAR) ADCs have been researched for high-speed CISs [2]–[5]. The $\Delta\Sigma$ and cyclic ADCs perform low noise and short conversion time, respectively, but both of them require high power-consuming operational amplifiers [2], [3]. To solve the above problem, ADCs using the voltage-controlled oscillator or comparator with current source have been researched. However, it is difficult to implement these ADCs in the narrow readout channel pitch of the CIS due to circuit complexity [6], [7]. The SAR ADC achieves a short conversion time and low power consumption, but requires a large area to implement a capacitor digital-to-analog converter (DAC) [4], [5].

To overcome the drawbacks of the aforementioned ADCs, several hybrid and two-step ADCs have been developed [8]–[13]. The SS/SAR ADC in [11] reduces the A/D conversion time of the SS ADC and the area of the SAR ADC. It sequentially converts the pixel output into the upper bit and lower bit using the SS ADC and SAR ADC, respectively. However, it requires a lot of accurate reference voltages for the SAR ADC in order to achieve high resolution, as it selects reference voltages for the lower bit conversion according to the upper bit. The SAR/SS ADCs sequentially convert the pixel output into the upper bit and lower bit using the SAR ADC and SS ADC, respectively [12], [13]. The SAR/SS ADC in [12] connects one input of the comparator to the output of the capacitor DAC and the other input to the ramp signal. However, it is vulnerable to the error in the step size of the ramp signal and the gain error of the capacitor DAC.

This paper proposes an area-efficient and low-power 12-b SAR/SS ADC for CIS applications. The proposed SAR/SS ADC reduces the capacitor area using only a 6-b capacitor DAC for 12-b conversion and consumes less power by sharing analog circuits between the SAR and SS ADCs. In addition, it is designed to be robust to the variation in the ramp signal including the errors in the ramp step size and ramp offset, and the gain error of the capacitor DAC, and thereby complex calibration methods in [10]–[12] are not required. In Section II, the architecture of the developed CIS and the operating principle of the proposed SAR/SS ADC are explained. Section III describes the circuit implementation and linearity of the proposed SAR/SS ADC. In Section IV, the experimental results of the developed CIS are analyzed and compared with previous works. Finally, the conclusions are given in Section V.

II. CIS Architecture

A. Block Diagram

Fig. 1 shows the block diagram of the developed CIS with the proposed SAR/SS ADC. An active pixel array consists of 1936×840 pixels, of which each pixel has a pitch of 1.12 μm and 4 pixels share a source follower circuit. A readout channel,

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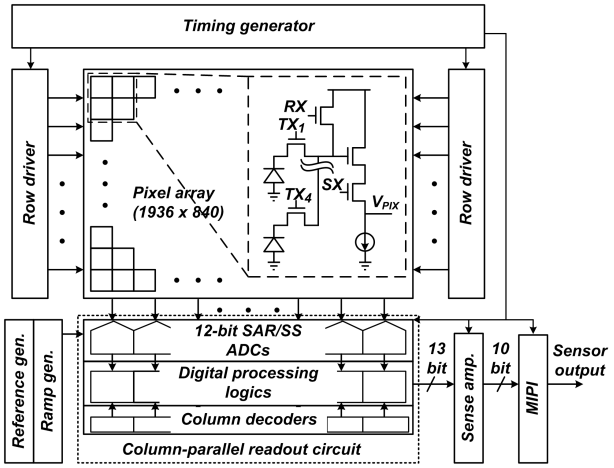


Fig. 1. Block diagram of the developed CIS with schematic of pixel structure.

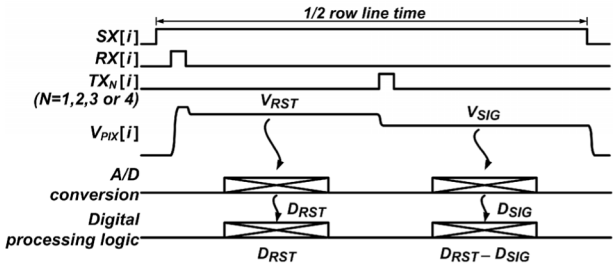


Fig. 2. Operating sequence in a half row line time.

which consists of the proposed 12-b SAR/SS ADC, digital processing logic, and column decoder, is implemented within a 2-pixel pitch of 2.24 μm, and sequentially converts the even and odd column outputs of the pixel array during a row line time. A timing generator provides the overall control signals for the row drivers, readout circuit, and sense amplifier. Two row drivers provide the control signals: SX, TX1, TX2, TX3, TX4, and RX, to the pixel array. The SAR/SS ADC converts the pixel output $V_{\rm PIX}$ into a digital signal using the reference voltages and ramp signal, which are provided by the reference and ramp generators, respectively. The digital processing logic receives the output of the SAR/SS ADC and performs the digital correlated double sampling (CDS) calculation. It has a 13-b output, of which the 12-b output is used for the sensor output and the most significant bit (MSB) generated via subtraction is used as a sign bit. The output of the digital processing logic is selected by the column decoder and is transferred to the mobile industry processor interface (MIPI) using the sense amplifier. Since the MIPI has a 10-b digital output in mobile applications, the sense amplifier selects one of the lower 10-b, middle 10-b, or upper 10-b among the 12-b output except for the MSB, according to the light intensity and sends it to the sensor output through the MIPI.

Fig. 2 shows the operating sequence of the developed CIS in a half row line time. The pixels on the ith row, which are selected by SX[i], sequentially generate the pixel reset and photo-induced signal voltages, $V_{\rm RST}$ and $V_{\rm SIG}$, respectively, according to the pixel control signals RX[i] and

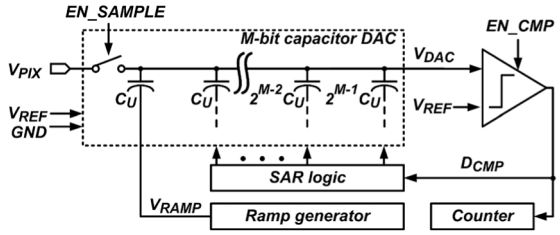


Fig. 3. Block diagram of the proposed SAR/SS ADC.

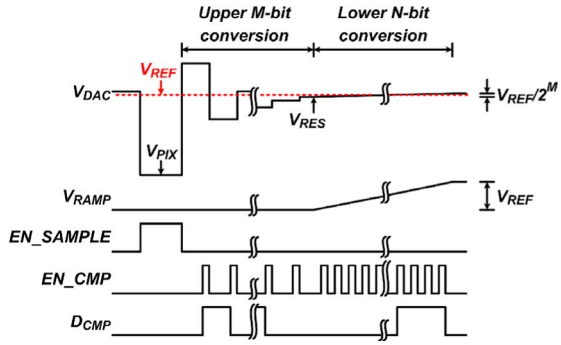


Fig. 4. Timing diagram of the proposed SAR/SS ADC.

TX1[i] or TX2[i]. Then, the SAR/SS ADC converts $V_{\rm RST}$ and $V_{\rm SIG}$ into the digital signals, $D_{\rm RST}$ and $D_{\rm SIG}$, respectively. The digital processing logic stores the sequential outputs of the comparator for the SAR ADC, counts the clock for the SS ADC, and subtracts $D_{\rm SIG}$ from $D_{\rm RST}$ for the digital CDS calculation.

B. Operating Principle of the Proposed SAR/SS ADC

Fig. 3 shows the block diagram of the proposed (M+N)-b SAR/SS ADC. The input of the SAR/SS ADC $V_{\rm PIX}$ is sequentially converted into the upper M-b and lower N-b using the SAR ADC and SS ADC, respectively. $V_{\rm REF}$ and GND are used as reference voltages for the M-b capacitor DAC, and a ramp signal $V_{\rm RAMP}$ is connected to the bottom plate of one of the two unit capacitors C_U in the capacitor DAC. The comparator, which is shared by the SAR ADC and SS ADC for reducing power consumption, compares the output of the capacitor DAC $V_{\rm DAC}$ with $V_{\rm REF}$ at the rising edge of the control signal EN_CMP and the SAR logic selects $V_{\rm REF}$ or GND, which is connected to the bottom plate of each capacitor in the capacitor DAC according to the comparator output $D_{\rm CMP}$.

Fig. 4 shows the timing diagram of the SAR/SS ADC. For the first bit conversion in the upper M-b conversion, the top and bottom plates of all the capacitors are connected to $V_{\rm PIX}$ and GND, respectively, when the control signal EN_SAMPLE is high, and then $V_{\rm DAC}$ becomes $V_{\rm PIX}$ and $V_{\rm RAMP}$ is fixed to GND. Then, the bottom plate of the largest capacitor $2^{M-1}C_U$ is connected from GND to $V_{\rm REF}$, and thereby $V_{\rm DAC}$ is increased by 1/2$V_{\rm REF}$ from $V_{\rm PIX}$, and then compared with $V_{\rm REF}$ to obtain the MSB. For the second bit conversion, when the MSB is 1, $2^{M-1}C_U$ is connected to GND, whereas when the MSB is 0, $2^{M-1}C_U$ remains connected to $V_{\rm REF}$. At the same time, the second largest capacitor $2^{M-2}C_U$ is connected

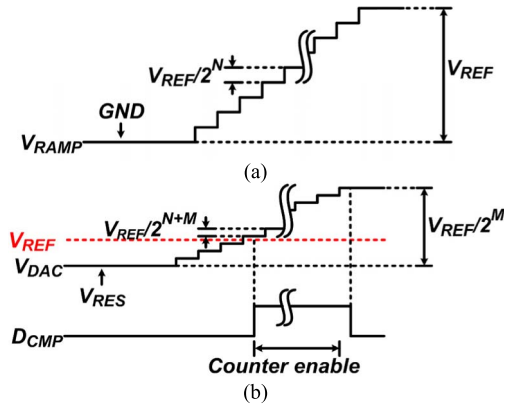


Fig. 5. Timing diagram during lower N-b conversion. (a) Ramp signal V_{RAMP}. (b) Capacitor DAC output V_{DAC} and comparator output D_{CMP}.

from GND to V_{REF} regardless of the MSB. Accordingly, V_{DAC} is decreased or increased by $1/4V_{\mathrm{REF}}$ according to an MSB of 1 or 0, respectively, and then compared with V_{REF} to obtain the second bit. These operations are repeated until the Mth bit of the upper M-b is obtained, and the bottom plate of the other of the two unit capacitors is connected to V_{REF} or GND. After the upper M-b conversion, V_{DAC} becomes a residue voltage V_{RES} ranging from $V_{\mathrm{REF}} - V_{\mathrm{REF}}/2^M$ to V_{REF}, and can be expressed as

$$V_{\mathrm{DAC}} = V_{\mathrm{RES}} = V_{PIX} + \sum_{i=1}^{M}\left[\frac{V_{\mathrm{REF}}}{2^i}\cdot(1 - D_U[i])\right] \quad (1)$$

where $D_U[i]$ is the ith bit of the upper M-b.

In the lower N-b conversion, V_{RAMP} varies from GND to V_{REF}, consisting of a total number of 2^N steps with a step size of $V_{\mathrm{REF}}/2^N$, as shown in Fig. 5(a). By the capacitor voltage dividing, V_{DAC} is changed from V_{RES} to $V_{\mathrm{RES}} + V_{\mathrm{REF}}/2^M$ with a step size of $V_{\mathrm{REF}}/2^{M+N}$ according to V_{RAMP}. To obtain the lower N-b, the counter counts the number of V_{RAMP} steps when the comparator output D_{CMP} becomes high, as shown in Fig. 5(b). Since EN_CMP is provided to all readout channels at the same time, EN_CMP periodically operates to drive the other SAR/SS ADCs after D_{CMP} in an SAR/SS ADC is triggered. After the lower N-b conversion, V_{DAC} can be expressed as

$$V_{\mathrm{DAC}} = V_{\mathrm{RES}} + \frac{V_{\mathrm{REF}}}{2^M} \approx V_{\mathrm{REF}} + \frac{V_{\mathrm{REF}}}{2^{M+N}}\cdot\sum_{i=1}^{N}\left(2^{N-i}\cdot D_L[i]\right) \quad (2)$$

where $D_L[i]$ is the ith bit of the lower N-b. By simplifying (1) and (2), V_{PIX} can be expressed as

$$V_{\mathrm{PIX}} \approx \sum_{i=1}^{M}\left(\frac{V_{\mathrm{REF}}}{2^i}\cdot D_U[i]\right) + \sum_{i=1}^{N}\left(\frac{V_{\mathrm{REF}}}{2^{M+i}}\cdot D_L[i]\right). \quad (3)$$

As a result, the final result of the A/D conversion is obtained by concatenating the upper M-b and lower N-b.

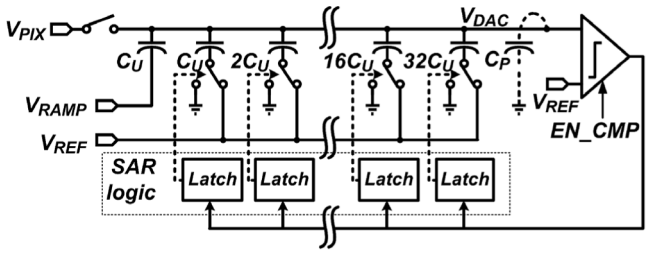


Fig. 6. Block diagram of the proposed 12-b SAR/SS ADC.

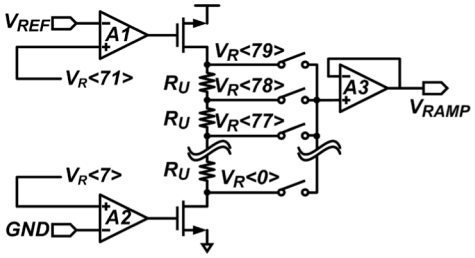


Fig. 7. Block diagram of the ramp generator.

III. Circuit Implementation

A. Design of the Proposed 12-b SAR/SS ADC

Fig. 6 shows the block diagram of the proposed 12-b SAR/SS ADC, which sequentially converts V_{PIX} into the upper 6-b and lower 6-b using the SAR ADC and SS ADC, respectively. The upper 6-b and lower 6-b SAR/SS split is chosen to achieve the A/D conversion time and readout channel area, which are less than 3 μs for 60 frames/s and 2.24 μm $\times$ 1000 μm, respectively, for mobile applications. Considering the thermal noise, a 6-b capacitor DAC is implemented with a total capacitance of 1.28 pF with an input range of 0.8 V and a C_U of 20 fF using a metal-insulator-metal capacitor. The clocked comparator, which consists of two one-stage preamplifiers and a strong arm latch in [14], compares V_{DAC} with V_{REF} at the rising edge of EN_CMP. The ADC offset, which is caused by the offset voltage of the comparator [12], is removed by the digital CDS [4]. The SAR logic, which consists of latches, sequentially stores the outputs of the clocked comparator and selects V_{REF} or GND connected to the capacitor in the 6-b capacitor DAC.

Fig. 7 shows the block diagram of the ramp generator, which consists of an R-string made up of 79 unit resistors R_U of which each has 63 Ω. V_{RAMP} has a total number of 80 steps, of which 64 steps with a step size of $V_{\mathrm{REF}}/64$ are used to convert the lower 6-b and 16 steps are used to compensate for the comparator output error caused by insufficient reference voltage settling and noise [6]. In the upper 6-b conversion, the R-string output $V_R\langle 7\rangle$ is selected as an input of the output buffer, and thereby V_{RAMP} becomes GND, whereas in the lower 6-b conversion, the R-string outputs, $V_R\langle 0\rangle$ to $V_R\langle 79\rangle$, are sequentially selected and V_{RAMP} is changed from $-7/64$ to $9/8$ V_{REF}. When the two-step ADC converts a lot of lower bits in the second step, compared with the multireference voltage generator in [15], the ramp generator in the developed CIS uses only one output buffer A3, thereby

guaranteeing monotonicity of V_{RAMP} and achieving low power consumption.

In the upper 6-b conversion of the proposed SAR/SS ADC, each bit conversion step takes 100 ns except for the MSB and second bit conversion steps which take 300 and 200 ns, respectively, to improve the reference voltage settling. Before the lower 6-b conversion, it takes 200 ns for settling V_{RAMP} which changes from GND to $-7/64V_{\mathrm{REF}}$. On the other hand, in the lower 6-b conversion, V_{RAMP} spends 20 ns for each step. As a result, the SAR/SS ADC spends a total A/D conversion time of 2.7 μs for the 12-b conversion. The SAR/SS ADC and digital CDS logic use supply voltages of 2.8 and 1.2 V, respectively and the power consumption of one readout channel is 30 μW, which includes the power consumptions of the SAR/SS ADC (26 μW) and the digital processing logic (4 μW). In addition, the peripheral circuit with the reference voltage and ramp generators consumes 23.7 mW.

B. Linearity of the Proposed SAR/SS ADC

In the proposed SAR/SS ADC, a ramp signal V_{RAMP} is connected to the bottom plate of the unit capacitor C_U in the 6-b capacitor DAC to reduce the linearity error due to the variation in the ramp signal, and the gain error of the capacitor DAC.

The ADC linearity is affected by the error in the step size of V_{DAC} due to the variation in V_{RAMP}, which is caused by the offset voltages of the operational amplifiers, A1 and A2, and the output buffer A3, of the ramp generator in Fig. 7. Since the step size of V_{DAC} is 1/64th of that of V_{RAMP} by the capacitor voltage dividing, the error in the step size of V_{DAC} becomes only 1/64th of that of V_{RAMP} caused by the offset voltage of A1 and A2. Therefore, the offset of A1 and A2, 12.5 mV, causes only 1 LSB error at each 64 LSB. Moreover, the offset error of V_{RAMP}, which is caused by the offset voltage of A3, does not affect V_{DAC} and A/D conversion result because it is stored in C_U when V_{PIX} is sampled in the capacitor DAC. Therefore, the linearity of the SAR/SS ADC becomes robust to the variation in V_{RAMP}.

The gain error of the capacitor DAC is caused by the parasitic capacitance C_P which occurs in V_{DAC}. Accordingly, the residue voltage V_{RES} ranges from $V_{\mathrm{REF}} - V_{\mathrm{REF}} \cdot C_U/(64 \cdot C_U + C_P)$ to V_{REF} after completing the upper M-b conversion. However, since V_{DAC} in the lower 6-b conversion also varies from V_{RES} to $V_{\mathrm{RES}}+V_{\mathrm{REF}} \cdot C_U/(64 \cdot C_U + C_P)$ according to V_{RAMP}, the change of V_{DAC}, $V_{\mathrm{REF}} \cdot C_U/(64 \cdot C_U+C_P)$, becomes equal to the range of V_{RES} regardless of C_P, and thereby the ADC linearity error becomes independent of C_P.

Since the differential nonlinearity (DNL) is more sensitive to the capacitor mismatch than the resistive mismatch [16], the proposed SAR/SS ADC requires a careful layout of the capacitor DAC in order to convert the upper 6-b accurately. Accordingly, dummy capacitors are implemented on both sides of the capacitors in the 6-b capacitor DAC to reduce the capacitance mismatch.

IV. Experimental Results

The developed CIS, which was fabricated using a 90-nm CMOS process, has a chip area of 3.8 mm $\times$ 3.7 mm as shown in Fig. 8. Each readout channel and the proposed SAR/SS ADC occupy an area of 2.24 μm $\times$ 988 μm and 2.24 μm $\times$ 498 μm, respectively. In the developed CIS, it was difficult to evaluate the linearity of the 12-b SAR/SS ADC because the developed CIS used a 10-b digital output for mobile application. Accordingly, an ADC test circuit with a 12-b digital output was separately fabricated and measured to verify the linearity of the 12-b SAR/SS ADC. Fig. 9 shows the captured image using the developed CIS. A dead row in the image might be caused by the defect occurred during fabrication without the wafer probe test.

Fig. 10 shows the light response of the developed CIS, which is obtained from the measured sensor output of a pixel according to the exposure time under a constant light intensity. Since the developed CIS has a 10-b digital output, one of the lower 10-b, middle 10-b, or upper 10-b among the 12-b output of the digital processing logic is selected. The sensor output is saturated to 3300 LSB, although the maximum output of the 12-b SAR/SS ADC is 4095 LSB, because the A/D conversion

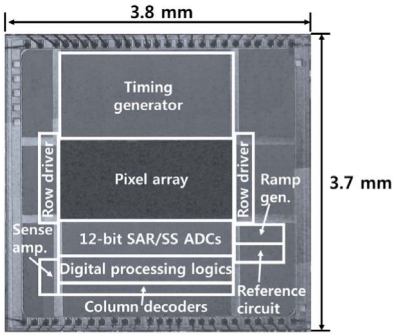


Fig. 8. Photomicrographs of the developed CIS.

Fig. 9. Captured image using the developed CIS.

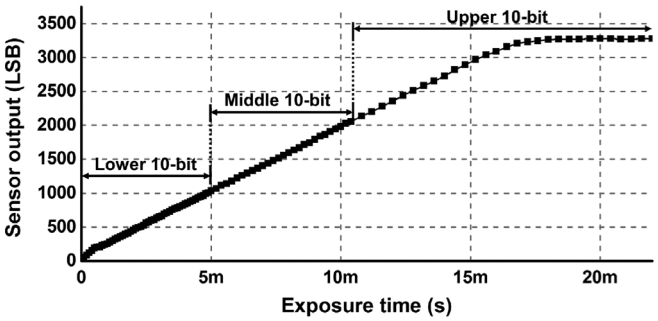


Fig. 10. Light response of the developed CIS.

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

		[2]	[3]	[4]	[8]	[11]	[12]	This work
Process		0.13 μm	0.18 μm	0.18 μm	0.25 μm	0.18 μm	0.18 μm	90 nm
Supply voltage (V)		2.8/1.2	1.8	3.3/1.2	2.5/3.3	3.3/1.8	3.3/1.8	2.8/1.2
CIS	Pixel size (μm^2)	2.25 × 2.25	-	4.2 × 4.2	7.4 × 7.4	3.5 × 3.5	1.85 × 1.85	1.12 × 1.12
	Pixel array size	1696 × 1212	-	4112 × 2168	440 × 330	1200 × 800	816 × 640	1936 × 840
	Frame rate (frames/s)	120	-	50	142	35	111	60
	Temporal noise (μV_{rms})	192	-	130.5	-	1500	4 LSB	527(=2.7 LSB)
	Dynamic range (dB)	73	-	80	72	58.3	34	62
ADC	Architecture	ΔΣ	Cyclic	SAR	MRSS	SS/SAR	SAR/SS	SAR/SS
	Resolution (bit)	12	12	14	10	11	9	12
	Conversion time (μs)	2.3	2.0	1.7	16	12	3.3[1)]	2.7
	DNL (LSB)	-0.64/+0.55	9.9	< -/+1	-	-1.45/+1.65	-1.0/+9.9	-0.45/+0.84
	INL (LSB)	-0.8/3.7	-9.8/4.7	-15/+2	< -1/+1.2	-	-9.8/+4.7	-1.5/+0.74
	Power (μW)	-	-	41	86[2)]	7[3)]	3	56[4)]
	FOM1 (fJ/step)[5)]	-	-	4.3	1349	41.7	37.8	36.9
Readout channel	Area (μm^2)	4.5 × 600[6)]	10.8 × 750	8.4 × 1320[7)]	-	7 × 1100	14.8 × 642	2.24 × 998
	power (μW)	55	120	-	68.2	4.4	-	30
	FOM2 (fJ/step)[8)]	30.9	58.6	-	1065	26.0	-	19.8

1) A/D conversion time is estimated from the operating clock frequency of the test chip, 4MHz.
2), 3), 4) ADC power = [ADC power in the readout channel] + [ADC peripheral circuit power] / [The number of readout channels].
5) FOM1 = [ADC power] × [A/D conversion time] / 2^ [ADC resolution].
6) Readout channel area except the column decoder.
7) SAR ADC cell size in the readout channel.
8) FOM2 = [Readout channel power except programmable gain amplifier] × [A/D conversion time] / 2^ [ADC resolution].

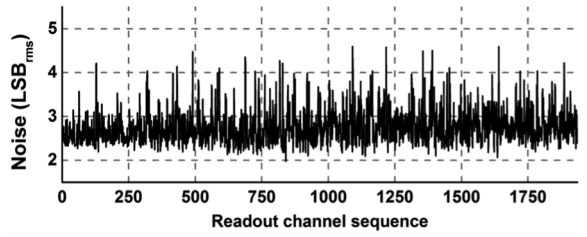


Fig. 11. Measured temporal noise under the dark condition.

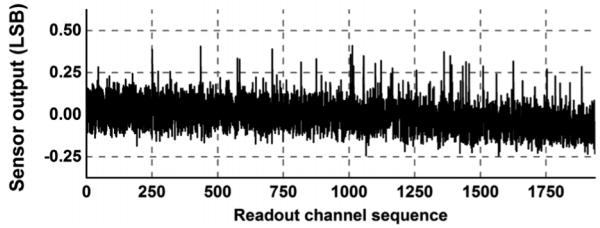
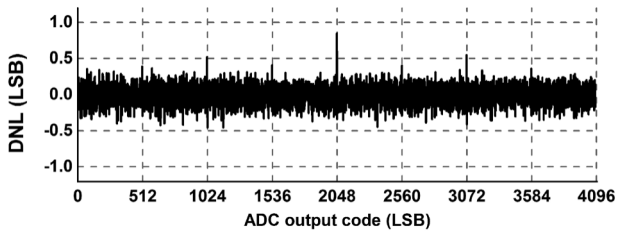
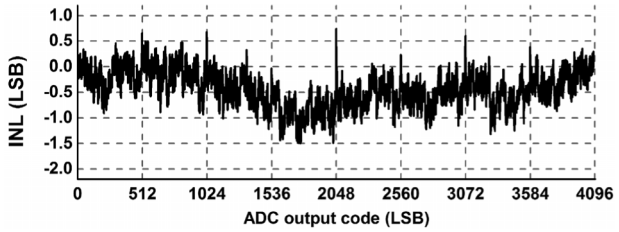


Fig. 12. Measured sensor output under the dark condition.



(a)



(b)

Fig. 13. Measured (a) DNL and (b) INL of the 12-b SAR/SS ADC.

range is set to be wider than the pixel output range in order to include the pixel and readout circuit variations.

Fig. 11 shows the measured temporal noise according to the readout channel sequence under the dark condition. An average value of the temporal noises is 2.7 LSB_{rms}, which corresponds to 527 μV_{rms}. The temporal noise is slightly increased because the clocked comparators used to improve the power efficiency cause supply noise when they operate simultaneously. The dynamic range of the developed CIS is measured to be 62 dB, which is obtained using the ratio between the temporal noise and the saturation level of the sensor output.

Fig. 12 shows the measured sensor output according to the readout channel sequence under the dark condition. A column fixed pattern noise (FPN), which is calculated from the standard deviation of the sensor output, is 0.07 LSB_{rms}.

Fig. 13 shows the measured DNL and integral nonlinearity (INL) of the 12-b SAR/SS ADC. The measurement results of the DNL and INL are −0.45/+0.84 LSB and −1.5/+0.74 LSB, respectively. The measured DNL in Fig. 13(a) has an LSB of within −1/+1, which satisfies the 12-b resolution without calibration. However, the capacitance mismatch due to parasitic capacitors in the 6-b capacitor DAC repeatedly causes spikes of the DNL and INL. Since the top plate sampling method as shown in Fig. 6 is adopted to simplify the signal routing in the capacitor DAC, an asymmetric INL occurs as shown in Fig. 13(b) due to the input-dependent charge injection.

Table I shows the performance comparison of the proposed SAR/SS ADC with the prior works. Figure of merits (FOMs) are obtained from an equation in [4] to compare the power efficiency of the ADCs. An ADC resolution instead of an effective number of bits is used to calculate the FOMs in order to simplify the comparison. The $\Delta\Sigma$ ADC in [2] and the cyclic ADC in [3] consume large power due to the power-consuming operational amplifier, whereas the SAR ADC in [5] exhibits the best FOM but requires a large area for the capacitor DAC. The SS/SAR ADC in [11] and the SAR/SS ADC in [12] require an external or internal calibration method to improve the ADC linearity [10]. However, the proposed SAR/SS ADC, which achieves a DNL of $-0.45/+0.84$ LSB and an INL of $-1.5/+0.74$ LSB, does not require any calibration method because it is designed to be robust to the variation in the ramp signal, and the gain error of the capacitor DAC. In addition, a readout channel with the proposed SAR/SS ADC consumes a low power of 30 μW by sharing analog circuits between the SAR and SS ADCs.

V. Conclusion

In this paper, a SAR/SS ADC is presented and verified using 1.6 Mpixels 60 frames/s CIS. Since the proposed SAR/SS ADC is robust to the variation in the ramp signal, and the gain error of the capacitor DAC, no calibration method is required. The developed CIS was fabricated using a 90-nm CMOS process, and a readout channel with the proposed SAR/SS ADC occupies a small area of 2.24 μm $\times$ 998 μm by reducing the number of unit capacitors to 1/64th of that of a conventional 12-b SAR ADC, while achieving a low power consumption of 30 μW by sharing analog circuits between the SAR and SS ADCs. The measurement results show that the SAR/SS ADC has a DNL of $-0.45/+0.84$ LSB and an INL of $-1.5/+0.74$ LSB. In addition, using the digital CDS method, a low column FPN of 0.07 LSB_{rms} and a dynamic range of 62 dB are achieved for the developed CIS. Therefore, the proposed SAR/SS ADC is suitable for high-speed CIS applications.

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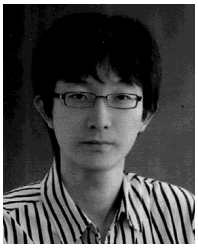

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