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MIXED SIGNAL LETTER

A 0.6 V 100 KS/s 8–10 b resolution configurable SAR ADC in 0.18 μm CMOS

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Abstract A resolution configurable ultra-low power SAR ADC in 0.18 μm CMOS process is presented. The proposed ADC has maximum sampling rate of 100 KS/s with configurable resolution from 8 to 10 b and operates at a supply of 0.6 V. Two-stage bootstrapped switch and voltage boosting techniques are introduced to improve the performance of the ADC at low voltage. To reduce the power consumption of the analog components of the ADC, monotonic capacitor switching procedure and fully dynamic comparator are utilized. The implementation of dynamic logic further reduces the power of the digital circuits. Post-layout simulation results show that the proposed SAR ADC consumes 521 nW and achieves an SNDR of 60.54 dB at 10 b mode, resulting in an ultra-low figure-of-merit of 6.0 fJ/conversion-step. The ADC core occupies an active area of only 350 × 280 μm^2.

Keywords Successive approximation register (SAR) A/D converter · Ultra-low power · Configurable · Low voltage · CMOS

1 Introduction

Nowadays, energy-limited applications such as wireless sensor networks and biomedical applications demand the power-efficient analog-to-digital converters (ADCs) to extend products' life-span. ADCs for such applications are usually required to operate at ultra-low voltage with wide range of flexibility (8–12 bit (b) resolution, 1 KS/s–10 MS/s sampling rate) [1–3]. The successive approximation register (SAR) A/D converters have been a suitable choice due to its simple structure and high energy efficiency. Furthermore, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital components.

Lowering the supply voltage is the most straightforward and effective way to reduce power consumption of A/D converters. But it makes the analog circuit design more challenging. In prior works, several techniques have been proposed to accommodate low-voltage analog circuit design such as using special low-V_{TH} devices [4], gate voltage boosting [5], or body driven circuits [6]. This paper presents a 100 KS/s SAR ADC in 0.18 μm CMOS process that operates at a 0.6 V supply with configurable resolution. The proposed ADC has 3 resolution modes from 8 to 10 b. The D/A converter and SAR logic are designed to be configurable in order to scale its power consumption to the required resolution accordingly. The flexibility of resolution reduces the cost, design time and system complexity. Since the proposed ADC works at ultra-low voltage, several techniques are introduced to achieve high performance. First, the two-stage bootstrapped switches improve the sampling linearity. Second, the transmission gates are used as the resolution switches and the high-level of resolution switch control voltage is boosted by the three-stage clock boosting circuit to reduce on-resistance. Furthermore, the monotonic capacitor switching procedure, fully dynamic comparator, and dynamic logic are utilized to implement the ADC in a power-efficient way. The simulation results indicate the power consumption of the proposed ADC equals to 521 nW at 10 b mode, and scales down to 320 nW at 8 b mode, resulting in figure-of-merits (FOMs) range from 6.0 to 16.7 fJ/conversion-step.

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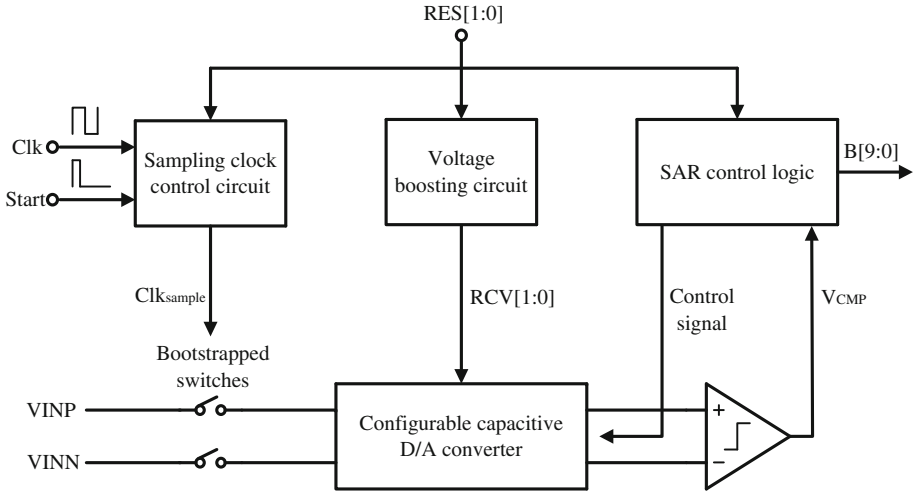

Fig. 1 Block diagram of the proposed 0.6 V 8–10 bit configurable SAR ADC

2 Architecture of the proposed 0.6 V configurable SAR ADC

Figure 1 shows the complete block diagram of the proposed 0.6 V 8–10 b configurable SAR ADC. The ADC core consists of two configurable capacitive D/A converters, two bootstrapped switches, voltage boosting circuit, sampling clock control circuit, SAR control logic, and fully dynamic CMOS comparator.

As shown in Fig. 1, the differential input signal is sampled on capacitors via bootstrapped switches to reduce distortion. *Clk* is the system clock while *Start* is a short pulse to reset and start the ADC. The resolution of the D/A converter, sampling clock, and corresponding SAR logic are digitally controlled by 2 b (RES[1:0]). To improve the performance of the resolution switches, its high-level of control voltage (RCV[1:0]) is boosted by the clock boosting circuit. B[9:0] are the digital outputs of the ADC, and when the resolution of the ADC scales down to 9 and 8 b, the digital outputs are B[8:0] and B[7:0], respectively.

The sampling rate of the proposed ADC is set to 100 KS/s. The ADC can operate at different maximal clock frequencies (1, 1.1, or 1.2 MHz) according to the selected resolution mode (8, 9, or 10 b). To reduce power consumption, relevant circuits will be disabled when the ADC is operating at low resolution modes.

3 Circuit implementation

3.1 S/H circuit

Figure 2 shows the configurable capacitive D/A converters. In order to reduce power consumption and circuit complexity, the monotonic capacitor switching procedure [7] is chosen in this paper. Although the monotonic capacitor switching sequence will induce a dynamic offset of the comparator that affect the ADC linearity, the degradation of performance is acceptable in this work. The unit-element capacitor of the D/A converters is set to 20 fF to reduce nonlinearity caused by mismatch. The proposed ADC samples the differential input signal on the top plates of capacitor through bootstrapped switches.

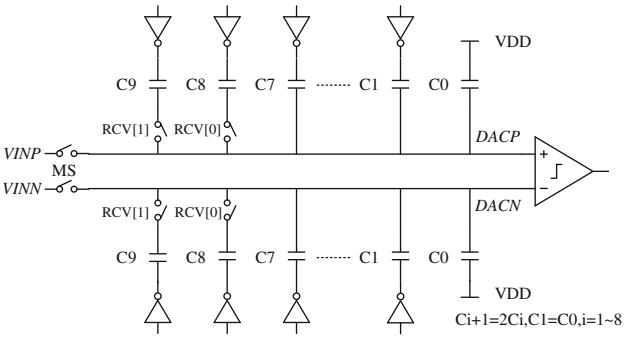

Fig. 2 The D/A converter

For high accuracy A/D converters, a high performance S/H circuit is needed. Therefore, the bootstrapped switch is often adopted to achieve low distortion and rail-to-rail operation. However, when the supply voltage decreases to 0.6 V or even lower, the conventional bootstrapped switch can hardly meet the requirements. This paper introduces a novel two-stage bootstrapped switch to reduce the sampling nonlinearity, as shown in Fig. 3(a). The operation of the proposed bootstrapped switch can be decomposed in two phases: (a) precharge phase, and (b) bootstrap phase. As shown in Fig. 3(b), the operation can be explained as follows: during the precharge phase, *Clks* is low, C_1 and C_2 are both charged to V_{DD}, while V_G (the gate voltage of sampling switch M_S) is V_{GND}. During the bootstrap phase, *Clks* goes high, M_1 and M_4 are turned on and V_G tracks the input signal V_{IN} shifted by $2V_{DD}$, and V_{IN} is sampled on the capacitors. Note that C_1 and C_2 must be sufficiently large to supply charge to the gate of the switching device in

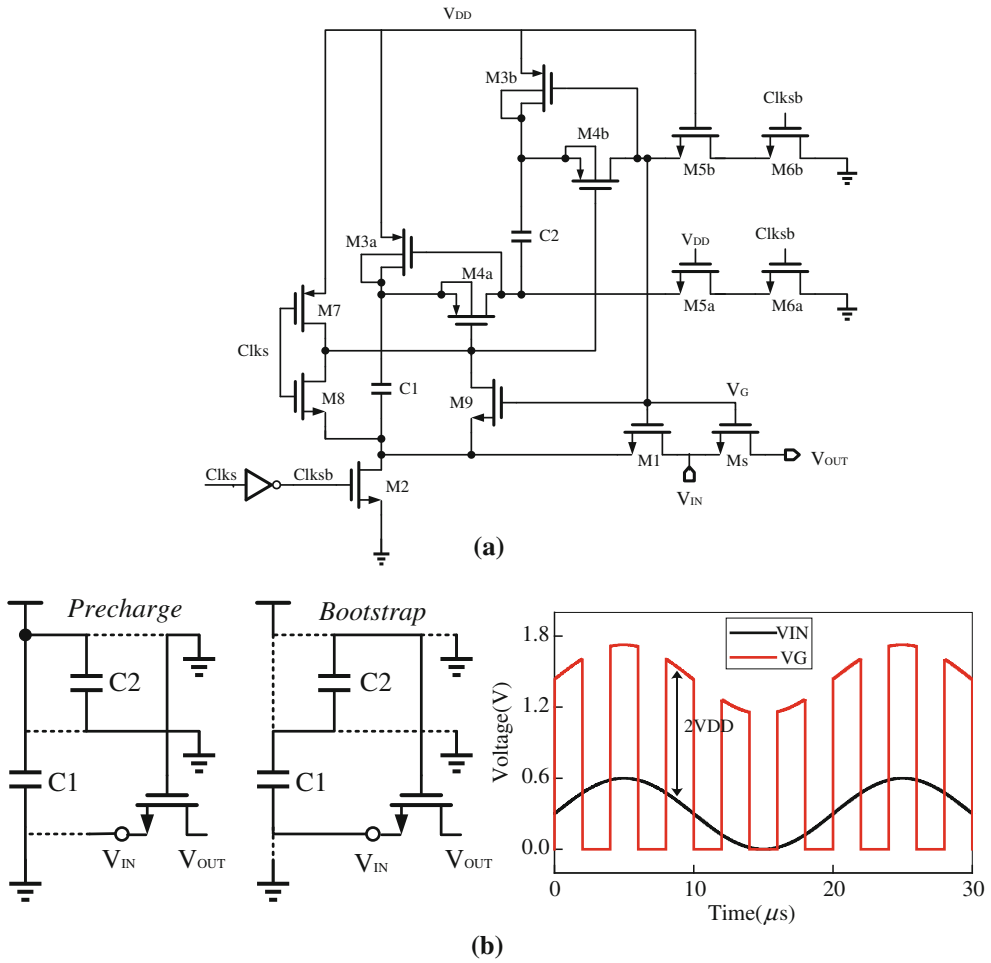

Fig. 3 **a** Two-stage bootstrapped switch. **b** Operation and output

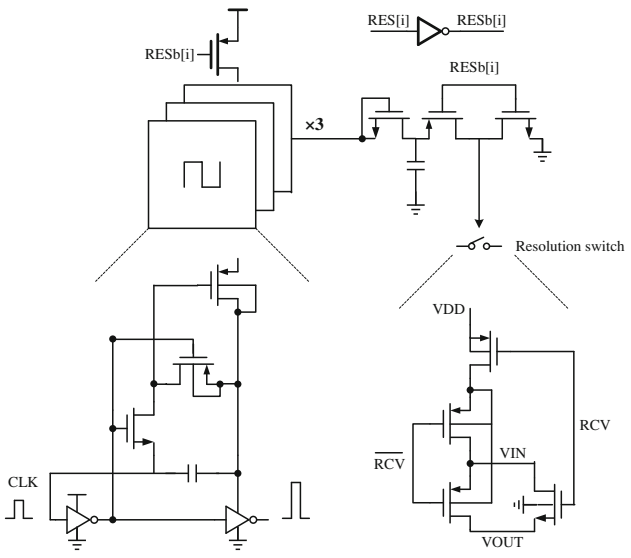

Fig. 4 Resolution switch and voltage boosting circuits

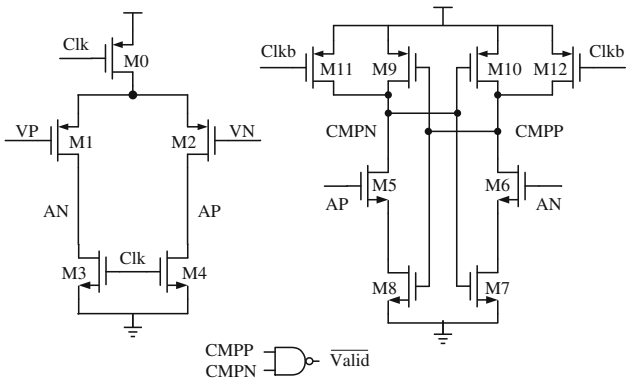

Fig. 5 Two-stage fully dynamic CMOS comparator

addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to (1), where C_{P1} and C_{P2} are

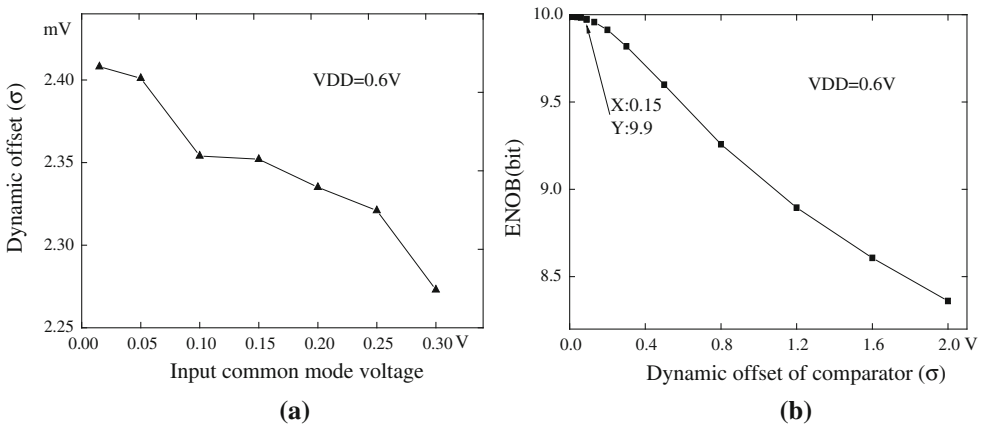

Fig. 6 **a** Offset versus input common mode voltage. **b** ENOB versus dynamic offset of comparator

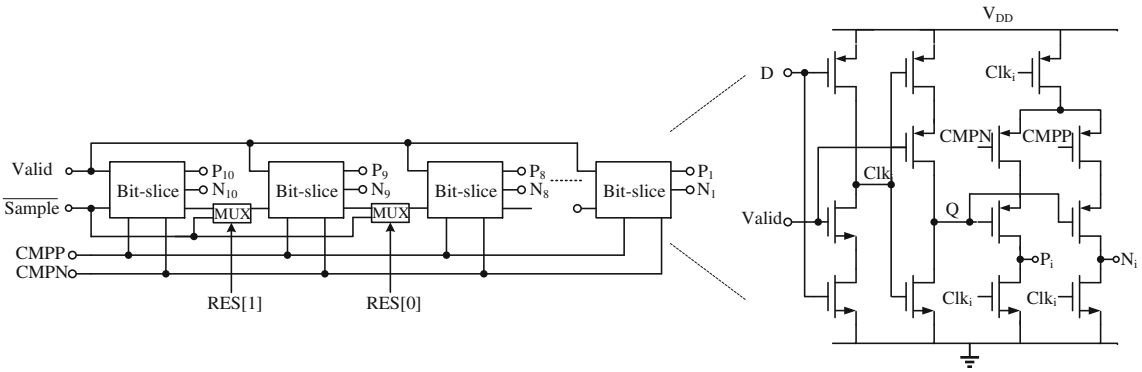

Fig. 7 SAR control logic of the proposed ADC

the total parasitic capacitance connected to the top plates of C_1 and C_2 respectively.

$$V_G = V_{IN} + \frac{C_1}{C_1 + C_{P1}} V_{DD} + \frac{C_2}{C_2 + C_{P2}} V_{DD} \quad (1)$$

Moreover, several transistors are required to improve the circuit reliability. The bootstrap output is also shown in Fig. 3(b).

3.2 Resolution switch and control voltage boosting circuit

The resolution scaling in the D/A converter is implemented by the resolution switch. As shown in Fig. 2, switches are inserted between the top plates of the MSBs capacitors (C_9 and C_8) and comparator input terminals. The capacitors for MSB (C_9) and 2MSBs (C_9 and C_8) are disconnected from the arrays for 9 and 8 b mode, respectively. During the sampling and comparing phase, the switch may introduce nonlinear effects caused by the variation of on-resistance. The transmission gate using bulk-switching of the pMOS transistor [8] is hence chosen as a resolution switch to achieve better linearity by allowing rail-to-rail swing. When the switch is on, the bulk of the pMOS transistor is switched to source, resulting in lower threshold voltage and subsequently low on-resistance. When the switch is off, the bulk is switched to V_{DD} to increase the on-resistance. In order to reduce the gain error caused by parasitic capacitance and distortion induced by leakage current, it is necessary to size the switches carefully.

Figure 4 shows the resolution switch and the circuit used to generate the control voltage of the resolution switch. The high-level is boosted by the clock boosting circuit [9] to reduce the on-resistance. When *RES*[i] is high, the three-stage boosting circuit is active. The boosted voltage is simulated to reach a maximum value around 1.65 V from a supply of 0.6 V. When *RES*[i] is low, the control voltage is pulled down to ground, meanwhile, *RESb*[i] disables the boosting circuit to save power.

3.3 Comparator

The two-stage dynamic comparator [10] shown in Fig. 5 is used to save power. The first stage is a dynamic voltage amplifier and the second stage is a latch. Since the input voltage of the comparator gradually decreases to ground, p-type transistors are used at the input. Benefiting from no static biasing, the average power consumption is proportional to the conversion rate. The proposed comparator has a precision of 1 μV at a clock frequency of 1.2 MHz from

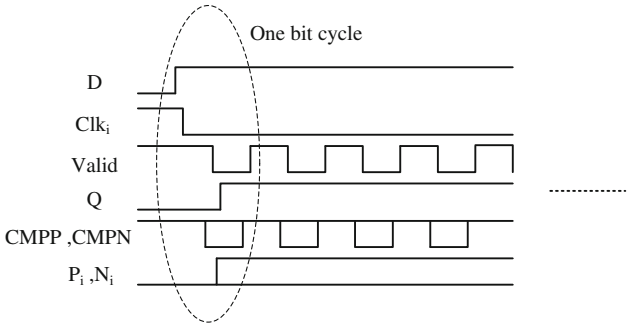

Fig. 8 Time diagram

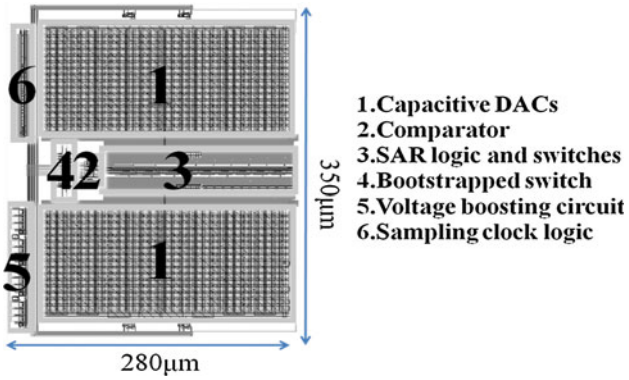

Fig. 10 The layout of the proposed ADC

0.6 V supply. The *Valid* is used as a control signal to enable the SAR logic.

As mentioned before, the monotonic capacitor switching sequence will induce a dynamic offset of the comparator that affects the ADC linearity. Monte-Carlo simulations are performed to measure the comparator offset with its input common mode voltage. Figure 6(a) shows the offset versus common mode voltage. Figure 6(b) reveals the ENOB of a 10-b ADC as a function of dynamic offset of the comparator. The results show the dynamic offset will slightly degrade the performance of ADC, which is acceptable in this work. As for the comparator input referred noise, it is designed much lower than the 10-b quantization noise [10].

3.4 SAR logic and sampling clock control circuit

Figure 7 shows dynamic logic implementation of the SAR control logic, which is basically modified version derived from [11]. By using dynamic logic instead of complementary logic, less transistors are needed, thus offering a better performance in speed and in power consumption.

At the sampling phase, all the outputs of bit-slice cell are reset to low, thus the bottom plates of capacitors are reset to V_{DD}. During the conversion phase, for each bit cycle, according to the comparator output, the capacitor on the higher voltage potential side is switched to ground and the other one remains unchanged. The ADC repeats this procedure until the LSB is decided. The operation of bit-slice cell is as follows: at first the *D* is low and reset the output nodes *P* and *N*, then the *D* is turned to high and *Clk* is pulled down to ground. When the comparator outputs *CMPP* and *CMPN* are ready, the results are stored by *P* and *N*, simultaneously the *Valid* goes low and *Q* is charged to V_{DD} to indicate that this iteration is completed. A time diagram is shown in Fig. 8.

As shown in Fig. 7, two MUXs are inserted in the bit-slice cells to realize the SAR logic at different resolution modes. Since the proposed SAR ADC works at 100 KS/s, the synchronous SAR logic is utilized to avoid delay line circuits where asynchronous logic is required. The sampling time is set to 2 periods of the system clock to reduce the sampling error. The sampling clock for different modes is generated by a 4-b counter and combinational circuits, as shown in Fig. 9.

4 Simulation results

The proposed ADC is designed in 0.18 μm 1.8 V CMOS process and occupies an area of 0.098 mm^2. Figure 10 shows the layout of the ADC. The DACs use metal–insulator–metal capacitors. The capacitance of a unit cell is about 20 fF. The total input capacitance of the proposed ADC is about 10.24 pF. The binary-weight capacitor array is laid out based on partial common-centroid layout strategy [12].

Post-layout simulations are performed to characterize the dynamic performance of the ADC for all resolution modes. The 1,024-point FFT spectrum of the proposed ADC at 10 b mode is shown in Fig. 11, for a sinusoidal wave input at 47.37 kHz, sampling rate of 100 KS/s and supply of 0.6 V. The SNDR is 60.54 dB providing an

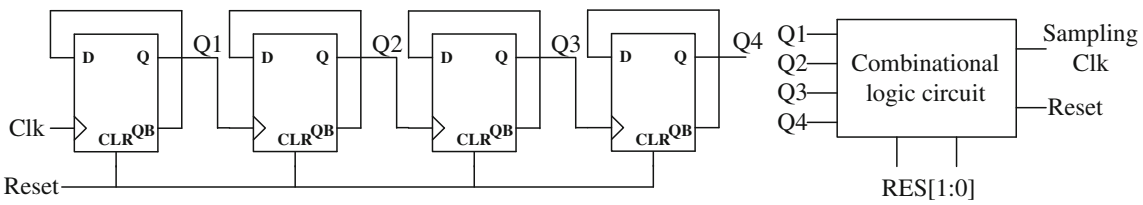

Fig. 9 Sampling clock control circuit

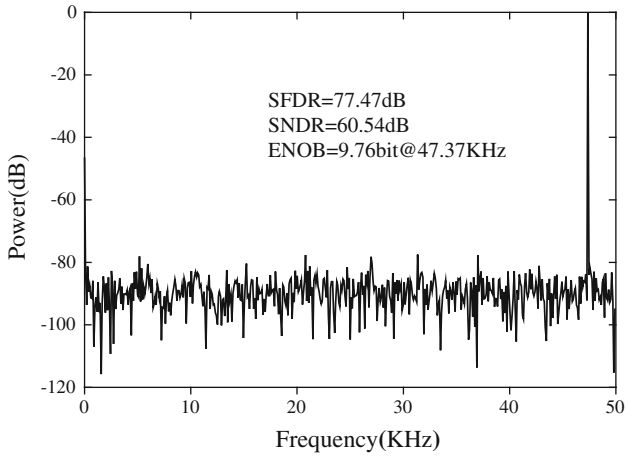

Fig. 11 Simulated 1,024-point FFT spectrum of the proposed ADC at 10-bit mode

Table 1 Power consumption of the proposed SAR ADC at 3 resolution modes

	8 bit	9 bit	10 bit
DACs (nW)	63	113	204
Comparator (nW)	15	17	19
SAR logic (nW)	26	27	28
Sampling clock control circuit (nW)	21	23	25
Voltage boosting circuit (nW)	78	86	94
Parasitics	117	133	151
Total power (nW)	320	399	521

ENOB of 9.76 b. The ENOBs of the ADC for the 9 and 8 b resolution modes are 8.59 and 7.58 b, respectively.

Table 1 shows the power consumption of ADC blocks for all resolution modes. It confirms that the total simulated power consumption of the proposed SAR ADC scales with the resolution. The parasitic component is obtained by subtracting the schematic-based result from the post-layout result. As shown in Table 1, DACs consume the largest amount of power at 10 b mode, and the power of DACs decreases rapidly as the resolution scales down. Therefore, using a more energy-efficient switching scheme or smaller unit capacitor could further improve the power-efficiency of this work. When the ADC operates at low resolution mode, the undesired parasitics consumes the largest part of the total power.

Table 2 summarizes the simulated performance of SAR ADC for all modes and compares the proposed ADC with other state-of-the-art ADCs. Here, the FoM used to evaluate the power efficiency is configured as

$$FOM = \frac{Power}{\min\{f_s, 2 \times ERBW\} \times 2^{ENOB}} \quad (2)$$

where the f_s is the sampling rate, and the ENOB is the effective number of bits at the effective resolution bandwidth. The FOMs of the proposed ADC range from 6.0 to 16.7 fJ/conversion-step, depending on the selected resolution.

5 Conclusion

In this paper, a 100 KS/s configurable ultra-low power SAR ADC in 0.18 μm CMOS process is presented. The proposed ADC resolution can be varied from 8 to 10 b with supply voltage of 0.6 V. The two-stage bootstrapped switches are used to improve the sampling linearity of the ADC at low supply voltage. Furthermore, the high-level of resolution switch control voltage is boosted by the three-stage clock boosting circuit to reduce the switch on-resistance during the successive approximation operation. The use of monotonic capacitor switching procedure, fully dynamic comparator, and dynamic logic brings a considerable reduction of the total power of the ADC. The

Table 2 Performance summary and comparison

	[1]*	[2]*	[3]*	[10]*	[12]*	This work**		
Technology	90 nm	180 nm	180 nm	65 nm	130 nm	180 nm		
Resolution (bit)	9	10	8	10	10	8	9	10
Sampling rate (Hz)	4 M	100 K	100 K	1 M	1 K	100 K		
Supply (V)	1.1	0.6	1.0	1.0	1.0	0.6		
Diff. input range (V_{PP})	1.36	1.2	2.0	1.25	1.78	1.12		
Power (μW)	13.57	1.3	19	1.9	0.053	0.32	0.40	0.52
SFDR (dB)	N/A	67	63.2	N/A	67.6	56.6	61.7	77.5
SNDR (dB)	54.1	57.7	49.7	54.4	56.7	47.4	53.5	60.5
ENOB (bits)	8.7	9.3	7.96	8.75	9.1	7.58	8.59	9.76
FOM (fJ/conv.-step)	8.2	21	76.3	4.4	94.5	16.7	10.4	6.0

* Measure results

** Post-layout simulation results

simulation results show the ADC offers an FOM of 6.0 fJ/conversion-step while consumes 521 nW at 10-b mode.

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