An Energy/Illumination-Adaptive CMOS Image Sensor With Reconfigurable Modes of Operations

Jaehyuk Choi, Seokjun Park, Jihyun Cho, and Euisik Yoon

***Abstract*—We present an energy/illumination-adaptive CMOS image sensor for distributed wireless sensor applications. The adaptive feature enables always-on imaging operation with extremely low power consumption for extended lifetime of wireless image sensor nodes and provides optimum images in a wide range of illuminations. For adaptive operation, the sensor employs reconfigurable modes of operation. Most of time, the sensor is in a monitoring mode, which keeps imaging at extremely low power consumption. The sensor turns into a high-sensitivity imaging mode or a wide dynamic range imaging mode when illumination varies and sufficient power supply is available from energy harvesting. The sensor changes its operation back to the monitoring mode in order to save energy in the battery. The sensor operates at 1.36 μW/frame in the monitoring mode from harvested energy and provides high-sensitive (24 V/lx $\cdot$ sec) and wide dynamic range images (99.2 dB) at 867 μW in battery operation. The chip achieved power FOM of 15.4 pW/pixel $\cdot$ frame in 0.18 μm technology.**

***Index Terms*—CMOS image sensor, CMOS imager, low power, wide dynamic range, wireless sensor network, wireless sensor node.**

I. Introduction

IMAGING systems are integrated in most mobile devices, which are enabled by low-cost CMOS image sensors. In mobile applications, imaging systems are battery-operated, and transmit images through wireless networks. Currently, tiny wireless sensor nodes equip image sensors and collect information from the wide area covered by wireless sensor networks (WSN) [1]–[3]. In the WSN, distributed sensor nodes autonomously operate at extremely low power consumption from energy harvesting to monitor wide and unreachable areas for military surveillance, environmental monitoring, traffic management, etc. The wireless sensor nodes are also applicable to biomedical systems such as endoscopy, microscopy, retinal prosthesis, etc [4]–[6].

In applications for wireless sensor nodes, the biggest challenge is low power consumption from the limited energy sources such as batteries and/or energy harvesting from the ambient. From solar energy harvesting, we can get power delivery of only 360 pW/mm^2 $\cdot$ lx [19]. In overcast days under 1,000 lx illuminance, available power from a 5×5 mm^2 solar cell would be only 9 μW. Because most state-of-the-art image sensors require large power consumption of over 50 mW [17], they are not applicable to wireless sensor nodes. Moreover, the power consumption of CMOS image sensors is difficult to scale down because voltage scaling directly suppresses SNR and degrades image quality. For applications in wireless sensor nodes, many low power imagers have been reported. A vision sensor that asynchronously generates outputs only when events are detected is useful for WSN applications because the amount of data can be significantly reduced [32], [33]. However, these vision sensors should include in-pixel circuits for detecting events based upon contrast or motion changes [34], which increase a form factor of the sensor and may not be able to provide post image processing capabilities such as object detection and recognition [13]. Some image sensors employed in-pixel pulse-width-modulation to achieve low power consumption from low supply voltage instead of conventional analog readout [13]–[16], [28]. Even though these low power imagers enabled a long lifetime of the sensor node, an additional challenge for wireless sensor nodes is to accommodate the wide range of illumination. In outdoor surveillance and biomedical applications, sensors should provide both high sensitivity in low illumination [7]–[9] and wide dynamic range (WDR) to prevent saturation in high illumination [10]–[12]. However, the dynamic range (DR) should be traded off by higher sensitivity because the enhanced signal swing from low illumination will make saturation even at moderate illumination. Moreover, imagers with the integrated DR extension scheme consume large power over 100 mW [10], [12], which is unsuitable for WSN applications.

Constant operation at the maximum awareness requires large power consumption and is not feasible for energy-limited applications. Moreover, both the sensitivity and DR cannot be simultaneously optimized for image capturing in the wide range of illumination. Therefore, it is imperative to implement an image sensor adaptable to energy availability and illumination levels; i.e., the sensor keeps monitoring at an extremely low power consumption, but only turns into providing high sensitivity or WDR imaging when illumination varies or sufficient power is available from energy harvesting. In this paper, we report an energy/illumination adaptive CMOS image sensor, which employs four different modes of operation: monitoring, normal, high-sensitivity and wide-dynamic-range (WDR) modes. The adaptive sensor consumes low power of < 1.36 μW/frame in the monitoring mode, while provides high sensitivity of > 23.9 V/lx$\cdot$sec in the high-sensitivity mode and extends its DR over 99.2 dB in

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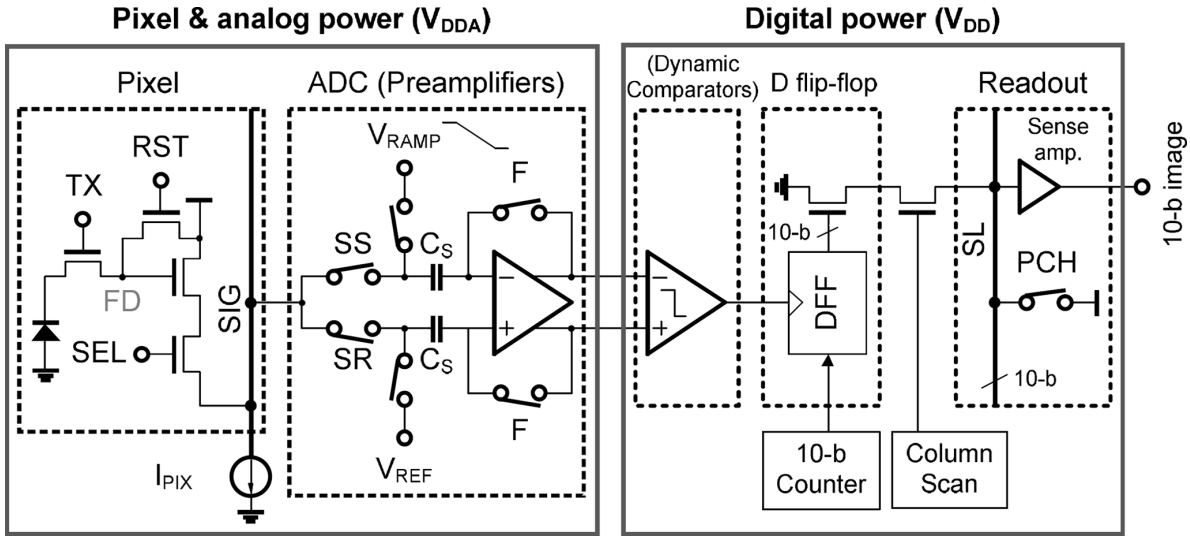


Fig. 1. Image signal chain of conventional image sensors.

the WDR mode. For adaptive operation, we designed a reconfigurable pixel with a small pitch of 5.6 μm and a reconfigurable ADC, which operates at low voltage (0.8 V) and gives adaptive sensitivity and DR (1.8 V). In addition, we implemented a low-power digital signal readout scheme that suppresses redundant switching operation. For the DR extension, we implemented a novel low-power dual exposure scheme without increasing area overhead.

This paper is organized as follows. Section II introduces low power design approaches. Section III presents the operation of adaptive imaging to accommodate variation in illumination and energy availability. Section IV describes circuits for adaptive imaging and suppressed switching for power reduction. The experimental results are presented in Section V, followed by conclusion in Section VI.

II. Power Reduction Methodologies in CMOS Image Sensors

Low power consumption is the most critical factor to extend lifetime in battery-operated wireless sensor nodes. However, power reduction without performance degradation in conventional image sensors is challenging. Fig. 1 shows a signal chain of the conventional CMOS image sensors that employ a column-parallel single-slope (SS) ADC. Typically, separate power supplies are used for enhanced noise immunity: V_{DDA} for analog circuits and V_{DD} for digital circuits. The SS ADC consists of a static preamplifier for suppressing fixed pattern noise (FPN) from the offset voltage of dynamic comparators by providing a high gain, a dynamic comparator for regeneration, and a N-bit D flip-flop (DFF) that latches N-bit counter outputs. For power estimation, we designed circuits for the image signal chain illustrated in Fig. 1 and performed circuit simulation with 0.13 μm CMOS technology. For comparison and analysis of circuit simulations, we assumed a 320 $\times$ 240 image array that operates with a rolling shutter at 15 fps. The row access time (T_{ROW}) includes pixel access time (T_{PIX}, for readout of reset and signal voltages though in-pixel source followers), A/D conversion time (T_{ADC}), and digital signal readout time (T_{RD}, for column scanning and readout of digital signals using sense amplifiers).Fig. 2 shows the composition of simulated power consumption of the CMOS image sensor from the given parameters summarized in Table I. We investigated power consumption according to the variation of power supply voltage, resolution, pixel pitch, etc., when scaling design parameters (voltage, bandwidth, load capacitance, etc.) using MATLAB. Upon this simulation result, low power design approaches are discussed in the following subsections.

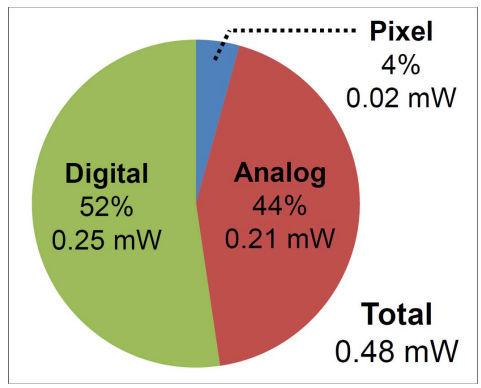


Fig. 2. Power consumption of a 320 $\times$ 240 (QVGA) image sensor.

A. Voltage Scaling

Voltage scaling in digital circuits significantly saves power consumption because dynamic power consumption is proportional to $V_{DD}{}^2$. As shown in Fig. 2, digital power consumption takes more than 50% with 1.8 V supply voltage. Fig. 3 shows the power consumption of digital circuits can significantly reduce from voltage scaling. However, benefit of voltage scaling has limitation in analog circuits. The reduced output swing of in-pixel source followers due to voltage scaling will suppress SNR. Therefore, it is desirable to implement a reconfigurable pixel that can operate with adaptable supply voltages; i.e., low supply voltage for constant monitoring and high supply voltage only for quality imaging, which will be described in Section III.

TABLE I
PARAMETERS FOR THE SIMULATION OF POWER CONSUMPTION

Pixel array	$\#_{COL} \times \#_{ROW}$	320 × 240 (QVGA)
Pixel pitch	W_{PIX}	5 μm
Frame rate	$FR = 1/T_{INT}$	15 fps
Integration time	T_{INT}	66.6 ms
Row access time	$T_{ROW} = 1/(FR \cdot \#_{ROW}) = T_{PIX} + T_{ADC} + T_{RD}$	277.5 μs
Pixel access time	T_{PIX}	8 μs
ADC resolution	N	10 bit
ADC time	$T_{ADC} = 2^N \cdot T_{CLK}$	204.8 μs
Digital signal readout time	$T_{RD} = \#_{COL} \cdot T_{CLK}$	64 μs
Clock frequency	$f_{CLK} = 1/T_{CLK}$	5 MHz
Pixel&analog power supply	V_{DDA}	2.8 V
Digital power supply	V_{DD}	1.8 V

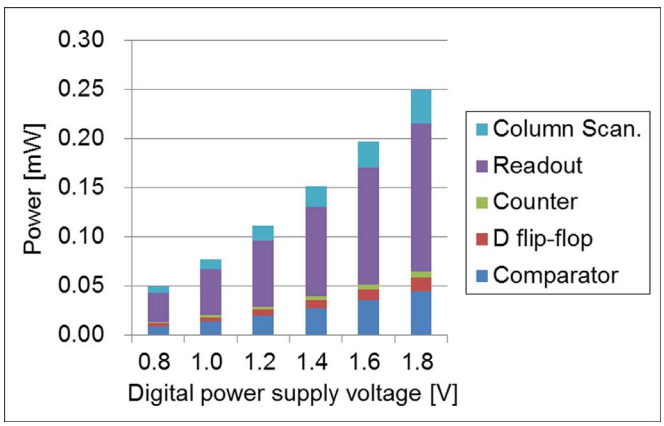
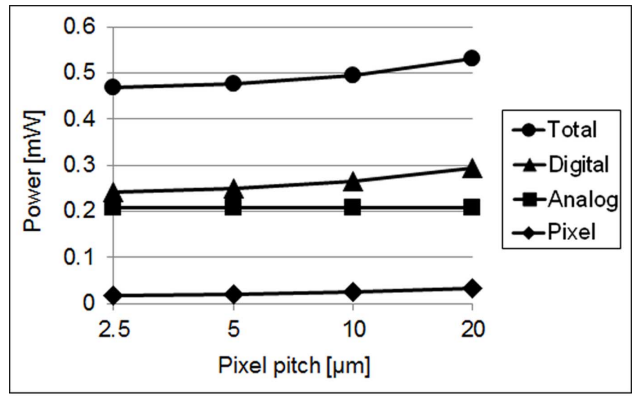
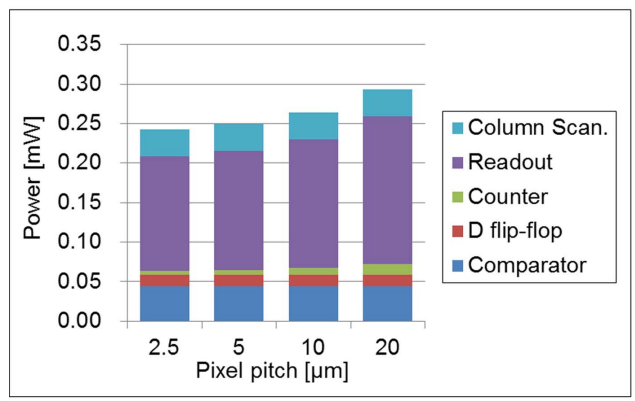


Fig. 3. Digital power consumption as digital supply voltage (V_{DD}) scales.



(a)



(b)

Fig. 4. Power consumption as a function of pixel pitch: (a) Total power consumption and (b) Digital power consumption.

B. In-Pixel Comparator for A/D Conversion

As illustrated in Fig. 2, analog power consumption takes a little more than 40% of total power consumption. In order to reduce the analog power consumption, many low power imagers employed in-pixel comparators for ADC [13]–[16] instead of column-parallel comparators. However, in-pixel comparators take the significant portion of pixel area and increases the pixel size. The large pixel pitch from in-pixel circuits increases a form factor of the sensor, which is not desirable for low-cost, compact wireless sensor nodes. Section IV will present how to achieve in-pixel comparison without sacrificing the pixel size.

C. Small Pixel Size

As shown in Fig. 4, the power consumption increases as a pixel pitch becomes larger due to the additional parasitic capacitance increase in signal lines. Note that the analog power consumption (mainly come from the preamplifier of ADCs) remains constant because it has the fixed load capacitance in the dynamic comparator that is driven by the preamplifiers. In Fig. 4(b), the power consumption of the counter increases, although small, because the load capacitance of driving buffer circuits increases as the pixel pitch increases. As shown in Fig. 4, a small pixel pitch ($< 5\ \mu$m) can save the total power by more than 0.06 mW when compared to a large pixel pitch ($> 20\ \mu$m) due to reduction in digital power consumption, which is critical in low power imagers targeting under 100 μW. Although contemporary image sensors employing in-pixel source followers offer a small pixel size [17], [18], they have limitations in voltage scaling due to reduced signal swing, gain loss from the body effect, and non-linearity. Instead of using source followers, an in-pixel comparator can be used for SS A/D conversion (in-pixel PWM) for low supply voltage. The advantage is that it is less vulnerable from body effect and bias current variation which are main sources of inducing non-linearity. However, this scheme requires a large pixel size with additional transistors [13], [16] and pMOS transistors [14], [15] in the pixel. Another possible issue is input voltage variation during long A/D conversion time (2^N cycles) in the rolling shutter operation. Even in the global shutter operation, short conversion time is desirable because the stored signals in the floating diffusion can be corrupted from the spilled charges in high illumination. Section IV explains our proposed reconfigurable pixel circuit with a small pixel size and short A/D conversion time.

D. Suppression of Switching

Power consumption can be further reduced by suppressing unnecessary switching operations. One example is a DFF in the SS ADC. The DFF continuously changes states for latching counter outputs before the comparator output is toggled. Since power consumption is dependent on the number of toggles,

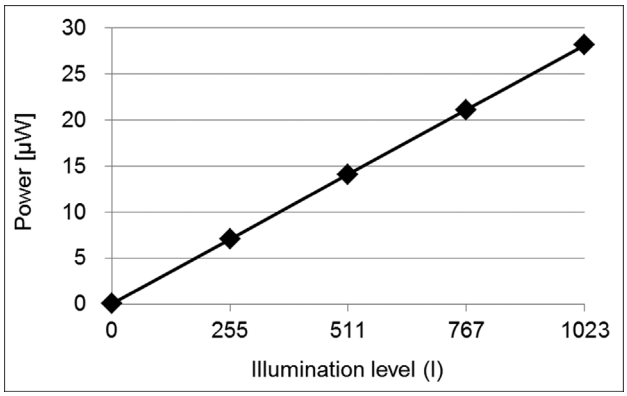


Fig. 5. Power consumption of 10-bit D-flip flop in the single slope ADC according to signal levels (or illumination levels).

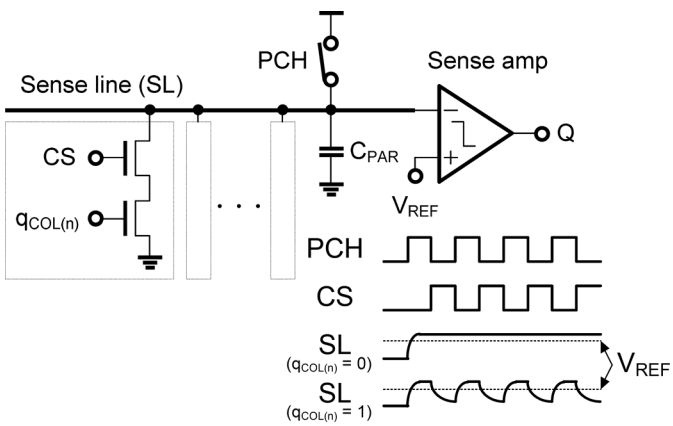


Fig. 6. Digital signal readout circuit.

power consumption increases when signal levels increase (i.e., higher illumination). Fig. 5 shows simulated power consumption of 10-bit DFF as the average signal level varies 0 (dark) to 1023 (bright). Another source of redundant switching is the digital signal readout circuit shown in Fig. 6. For digital signal readout, multiple sense lines (SL) with a large parasitic RC should be precharged (PCH ='1') in each cycle. Whenever the digital signal stored in the DFF is '1', the precharged voltage drops and dissipates dynamic power and precharged again in the next cycle. In Section IV, the proposed scheme to suppress these redundant switching operations will be introduced.

III. Energy/Illumination Adaptive Imaging

A. Reconfigurable Modes of Operation for Adaptive Imaging

The proposed adaptive imaging scheme has four different modes of operation according to available energy and illumination, as illustrated in Fig. 7. In the monitoring mode, the sensor keeps capturing images at extremely low power consumption from harvested energy. The sensor generates 8-bit image data at low temporal resolution (1 fps). Even though each sensor node operates at low frame rates, the multiple sensor nodes in different locations can monitor the scene at different timing to produce collective information without missing any events. When enough energy is available either from harvesting or from battery, the sensor turns into one of three modes according to illumination: high-sensitivity mode, normal mode, and WDR mode. The sensor generates 10-bit images at a higher temporal resolution (controllable below 15 fps), as long as the stored energy allows. The sensor provides high sensitivity in low illumination and it extends its maximum detectable range in high illumination. The sensor switches its operation back to the monitoring mode when it is needed to save charges in the battery.

Fig. 8 shows the sensor architecture. Image signals are read out through the column parallel ADC and stored in the latch. The column scanner accesses the latch for digital signal readout through sense amplifiers. The sensor operates with dual supply voltages for energy efficiency: 0.8 V for low power consumption in the monitoring mode and 1.8 V for the rest three modes. Pixel circuits are designed to be reconfigurable for low voltage operation as well as for adaptive sensitivity and DR. The column-parallel ADC is reconfigured to operate in one of the two ADC schemes. It operates as an 8-bit successive approximation (SAR) ADC for low power consumption in the monitoring mode. But it operates as an a 10-bit SS ADC for high linearity and superior column-to-column matching in the other three modes. A 10-bit gray counter is used for the SS ADC. We chose a SAR ADC in the monitoring mode for three reasons: First, it has a short A/D conversion time (eight cycles for 8-bit), which provides negligible variation of input voltage (in pixels) from incident light. This allows for direct conversion of analog signals in pixels into digital signals without additional sampling capacitors. Second, it gives low power consumption due to reduced switching time (8 times of switching), whereas the SS ADC has 2^8 times. Third, its operation is compatible with low supply voltage because it is composed of a simple comparator and does not require any additional analog circuits such as ramp generators [31] required in the SS ADCs.

B. Dual-Exposure With Pixel Merging for Dynamic Range (DR) Extension

Many DR extension schemes have been reported using linear-logarithmic pixels [20], [24], lateral overflow [11], [21], and conditional reset [10], [22]. Among many schemes, the multiple-exposure scheme [12], [23] is advantageous because no additional in-pixel circuits are required. However, it should need embedded storage circuits. In the case of triple exposure scheme, three image signals with three different integration times need to be synthesized. In order to do this, two image signals should be temporarily stored in the line memory until the last image signal is available [12]. The multiple-exposure scheme also entails large power consumption due to multiple readouts.

In this work, we implemented a low power dual-exposure scheme with pixel merging. The operation principle of the dual-exposure scheme is shown in Fig. 9(a). One signal from short integration time (T_{INT2}) and the other signal from long integration time (T_{INT1}) are synthesized for capturing images to prevent saturation. In order to avoid additional memory requirement, we proposed the dual-exposure scheme based on pixel merging. As shown in Fig. 9(b), two rows have T_{INT1} and the other two rows have T_{INT2}. In the readout, one row with T_{INT1} and one row with T_{INT2} are merged to generate a signal with the extended DR. Although this scheme sacrifices a spatial resolution by half, it is adequate for low-power applications be-

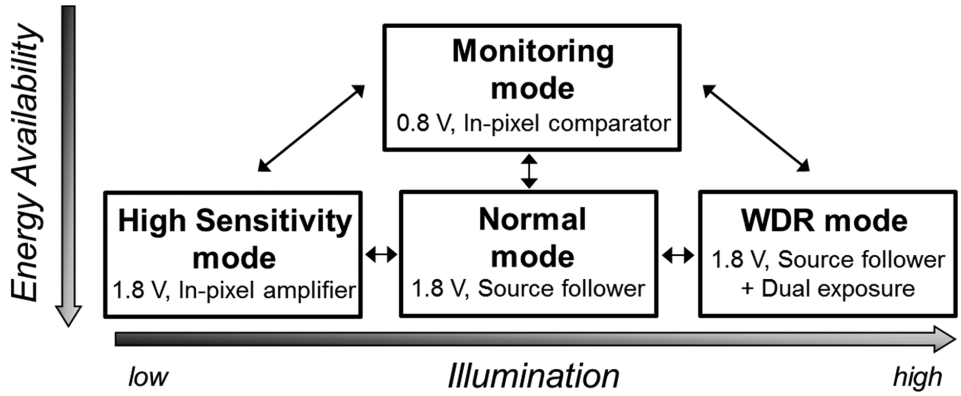


Fig. 7. Energy/illumination adaptive imaging operation.

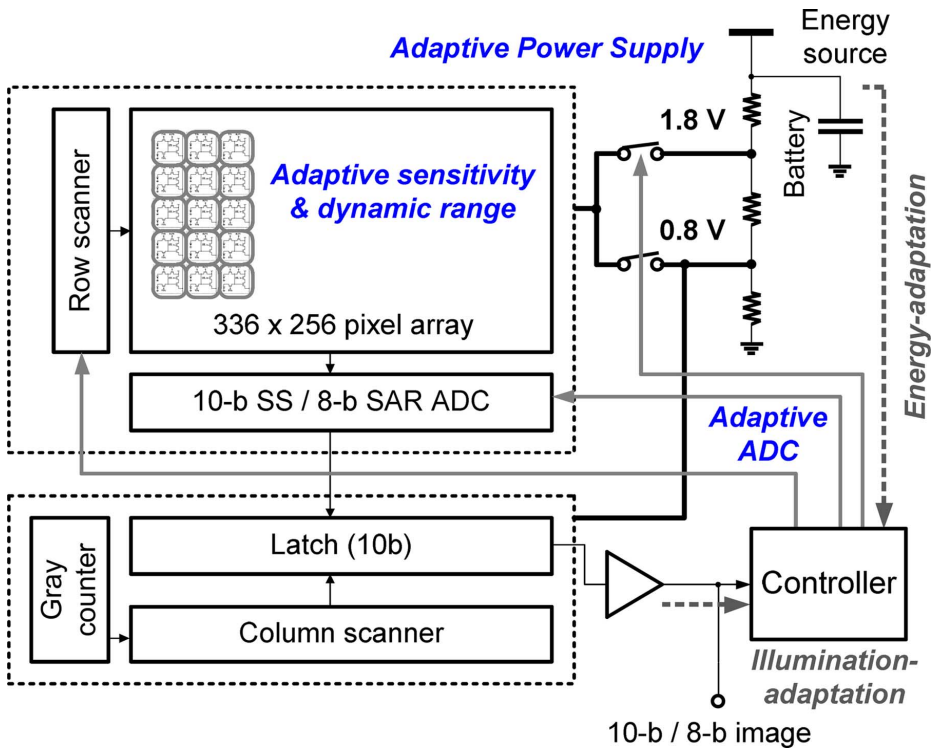


Fig. 8. Architecture of the proposed adaptive CMOS image sensor.

cause the operation requires only one time readout without additional memory circuits. Detailed operation will be described in Section IV.

IV. Circuits for Reconfigurable Modes

A. Reconfigurable Pixel Circuit

In order to provide optimum signals according to variation in supply voltage and illumination, we used a reconfigurable pixel circuit that adaptively changes its topology for various operation modes. In the monitoring mode, the pixel circuit operates as a part of a comparator (preamplifier) for SAR ADC with the reduced supply voltage (0.8 V). In the high-sensitivity mode, the pixel circuit amplifies small signals and enhances sensitivity. The pixel circuit is also reconfigured to become a source follower to handle large signals for higher illumination. Fig. 10 shows the pixel architecture and equivalent circuits. Two pixels are vertically shared and grouped together. Two groups of pixels form a differential pair for in-pixel amplification. In the vertically-shared pixels, two electronic shutters are driven separately: $TX0_E$ (or $TX1_E$) for the upper row and $TX0_O$ (or $TX1_O$) for the lower row. Note that $TX0_{E,O}$ controls one group and $TX1_{E,O}$ controls the other group in a differential pair. In order to reduce V_{GS} drop and increase signal swing, low-V_T transistors are used for T_{AMP}. In this work, we used a 4-T pixel architecture with a pinned photodiode (PPD) that requires high voltage for TX in order to transfer all the charges from the PPD into the floating diffusion (FD) node. Because the highest supply voltage in the sensor is 1.8 V, the TX is boosted to 2.5 V (implemented outside of the chip) to achieve complete charge transfer. For differential readout, each group has separate signal lines (SIG0, SIG1). A common line (COM), shared by two groups, is

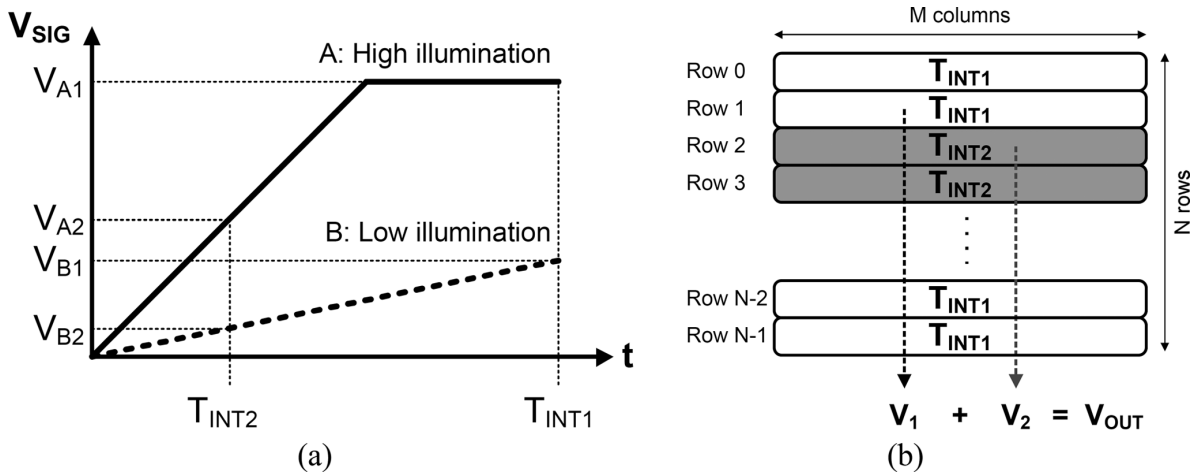


Fig. 9. Dual exposure scheme: (a) Operation principle and (b) Dual exposure with pixel merging.

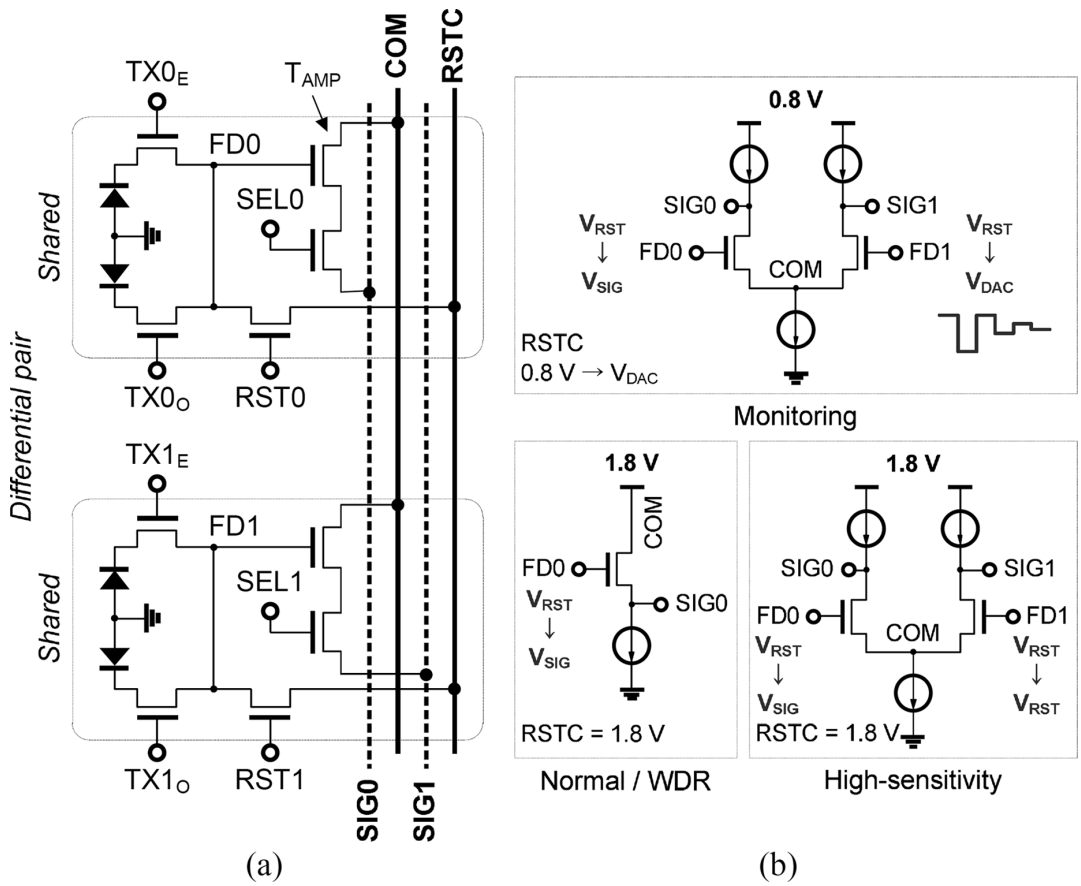


Fig. 10. Reconfigurable pixel circuit: (a) Pixel architecture and (b) Equivalent circuits in each mode.

connected to either supply voltage (for source follower) or current bias (for differential amplifier). An additional line (RSTC) is connected either to the column-parallel capacitive DAC in the monitoring mode or to the supply voltage for reset operation.

In the monitoring mode, the pixel circuit operates as a preamplifier for SAR ADC, as shown in Fig. 11(a). The signal from the capacitive DAC, located in the column circuit, is provided through RSTC. The output of the in-pixel preamplifier is regenerated through the dynamic comparator in the column circuit. The operation procedure is illustrated in Fig. 11(b). First, two FDs (FD_0 and FD_1) are reset. The amplified offset voltage of the in-pixel preamplifier is stored in capacitors located in the column circuit for offset cancelling. Second, the integrated charges in the PPD are shared with the reset charges in FD_0. Third, SAR A/D conversion starts. Fourth, both PPD and FD_0 are reset to start integration cycles for the next frame. For complete charge transfer from the PPDs, the FD should be reset with high voltage (typically over 2.8 V). Accordingly, high supply voltage is required for in-pixel source followers and column-parallel ADC circuits to access and process high-voltage sig-

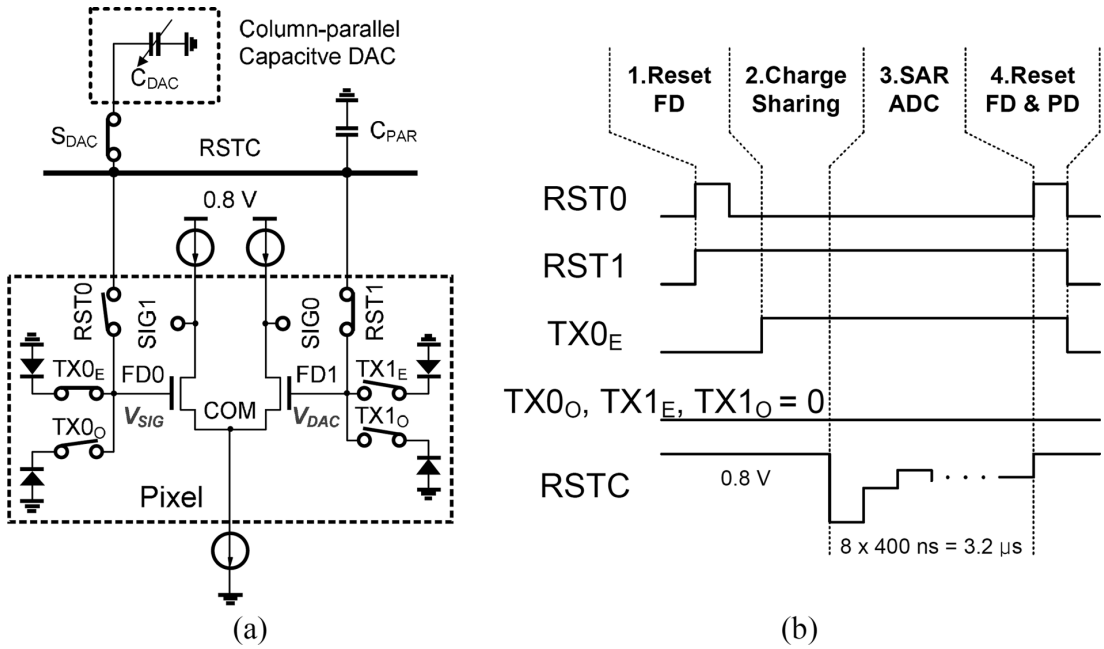


Fig. 11. Equivalent ADC circuit in the monitoring mode: (a) Circuit and (b) Timing diagram.

nals from the FD. Therefore, overall power consumption of the sensor is increased. In order to address this problem, we used the charge sharing method instead of the charge transfer. Charge sharing between the PPD and the FD can be easily performed by enabling TX. The shared node is reset by low voltage of 0.8 V, allowing low supply voltage (0.8 V) for both pixel and ADC circuits. In the readout, we employed a double sampling (DS) for offset cancellation: sampling reset voltage (at phase 1) and signal voltage (at phase 2) consecutively. Since the reset voltage is not correlated with the signal, true correlated double sampling (CDS) that suppresses kTC reset noise cannot be achieved. Instead, we can achieve significant power savings from voltage scaling. The CDS is enabled in the other three modes with charge transfer. In the capacitive DAC ($\mathrm{C_{DAC}}$), we need an additional capacitor, $\mathrm{C_{REF}}$, for generating $\mathrm{V_{REF}} = \mathrm{C_{DAC}V_{DD}}/(\mathrm{C_{REF}} + \mathrm{C_{DAC}})$ from supply voltage of $\mathrm{V_{DD}}$ and an analog buffer circuit driving the RSTC line. However, in our approach, we reduced both power and area overhead by using the inherent parasitic line-capacitance of RSTC ($\mathrm{C_{PAR}}$) as a reference capacitor without buffering, which generates $\mathrm{V_{REF}} = \mathrm{C_{DAC}V_{DD}}/(\mathrm{C_{PAR}} + \mathrm{C_{DAC}})$. The measured $\mathrm{V_{REF}}$ from the fabricated sensor is 0.41 V. In order to address any possible capacitance mismatching and suppress column FPN, we used enough unit capacitance (30 fF MIM) and added four small capacitors to calibrate the variation of $\mathrm{C_{PAR}}$.

In the high-sensitivity mode, the pixel circuit operates as a differential common-source amplifier and provides a high gain over 6. In the common source amplifier, the closed loop gain is determined by $\mathrm{C_{FD}}/\mathrm{C_{gd}}$ [8], [9], where $\mathrm{C_{gd}}$ is the parasitic capacitance between gate and drain. The equivalent thermal noise charge of the in-pixel amplifier is reduced to $C_{FD}\sqrt{(\gamma kT)/(g_m r_{ds} C_{SIG})}$ [9], where $\mathrm{C_{FD}}$ is the FD capacitance, $\mathrm{C_{SIG}}$ is the load capacitance, and $\mathrm{g_m r_{ds}}$ is an open loop gain. In addition, the input referred noise from the column-parallel ADC circuit is suppressed by gain amplification. The differential amplifier generates output signals from two FDs: one captures signal voltage and the other contains reset voltage. The amplified differential output is delivered to the column-parallel ADC. The operation procedure is as follow. First, two FDs are simultaneously reset. Second, the integrated charges in the PPD are transferred to $\mathrm{FD_0}$. Note that $\mathrm{FD_1}$ keeps the reset voltage without charge transfer. Third, SS A/D conversion starts. The mismatch between transistors ($\mathrm{T_{AMP}}$, shown in Fig. 10) may introduce gain variation. One easy way to improve matching is to increase the size of $\mathrm{T_{AMP}}$. This can result in the increase of $\mathrm{C_{FD}}$, which suppress sensitivity in the other three modes. However, this scheme has two advantages. First, the in-pixel gain amplification enables low power consumption without using column-level amplifiers. Second, the common source amplification can be implemented without additional in-pixel circuits.

In the normal and WDR mode, the pixel circuit is reconfigured to form a simple source follower. For WDR operation, the sensor operates in dual exposure using the pixel merging. In the two-shared pixels, two signals with different integration times can be easily combined by charge summing, as shown in Fig. 12(a). Two transfer gates are opened simultaneously, and charges are summed in the FD. However, the charge summing may have signal corruption when the high illumination pixel spills its charges into the FD as shown in Fig. 12(a). Also, the FD can be saturated after summing the large amount of charges from two PPDs. In order to address this problem, we use the same integration time in the two-shared pixels, as shown in Fig. 12(b), but assign the different integration time to each group. In the two groups of two-shared pixels, one group has $\mathrm{T_{INT2}}$ and the other group has $\mathrm{T_{INT1}}$. Since the pixels with $\mathrm{T_{INT2}}$ are isolated from those with $\mathrm{T_{INT1}}$, charge spillover will not contaminate the signals. This signal synthesis is performed after A/D con-

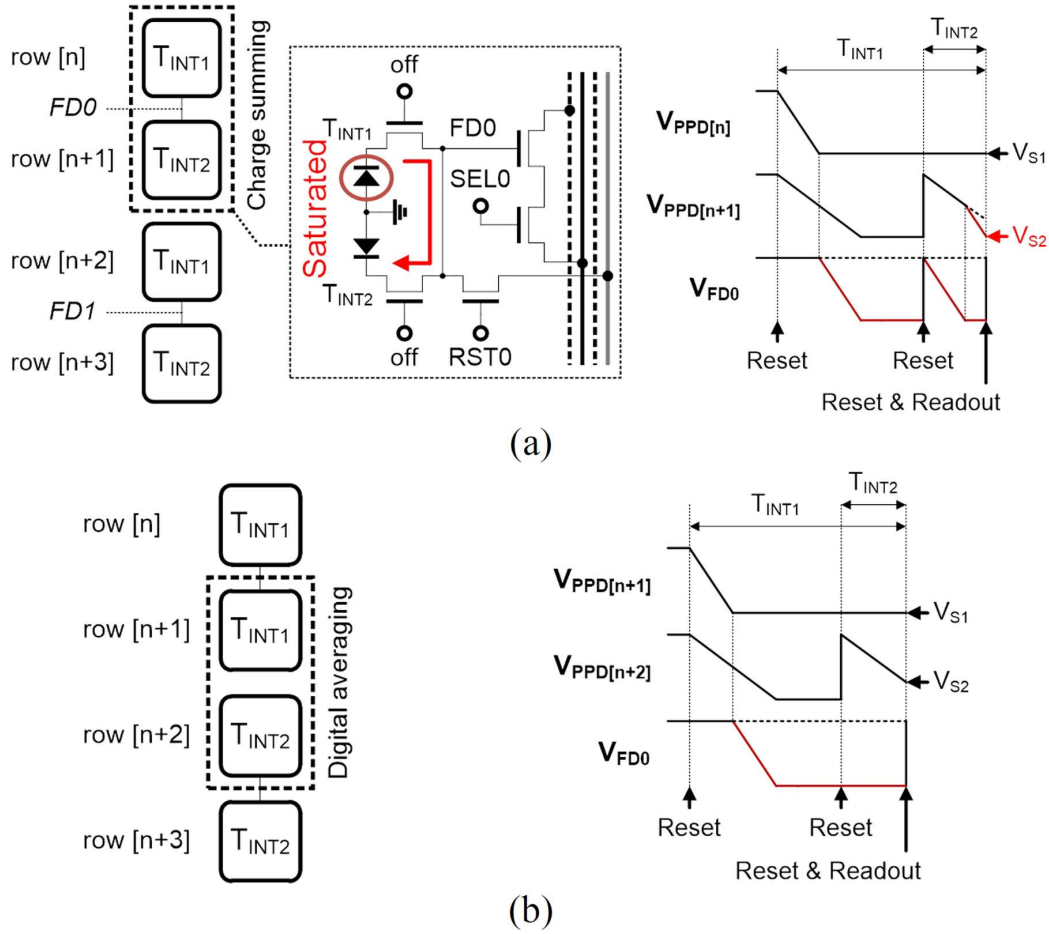


Fig. 12. Pixel merging in WDR mode: (a) Charge summing with leakage problem and (b) Digital averaging without leakage problem. V_{PPD} is a cathode voltage of the pinned photodiode.

version through a digital adder, which is actually implemented in the FPGA of testing circuit board.

B. Reconfigurable ADC Circuit

The reconfigurable ADC circuit for multi-mode operations is shown in Fig. 13. The ADC consists of a preamplifier operating at 1.8 V, a dynamic comparator at 0.8V, and mode selection switches. In the monitoring mode, only 0.8 V supply voltage is used and the column preamplifiers are turned off for power saving. The amplified signal from the signal lines (SIG0, SIG1) is directly delivered to a dynamic comparator through 'SM' for SAR ADC. The capacitive DAC (C_{DAC}) is connected to RSTC through switch S_{DAC}. The q_{0-7} is the output from the 8-bit latch that controls the driving of C_{DAC}. In the other three modes, the ADC operates as a SS ADC. The coupling capacitor (C_C) stores the offset voltage of the preamplifier and suppresses the column FPN. In the normal and WDR modes, reset voltage is sampled to C_{DAC}, signal voltage is sampled to C_S, and then V_{RAMP} is being swept. In the high-sensitivity mode, operation is fully differential, i.e., the differential signals from pixels are sampled to C_S and C_{DAC}, respectively.

C. Latch Circuit With Reduced Switching

The switching occurs up to 2^{10} times in the DFF of 10-bit SS ADC. In order to suppress dynamic power consumption, we implemented the latch circuit with the reduced number of switching as shown in Fig. 14(a). The latch operates for both SAR and SS ADC operations by multiplexing. For SAR ADC operation in the monitoring mode (SAR ='1'), the latch stores the comparator output (T) at clock signal (CLK_{SAR}). For SS ADC operation in the other three modes (SAR ='0'), the latch stores the counter output using the comparator output (T) as a clock signal. As shown in Fig. 14(b), the differential latch circuit switches only once during the whole SS ADC cycles, whereas the conventional DFF changes its state whenever a counter output toggles.

D. In-Equality Readout Circuit

As shown in Fig. 6, digital signal readout involves high frequency switching to precharge the sense lines (SL), which entails huge dynamic power consumption. Fortunately, image signals have strong locality, i.e., high probability that neighbor pixels have similar values [25], [26]. Using the locality attribute of in image signals, we implemented the inequality readout scheme in which the output only toggles when there are unequal signals among neighbor columns as shown in Fig. 15. We simply add one XOR gate in each readout cell in the 4 MSBs that have strong locality. One of the two inputs in the XOR gate comes from the left column. The SL keeps the precharged voltage if two consecutive columns have the

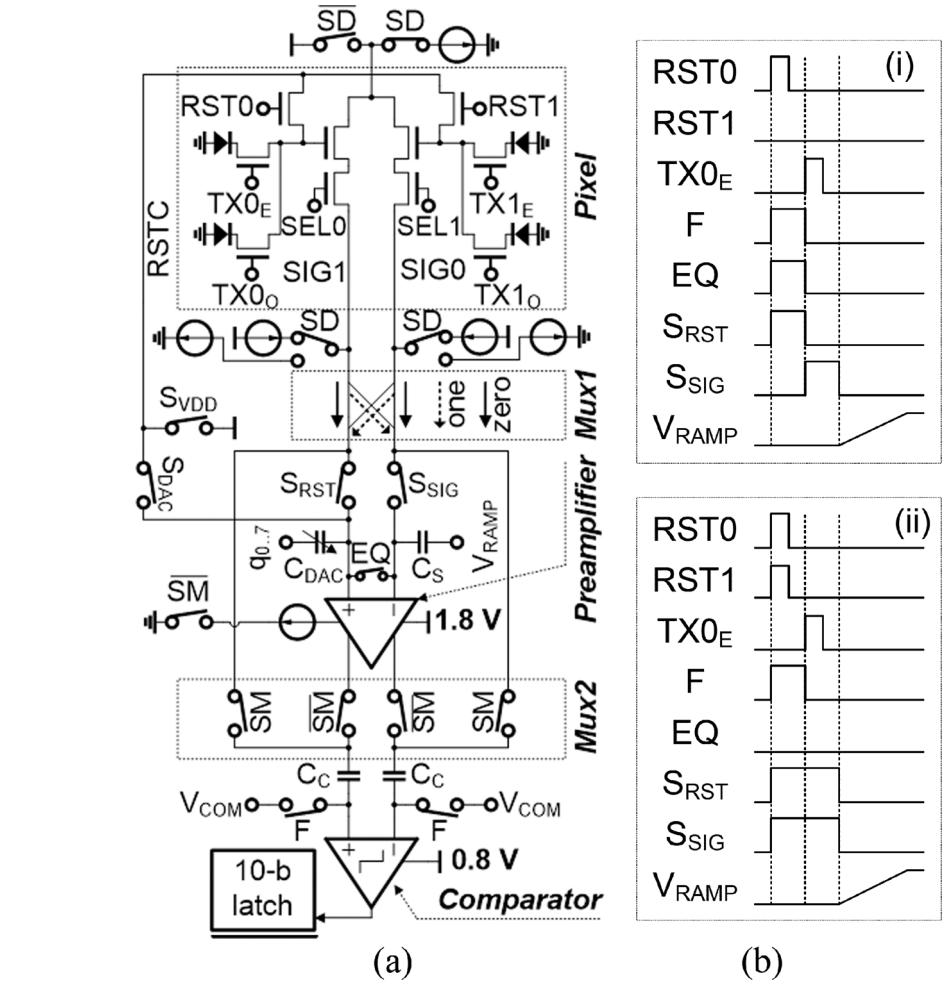


Fig. 13. Reconfigurable column-parallel ADC circuit: (a) Circuit and (b) Timing diagram for (i) normal/WDR mode and (ii) high-sensitivity mode. The switch SD is '1' for differential readout and '0' for source follower readout. Multiplexer 1 (Mux1) changes the output polarity of the in-pixel differential amplifiers. In multiplexer 2 (Mux2), the switch SM is '1' for monitoring mode, and '0' for the other three modes.

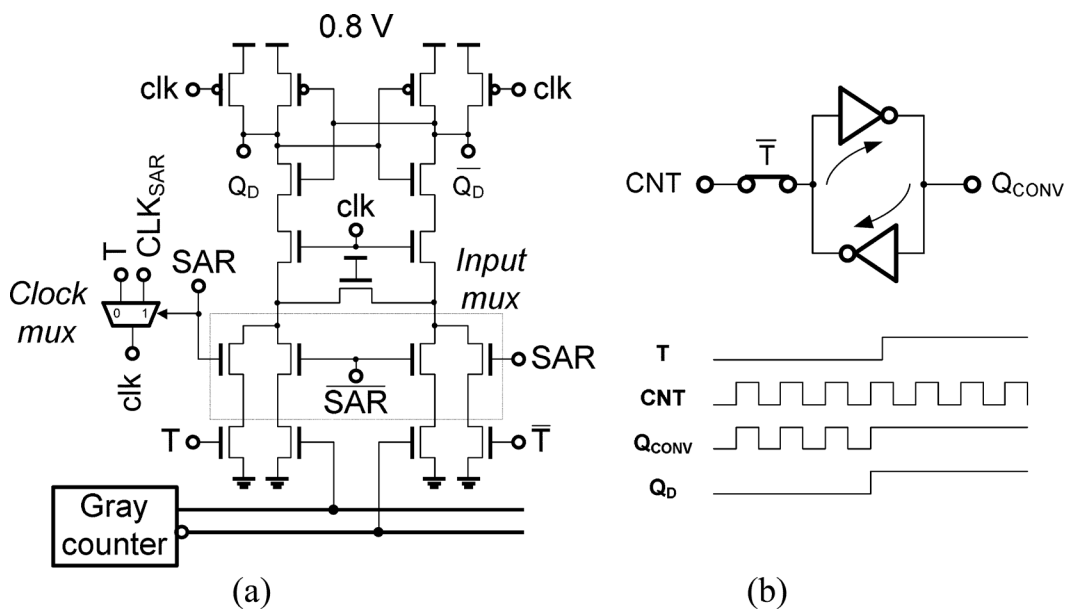


Fig. 14. Latch circuit: (a) Differential latch circuit with the reduced number of switching and (b) Switching in conventional latch circuit.

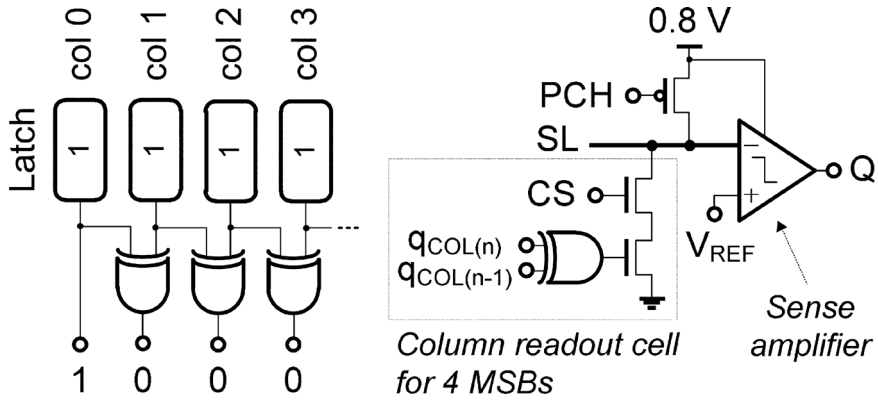


Fig. 15. In-equality readout: Architecture and circuit.

same value, which significantly suppresses dynamic power consumption by reducing the precharge occurrence in the huge capacitive node of SL. Note that we read a digital signal level (0 or 1) in the 1st column. From the 2nd column, we read the inequality signals, from which full digital signals can be easily decoded according to inequality toggles.

V. Experimental Results

A prototype chip has been fabricated using 0.18 μm 2P4M CIS process and fully characterized. A chip photograph is shown in Fig. 16. Fig. 17 shows captured images from the fabricated sensor. First two images were captured in the monitoring mode (@ 9 lx). Next two images were captured in the normal mode at low illumination (left, @ 0.4 lx) and high illumination (right, @ 340 lx), respectively. Sensitivity was enhanced by providing a high gain in the high-sensitivity mode, and the saturation is eliminated in the WDR mode as shown in the last two images of Fig. 17. Regular non-uniform patterns (repeated in every eighth row) were observed in the captured images, which come from fabrication process of microlens. These patterns are not measured when we read out the FD node by linearly decreasing the external analog voltage (emulating increased illumination) through reset transistors for testing purpose. In order to calibrate these patterns, we measured the output response of eight rows for various illumination levels (by adjusting T_{INT}) and applied the adjusted sensitivity of each row in Fig. 17, such that eight rows have the same response to given illumination. Table II summarizes characteristics of the fabricated chip. We achieved a small pixel pitch of 5.6 μm with a high fill factor of 45.5% by employing the reconfigurable pixel circuit with two-shared pixels. Sensitivity is enhanced to 23.9 $V/lx \cdot sec$ in the high-sensitivity mode. In the monitoring mode, sensitivity has been decreased due to reduced conversion gain from charge sharing. In the WDR mode, the minimum integration time (T_{INT2}) is set by $T_{INT1}/128$, which can increase the maximum detectable signal by 128 times (42 dB). Using the dual exposure scheme, the DR is extended to 99.2 dB in the WDR mode. The FPN has been increased in the high-sensitivity mode due to gain mismatch between pixels. However, input-referred random noise has been reduced by more than a factor of two from gain amplification. The FPN in the monitoring mode also increased mainly due to low supply

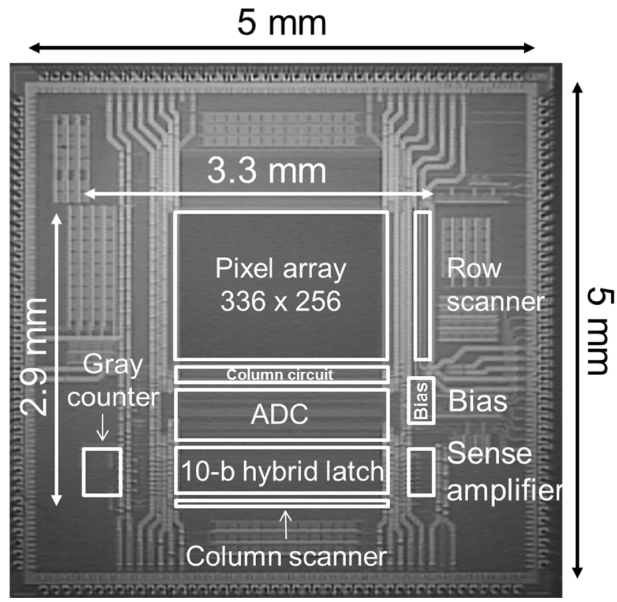


Fig. 16. Chip microphotograph.

voltage and capacitance mismatch in the SAR ADC. Random noise is increased in the monitoring mode due to kTC reset noise, which cannot be suppressed by double sampling. In the other three modes, kTC noise is suppressed with CDS. Total power consumption of the monitoring mode is only 19.9 μW (@ 15 fps), which is 39 times lower than that of the normal mode. Fig. 18 shows the distribution of power consumption in each mode. Compared with the simulation results in Fig. 2, we have higher analog power in the normal and high-sensitivity modes because we adopted the SS ADC operating at 10 MHz for enough margin, instead of using 5 MHz as in the simulation. The digital power decreased owing to voltage scaling. The pixel power takes 71.5% of total power in the monitoring mode because of in-pixel preamplification. The analog power from the column-parallel preamplifier is negligible.

In order to verify power reduction in the inequality readout, we tested 100 images from the public image database [27] and measured the probability of equality (P_{EQ}) as shown in Fig. 19(a). The P_{EQ} is the probability that 1-bit digital signals in specific bit position are same as the left column. For comparison with the conventional readout scheme, we

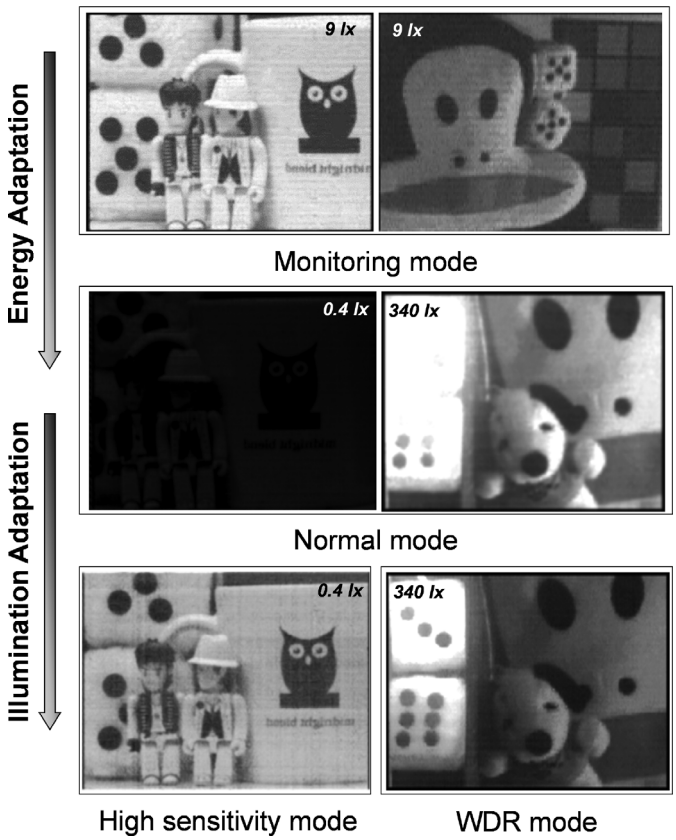


Fig. 17. Sample images (@15 fps): Images captured in the monitoring mode (top, 9 lx), images captured in the normal mode (middle left: 0.4 lx, middle right: 340 lx), an image captured in the high-sensitivity mode (bottom left, 0.4 lx), and an image captured in the WDR mode (bottom right, 340 lx, $T_{INT2} = T_{INT1}/16$).

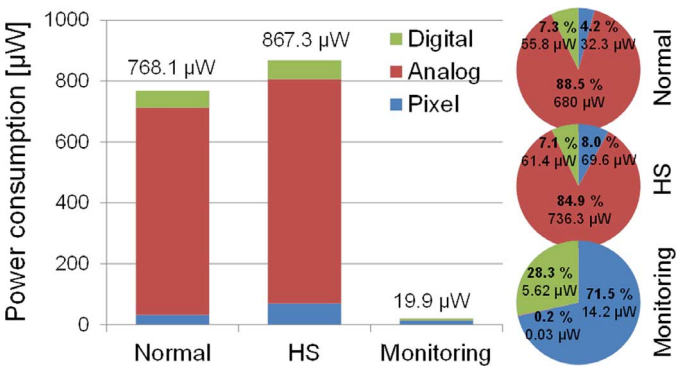


Fig. 18. Comparison of power consumption in each operation mode.

also measured the probability of '1' (P_1) from the same test images (Fig. 19(b)). The P_1 is the probability that the 1-bit digital signal in a specific bit position is '1'. The P_{EQ} is 0.73 in the 4th bit and 0.94 in the MSB, whereas the P_1 is around 0.5 in every bit position. The power consumption overhead from the transmission-gate based XOR is negligible and the area overhead is only 0.36%. According to this analysis, we can estimate 68% power reduction in the precharging circuits, which gives 5% reduction in total power consumption in the monitoring mode.

TABLE II
CHIP CHARACTERISTICS

Process	0.18 μm 2P4M CIS		
Pixel size	5.6 × 5.6 μm²		
Pixel array	336 × 256		
Fill factor	45.5 %		
Dynamic range	57.1 dB (normal) / 99.2 dB (WDR)		
Mode	Normal	High sensitivity	Monitoring
Sensitivity [V/lx·sec]	4.02	23.9	0.65
FPN (@dark) [%] (1)	0.29	0.75	1.35
Random noise (@dark) [DN]	0.33 (0.78 mV / DN)	0.98 (0.36 mV / DN)	0.95 (1.5 mV / DN)
V_{REF} (ADC)	0.8 V	0.4 V	0.4 V
Power (Pixel, @ 15 fps)	32.3 μW	69.6 μW	14.2 μW
Power (Analog, 1.8 V, @ 15 fps)	680 μW	736.3 μW	0.03 μW
Power (Digital, 0.8 V, @ 15 fps)	55.8 μW	61.4 μW	5.62 μW
Total Power (@ 15 fps)	768.1 μW	867.3 μW	19.9 μW
			1.36 μW (@ 1fps)
Power FOM [pW/pixel·frame]	595.32	672.2	15.4

(1) $100 \times \sqrt{\sigma}/2^N$ [%] for N-bit, measured from averaging of 50 consecutive images at 15 fps

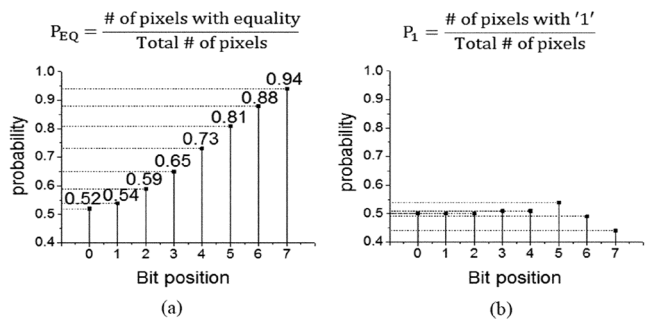


Fig. 19. Testing result of digital signal readout: (a) Probability of equality in inequality readout and (b) Probability of '1' in conventional readout.

The power figure of merit (power FOM) is defined as the power consumption normalized to the number of pixels and the frame rate, given by power/pixel · frame [16], [28]. The fabricated sensor shows a power FOM of 15.4 pW/pixel · frame in the monitoring mode. Power consumption is the most critical factor in wireless sensor nodes, and it is important to have a low power FOM. However, the power FOM does not accurately reflect the performance of low-power imagers because SNR can be compromised with power reduction.

Table III summarizes the performance comparison with the previous low-power imagers. Fig. 20 shows the performance plot in terms of SNR and power FOM. In wireless sensor nodes, the sensor should be able to operate solely depending on harvested energy, which requires the power FOM of a QVGA (320×240) image sensor under 117 pW, assuming that energy harvesting can deliver 9 μW (5×5 mm^2 solar cells, 1 klx). At the same time, an effective bit-depth of images should be over 8 bits ($<$ 1 LSB noise, 48.2 dB SNR) in order to provide images without significant loss of information and performance degradation. The fabricated adaptive sensor has a power FOM of 15.4 pW/pixel · frame with 48.6 dB SNR, which satisfies both requirements in power $<$ 117 pW/pixel · frame and SNR $>$ 48.2 dB. Since the power FOM is still 7.5 times lower than the requirement, SNR can be further improved

TABLE III
PERFORMANCE COMPARISON WITH PREVIOUS LOW-POWER IMAGE SENSORS

Ref.	[29] TED'03	[28] ISSCC'08	[15] JSSC'10	[30] ISSCC'11	[16] JSSC'13	[32] JSSC'13	[14] JSSC'14	[35] VLSI'14	This work
Readout of pixels	Analog	PWM	PWM	Analog	PWM	LPF	PWM	PWM	SAR (monitoring)
Process	.5 μm CMOS	.35 μm CMOS	.5 μm CMOS	.5 μm CMOS	.18 μm CMOS	.18 μm CMOS	.35 μm CMOS	65 nm CMOS	.18 μm CIS
Resolution	176× 144	128× 96	256× 256	54× 50	64× 40	64× 64	256× 256	128× 128	336× 256
Pixel pitch [μm]	5	10	5	21	10	26	5.9	4	5.6
Fill factor [%]	38	18.5	31.6	32	25.4	12	30	57	45.5
Supply [V]	1.5	1.35	0.5	1.2	0.5	3.3	1.3	0.5	0.8
Power [μW] (@ frame rate)	550 (30)	55.2 (9.6)	1.2 (8.5)	14.25 (7.4)	4.95 (11.8)	33 (13)	51.06 (15)	NA	19.9 (15)
Power FOM [pW/pixel·frame]	723 .3	467.9	8.6	713.2	147.3	620	51.94	17	15.4
SNR [dB]	49.6	54.63	23.05	60.38	63.95	52	NA	44.4	48.6

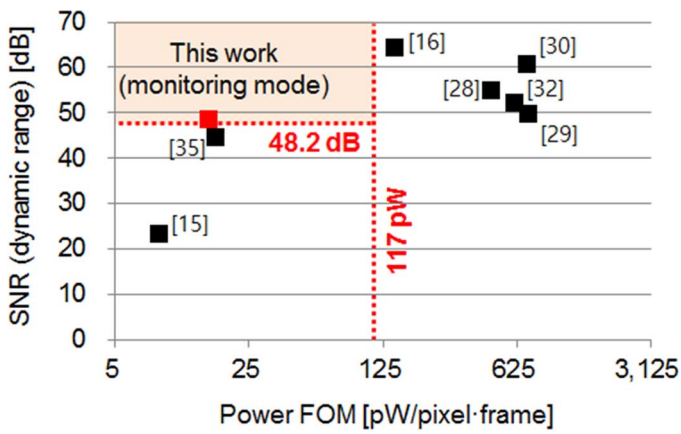


Fig. 20. Performance comparison: SNR vs. power FOM.

by enhancing the signal swing. In this work, we used a fixed supply voltage (0.8 V).

VI. CONCLUSION

An energy/illumination adaptive image sensor has been implemented by reconfigurable pixels for various modes of operations, which significantly reduce power consumption while providing high-quality images with high SNR and WDR. The sensor employs four different modes of operation: monitoring mode, high-sensitivity mode, normal mode and WDR mode, adaptively switching the mode according to available power and illumination and levels. The reconfigurable pixel was implemented with a small pitch of 5.6 μm, and the ADC circuit employed an in-pixel comparator without area overhead. For dynamic range extension, we implemented a low power dual exposures scheme with pixel merging. Further power reduction was achieved from differential latch and inequality readout scheme by eliminating redundant switching in digital outputs. The sensor operates at 1.36 μW/frame or a power FOM of 15.4 pW/pixel $\cdot$ frame in the monitoring mode, and reconfigures to capture high-sensitive images at 24 V/lx $\cdot$ sec and WDR images up to 99.2 dB.

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