A 10 000 Frames/s CMOS Digital Pixel Sensor

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, and Abbas El Gamal, *Fellow, IEEE*

***Abstract*—A 352 × 288 pixel CMOS image sensor chip with per-pixel single-slope ADC and dynamic memory in a standard digital 0.18-μm CMOS process is described. The chip performs "snap-shot" image acquisition, parallel 8-bit A/D conversion, and digital readout at continuous rate of 10 000 frames/s or 1 Gpixels/s with power consumption of 50 mW. Each pixel consists of a photogate circuit, a three-stage comparator, and an 8-bit 3T dynamic memory comprising a total of 37 transistors in 9.4 × 9.4 μm with a fill factor of 15%. The photogate quantum efficiency is 13.6%, and the sensor conversion gain is 13.1 μV/e$^-$. At 1000 frames/s, measured integral nonlinearity is 0.22% over a 1-V range, rms temporal noise with digital CDS is 0.15%, and rms FPN with digital CDS is 0.027%. When operated at low frame rates, on-chip power management circuits permit complete powerdown between each frame conversion and readout. The digitized pixel data is read out over a 64-bit (8-pixel) wide bus operating at 167 MHz, i.e., over 1.33 GB/s. The chip is suitable for general high-speed imaging applications as well as for the implementation of several still and standard video rate applications that benefit from high-speed capture, such as dynamic range enhancement, motion estimation and compensation, and image stabilization.**

***Index Terms*—ADC, CMOS image sensor, digital pixel sensor, high-speed imaging, image sensor, memory.**

I. Introduction

SEVERAL CMOS image sensor architectures have been developed in recent years. Whereas most of these architectures, for example, the passive pixel sensor (PPS) [1] and the active pixel sensor (APS) [2]–[4], have analog readouts, the more recently developed digital pixel sensor (DPS) [5] employs an analog-to-digital converter (ADC) per pixel and digital data is read out of the image sensor array (see Fig. 1). The DPS architecture offers several advantages over analog image sensors. These include better scaling with CMOS technology due to reduced analog circuit performance demands, and the elimination of read-related column fixed-pattern noise (FPN) and column readout noise. More significantly, by employing an ADC and memory at each pixel, massively parallel A/D conversion and high-speed digital readout provide unlimited potential for high-speed "snap-shot" digital imaging. This benefits traditional high-speed imaging applications (e.g., [6], [7]) and enables the implementation of several still and standard video rate applications that require high-speed capture such as sensor dynamic range enhancement and motion estimation [8]–[10].

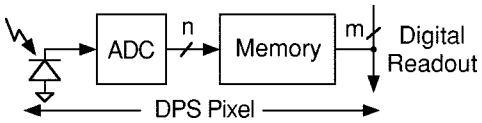


Fig. 1. Simple DPS pixel block diagram.

The main drawback of DPS is that it uses more transistors per pixel than conventional analog image sensors and therefore can have larger pixel sizes. Since there is a lower bound on practical pixel size imposed by the wavelength of light, imaging optics, and dynamic range, this drawback quickly disappears as CMOS technology scales down to 0.18 μm and below. Designing image sensors in such advanced technologies, which will be needed for implementing true camera-on-chip systems, is challenging due to the scaling of supply voltage and the increase in leakage currents [12].

In this paper, we describe a 352 × 288 CMOS DPS with per-pixel ADC and digital memory fabricated in a standard digital 0.18-μm CMOS technology. The goals of our design are: 1) to demonstrate a DPS with bit-parallel ADC and memory per pixel (our earlier implementations [8], [11] employed a shared bit-serial ADC and a 1-bit latch per 2 × 2 block of pixels); 2) to evaluate the scalability and performance of image sensors implemented in a standard digital 0.18-μm CMOS process; 3) to demonstrate the speed potential of DPS, in particular, to reach or exceed continuous 10 000 frames/s operation and sustain 1 Gpixels/s throughput; and 4) to provide a platform for experimenting with algorithms and circuits that exploit high-speed imaging and embedded pixel-level digital memory.

Several high-speed CMOS APS chips have been reported. Krymski *et al.* [13] describe a 1024 × 1024 APS, followed by column-level 8-bit ADCs that achieves over 500 frames/s. Readout and digitization are performed one row at a time and each digitized row is read out over a 64-bit wide output bus. Fully pixel-parallel image acquisition ("snap-shot" acquisition) and short shutter durations are important requirements in high-speed imaging to prevent image distortion due to motion. These requirements, however, cannot be achieved using the standard APS architecture used in [13]. To address this limitation, Stevanovic *et al.* [14] describe a 256 × 256 APS with per-pixel storage capacitor to facilitate pixel-parallel image acquisition. Analog pixel values are multiplexed and read out through four analog outputs, achieving over 1000 frames/s.

The DPS architecture described in this paper fulfills the requirements of high-speed imaging with practically no limit on array size. It performs fully pixel-parallel image acquisition. Pixel reset is performed in parallel for all pixels and the reset duration is completely programmable, permitting higher shutter

Manuscript received April 17, 2001; revised August 2, 2001. This work was supported in part by Kodak, Canon, Hewlett-Packard, Agilent Technologies, and Interval Research Inc.

S. Kleinfelder was with the Information Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA. He is now with the Department of Electrical and Computer Engineering, University of California, Irvine, CA 92697 USA (e-mail: stuartk@uci.edu).

S. Lim, X. Liu, and A. El Gamal are with the Information Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA.

Publisher Item Identifier S 0018-9200(01)09332-5.

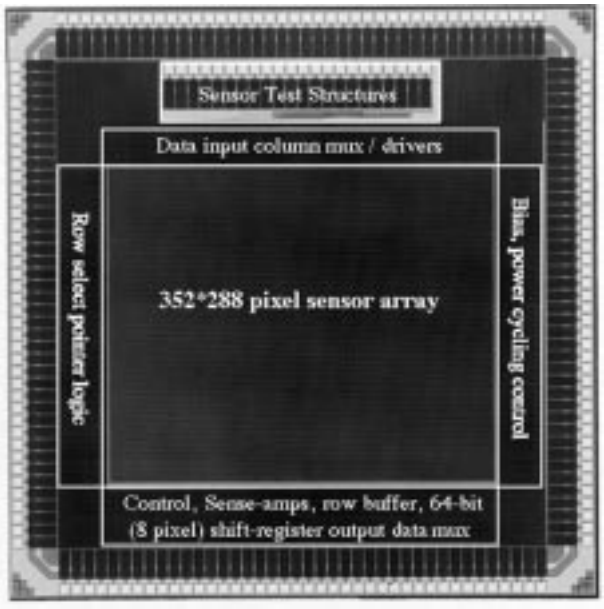


Fig. 2. DPS chip photomicrograph. The chip size is 5×5 mm.

speeds that are independent of frame rates. The massively parallel per-pixel A/D conversion scheme demonstrated here results in a high digitization rate (of up to 5 gigaconversions per second) that is independent of array size. This is a key advantage of DPS over APS employing column-level, chip-level, or off-chip ADCs where digitization rates do not scale linearly with the number of pixels in the array.

The rest of the paper is organized as follows. In Section II, we describe the DPS chip architecture and main characteristics. In Section III, we describe the details of the pixel design. In Section IV, we discuss the chip operation including the different imaging modes. In Section V, we describe the test setup and chip characterization results including ADC performance, quantum efficiency (QE), dark current, noise, and digital noise coupling. Sample images are provided in Section VI. Finally, in Section VII, we discuss the performance limits of DPS, including pixel size scaling and achievable readout speeds.

II. DPS Chip Overview

A photomicrograph of the DPS chip is shown in Fig. 2 and the main chip characteristics are listed in Table I. The chip contains 3.8 million transistors on a 5×5 mm die. The sensor array is 352×288 pixels in size, conforming to the CIF format. Each pixel is 9.4 μm on a side and contains 37 transistors including a photogate, transfer gate, reset transistor, a storage capacitor, and an 8-bit single-slope ADC with an 8-bit 3T-DRAM. The chip also contains test structures that we used for detailed characterization of APS and DPS pixels [16]. The test structures can be seen in the upper center area of the chip.

Fig. 3 shows a block diagram of the DPS chip. At the center is the sensor array. The periphery above the sensor core contains an 8-bit gray code counter, an auxiliary code input, and multiplexers and tristate column data drivers that are used to write data into the memory within the pixel array. The column multiplexers can be used to substitute arbitrary patterns for the standard gray code during data conversion. This facilitates the use of nonlinear ADC transfer functions, for example, for compression of dynamic range and contrast stretching. To the left of the sensor array is the readout control periphery that includes a row select pointer for addressing the pixel-level memory during readout. To the right of the sensor array is the bias generation and power-down circuits, which are used to digitally control the per-pixel ADC and memory sense-amp biases. The analog ramp signal input to the array needed for the per-pixel ADCs is supplied by an off-chip DAC.

TABLE I
Chip Characteristics

Technology	0.18μm 5-metal CMOS
Die size	5×5 mm
Array size	352×288 pixels
Number of transistors	3.8 million
Readout architecture	64-bit (167 MHz)
Max output data rate	> 1.33 GB/s
Max continuous frame rate	$> 10,000$ frames/s
Max continuous pixel rate	> 1 Gpixels/s
Pixel size	$9.4 \times 9.4\mu$m
Photodetector type	nMOS Photogate
Number of transistors/pixel	37
Sensor fill factor	15%

Below the sensor core are the digital readout circuits which include column sense-amps for reading the pixel-level memory and an output multiplexing shift register. The pixel values are read out of the memory one row at a time using the row select pointer and column sense-amps. Each row is then buffered and pipelined so that as one row is being shifted out of the chip, the following row is read out of the memory. A 64-bit wide parallel-in, serial-out shift-register bank was used instead of a large multiplexer, since in a shift register data moves in small increments, reducing local capacitance and drive circuit performance requirements. With each clock cycle, eight 8-bit pixel values are read out in a continuous stream with no waits or gaps between rows. An entirely closed-loop clocking system is used to assure clock and data integrity. The 64-bit output bus is clocked at 167 MHz for a 1.33-GB/s readout rate.

In the lower left corner of the chip is the readout control block. Since the chip is to be clocked at upwards of 167 MHz, it was important to keep off-chip high-speed controls to a minimum. The control block generates all the signals needed for readout from a single frame reset followed by a single continuous clock burst. A 6-phase clock generator using feedback to ensure correct margins is used to drive the shift registers. During chip testing or experimental operation, the control block can be bypassed and a set of auxiliary input controls used. Almost all digital circuitry in the periphery of the chip was designed using static logic to permit arbitrarily low clock rates.

III. Pixel Design

The pixel circuit is shown in Fig. 4. It consists of a photogate circuit, a comparator, and an 8-bit memory. The photogate

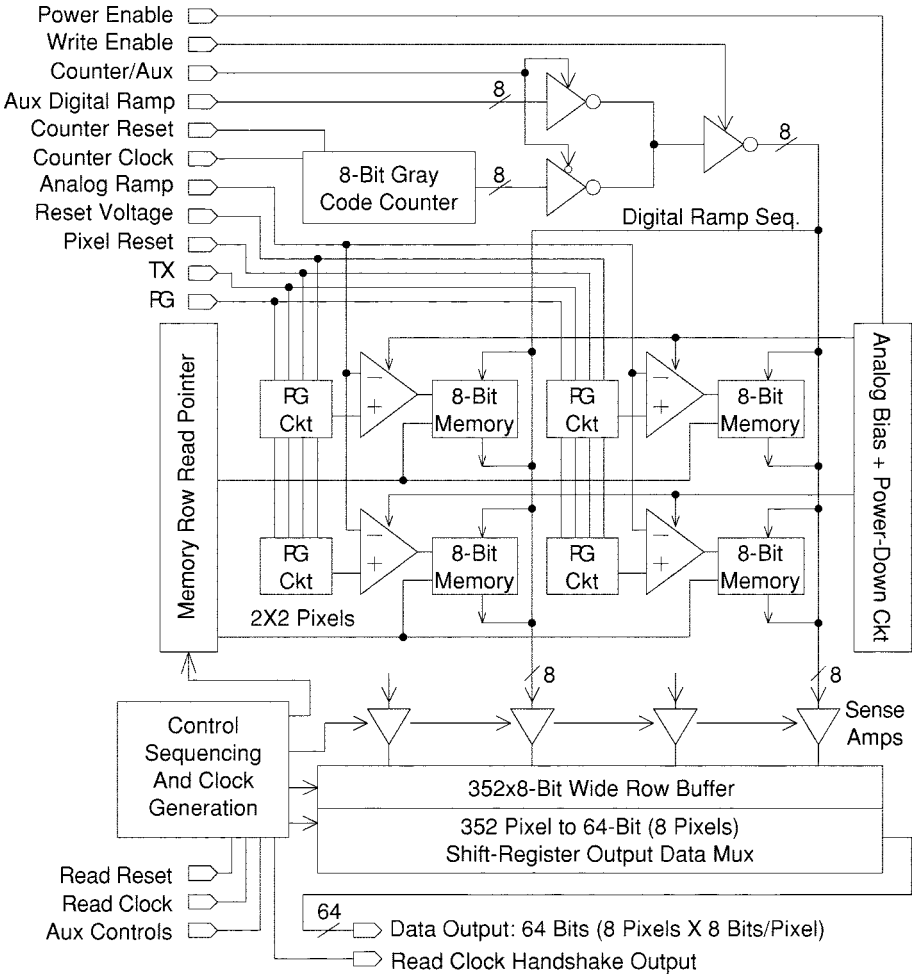


Fig. 3. DPS block diagram.

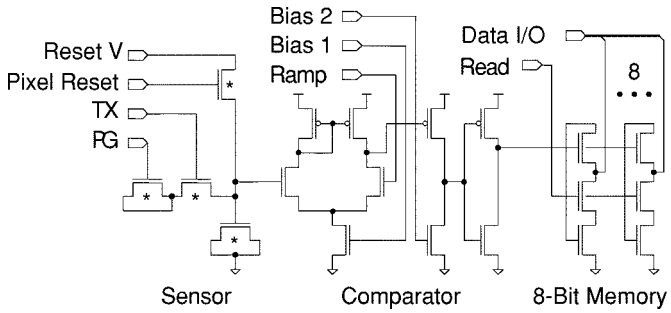


Fig. 4. Pixel schematic.

circuit consists of an nMOS photogate, a transfer gate, a reset transistor, and a sample capacitor. We decided to use a photogate to achieve high conversion gain and because preliminary process data indicated that native photodiodes have unacceptably high leakags. We implemented the photogate circuit using the standard thick oxide (3.3 V) transistors (denoted by * in the figure), normally used in I/O circuits, to avoid the high gate and subthreshold leakage currents of the thin oxide (1.8 V) transistors. Implementing the photogate and reset transistor using thick oxide transistors also makes it possible to use higher gate voltages than the nominal 1.8-V supply to increase voltage swing.

The comparator consists of a differential gain stage and a single-ended gain stage, followed by a CMOS inverter. It is designed to provide gain sufficient for ten bits of resolution with an input swing of 1 V and a worst-case settling time of 80 ns. This provides the flexibility to perform 8-bit A/D conversion over a 0.25-V range in under 25 μs, which is desirable for high-speed and/or low-light operation. In our earlier implementation [8], the pixel-level comparator was configured as a unity feedback amplifier during reset to perform autozeroing. Since in this implementation, we needed very high gain-bandwidth product at low power consumption and small area, we chose to run the comparator open loop and sacrifice an autozeroing capability. To cancel the high comparator offset voltages, we rely on digital correlated double sampling (CDS). Due to the low operating voltage and the desire for a large input swing, we could not use a cascode architecture. Instead, we used a three-stage architecture, with a CMOS inverter as the third stage to saturate the output voltage levels.

The pixel-level memory was implemented using 3T dynamic memory cells with a single read/write port to achieve small area and high-speed readout. The memory was designed for a maximum data hold time of 10 ms. This required the use of larger than minimum gate length access transistors and holding the bit lines at around $V_{\mathrm{dd}/2}$ to combat high transistor off-currents. Writing into the memory is locally controlled by the comparator. During readout, single-ended charge-redistribution column sense-amps, located in the periphery and not shown

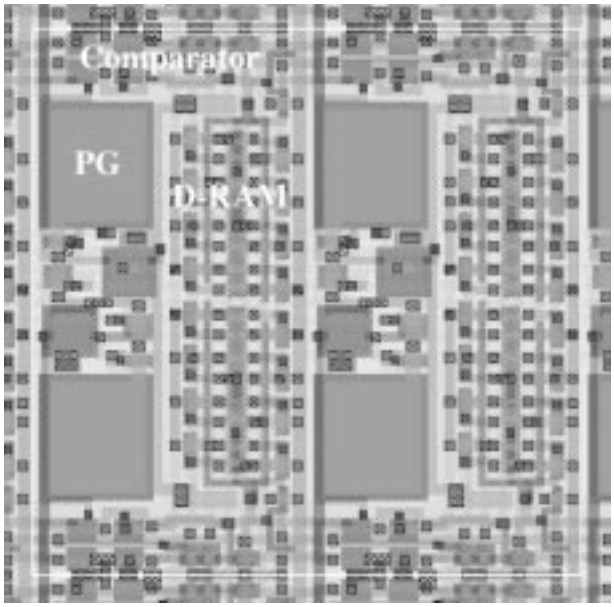


Fig. 5. DPS pixel layout (2 × 2 pixel block shown). Pixel size is 9.4 × 9.4 μm.

in the figure, are used for robustness against the effects of capacitive coupling between the closely spaced bit lines.

The comparator and pixel-level memory circuits can be electrically tested by applying analog signals to the sense node through the "Reset Voltage" signal, performing A/D conversion using the normal input ramp and the on-chip gray-code generator, and then reading out the digitized values. In this way, except for the photodetectors, the DPS chip can be electrically tested and characterized without the need for light or optics.

Fig. 5 shows the layout of a 2 × 2 pixel block. The four large squares are the photogates, which are sized and spaced equally in the horizontal and vertical dimensions. The fill factor of this pixel is 15%. The silicide layer, which is opaque, was blocked from the photogates. The three-stage comparators are seen near the top and bottom of the pixel quad. The digital memory is located in the two sections near the center of the quad. The smaller squares are the capacitors, with the transfer and reset transistors nearby.

The pixels are mirrored about the horizontal axis in order to share the n-well and some of the power and bias lines. With digital CDS as discussed in Section IV.C, we did not observe any offset FPN due to mirroring. A small layout asymmetry, however, has resulted in odd/even row gain FPN. Memory bitlines (metal 3) and digital ground (metal 1) run vertically over the memory, while analog signal (metal 2) and power distribution (metal 4) run horizontally on top of the comparators. Metal 5 covers most of the array and acts as a light shield. Pixel array analog and digital grounds are kept separate in order to reduce noise coupling from the digital memory into the sensitive analog components.

IV. Sensor Operation

In this section, we describe the details of the DPS chip operation. First, we describe the A/D conversion operation. Next, we discuss the basic imaging modes of operation including single frame capture, digital correlated double sampling, high-speed operation, and multiple image capture.

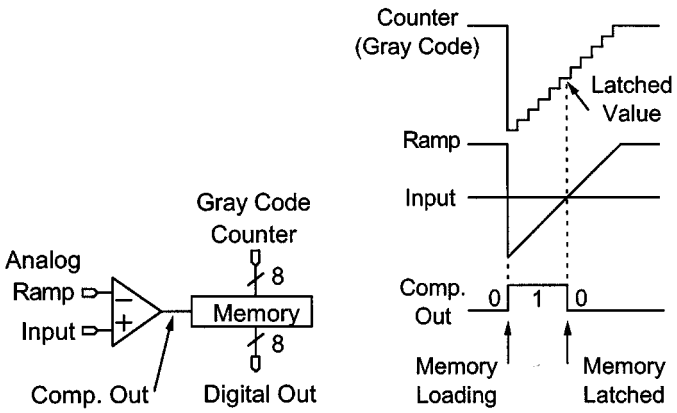


Fig. 6. Single-slope ADC operation.

A. A/D Conversion Operation

Fig. 6 illustrates the per-pixel single-slope A/D conversion technique used in our chip. The globally distributed voltage ramp is connected to each pixel's comparator inverting ("−") input. The noninverting ("+") input on each comparator is directly connected to the sense node. The globally distributed gray coded counter values, shown as a stepped "digital ramp," are simultaneously applied to the per-pixel memory bit lines.

At the beginning of conversion, the ramp voltage is lowered to just below the lowest expected sense node voltage, which sets the comparator output to high. This enables the per-pixel memory to begin loading the gray code values. The ramp is then swept linearly until it exceeds the reset voltage. Simultaneously, the gray code counter sweeps across an equivalent set of values (256 for eight bits). As the ramp crosses each pixel's sense node voltage, its comparator output switches low, and the gray code value present at that moment is latched in the pixel's memory. At the end of conversion, each pixel's memory contains an 8-bit gray coded value that is a digital representation of its input voltage.

Although using a linear ramp is the typical approach, it is possible to use alternative ramp profiles such as piecewise linear or exponential curves that compress or expand different illumination ranges. It is also possible to change the gain of the A/D conversion by changing the voltage range of the analog ramp. One may also use alternate sequences for the digital inputs using the auxiliary inputs.

B. Single Frame Capture

Fig. 7 depicts a simplified timing diagram for the DPS chip. Operation can be divided into four main phases: reset, integration, A/D conversion, and readout. The reset, integration and A/D conversion phases occur completely in parallel over the entire array, i.e., in "snap-shot" mode, thus avoiding image distortion due to the row by row reset and readout of APS. To minimize charge injection into the sense node, which causes high FPN, a shallow reset signal falling edge is used. Sensor integration is limited by dark current or signal saturation on the long end and by internal time constants on the short end. Practical lower and upper bounds on integration time were found to be under 10 μs to well over 100 ms.

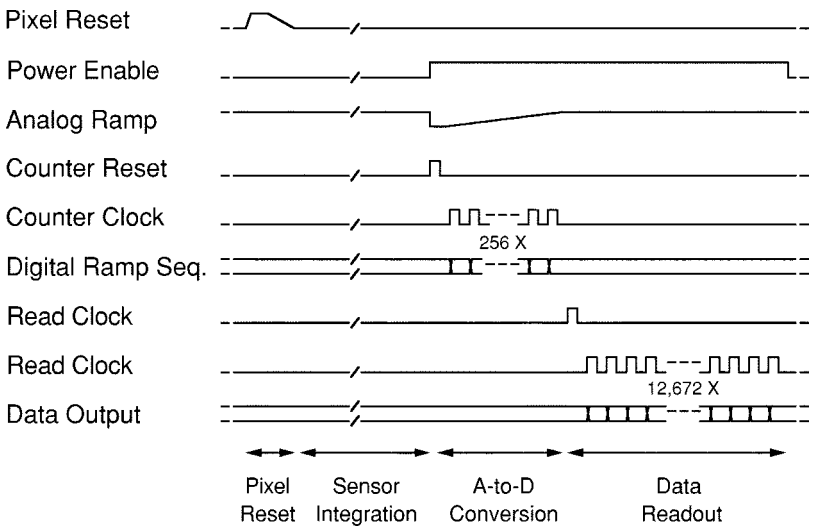


Fig. 7. Simplified DPS timing diagram.

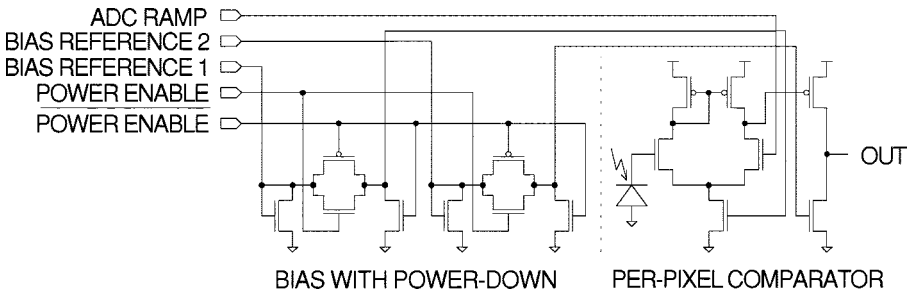


Fig. 8. Comparator bias generation with powerdown.

After integration, per-pixel single-slope A/D conversion is simultaneously performed for all pixels, as discussed in the previous subsection. Typical conversion time is 25 μs, and can be as low as 20 μs at the highest frame rates. After conversion, readout commences. The readout of one frame is completed in around 75 μs.

Fig. 8 shows the bias generation circuits for the pixel-level comparators, including the power-down circuitry. It consists of two sections, each with a current mirror, a transmission gate and a pull-down transistor. The comparators and the sense amps are turned on only during A/D conversion and readout phases by raising the Power Enable control. Power cycling is not essential, but since full frame conversion and readout can be accomplished in as little as 100 μs, it can save several orders of magnitude of power when the chip is running at low frame rates and hence low A/D conversion/readout duty cycles.

The current mirrors divide down the external references (Bias1, Bias2) by a factor of 100 in order to reduce the impedance of the external references for higher noise immunity. The transmission gates, operated by Power Enable and its complement, control whether the current mirror outputs are connected to the pixel array. When they are not connected, a pull-down transistor in each bias section connects the bias lines to ground, which shuts off the current source transistors in the two biased comparator stages. The circuits were designed, based on the loading of the 352×288 pixel array, to power down or up within 100 ns.

C. Imaging Modes

The DPS chip operation is quite flexible. The timing and order of different phases can be easily programmed for different imaging applications. Fig. 9 illustrates some of the possible imaging modes of the chip. Mode (A) is the single frame capture scenario we detailed in the previous subsection. At low speeds, each phase can be kept completely separate so that, for example, noise coupling due to digital readout need not influence the sensor reset, integration or conversion. Mode (B) is used to implement digital correlated double sampling by converting and reading a "reset frame" right after reset. The digitized reset frame is subtracted from the the digitized image frame externally. This is a "true" CDS operation, albeit digital in nature, in the sense that the two frames are taken after the same reset. Since a full frame conversion and readout can be completed in 100 μs or less, more frames can be converted and read out during a single exposure time. This is denoted by mode (C) in Fig. 9. For example, in a typical 30 ms exposure time, tens or even hundreds of frames can be converted and read out. This "oversampling" can be used to implement several image enhancement and analysis applications such as dynamic range enhancement, motion estimation and compensation, and image stabilization. At the highest speeds, one can overlap and pipeline phases to maximize integration time and thus reduce the amount of illumination needed, as illustrated in mode (D). For example, at 10 000 frames/s, the combined reset, A/D conversion and readout time closely approaches the full frame pe-

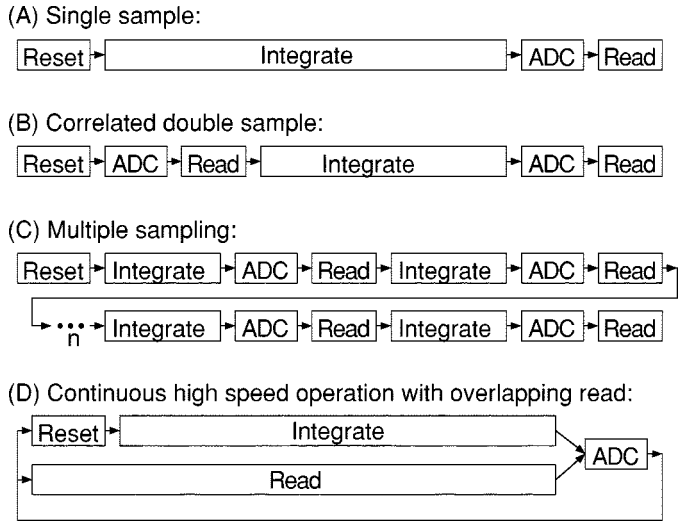


Fig. 9. Basic DPS operation schemes.

riod. By overlapping integration with readout of the previous frame, integration time can be increased from close to zero to about 75 μs out of the 100 μs frame period.

V. Testing and Characterization

The DPS chip has been tested and characterized and shown to be fully functional. In the following subsections, we briefly describe the test setup for the chip, present the electrical, optical, and noise characterization results, and show results demonstrating that digital readout noise has little or no effect on the imaging performance of the chip.

A. Test Setup

Achieving our goals of 10 000 frames/s and 1 Gpixels/s operation required an output data rate of over 1.33 GB/s as well as nanosecond-level real-time control over the chip. Since this data rate exceeds that of common contemporary computer systems, we assembled a rackmounted system centered around a high-speed digital pattern generator and logic analyzer that controlled the chip and other test hardware and downloaded the chip's output data to a PC. Additional hardware included a high-speed programmable pulse generator and several programmable analog waveform generators. The pulse generator was used to drive the DPS chip's readout clock and the waveform generators were used for the analog ramp, PG, TX, and Pixel Reset. As mentioned earlier, the DPS chip includes sequencing circuits to reduce the off-chip control demands. This on-chip capability, combined with the test equipment hardware, made it possible to only use the simple passive test board depicted in Fig. 10 to interface to the DPS chip.

The high-speed image capture required special attention to the optical test setup. An optical device mounting rail was used to hold the test board as well as various optical components such as an integrating sphere, test image projection hardware, lenses, and objects used as imaging targets. Illumination was generally provided by two standard tungsten light sources of up to 1000 W, with Fresnel lenses. This level of illumination is typical

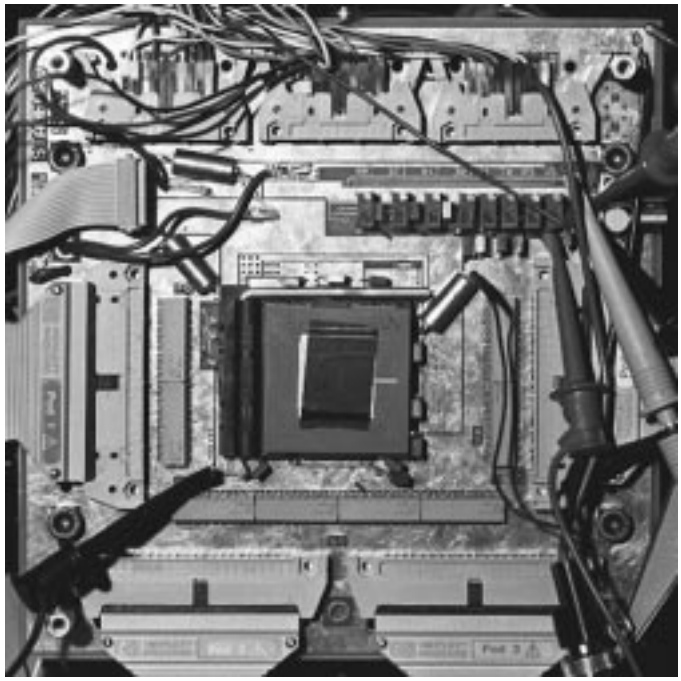


Fig. 10. DPS chip test support board.

in high-speed imaging applications [15]. To maximize the collected light, a variable focal length ("zoom") lens of $f/1.2$ maximum aperture was used. Targets were typically imaged from a distance of 18 inches. Since close focus and large lens apertures result in shallow depth of field and critical demands on image plane alignment, micrometer adjustments on lens placement and focusing were provided.

B. Electrical and Optical Characterization Results

Table II summarizes the DPS characterization results. Of particular interest is the measured average power consumption of only 50 mW at 10 000 frames/s. The pixel-level comparators consume around 30 mW of static power, while the digital readout circuits consume around 20 mW of dynamic power. The poor imaging performance of the standard 0.18-μm CMOS process resulted in high dark signal of 130 mV/s and low QE of 13.6%. With conversion gain of 13.1 μV/e$^-$, sensitivity was just over 0.1 V/lux/s. Dark current and QE can be significantly improved with minor process modifications that should not significantly affect pixel area or chip performance. The ADC integral nonlinearity (INL) was measured over the maximum useful input range of 1 V, at a typical 1000 frames/s, without correlated double sampling, and averaged for all pixels. It was found to be 0.22% or 0.56 LSB. We also found that reducing the swing to 0.9 V improves INL to 0.1% or 0.25 LSB.

To determine dark current, conversion gain, and QE of the DPS pixel, our chip included single pixel APS and DPS test structures that can be individually accessed and whose sense node voltages can be directly readout. The test structures are described in detail in [16]. For completeness, we provide the results that are relevant to the DPS chip.

The measured quantum efficiency curve for the photogate is shown in Fig. 11. The maximum QE is around 13.6% at

TABLE II
DPS CHIP CHARACTERIZATION SUMMARY. ALL NUMBERS EXCEPT FOR POWER CONSUMPTION ARE AT 1000 FRAMES/S

Power used at 10K fps	50 mW, typical
ADC architecture	Per-pixel single-slope
ADC resolution	8-bits
ADC conversion time, typical	$\sim 25\mu$s, ($\sim 20\mu$s, min.)
ADC range, typical	1 V
ADC integral nonlinearity	<0.22% (0.56 LSB)
Dark current	130 mV/s, 10 nA/cm^2
Quantum efficiency	13.6%
Conversion gain	13.1 μV/e$^-$
Sensitivity	0.107 V/lux.s
FPN, dark w/CDS	0.027% (0.069 LSB)
Temporal noise, dark w/CDS	0.15% (0.38 LSB)

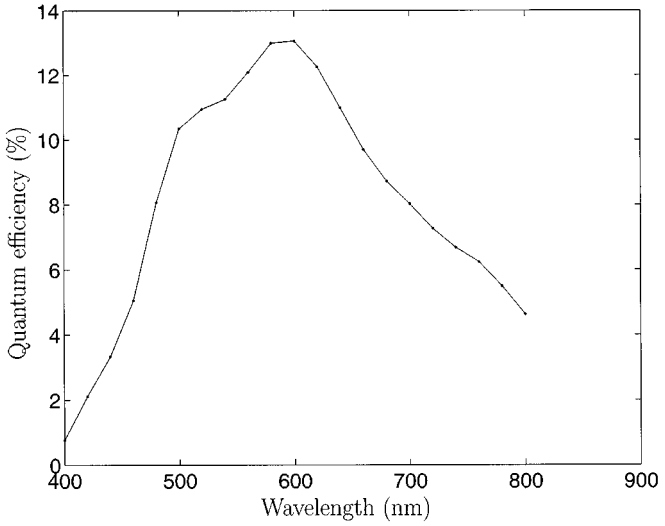


Fig. 11. Measured quantum efficiency.

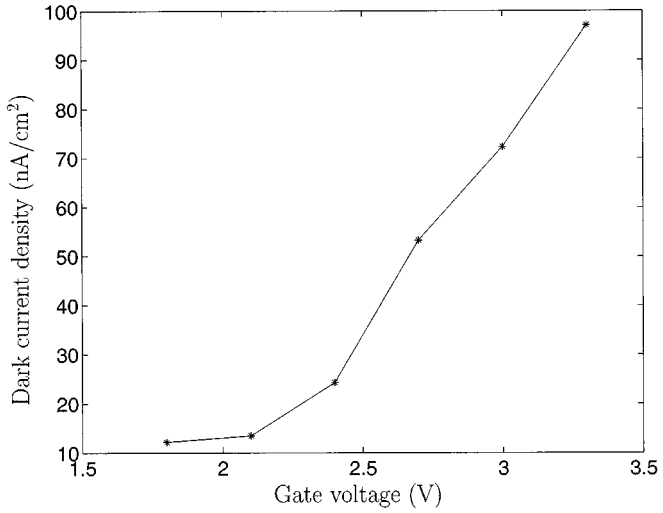


Fig. 12. Measured photogate leakage current as a function of gate voltage.

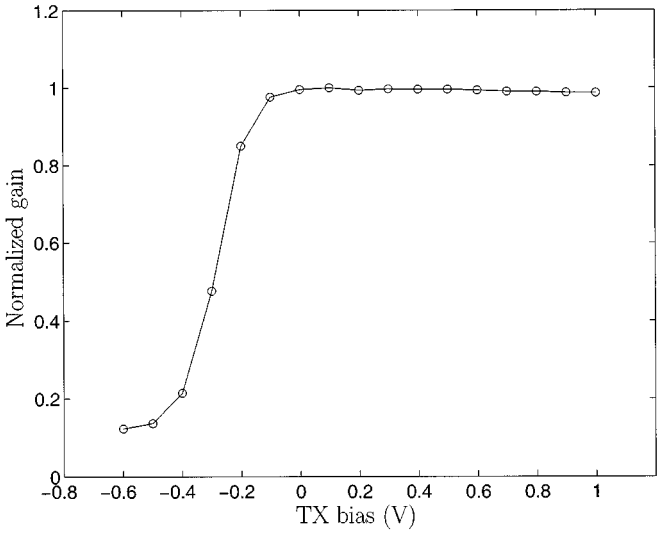


Fig. 13. Normalized gain versus TX bias voltage.

wavelegth of 600 nm. The major reason for the low QE is the high recombination rate in the highly doped substrate.

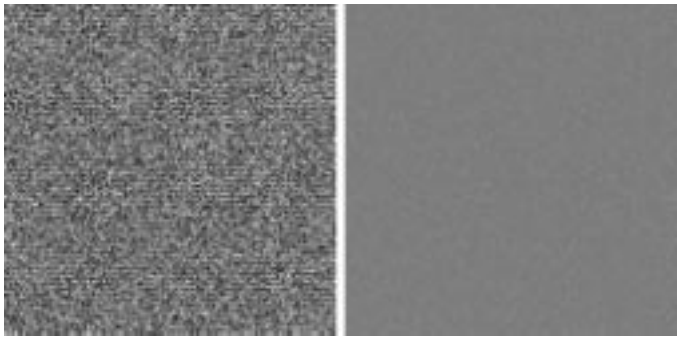
The measured dark current density was found to increase superlinearly with reverse bias voltage as shown in Fig. 12. Since lowering PG voltage was also found to have little effect on QE [16], we typically operated PG at 2.1 V or less.

We found that the transfer transistor of the photogate circuit suffered from high off-current in spite of using a thick oxide transistor. We performed an experiment to find out the transfer gate voltage needed to turn it off. Fig. 13 plots the normalized quantum efficiency of the photogate device for TX voltage from 1 V down to −0.6 V. During the experiment, the reset voltage is kept at 1.15 V and PG is pulsed between 0 and 2.1 V. It is clear that the transfer gate cannot be turned off unless the gate voltage (TX) is negative.

Since the transfer gate cannot be turned off using nonnegative TX voltages, we often operated the photogate as a photodiode by setting both PG and TX voltages to optimum fixed voltages. We found that QE in this mode is only slightly lower than when operating in the normal photogate mode. In this photodiode mode, however, ADC linearity is slightly compromised at high frame rates, since integration continues during A/D conversion.

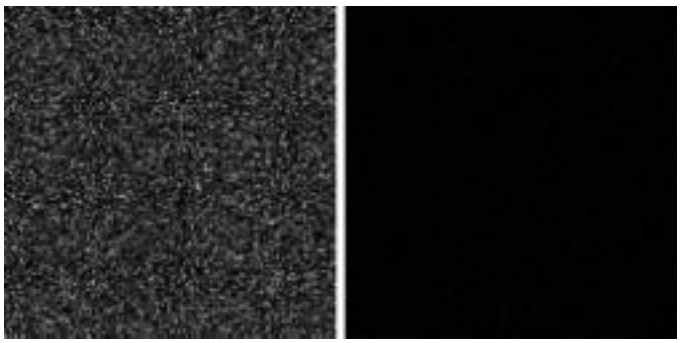
C. Temporal Noise and FPN

Correlated double sampling is perhaps the simplest example of how multiple image acquisitions within one integration can improve image quality. With digital CDS, FPN due to comparator offset and reset transistor threshold voltage and reset temporal noise are greatly reduced. In Fig. 14, two images rendered using the same scale, show fixed pattern noise with and without correlated double sampling (performed digitally off-chip). On the left one can see significant noise that is primarily due to random variations in the pixel-level ADC comparator offset voltages. This random pattern of noise tends to be less visually objectionable than column fixed pattern noise, common in typical analog APS designs, that results in streaks. On the right is the result after external digital CDS. The FPN has been reduced from 0.79% to 0.027%, rms, a reduction by nearly a factor of 30. The final FPN number is about 1/15th of an LSB.



(a) (b)

Fig. 14. Images of fixed pattern noise (a) without digital CDS and (b) with digital CDS for an integration time of 1 ms.



(a) (b)

Fig. 15. Images of temporal noise (a) without digital CDS and (b) with digital CDS.

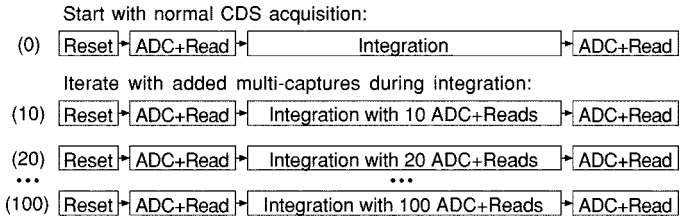


Fig. 16. Digital read-induced noise experiment.

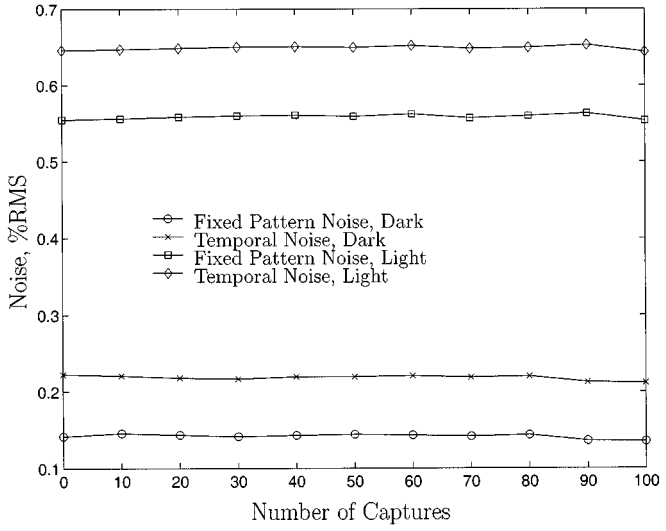


Fig. 17. Plot of digital noise coupling results.

Fig. 15 shows two images of temporal noise, with and without CDS, using a 1-ms integration time, in the dark. In this case, the images show the variability in pixel values over time, with FPN removed. Using digital CDS, temporal noise has been reduced from 1.6% to 0.15% rms, which is less than $1/3$ of an LSB.

D. Digital Noise Coupling

Since DPS operation involves per-pixel digitization, digital pixel readout and high-speed I/O switching during integration, it is important to investigate the impact of digital coupling on the sensor performance. This is an especially important question given the ability of the DPS architecture to take hundreds of image samples within a single integration. To examine this issue, we devised the experiment explained with the aid of Fig. 16. The experiment was conducted under worst-case noise conditions, where the total integration time was minimized and the time spent converting and reading out was maximized to the point of being continuous.

The experiment consisted of 11 sets of measurements. In the first set we performed a reset followed by an A/D conversion and a readout, integrated for 24 ms, and then performed a final A/D conversion and a readout. Digital CDS was performed on the two captures to increase the sensitivity of the measurements. This is our baseline measurement that should include the least amount of digital coupling noise. The remaining 10 measurements were performed with $10, 20, \ldots, 100$ additional captures (i.e., A/D conversions and frame readouts) within the 24-ms integration time, respectively. Digital CDS was performed in each case, using the first and last samples immediately before and after the 24 ms integration. Readout speed was set at 1.33 GB/s and the total A/D conversion and readout time was 240 μs per capture. With 100 captures within the 24 ms integration, the chip was continuously converting and reading out during the integration period, with no gaps. The entire experiment was repeated twice: once in the dark and once using light from a stabilized light source and an integrating sphere to provide stable, uniform illumination.

The results are plotted in Fig. 17. It is evident from the data that the noise curves are essentially flat: any trend is insignificant compared to the baseline (with no multicapture) noise levels.

VI. Sample Images

Fig. 18 shows an image acquired from a 1000 frames/s (integration time just under 1 ms) video stream. Except for digital CDS, no other processing was performed on the image. While the image is of a stationary subject, the chip was operated in continuous video mode. It highlights the image quality that can be obtained at these speeds, even with a small array size and fill factor. Note the subtle aliasing patterns in the finely engraved hair and downsampling of the background engraving due to the low spatial resolution of the sensor.

Fig. 19 shows four frames (1, 11, 12, and 31) from a continuous 10 000 frames/s video sequence. They show a model airplane propeller rotating in front of a stationary resolution chart. The propeller is rotating at about 2200 rpm, which results in the visible blade rotating by about 40°. The scene is lit from two sides, forming two shadows that follow the propeller. At this

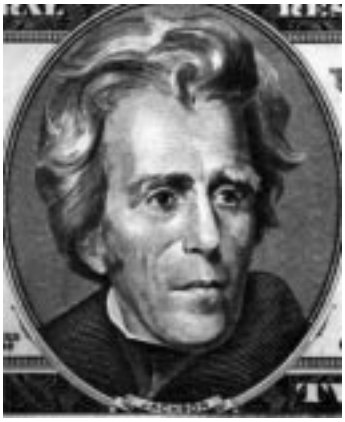


Fig. 18. Sample image using 1-ms integration.

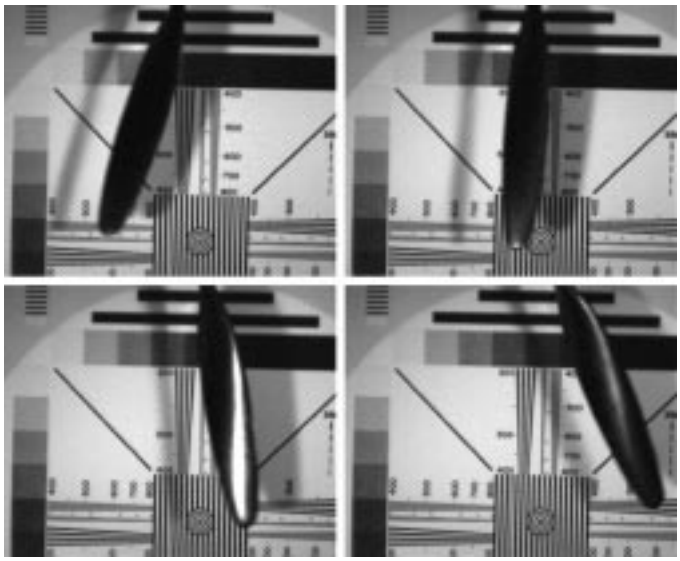


Fig. 19. 10 000 frames/s image sequence (frames 1, 10, 20, and 30 are shown).

speed, neither CDS nor power cycling is used, and each frame's reset and integration is overlapped with the readout of the previous frame's data [mode (D) in Fig. 9], as explained earlier. The overall image quality appears to be satisfactory for high-speed motion analysis and other high-speed video applications.

VII. Performance Limits

In this section, we discuss the scaling and performance limits of the DPS architecture.

A. Pixel Size

The DPS chip we described has a 9.4×9.4 μm pixel with 15% fill factor. The low fill factor is in part due to the use of a photogate. The fill factor using a photodiode would be around 25%. In Fig. 20 we plot estimates of pixel size versus fill factor assuming the use of a photodiode for CMOS technologies down to 0.1 μm.

Our implementation employed a 3T type DRAM because of its simple design and compatibility with standard digital CMOS process. The memory occupies around 28% of the pixel area. If a 1T DRAM were used instead, the area occupied by the memory would be significantly decreased. However, since our pixel layout is metal limited, using 1T DRAM is not expected to reduce the overall pixel size. In more advanced processes, using 1T DRAM may yield smaller pixel designs. But since memory occupies a fraction of the pixel, such improvements will at best be marginal.

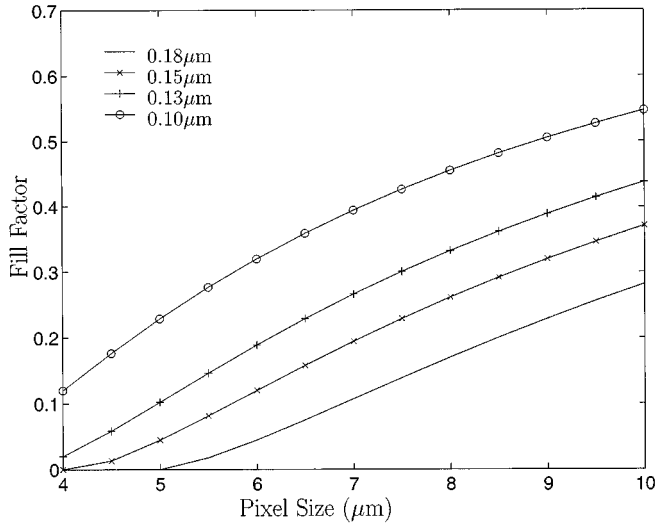


Fig. 20. Fill factor versus pixel size for different technology generations.

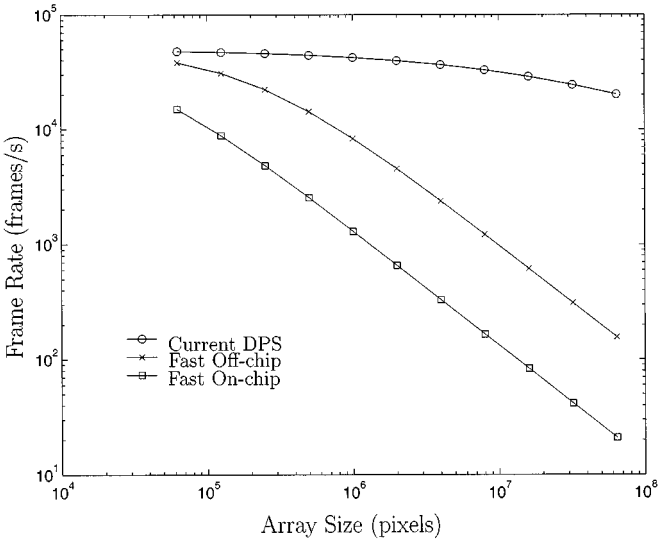


Fig. 21. Projected frame rates versus image sensor array size for the current DPS implementation, using faster output throughput, and using faster memory. Output frame rates are reported for the first two cases while on-chip frame rate is reported for the third.

B. Frame Rate

The architecture of the DPS chip we described can be easily scaled to larger array sizes and/or higher speeds than those demonstrated by our implementation. Throughput can be increased by employing high-speed memory (e.g., [17]) and high-speed I/O techniques (e.g., [18]) without the need to speed up the per-pixel ADCs, since their throughput scales linearly with array size. Fig. 21 plots three curves comparing projected frame rates versus array size: the first assumes our

current implementation, the second assumes an I/O throughput that is five times faster than the current implementation, and the third is the internal frame rate, i.e., the highset frame rate from the sensor to an on-chip memory or processors assuming a state-of-the-art high-speed pixel-level memory.

VIII. Conclusion

A digital pixel sensor implemented in a standard digital CMOS 0.18-μm process was described. The 3.8 million transistor chip has 352×288 pixels. Each 9.4×9.4 μm pixel contains 37 transistors implementing a photogate circuit, an 8-bit single-slope ADC, and eight 3T DRAM cells. Pixel reset, integration, and A/D conversion occur in full frame parallel "snap-shot" fashion. Data is read out via a 64-bit-wide bus at 167 MHz for a peak data bandwidth of 1.34 GB/s. The DPS chip achieved continuous 10 000 frames/s operation and sustained 1 Gpixels/s throughput, while using only 50 mW of power. With further scaling, significant additional per-pixel memory, processing power, and speed will inevitably become practical, further enhancing the capabilities of the DPS approach.

Acknowledgment

The authors would like to acknowledge the many contributions of T. Chen, K. Salama, H. Tian, and Prof. B. Wandell.

References

[1] I. L. Fujimori and C. G. Sodini, "A 256×256 CMOS differential passive pixel imager with FPN reduction techniques," *IEEE J. Solid-State Circuits*, vol. 35, pp. 2031–2037, Dec. 2000.

[2] M. J. Loinaz, K. J. Singh, A. J. Blanksby, D. A. Inglis, K. Azadet, and B. D. Ackland, "A 200-mW 3.3-V CMOS color camera IC producing 352×288 24-b video at 30 frames/s," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2092–2103, Dec. 1998.

[3] E. R. Fossum, "CMOS image sensors: Electronic camera-on-chip," *IEEE Trans. Electron Devices*, vol. 44, pp. 1689–1698, Oct. 1997.

[4] R. H. Nixon, S. E. Kemeny, B. Pain, C. O. Staller, and E. R. Fossum, "256×256 CMOS active pixel sensor camera-on-chip," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2046–2050, Dec. 1996.

[5] A. El Gamal, D. Yang, and B. Fowler, "Pixel level processing—Why, what and how?," *Proc. SPIE*, vol. 3650, pp. 2–13, Jan. 1999.

[6] B. M. Coaker, N. S. Xu, R. V. Latham, and F. J. Jones, "High-speed imaging of the pulsed-field flashover of an alumina ceramic in vacuum," *IEEE Trans. Dielect. Electric. Insul.*, vol. 2, pp. 210–217, Apr. 1995.

[7] B. T. Turko and M. Fardo, "High-speed imaging with a tapped solid state sensor," *IEEE Trans. Nucl. Sci.*, vol. 37, pp. 320–325, Apr. 1990.

[8] D. Yang, A. El Gamal, B. Fowler, and H. Tian, "A 640×512 CMOS image sensor with ultra wide dynamic range floating point pixel-level ADC," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1821–1834, Dec. 1999.

[9] X. Q. Liu and A. El Gamal, "Photocurrent estimation from multiple non-destructive samples in a CMOS image sensor," *Proc. SPIE*, vol. 4306, Jan. 2001.

[10] S. H. Lim and A. El Gamal, "Integrating image capture and processing—Beyond single chip digital camera," *Proc. SPIE*, vol. 4306, Jan. 2001.

[11] D. Yang, B. Fowler, and A. El Gamal, "A Nyquist rate pixel level ADC for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol. 34, pp. 348–356, Mar. 1999.

[12] H.-S. Wong, "Technology and device scaling considerations for CMOS imagers," *IEEE Trans. Electron Devices*, vol. 43, pp. 2131–2141, Dec. 1996.

[13] A. Krymski, D. Van Blerkom, A. Andersson, N. Block, B. Mansoorian, and E. R. Fossum, "A high-speed, 500 Frames/s, 1024×1024 CMOS active pixel sensor," in *Proc. Symp. VLSI Circuits*, June 1999, pp. 137–138.

[14] N. Stevanovic, M. Hillegrand, B. J. Hostica, and A. Teuner, "A CMOS image sensor for high-speed imaging," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2000, pp. 104–105.

[15] R. G. Root and P. Falkos, "Repetitively pulsed plasma illumination source improvements," *Proc. SPIE*, vol. 3642, pp. 104–115, Feb. 1999.

[16] H. Tian, X. Q. Liu, S. H. Lim, S. Kleinfelder, and A. El Gamal, "Active pixel sensors fabricated in a standard 0.18-μ CMOS technology," *Proc. SPIE*, vol. 4306, Jan. 2001.

[17] O. Takahashi *et al.*, "A 1 GHz fully pipelined 3.7 ns address time 8 k $\times$ 1024 embedded DRAM macro," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2000, pp. 396–397.

[18] M. Fukaishi *et al.*, "A 20 Gb/s CMOS multi-channel transmitter and receiver chip set for ultra-high resolution digital display," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2000, pp. 260–261.

Stuart Kleinfelder received the B.S. degree in computer science from the State University of New York (SUNY), Stony Brook, in 1984, the M.S. degree in electrical engineering from the University of California, Berkeley, in 1992, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 2001.

He was with the Physics Department of SUNY from 1984 to 1986. He was with Lawrence Berkeley National Laboratory from 1986 through 2001, applying research in mixed-mode integrated circuits and sensors for high-energy physics, astrophysics, nuclear science, and medical applications. His recent research interests have included high-speed imaging arrays for IR, visual light, X-rays and charged particles. He is currently an Assistant Professor of Electrical and Computer Engineering at the University of California, Irvine.

SukHwan Lim received the B.S. degree with honors in electrical engineering from Seoul National University, Seoul, Korea, in 1996 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1998. He is currently working toward the Ph.D. degree in electrical engineering at Stanford University.

His research interests include CMOS image sensors, programmable digital camera architecture design, and video processing applications using high-speed imaging and smart vision sensors. He is also interested in image sequence processing algorithms such as optical flow estimation, image restoration, and superresolution.

Xinqiao (Chiao) Liu received the B.S. degree in physics from the University of Science and Technology of China, Anhui, China, in 1993 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1997. He is currently working toward the Ph.D. degree in electrical engineering at Stanford University.

During the summer of 1998, he worked as a Research Intern at Interval Research Inc., Palo Alto, CA, on CMOS image sensor characterization and novel imaging system design. From 1994 to 1995, he worked as an Engineer at Glenayre Electronics, Inc., Beijing Representative Office, China, on wireless paging network projects. From 1993 to 1994, he was with Kehai Corporation, Beijing, working on the digital communication and networking project. At Stanford, his research is focused on CMOS imager dynamic range and sensitivity enhancement through innovative circuit design and statistical signal processing algorithms. He is also interested in electronic sensing and imaging, statistical signal processing applications in bioscience area.

Abbas El Gamal (M'73–SM'83–F'00) received the B.S. degree in electrical engineering from Cairo University, Cairo, Egypt, in 1972, and the M.S. degree in statistics and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1977 and 1978, respectively.

From 1978 to 1980, he was an Assistant Professor of Electrical Engineering at the University of Southern California, Los Angeles. He joined the Stanford faculty in 1981, where he is currently a Professor of Electrical Engineering. From 1984 to 1988, while on leave from Stanford, he was Director of LSI Logic Research Lab, and subsequently was cofounder and Chief Scientist of Actel Corporation. From 1990 to 1995, he was a cofounder and Chief Technical Officer of Silicon Architects, currently part of Synopsys. He is currently the Principal Investigator on the Stanford Programmable Digital Camera project. His research interests include CMOS image sensors and digital camera design, image processing, network information theory, and electrically configurable VLSI design and CAD. He has authored or coauthored over 100 papers and 20 patents in these areas. He serves on the board of directors and advisory boards of several IC and CAD companies.

Dr. El Gamal is a member of the IEEE ISSCC Technical Program Committee.