A Resolution-Reconfigurable 5-to-10-Bit 0.4-to-1 V Power Scalable SAR ADC for Sensor Applications

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***Abstract*—A power-scalable SAR ADC for sensor applications is presented. The ADC features a reconfigurable 5-to-10-bit DAC whose power scales exponentially with resolution. At low resolutions where noise and linearity requirements are reduced, supply voltage scaling is leveraged to further reduce the energy-per-conversion. The ADC operates up to 2 MS/s at 1 V and 5 kS/s at 0.4 V, and its power scales linearly with sample rate down to leakage levels of 53 nW at 1 V and 4 nW at 0.4 V. Leakage power-gating during a *SLEEP* mode in between conversions reduces total power by up to 14% at sample rates below 1 kS/s. Prototyped in a low-power 65 nm CMOS process, the ADC in 10-bit mode achieves an INL and DNL of 0.57 LSB and 0.58 LSB respectively at 0.6 V, and the Nyquist SNDR and SFDR are 55 dB and 69 dB respectively at 0.55 V and 20 kS/s. The ADC achieves an optimal FOM of 22.4 fJ/conversion-step at 0.55 V in 10-bit mode. The combined techniques of DAC resolution and voltage scaling maximize efficiency at low resolutions, resulting in an FOM that increases by only 7x over the 5-bit scaling range, improving upon a 32x degradation that would otherwise arise from truncation of bits from an ADC of fixed resolution and voltage.**

***Index Terms*—ADC, analog-to-digital converter, leakage reduction, power-gating, power scaling, reconfigurable, resolution, scalable, successive approximation, voltage scaling.**

I. Introduction

ADVANCES in the semiconductor industry have spurred the development of wireless sensor networks, which consist of a collection of distributed micro-power sensor nodes capable of sensing, processing, and relaying data to a central basestation [1]. These networks have potential applications such as structural health monitoring, industrial process monitoring, and personal health monitoring. Using the latter as an example, wearable biopotential sensor nodes [2] can be used to monitor vital signs such as the electrocardiogram (ECG), electroencephalogram (EEG), respiratory rate, and blood oxygenation, all of which have varying bandwidth and dynamic range requirements. Furthermore, within a given application such as ECG monitoring, variable resolution can also be desirable in order to accomplish tasks such as heart rate detection (low resolution) or ST pattern changes (high resolution) [3]. In this context, hardware that is energy-efficient and reconfigurable can significantly reduce the size and cost of such a system.

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The analog-to-digital converter (ADC) is an indispensable part of every sensor node, responsible for interfacing the physical world to the digital signal processing unit. In particular, for energy-constrained systems powered off small batteries or energy harvesting, adapting the ADC performance to the signal of interest to avoid consuming power on unnecessary bandwidth or accuracy can extend the device lifetime. Therefore, this paper presents a single reconfigurable ADC whose power scales with resolution and sample rate to maximize energy-efficiency for a broad range of applications [4].

The target resolution of the ADC is chosen to cover 5 to 10 bits of resolution in 1-bit increments which encompasses low resolution applications like neural spike sorting (up to 8 bits) [5], as well as moderate resolution applications like ambulatory ECG monitoring (8 to 10 bits) [6]. The target sampling rate is scalable from a maximum of 1 MS/s down to 10's of samples per second to accomodate high bandwidth modes and multi-channel applications where many channels are multiplexed into a single ADC, or low-power modes where the sensor node is highly duty cycled. For this performance range, the successive approximation register (SAR) ADC is a good candidate [7].

Recent SAR ADCs have achieved exceptional energy-efficiency but most lack the ability to reconfigure its resolution [8], [9]. In [5], a 3-to-8-bit SAR ADC is presented, but it is not optimized for scalability over sampling rate. The ADC presented in this paper has 6 resolution modes from 5-bits to 10-bits, and scalable sample rate up to 2 MS/s at 1 V and 5 kS/s at 0.4 V. Several techniques are used to enable power scaling across the entire performance range. First, a resolution-reconfigurable digital-to-analog converter (DAC) improves power scaling with resolution. Second, a fully dynamic architecture with bootstrapped sampling and no static currents enables ultra-low-voltage operation which provides CV^2 power savings [10]. Lastly, the use of a low-leakage 65 nm CMOS process together with leakage power-gating extends efficiency to low sample rates.

Section II presents the ADC architecture and describes techniques used to achieve resolution reconfigurability. Section III proposes voltage scaling as an effective way to reduce the ADC energy-per-conversion, and discusses its implications on dynamic range and linearity. Section IV describes the use of leakage power-gating as a leakage reduction technique during the ADC conversion cycle. Section V presents prototype measurement results, and Section VI concludes the paper.

II. Architecture Description

This section describes the details of the ADC architecture, examines the design and energy consumption of the DAC circuits,

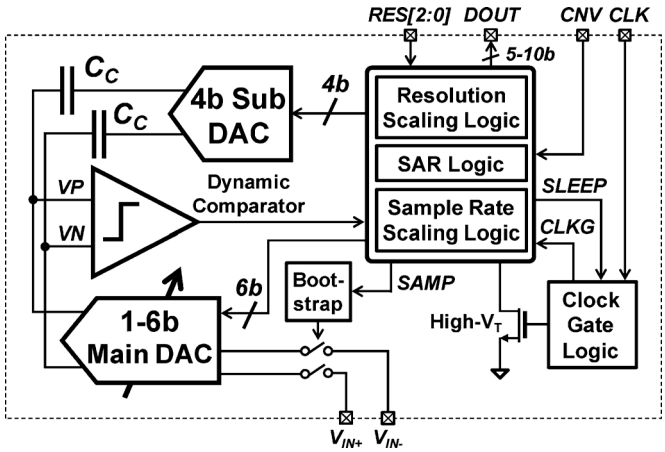

Fig. 1. Block diagram of the proposed reconfigurable SAR ADC.

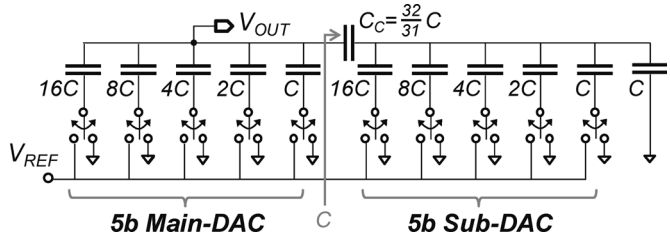

Fig. 2. Conventional array segmented into a 5-bit main-DAC and a 5-bit sub-DAC.

and presents trade-offs and techniques used to achieve resolution reconfigurability in the ADC.

A. ADC Architecture

A block diagram of the proposed SAR ADC is shown in Fig. 1. It comprises a resolution-reconfigurable DAC segmented into a 1-to-6-bit main-DAC and 4-bit sub-DAC [11] using the split-capacitor array switching scheme [12], a dynamic comparator, and the SAR digital control logic. A differential architecture is chosen to improve power supply and common-mode rejection for higher resolution modes. At lower resolutions where linearity and noise requirements are reduced, voltage scaling is used to improve energy-efficiency. In order to ensure adequate sampling linearity at low voltages, a switch bootstrap circuit is used [10].

Each conversion begins with the assertion of the CNV input pulse and consists of 4 phases as in [13]: DAC reset, input sampling, bit cycling, and *SLEEP*. First, the DAC is reset to remove all residual charge so that the top plates (VP, VN) of the DAC settle passively to the input common-mode while the inputs are sampled onto the DAC bottom plates, eliminating the need for a common-mode reference. Then, the SAR control logic starts bit cycling at the appropriate bit capacitor to achieve resolution scaling. The resolution mode is digitally controlled with 3 bits $(RES[2:0])$, and internal thermometer and one-hot decoders. After the bits are resolved, the ADC is put into *SLEEP* mode where the clock is gated $(CLKG)$ to minimize clock power and aid power scalability with sample rate, and the digital circuits are power-gated with a low-leakage high-V_T device to minimize leakage energy at low sample rates. The duration of the *SLEEP* phase is variable to enable sample rate scaling.

B. DAC Architecture

The DAC is an integral part of a SAR ADC since it determines the accuracy of the successive approximations of the sampled input. The two common DAC approaches are resistive DACs (RDACs) or capacitive DACs (CDACs). Fast-settling RDACs consuming static power have been shown to be appropriate for high-speed SAR ADCs employing a multi-bit/cycle topology [14], while CDACs consuming only dynamic switching power are appropriate for low-power, voltage-scalable implementations [9], [15]. Although RDACs can be made lower power by duty cycling, they require series switches to pass rail-to-rail voltages which can limit the amount of voltage scaling in the ADC, or require a large number of boostrapped switches which would increase power and area. Since voltage scaling is used extensively in this work to improve energy-efficiency, the CDAC approach is chosen because it is more amenable to voltage scaling since switches are used to pass voltages only at the rails.

The conventional CDAC uses an array of binary-weighted capacitors to generate the analog output through charge-redistribution [16]. Although the conventional capacitor array is simple to implement, it is quite inefficient for "down" (i.e., decreasing voltage) transitions [12]. Recently, a variety of new switching methods have been proposed to reduce the switching energy. In [12], the split-capacitor switching scheme reduces the average switching energy by 37% by improving the efficiency of the "down" transitions. This is accomplished by splitting the MSB capacitor into a separate *MSB sub-array* that is identical in structure to the rest of the array. The energy-saving approach of [17] applies the split-capacitor approach to the MSB-1 capacitor and eliminates energy consumption during the first switching phase, reducing the switching energy by 56% when compared to the conventional case. In [18], a monotonic set-and-down switching scheme further improves the energy reduction to 81% by avoiding energy consumption during the first transition, reducing the total capacitance by 50%, and only discharging a single capacitor during any subsequent transition. A review of the various switching strategies can be found in [19].

A major limitation of the above switching schemes is the binary weighting between the MSB and LSB capacitor. For example, the MSB capacitor in a 10-bit array is 512$\times$ larger than the LSB capacitor. One way to reduce the ratio, and therefore the energy and area, is to use a lower resolution sub-DAC to interpolate between the transitions of the main-DAC [11]. Fig. 2 shows a conventional 10-bit capacitor array that is segmented into a 5-bit main-DAC and a 5-bit sub-DAC, where the ratio is reduced to just 16. The sub-DAC is coupled to the main-DAC through a series capacitor C_C which is sized to make the series combination of C_C and the sub-DAC look like the unit capacitance C.

In order to yield both area and energy savings, the proposed ADC combines the split-capacitor switching scheme with the use of a sub-DAC as shown in Fig. 3. Here, the capacitor array is segmented into a 6-bit main-DAC and a 4-bit sub-DAC, and the $32C$ MSB capacitor of the main-DAC is split into its own *MSB sub-array* that is identical in structure to the rest of the

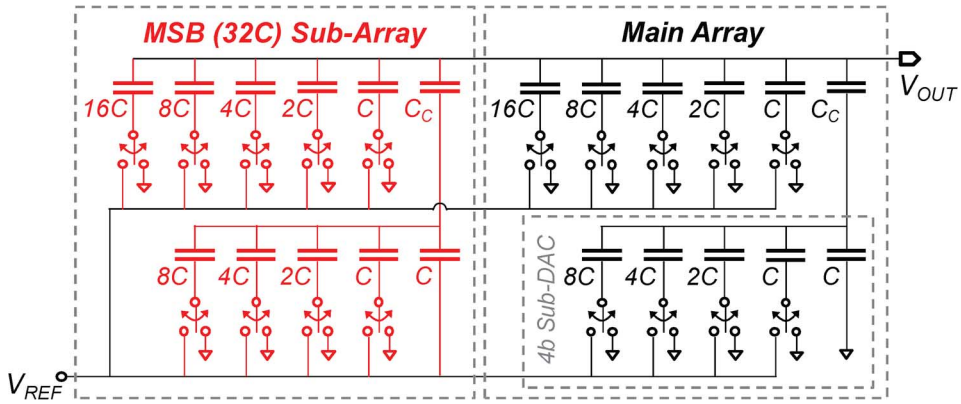

Fig. 3. Split-capacitor array comprising the MSB sub-array and the main array, both segmented into a 5-bit main-DAC and a 4-bit sub-DAC.

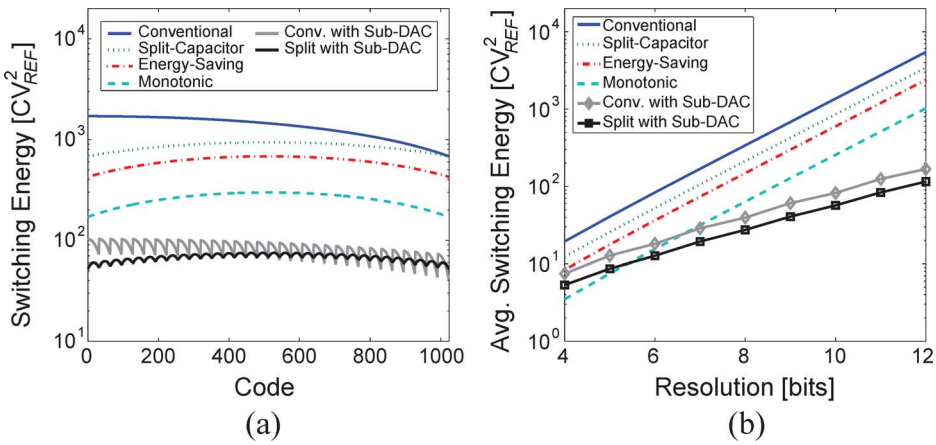

Fig. 4. (a) Comparison of switching energy versus output code for a 10-bit DAC. (b) Average switching energy versus resolution.

main array. The choice of a 4-bit sub-DAC will be discussed later in Section II.D.

In order to compare the energy-efficiency of the various switching schemes, Fig. 4(a) shows the switching energy (normalized to units of CV^2_{REF}) versus the output code for a differential 10-bit array. Assuming that the output codes are uniformly distributed, the split-capacitor array combined with a sub-DAC implemented in the proposed ADC consumes an average of $67.3CV^2_{\mathrm{REF}}$, which is a 20× reduction from the conventional array ($1363CV^2_{\mathrm{REF}}$). While the split-capacitor array with sub-DAC approach is very energy-efficient at 10 bits, Fig. 4(b) shows the average switching energy versus resolution for each of the switching schemes, demonstrating that it remains quite energy-efficient down to around 5 bits. In the comparison of Fig. 4(b), for arrays that use a sub-DAC, the resolution of the sub-DAC is chosen to be equal to or one greater than the main-DAC resolution to minimize switching energy.

C. Resolution Reconfigurability

In addition to optimizing the energy-efficiency of the capacitor array, further energy savings can be achieved by scaling its resolution. With a fixed-resolution DAC, resolution scaling can traditionally be done in two ways. First, it is possible to bit cycle starting at the MSB capacitor, and stop at the desired resolution [13]. However, this approach is avoided because by cycling the large MSB capacitors, the required DAC energy is much larger than necessary. For example, cycling the first 5 MSBs of a conventional 10-bit array to achieve 5-bit resolution would require $1302CV^2_{\mathrm{REF}}$ of energy, which is 32× more energy required than just cycling a small 5-bit array ($40.7CV^2_{\mathrm{REF}}$). The alternative is to start bit cycling in the middle of the array, and bit cycle to the LSB capacitor. However, in this case, the MSB capacitors attenuate the DAC output which increases the resolution requirement of the comparator. Therefore, in the proposed ADC, two modifications are made to the array shown in Fig. 3 to achieve resolution reconfigurability while avoiding the above issues. First, the capacitors of the MSB sub-array and the main-array are interleaved. Secondly, switches are inserted in between each pair of MSB capacitors to decouple capacitors as resolution is scaled. By interleaving the MSB sub-array and main array, it is possible to decouple the same number of capacitors from both arrays, maintaining an identical structure between the two arrays as resolution is scaled. In this prototype, the switches are controlled by the thermometer coded bits R[4:0], and are driven off a fixed 1.2 V supply with negligible current draw. The resulting capacitor array reconfigured in the 10-bit, 8-bit, and 5-bit modes are shown in Figs. 5(a)-(c) respectively.

D. Resolution Scaling Trade-Offs

As resolution is scaled, in order to minimize area and switching energy, the optimal distribution of bits between the

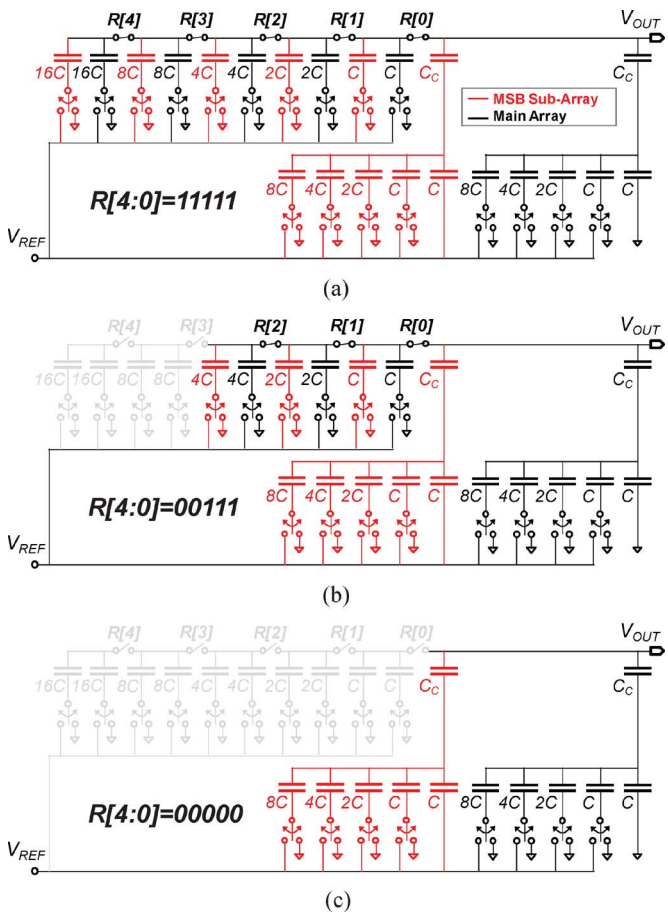

Fig. 5. Reconfigurable DAC in (a) 10-bit mode, (b) 8-bit mode, and (c) 5-bit mode.

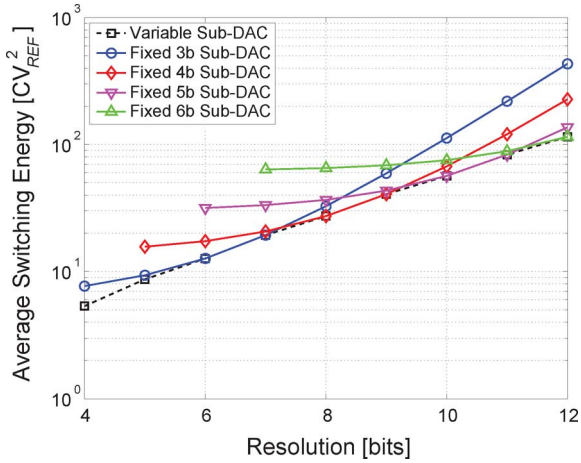

Fig. 6. Comparison of average switching energy for a split-capacitor array with a sub-DAC, for sub-DACs of various resolutions.

main-DAC and sub-DAC is to set the sub-DAC resolution equal to (or one greater than) the main-DAC resolution. This rule is followed in the plot of Fig. 4(b) for arrays employing sub-DACs. However, in this work, the sub-DAC resolution is fixed over all resolution modes because it cannot easily be scaled without adjusting the value of the series capacitor C_C. In order to determine the sub-DAC resolution, Fig. 6 shows a comparison of the average switching energy for a split-capacitor array with a sub-DAC, for sub-DACs of various resolutions. For the target resolution range of 5 to 10 bits, a 4-bit sub-DAC comes close to the optimal case (dashed line) in the 7-to-10-bit range, while trading off some efficiency in the 6-bit and 5-bit modes. Therefore, a design choice is made to fix the sub-DAC resolution at 4 bits. The energy savings across resolution of the proposed approach when compared to the conventional array is summarized in Table I.

Aside from minimizing the switching energy of the capacitor array through architectural optimizations, the unit capacitance C should be sized for sufficient matching at each level of resolution. Since capacitor mismatch scales as $\Delta C \propto 1/\sqrt{C}$, this implies that the unit capacitance can be reduced by $4\times$ for each bit of resolution which would further improve efficiency at lower resolutions. This can be accomplished by using multiple capacitor arrays, each with a different unit capacitance, at the cost of increased area. Alternatively, a sea of smaller unit capacitors can be used, where a subset can be cycled for low resolution modes, and multiple small unit capacitors can be combined to form larger *unit* capacitors for higher resolutions. However, this approach requires extra switch complexity and control overhead. Therefore, in this work, a unit capacitance of $C = 65$ fF using interconnect fringe capacitors is used to achieve matching at the 10-bit level, and the same unit capacitance is used for all resolutions as a trade-off between circuit simplicity and efficiency at lower resolutions.

Fig. 7 shows the schematic of the final implemented 5-to-10-bit reconfigurable DAC in differential form, with the sample-and-hold function combined. In addition to exponential energy savings during bit cycling, the reconfigurable DAC also has the added advantage of exponentially scaling its input capacitance, thus reducing the power required for the ADC driver. The positive and negative DAC reference voltages are the supply voltage (V_{DD}) and ground respectively. During the input sampling phase, the bottom-plate sampling switches are implemented as a transmission gate with a bootstrapped NMOS device, while the top-plate sampling switches (TP[4:0] and *SAMP*) are bootstrapped NMOS devices. Details on the bootstrapped switches are presented in Section III.C.

III. Voltage Scaling and Dynamic Range

This section examines voltage scaling as a strategy to minimize the overall ADC energy-per-conversion. Although voltage scaling is an effective method to reduce digital circuit energy, the design of analog circuits becomes more difficult as a result of reduced voltage headroom, degraded switch resistance, and reduced dynamic range. However, as the resolution is scaled in the proposed ADC, both the noise and linearity requirements are relaxed, providing an opportunity to use voltage scaling to optimize energy-efficiency. This section discusses the sources of energy consumption in the ADC, and the emergence of a minimum energy point due to leakage energy. Furthermore, noise and linearity requirements are discussed, and a voltage scalable comparator is described.

TABLE I
ENERGY SAVINGS ACROSS RESOLUTION OF THE PROPOSED ARRAY COMPARED TO THE CONVENTIONAL ARRAY

Resolution	Switching energy of conventional array [CV_{REF}^2]	Switching energy of proposed array [CV_{REF}^2]	Reduction
5	40.7	15.7	2.6×
6	83.3	17.3	4.8×
7	168.7	20.7	8.2×
8	339.3	27.3	12.4×
9	680.7	40.7	16.7×
10	1363.3	67.3	20.3×

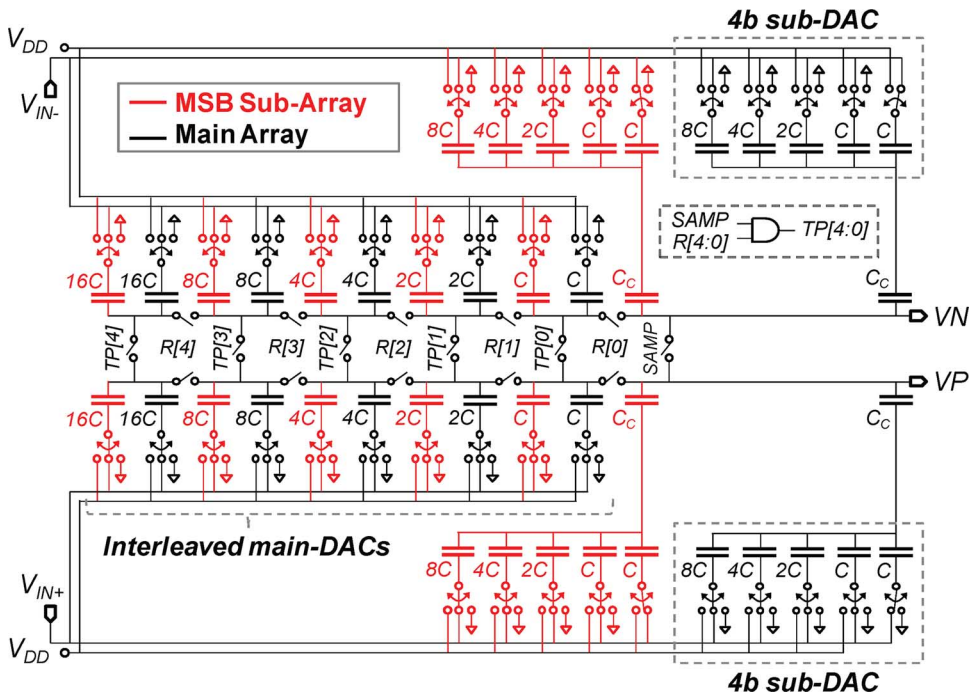

Fig. 7. Differential implementation of the 5-to-10-bit reconfigurable DAC.

A. Energy-Per-Conversion and Minimum Energy Point

This section discusses the energy-per-conversion of the constituent blocks of the ADC. It can be shown that the average switching energy of the DAC is

$$E_{\mathrm{DAC}} = \zeta \cdot \sum_{i=1}^{n} 2^{n+1-2i} \cdot (2^i - 1) \cdot CV_{DD}^2, \tag{1}$$

where n is the resolution and ζ is dependent on the switching scheme, and is equal to 1 for the conventional array [17] and 0.049 in the proposed ADC. In [20], the energy of a dynamic regenerative comparator is derived. When applied to an n-bit matching-limited SAR ADC that requires n comparisons per conversion, the comparator energy-per-conversion can be derived as

$$E_{\mathrm{COMP}} = 2 \cdot ln2 \cdot n^2 \cdot C_{LC} V_{\mathrm{eff}} V_{DD}, \tag{2}$$

where C_{LC} is the load capacitance, and V_{eff} is the transistor overdrive. For the digital circuits and clock network, the energy-per-conversion is given by

$$E_{\mathrm{DIG+CLK}} = C_{\mathrm{EFF}}(n) \cdot V_{DD}^2, \tag{3}$$

where $C_{EFF}(n)$ is the effective capacitance being switched, and is a function of the resolution. Finally, the leakage energy-per-conversion is given by

$$E_{\mathrm{LEAK}} = V_{DD} \cdot I_{\mathrm{LEAK}} \cdot T_S, \tag{4}$$

where I_{LEAK} is the leakage current, and T_S is the minimum conversion time at a given V_{DD}. As V_{DD} is scaled into the sub-threshold, the speed of CMOS devices decreases exponentially, thereby increasing T_S exponentially. The net result is that E_{LEAK} actually increases as the supply voltage is reduced. The energy-per-conversion versus supply voltage for each component of the ADC is illustrated in Fig. 8. The plotted data is based on measurements of dynamic power at 1 V and leakage measurements over all voltages, and extrapolated based on the energy models above. As voltage is scaled down from 1 V, the total energy E_{TOT} is reduced because the dynamic energy of the active blocks dominate. However, the opposing trends of dynamic energy reduction and increased leakage energy at low voltages lead to a minimum energy point (MEP) for the ADC. For low-bandwidth applications that are not throughput limited, it is beneficial to operate at the MEP.

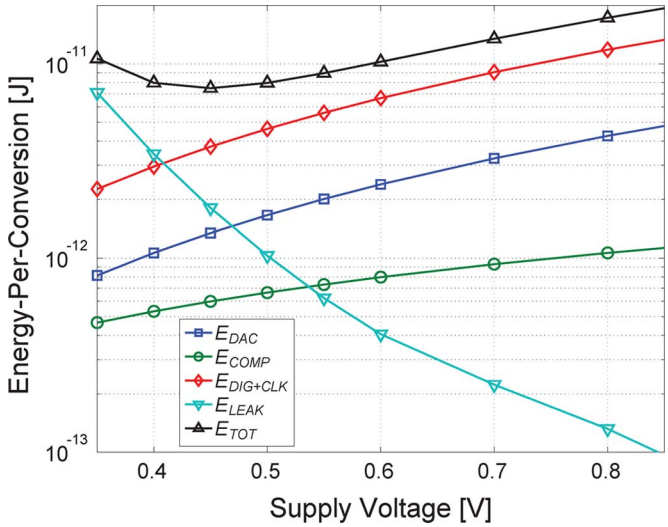

Fig. 8. Energy-per-conversion for each component versus supply voltage.

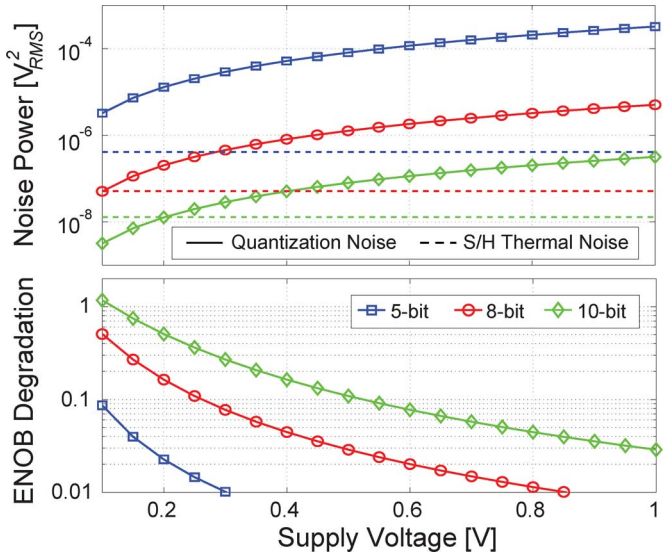

Fig. 9. Relative contributions of sampled thermal noise and quantization noise versus supply voltage, and the degradation in ENOB due to thermal noise. Plotted data assumes $C = 10$ fF to be conservative.

B. Noise and Dynamic Range

Although voltage scaling is an effective strategy for improving energy-efficiency, it proportionately reduces the input range. However, as long as the ADC is limited by quantization noise, the dynamic range stays constant since the LSB voltage also scales with the supply. This remains true until the quantization noise approaches the thermal noise floor, which is set by the sampling capacitance $C_{\rm IN}$ ($C_{\rm IN} = 2^{n-5}C$ for the proposed ADC). The top portion of Fig. 9 shows the quantization noise (solid lines) and sampled $kT/C_{\rm IN}$ thermal noise (dotted lines) versus supply voltage for the $n = 5$, 8, and 10-bit cases. As the voltage decreases, quantization noise approaches the thermal noise floor, which degrades the achievable effective number of bits (ENOB) as shown in the bottom of Fig. 9 (a degradation of 0 corresponds to $\rm ENOB = \it n$). It can be seen that thermal noise can degrade the ENOB by more than 0.1 bits in the 10-bit mode for $V_{DD} < 0.5$ V, while it is insignificant in the 5-bit mode. Therefore, noise requirements decrease with resolution, enabling greater voltage scaling at lower resolution modes.

C. Linearity Requirements

In addition to noise, the degraded "on" resistance of analog switches at low voltages can introduce distortion and limit the bandwidth. To address this, a bootstrap circuit is used to increase the gate-source voltage of the sampling switches. Fig. 10(a) shows the schematic of the differential DAC during the sampling phase and the bootstrap circuit [10] applied to the NMOS device of the complementary bottom-plate sampling switches. The same bootstrap circuit is applied to the NMOS top-plate sampling switches. Node V_X acts as the supply of the output inverter, and charge is stored across capacitor $C_{\rm BST}$ so that V_X swings to $1.5 \times V_{DD}$ when V_Y is driven high. The bootstrap can be bypassed ($\rm BYP = 1$) when operating at the nominal voltage of the process in order to avoid reliability concerns.

Fig. 10(b) shows the simulated total harmonic distortion (THD) of the sampling network versus the input frequency for supply voltages from 0.5 V to 0.8 V. The dotted lines indicate

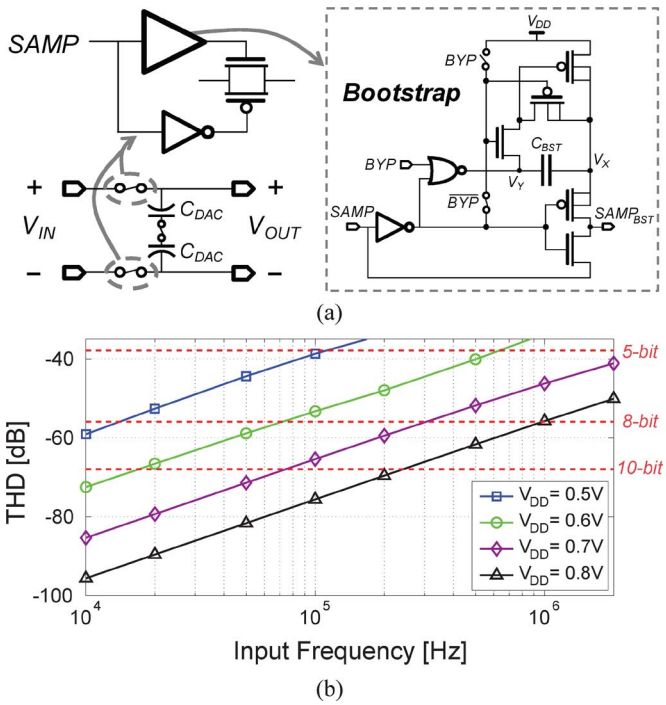

Fig. 10. (a) Schematic of the DAC during the sampling phase, bottom-plate sampling switch, and bootstrap circuit. (b) Simulated THD versus input frequency.

the THD requirement at various resolution modes. For example, in order to achieve 8-bit linearity, the required THD is below $-(6.02 \times 8 + 1.76 + 6) = -55.9$ dB, where an extra 6 dB is added for margin. To illustrate how linearity requirements vary with supply voltage, first consider sampling a 100 kHz signal with 10-bit linearity. Fig. 10(b) suggests that V_{DD} should be approximately 0.72 V or greater to achieve 10-bit linearity. However, to sample the same 100 kHz signal with only 5-bit linearity, it is possible to reduce the supply down to 0.5 V. Therefore, as with noise requirements, it is possible to leverage

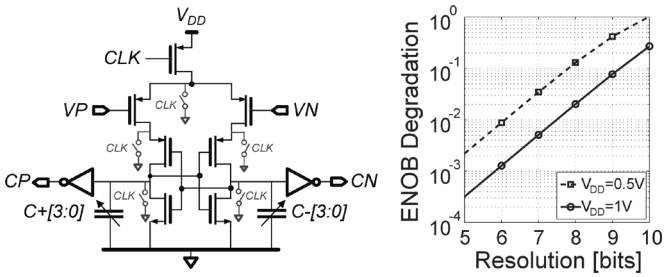

Fig. 11. (a) Schematic of the dynamic comparator. (b) Degradation in the ENOB due to comparator noise.

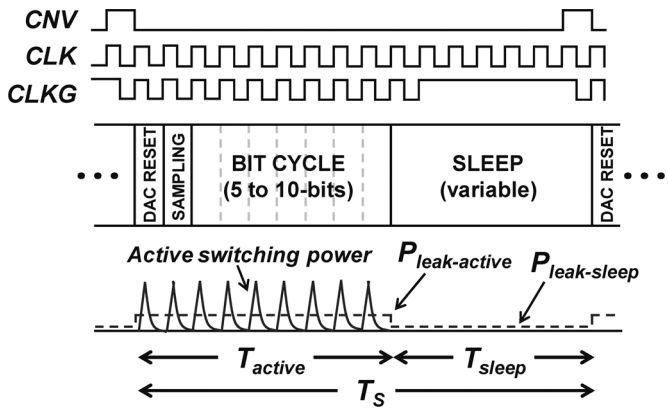

Fig. 12. ADC conversion plan.

reduced linearity requirements at lower resolution modes to scale the supply voltage in order to improve energy-efficiency.

D. Dynamic Comparator

Aside from the DAC and sampling network, the comparator also impacts the speed and precision of the ADC. To enable voltage scalability and achieve superior power-delay product [21], a linear preamplifier is avoided and the regenerative Strongarm comparator [22] shown in Fig. 11(a) is used. PMOS inputs and low-V_T devices are utilized to enable operation down to 0.4 V. Furthermore, since regenerative comparators often exhibit large offsets, 4-bit capacitor banks are used to provide ± 50 mV of tuning [23] in order to cover the simulated 3σ offset of 50 mV which is relatively constant over supply voltage at room temperature. Simulations also show that the expected offset varies by less than 30% over the temperature range from 0 to 100°C. In this work, static offset is manually calibrated once at start-up by adjusting the capacitor code to minimize the offset. However, more sophisticated offset calibration techniques for regenerative comparators can be found in [13], [15], and [24].

One final important consideration is the input-referred noise of the comparator, which shows up directly at the input of the ADC. A thorough noise analysis for fully-dynamic comparators is found in [25]. While the noise of dynamic comparators stems from thermal noise and takes on the familiar kT/C form, the actual amount of noise depends on architecture, transistor sizing, load capacitance, supply voltage, and input common mode [25]. Since dynamic comparators are non-linear large-signal circuits, transient noise simulations are used to estimate its noise. At $V_{DD} = 1$ V (20 MHz clock frequency) and $V_{DD} = 0.5$ V (100 kHz), the comparator noise is 380 μ $\mathrm{V_{rms}}$ and 500 μ $\mathrm{V_{rms}}$ respectively, which agrees with the prediction of increased noise at lower supply voltages [25]. Fig. 11(b) shows the corresponding ENOB degradation versus resolution at 1 V and 0.5 V. In the worst case operating point of 0.5 V in the 10-bit mode, comparator noise can degrade the achievable ENOB by 1 bit. Therefore, while dynamic comparators are very energy-efficient, their thermal noise can limit practical SAR ADC implementations to 10 bits and below.

IV. Leakage Power-Gating

In Section III.A, it was shown that the minimum energy point of the ADC is determined by the ratio of leakage to active energy consumption over supply voltage. One way to decrease the minimum energy point is to minimize the leakage energy of the ADC. This section discusses how leakage reduction is achieved during the ADC conversion cycle.

A. ADC Conversion Plan

Fig. 12 shows the conversion plan of the proposed ADC. As described in Section II.A, each conversion begins with the three active phases of DAC reset, input sampling, and bit cycling. The SAR logic controlling the phases of the conversion cycle is similar to [26], but extra resolution scaling logic is added to select the starting point of bit cycling. The active phases of duration T_{active} all consume active switching power, as well as leakage power $P_{\mathrm{leak-active}} = V_{DD} I_{\mathrm{leak-active}}$. After these active phases, the clock is gated $(CLKG)$ and the ADC enters the *SLEEP* mode. By varying the duration of the *SLEEP* mode, T_{sleep}, the sample rate can be scaled. During *SLEEP*, the leakage power of the ADC is reduced to $P_{\mathrm{leak-sleep}} = V_{DD} I_{\mathrm{leak-sleep}}$ by gating the digital logic with a high-V_T device. Since T_{sleep} can dominate the conversion period T_S ($T_S = T_{\mathrm{active}} + T_{\mathrm{sleep}}$) at low sample rates, the overall leakage energy can be significantly reduced.

B. Leakage Power-Gating Break-Even Point

Although leakage power-gating reduces the *SLEEP* mode leakage, there is energy overhead that must be accounted for. Fig. 13(a) shows the digital logic being power-gated by the high-V_T switch, and the associated capacitances. The first component of the overhead is the energy required to switch the gate capacitance C_G of the power switch, which must be sized relatively large (W $= 48$ μm) to limit the spike of the virtual ground node to a few millivolts. This energy is equal to

$$E_{\mathrm{SW}} = C_G V_{DD}^2 \tag{5}$$

per conversion. The second component of the overhead is the energy required to recover the virtual ground node. When the power switch is off, the virtual ground node will drift up toward the V_{DD} rail by an amount ΔV due to leakage. For sufficiently large T_{sleep}, ΔV can approach V_{DD}. The recovery energy is then equal to

$$E_{\mathrm{REC}} = C_X V_{DD} \Delta V \tag{6}$$

TABLE II
SUMMARY TABLE OF THE MEASURED ADC PERFORMANCE

Active die area	0.212mm^2 (65nm low-leakage CMOS)					
Supply voltage (V_{DD})	0.4V to 1V (differential input range is $\pm V_{DD}$)					
Maximum sampling frequency (all resolutions)	5kS/s @ 0.4V 2MS/s @ 1V					
Resolution mode	**5b**	**6b**	**7b**	**8b**	**9b**	**10b**
Differential input capacitance [fF]	65	130	260	520	1040	2080
INL [LSB] @ 0.6V, 100kS/s	0.07	0.33	0.33	0.43	0.50	0.57
DNL [LSB] @ 0.6V, 100kS/s	0.11	0.35	0.40	0.51	0.55	0.58
Dynamic performance @ 0.55V, f_S=20kS/s (*except for 5b data @ 0.5V, f_S=60kS/s)						
SFDR [dB] @ Nyquist	*44.0	48.5	54.6	61.2	63.0	68.8
SNDR [dB] @ Nyquist	*30.4	36.6	41.5	47.0	51.2	55.0
ENOB @ Nyquist	*4.77	5.79	6.60	7.51	8.21	8.84
Power [nW]	*234	116	133	146	159	206
FOM [fJ/conversion-step]	143.4	105.1	68.5	40.0	26.8	22.4

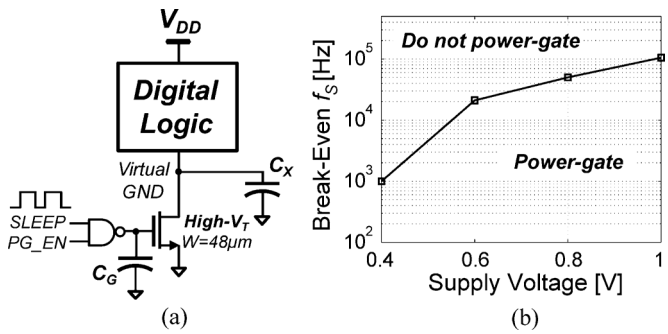

Fig. 13. (a) Schematic of the leakage power-gating switch and associated parasitic capacitances. (b) Simulated break-even time for leakage power-gating.

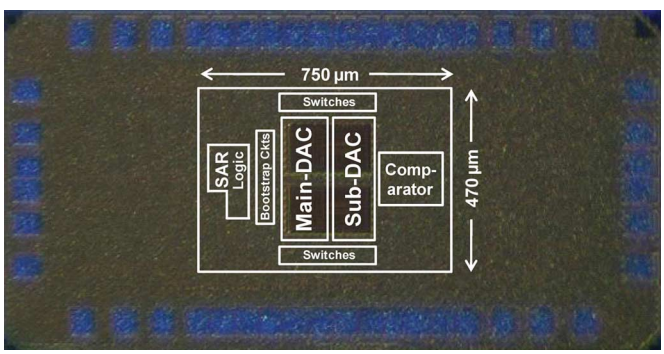

Fig. 14. Die micrograph of the ADC prototype.

per conversion, where C_X is the capacitance at the virtual ground node. Therefore, in order for leakage power-gating to be beneficial, the overhead energy must be less than the leakage energy savings which is summarized by

$$E_{\rm REC} + E_{\rm SW} < (P_{\rm leak-active} - P_{\rm leak-sleep})T_{\rm sleep}. \quad (7)$$

This condition sets a minimum on $T_{\rm sleep}$ which corresponds to a maximum sampling rate defined as $f_{S,BE}$, the break-even sampling frequency. If it is assumed that $T_{\rm sleep} \gg T_{\rm active}$ and $I_{\rm leak,sleep} \ll I_{\rm leak,active}$, $f_{S,BE}$ can be approximated by

$$f_{S,BE} \approx \frac{P_{\rm leak-active}}{E_{\rm REC} + E_{SW}} = \frac{I_{\rm leak-active}}{(C_X + C_G)V_{DD}}, \quad (8)$$

where $I_{\rm leak-active}$ is a sub-threshold current and has an exponential dependence on V_{DD} due to drain induced barrier lowering (DIBL), causing $f_{S,BE}$ to actually decrease with supply voltage. Fig. 13(b) shows the simulated $f_{S,BE}$ versus the supply voltage. At each volage, it is assumed that the active phases are completed as fast as possible to maximize the duration of the *SLEEP* mode. The region for which leakage power-gating is beneficial is under the line plotted in Fig. 13(b).

V. MEASUREMENT RESULTS

A prototype ADC was fabricated in a low-leakage 65 nm digital CMOS process, and the die micrograph is shown in Fig. 14. The ADC core occupies an area of 0.212 mm^2. This section presents the measured results, and a summary of the performance is provided in Table II.

A. Static Linearity

Fig. 15 shows the measured static linearity using the code density test with full-swing, low-frequency sinusoids at 0.6 V and a sampling rate of 100 kS/s in the 5-bit, 8-bit, and 10-bit modes. 10 samples were measured and the mean results are presented. In the 10-bit mode, the peak DNL and INL are $+0.58/-0.13$ LSB and $+0.57/-0.56$ LSB respectively. The 32-code sawtooth pattern in the INL arises from parasitic capacitance on the top-plate of the sub-DAC, resulting in a systematic mismatch with the main-DAC. The sawtooth can be corrected by properly adjusting the C_C capacitor in the DAC array using post-layout extraction. Alternatively, since this linearity error is systematic, it can also be calibrated out in the digital domain. No sawtooth pattern is present in the 5-bit mode because only

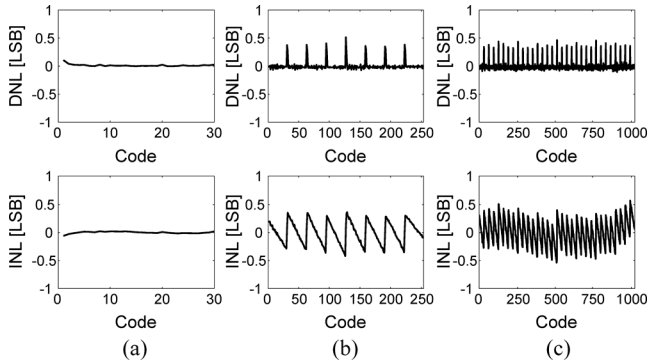

Fig. 15. Measured DNL and INL at 0.6 V in (a) 5-bit mode, (b) 8-bit mode, and (c) 10-bit mode.

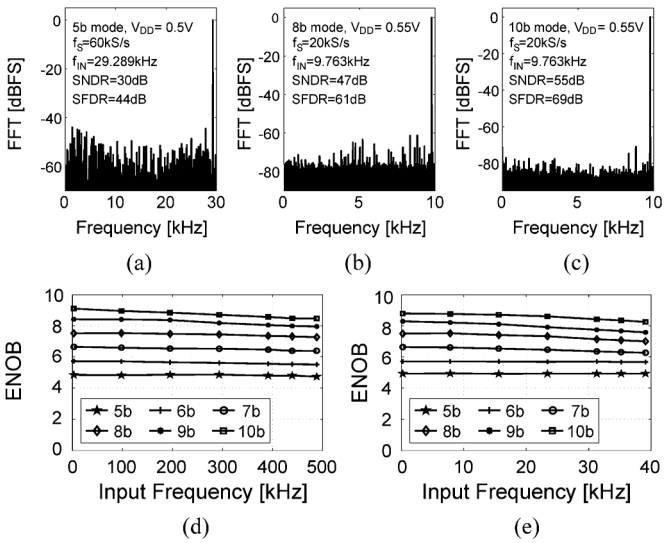

Fig. 16. Measured FFT in (a) 5-bit mode at 0.5 V, (b) 8-bit mode at 0.55 V, and (c) 10-bit mode at 0.55 V, and measured ENOB vs. input frequency over all resolution modes at (d) $f_S = 1$ MS/s at 1 V, and (e) $f_S = 80$ kS/s at 0.55 V.

the sub-DACs are used in that case (Fig. 5(c)). The measured offset has a standard deviation of 10.9 mV which is constant across resolution modes.

B. Dynamic Performance

Figs. 16(a), (b), and (c) show the fast Fourier transform (FFT) of the ADC in 5-bit, 8-bit, and 10-bit modes with near-Nyquist tone inputs at 60 kS/s ($V_{DD} = 0.5$ V), 20 kS/s ($V_{DD} = 0.55$ V), and 20 kS/s ($V_{DD} = 0.55$ V) respectively, which correspond to their optimal efficiency points (presented in Section V.E). In the 10-bit mode at 0.55 V, the Nyquist-rate SFDR and SNDR are 69 dB and 55 dB (ENOB of 8.84 bits) respectively.

Figs. 16(d) and (e) show the ENOB versus the input frequency for all resolution modes at 1 MS/s ($V_{DD} = 1$ V), and 80 kS/s ($V_{DD} = 0.55$ V) respectively. At $V_{DD} = 1$ V, the effective resolution bandwidth (ERBW) in the 5-bit to 9-bit modes is well above 500 kHz, while in the 10-bit mode, the ERBW falls to approximately 350 kHz. At $V_{DD} = 0.55$ V, the ERBW in the 5-bit to 8-bit modes is above 40 kHz, and decreases to approximately 35 kHz in the 9-bit and 10-bit modes.

The power supply sensitivity and common-mode rejection ratio (CMRR) are also measured across resolution modes

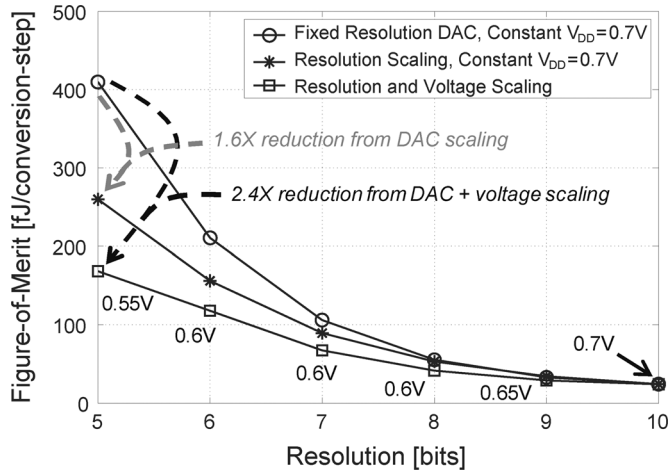

Fig. 17. Measured effect of voltage scaling (with respect to 0.7 V) and DAC resolution scaling on the ADC FOM at 200 kS/s. In the case of the fixed resolution DAC, the FOM at each resolution is calculated by truncating bits from 10-bit data.

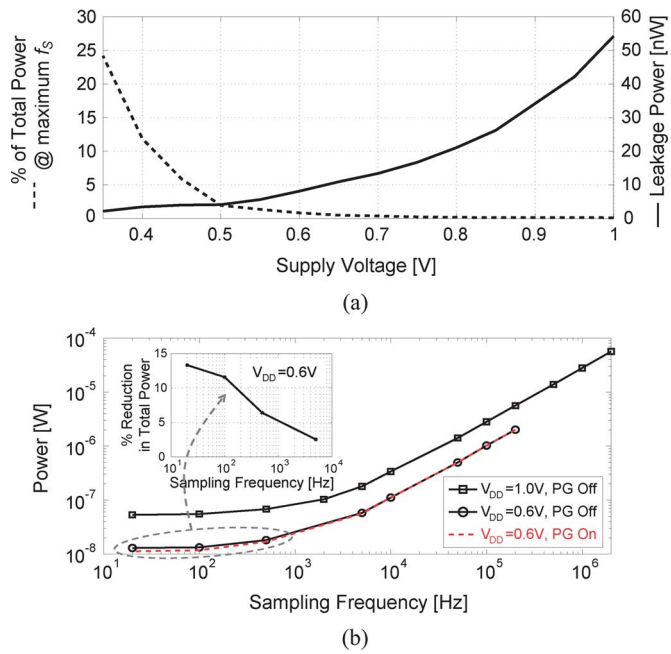

Fig. 18. (a) Leakage power versus supply voltage plotted in nW and as a percentage of the total ADC power at the maximum f_S. (b) Power versus sampling frequency. The insert at the top left of the plot shows the reduction in the total power at low frequencies as a result of leakage power gating at 0.6 V.

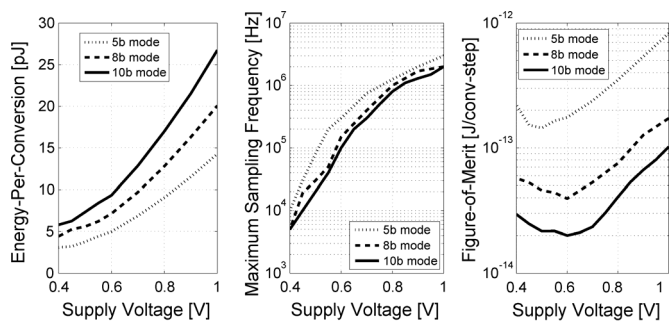

Fig. 19. Measured (a) energy-per-conversion (power/f_S), (b) maximum sampling frequency, and (c) figure-of-merit, versus the supply voltage.

at 0.55 V. For a power supply ripple of $\pm 5\%$, the worst case sensitivity is ± 0.47 LSB in the 10-bit mode. The CMRR across all resolution modes is better than 55 dB.

Resolution Mode	V_{DD} [V]	Total Power [μW]
5	0.55	0.91
6	0.6	1.23
7	0.6	1.41
8	0.6	1.55
9	0.65	2.08
10	0.7	2.77

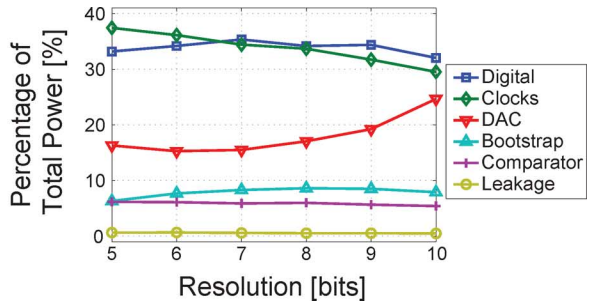

Fig. 20. Measured total ADC power at 200 kS/s, and breakdown by block as a percentage of the total power.

C. Resolution and Voltage Scaling

A widely used figure-of-merit (FOM) which describes the efficiency of the ADC with respect to the input bandwidth ($f_{\rm in}$) and dynamic range is given by

$$\text{FOM} = \frac{P}{2f_{\rm in}2^{\rm ENOB}} \tag{9}$$

where P is the power consumption, and ENOB is measured at the stated $f_{\rm in}$. Fig. 17 illustrates the improvement in energy-efficiency (or equivalently, the FOM) at 200 kS/s when the techniques of DAC resolution scaling and voltage scaling are applied. Comparison is made to the nominal case of a fixed 10-bit resolution DAC with the supply voltage fixed at 0.7 V. In this nominal case, the FOM for each resolution is calculated by truncating bits from 10-bit data. When DAC resolution scaling is applied (V_{DD} remains fixed at 0.7 V), a 1.6× improvement in the FOM in the 5-bit mode is achieved because the DAC power is scaled exponentially with resolution with no loss in accuracy. When both DAC resolution and voltage scaling are applied (scaled voltages are annotated on Fig. 17), a 2.4× improvement in the FOM in the 5-bit mode over the nominal case is achieved.

D. Leakage Reduction

Fig. 18(a) shows how the measured leakage power decreases with supply voltage (solid line). The ADC has a leakage of 53 nW at 1 V and 4 nW at 0.4 V. However, when the same data is plotted as a percentage of the total ADC power at the maximum sampling frequency at each voltage (dotted line), it is apparent that leakage becomes significant at low voltages due to reduced sampling rates. At 0.4 V, 4 nW of leakage represents 12% of the total power at the maximum sampling frequency. This percentage increases when the sampling frequency is decreased below the maximum.

Fig. 18(b) shows the total ADC power versus the sampling frequency at 1 V and 0.6 V without leakage power-gating, and at 0.6 V with leakage power-gating enabled. At high frequencies, the power scales linearly with frequency because active power dominates. Leakage becomes significant at sample rates below 2 kS/s and limits the energy-efficiency. When leakage power-gating of the digital circuits is enabled below 1 kS/s at 0.6 V, the total power is reduced by up to 14%. The effectiveness of this technique could be improved by extending the gating to the analog circuits as well. Lastly, leakage power-gating has the potential for greater impact as CMOS processes continue to scale.

E. Optimum Efficiency Point

Fig. 19(a) shows the measured energy-per-conversion versus supply voltage, and Fig. 19(b) shows the maximum sampling frequency versus supply voltage. At high voltages, dynamic CV_{DD}^2 losses degrade the energy-per-conversion. Conversely at low voltages, the maximum sampling frequency is reduced, leading to increased conversion time and increased leakage energy. In addition, leakage through the sampling switches during bit cycling at low frequencies will leak away charge from the DAC and degrade the ENOB. These opposing trends all affect the FOM and lead to an optimum efficiency point of approximately 0.5 V and 0.55 V for the 5-bit and 10-bit modes respectively as shown in Fig. 19(c). Note that the optimum efficiency point (OEP) is not necessarily equal to the minimum energy point because the OEP accounts for the effective dynamic range of the ADC.

F. Power Breakdown

The total power of the ADC at 200 kS/s for each resolution mode and the percentage breakdown by block is provided in Fig. 20. At 200 kS/s, the ADC consumes 2.77 μW from 0.7 V in the 10-bit mode, and 0.91 μW from 0.55 V in the 5-bit mode, corresponding to the data in Fig. 17.

VI. Conclusion

This paper presents a power-scalable SAR ADC with reconfigurable resolution from 5 to 10 bits. The voltage-scalable architecture features an energy-efficient DAC that combines the split-capacitor switching scheme with the use of a sub-DAC to reduce energy and input capacitance. Switches are used to decouple capacitors as resolution is scaled, leading to exponential DAC power savings with resolution. As noise and linearity requirements are reduced at lower resolutions, voltage scaling is leveraged to further improve the ADC energy-per-conversion. Finally, leakage power-gating is applied to minimize leakage at low sample rates.

The combined techniques of DAC resolution and voltage scaling maximize efficiency at low resolutions, resulting in an FOM that increases by only 7× over the 5-bit scaling range from 10 bits to 5 bits, improving upon a 32× degradation that would otherwise arise from truncation of bits from an ADC of fixed voltage and resolution.

Fig. 21 shows the energy-per-conversion versus SNDR for the proposed ADC and recently reported designs [27]. This work achieves good efficiency over a wide range of resolutions and sample rates. In the 10-bit mode, this ADC achieves an optimum

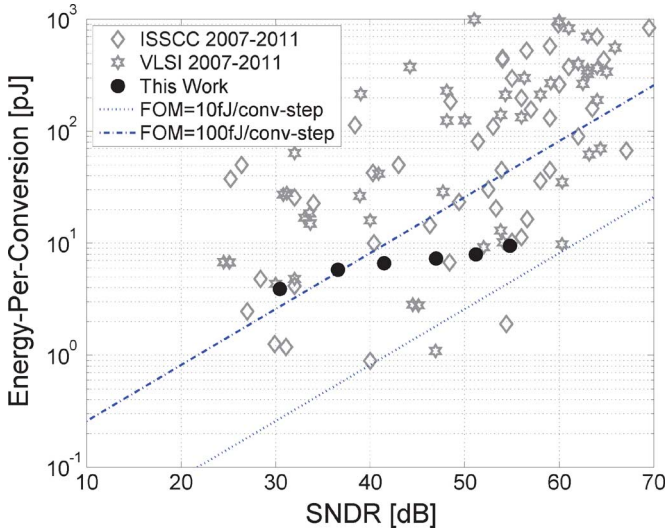

Fig. 21. Comparison with recently reported designs [27].

FOM of 22.4 fJ/conversion-step at 0.55 V, which is competitive with current state-of-the-art fixed resolution ADCs.

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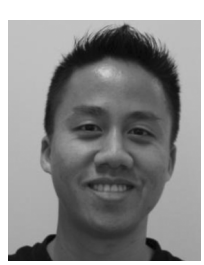

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