A 10-bit 44-MS/s 20-mW Configurable Time-Interleaved Pipeline ADC for a Dual-Mode 802.11b/Bluetooth Receiver

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***Abstract*—This work presents a configurable time-interleaved pipeline architecture as an efficient solution for the ADC design in high data rate multi-standard radios. The ADC is implemented in a 0.25-μm BiCMOS process as part of an integrated dual mode 802.11b/Bluetooth direct conversion receiver. Its structure can be configured to accommodate the different sampling rate and dynamic range requirements of both standards. The different techniques employed at the system and circuit levels to optimize the power consumption are described. An on-line digital calibration scheme is also incorporated to assure the conversion linearity and reduce mismatch among the parallel branches. The proposed ADC is a switched-capacitor implementation occupying an area of 2.1 mm^2. It achieves 60 dB/64 dB dynamic range at 44 MHz/11 MHz sampling frequency with a power consumption of 20.2 mW/14.8 mW for the 802.11b/Bluetooth baseband signals.**

***Index Terms*—Digital calibration, multi-standard receiver, pipeline ADC, time-interleaved ADC.**

I. Introduction

As a result of the rapid development in wireless technologies, various communication standards have emerged recently. End users look for devices that can support multiple standards, since they frequently require access to more than one type of wireless network. The multi-standard receiver promises to solve the incompatibility issue among different standards without duplicated investment and has drawn significant research interest recently [1]–[3].

Bluetooth (BT) and 802.11b are two of the most commonly used wireless standards and, with different data rate capabilities, target different applications in the home and office environments. Both standards use the 2.4 GHz ISM (Instrumentation, Scientific, and Medical) frequency band. For this reason, in a dual-mode 802.11b/BT receiver, a single RF front-end circuit can be employed in both receiving modes. In the radio implementation, the major difficulty falls in the design of the baseband circuits, because of the different requirements (e. g. signal-to-noise ratio (SNR) and bandwidth) between the two standards. As a key part of the receiver baseband, the ADC is one of the most challenging building blocks. For the 802.11b/BT dual-mode receiver, the ADC processes a total of 4 modulation formats and 4 data transfer rates. In addition, the power consumption of the ADC must be minimized to make the transceiver module suitable for portable devices. Therefore, how to efficiently implement the ADC becomes an important research topic in the development of a multi-standard receiver.

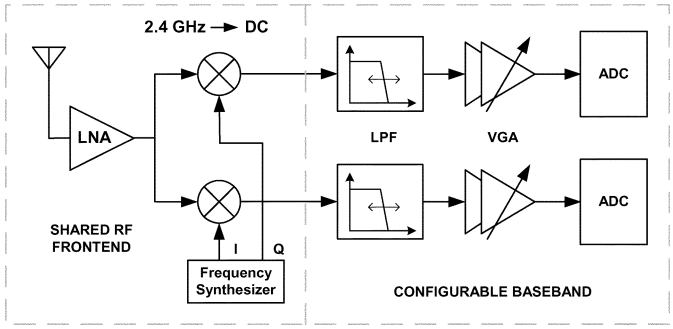

Fig. 1. Block diagram of the direct-conversion 802.11b/BT dual-mode receiver.

Fig. 1 shows an implementation of a direct-conversion 802.11b/BT dual-mode receiver [1]. To optimize the silicon area and power consumption, the receiver features a shared RF front-end and a programmable baseband. This work presents the ADC design for this dual-mode receiver. A configurable time-interleaved pipeline ADC is proposed to meet the requirements of both standards and to reduce power dissipation. As it will be described, this ADC structure can also be used in other wide-band multi-standard receiver systems. The design requirements and the architecture are described in Sections II and III, respectively. An on-line digital calibration scheme, which improves linearity and match properties, is presented in Section IV. Section V and VI cover the circuit implementation and experimental results of the ADC. Finally, conclusions are drawn in Section VII.

II. ADC Design for the Multi-Standard Receiver

The specifications of the ADC in a wireless receiver are governed by the signal modulation format. The quantization noise generated by the ADC must be low enough to guarantee the proper detection of the received signal. In addition, the ADC needs to accommodate signal amplitude variations. Therefore, the dynamic range, $\mathrm{DR_{ADC}}$, of the ADC can be calculated as

$$\mathrm{DR_{ADC}} = \mathrm{SNR_{DEM}} + \mathrm{DR_{SIG}} + \mathrm{DM} \qquad (1)$$

Manuscript received June 1, 2005; revised October 11, 2005. This work was supported in part by Texas Instruments Incorporated.

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Digital Object Identifier 10.1109/JSSC.2005.864131

TABLE I
SUMMARY OF THE ADC SPECIFICATIONS FOR 802.11b AND BT STANDARDS

Standard	Bluetooth	IEEE 802.11b
Modulation	GFSK	DBPSK, DQPSK, CCK
Data Rate	1 Mb/s	1, 2, 5.5, 11 Mb/s
BER	0.1%	0.001%
Preamble Length	4-bit	72-bit/144-bit
Dynamic Range	66 dB	46 dB
Sampling Rate	11 MS/s	44 MS/s
Signal Bandwidth	550 kHz	5.5 MHz
Differential Input Swing	2 V_{pp}	2 V_{pp}
Clock Jitter	14.1 ps	1.7 ps

where $\mathrm{SNR_{DEM}}$ is the SNR requirement of the demodulator and $\mathrm{DR_{SIG}}$ is the signal dynamic range in front of the ADC which is determined by the receiver structure and gain control scheme. A design margin (DM) of 4 to 10 dB is commonly applied in the design of ADCs for wireless receivers to accommodate sudden variations in the received signal strength. The sampling rate of the ADC should not only comply with the Nyquist rule, but also satisfy the synchronization requirement of the demodulator. Table I summarizes the ADC specifications for the dual mode 802.11b/BT receiver.

Matlab and SystemView system level simulation setups are developed with noncoherent demodulators for the 1 Mb/s BT and 11 Mb/s 802.11b systems. Fig. 2 illustrates the effect of the ADC resolution on the demodulator BER versus SNR performance. Observe that 5-bit of quantization are enough for both the 802.11b and BT baseband signals.

The delay in the automatic gain control (AGC) loop of the receiver includes the settling time of the VGA, and the latency of the ADC and subsequent DSP. A fine gain control requires several AGC loop iterations, which results in a long settling time for the receiver. For this reason, a single step gain control is applied to the receiver in BT mode to satisfy the fast settling requirement (4 μS) of the BT standard [1]. As a result, the dynamic range seen by the ADC in this mode increases by 30 dB. On the other hand, in the 802.11b receiving mode the settling time requirement is more relaxed. Fine gain control steps are applied through the VGA to reduce the variations in the amplitude of the signal power at the input of the ADC to 6 dB [1]. Using (1) including a design margin, the overall ADC dynamic range specifications for 802.11b and BT receiving modes are set as 46 dB and 64 dB, respectively.

In the direct-conversion receiver, the received signal is converted to 0 Hz IF directly. The DC offset is cancelled through passive RC high-pass filters placed in between the stages of the VGA [1]. The bandwidths of the down-converted 802.11b and BT signals are 5.5 MHz and 550 kHz respectively. The required sampling rate for each standard is higher than the corresponding Nyquist rate in order to provide sufficient synchronization accuracy in the demodulator. From system level simulation results, for a negligible degradation in the demodulator performance, the ADC is required to operate at 11 MS/s for the BT signal, and at 44 MS/s for the 802.11b signal.

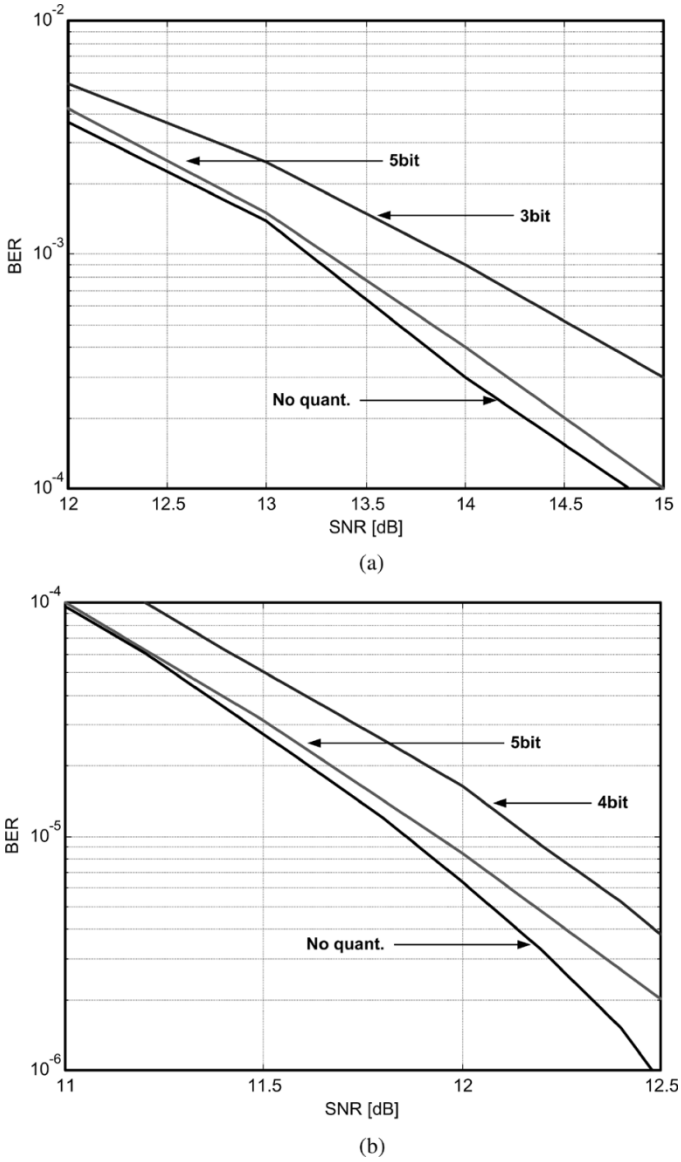


Fig. 2. Effect of ADC quantization error on receiver data detection performance, (a) bluetooth system (b) 802.11b system (11 Mbps).

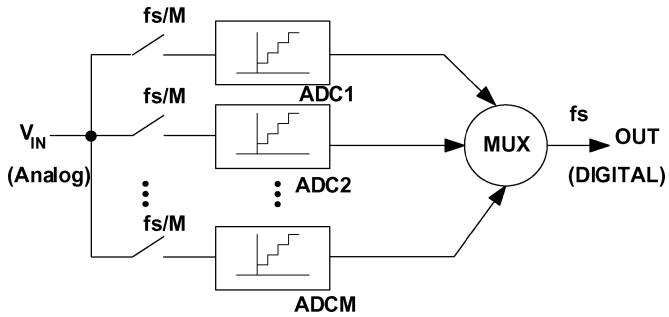


Fig. 3. Time-interleaved ADC structure.

III. TIME-INTERLEAVED PIPELINE STRUCTURE FOR THE MULTI-STANDARD ADC

The $\Sigma\Delta$ ADC is an attractive solution for a multi-standard receiver deign. It can be configured to achieve wider bandwidth with less resolution or narrower bandwidth with higher resolution by programming its digital decimation filter [4], [5]. A $\Sigma\Delta$

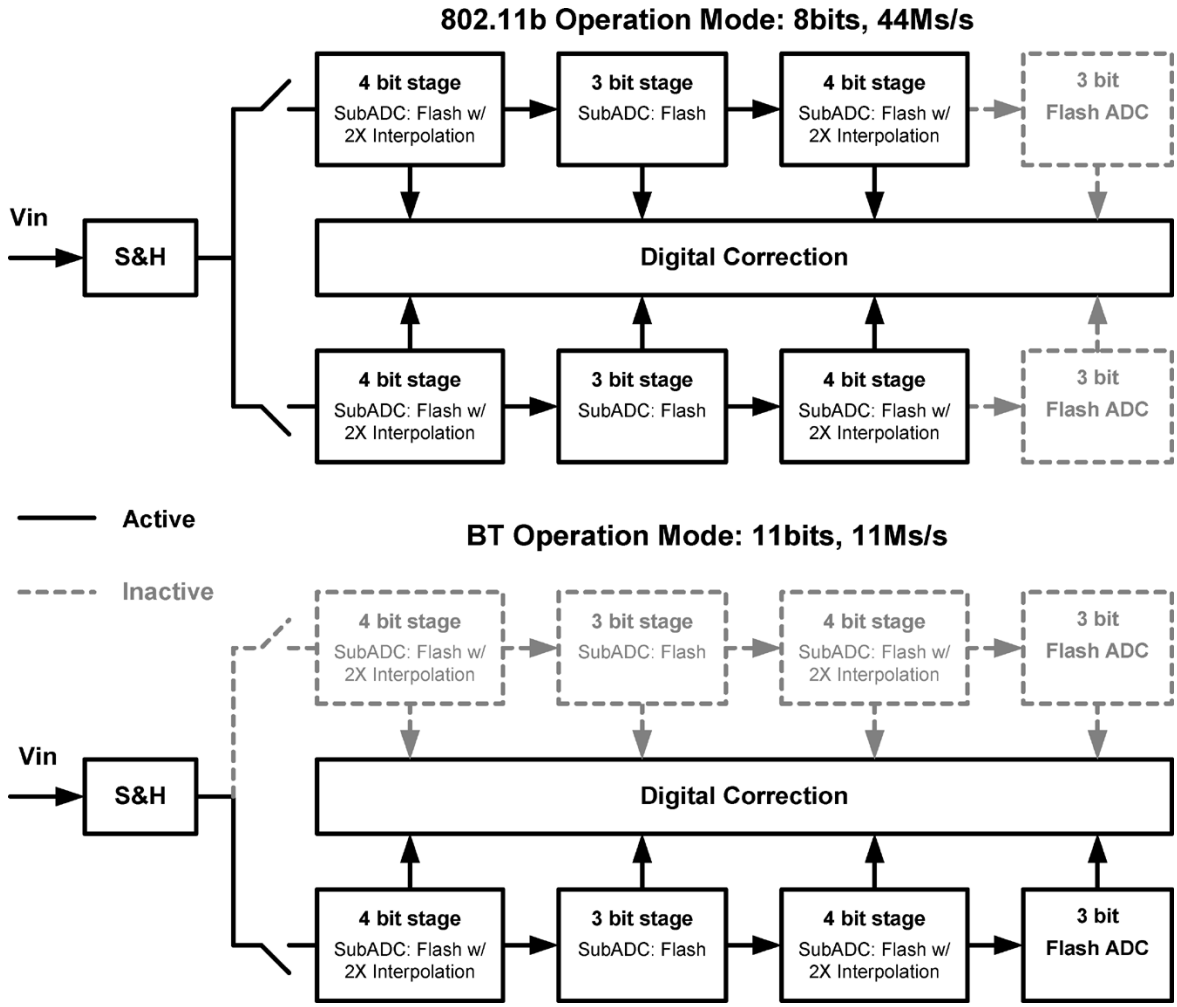


Fig. 4. Block diagram of the configurable time-interleaved pipeline ADC.

ADC uses over-sampling and operates at a significantly higher frequency than the signal bandwidth of interest. For wide bandwidth wireless systems, such as 802.11b, the high sampling frequency in a $\Sigma\Delta$ ADC would lead to a high power consumption, which is not affordable in portable devices.

Simple Nyquist-rate ADCs can also be used in a multi-standard receiver. However, these ADCs usually have a fixed circuit structure. To accommodate the different signal characteristics in a multi-standard receiver, the ADC has to be over-designed for the highest sampling rate and largest dynamic range. Alternatively, individual ADCs could be used in each different receiving mode but this approach demands more silicon area.

Fig. 3 shows a general time-interleaved ADC structure which has been used in high speed A/D conversion applications [6]. It consists of multiple identical ADC branches that operate in a time-interleaved fashion. The power consumption of the entire ADC is reduced by lowering the sampling rate of each ADC branch to f_S/M, where f_S is the overall sampling rate and M is the total number of branches. Note that the overall sampling rate, f_S, can also be interpreted as $(f_S/M) \cdot M$, the sampling rate in each ADC branch times the number branches. This observation indicates that the overall sampling rate of a time-interleaved ADC can be programmed by employing different number of ADC branches. The proposed ADC architecture for multi-standard receivers is based on this perspective [7].

The configurable time-interleaved ADC for the 802.11b/BT dual-mode receiver is illustrated in Fig. 4. It consists of two identical 11-bit pipelined ADC branches that are designed to sample at 22 MS/s. Both of them operate during the 802.11b receiving mode to provide an overall 44 MS/s sampling rate. Only one pipeline branch is activated in the BT receiving mode and its sampling rate is scaled down to 11 MS/s. In the high speed 802.11b receiving mode, the ADC benefits from the time-interleaved structure to reduce the power dissipation. To further save power in this mode, the last stage in each pipeline branch can be disabled while still providing the required 8-bit resolution. It is important to note that since 10-bit and 40 Ms/s have been chosen as the ADC characteristics for a direct-conversion 802.11a receiver [8], [9], the proposed configurable ADC structure is also suitable for a multi-mode BT/802.11a/b/g receiver.

For the implementation of the ADC branches, a pipeline architecture is preferred to meet the required the resolution and speed specifications. The choice of this particular 2-branch time-interleaved pipeline ADC with multi-bit stages is also the result of power optimization at system level. The power

optimization of a pipeline ADC with respect to the number of parallel branches and bits per stage has been addressed for different implementations throughout the years [10], [11]. The power consumption of a pipeline ADC depends significantly on the process characteristics and the circuit implementation. There is no simple conclusion on which architecture is the best for a given target performance. The power consumption of the front-end sample and hold (S&H) circuit does not depend strongly on the choice of number of branches or bits per stage since its operating frequency is fixed by the desired total sample rate. Multiplying DACs (MDACs) are used in the pipeline ADC stages to perform the functions of S&H, DAC, and detection and amplification of the residue (Section V). The choice of the pipeline ADC architecture has a significant impact on the number of MDACs employed, their specifications, and hence their total contribution to the power consumption. In this work, the system level power dissipation analysis and optimization focuses on the settling requirement of the MDACs.

If the ADC has M branches, the settling time available for each branch is $MT_S/2$, where $T_S = 1/f_S$ is the sampling period of the ADC. In this design, the typical settling requirement is limited to $MT_S/4$ to assure proper settling at the end of the sampling period over process and temperature corners. The settling time of the MDAC contains slewing phase, t_{slew}, and linear settling phase, t_{settle}. Each phase is constrained to be less than $MT_S/8$ to meet the total settling requirement of $MT_S/4$. This assumption greatly simplifies the analysis without compromising its objective. In this way, the slew rate requirement for the amplifier, SR, can be calculated as $\mathrm{SR} = V_{PP}/t_{slew} = 8V_{PP}/MT_S$, where V_{PP} is the maximum swing required at the MDAC output. The linear settling time is defined by the unity gain bandwidth (GBW) of the amplifier and the resolution requirement of the ADC. In the 802.11b/BT ADC, 11-bit resolution is required, which demands a settling error $\varepsilon_r < 1/2^{12} = 0.02\%$. If a first order approximation is applied to the MDAC amplifier, the GBW of the amplifier becomes $GBW = -\ln\varepsilon_r/2\pi t_{settle}\beta = -4\ln\varepsilon_r/\pi MT_S\beta$, where β is the feedback factor. Assuming all of the stages have a B-bit MDAC, $\beta = 2/(2^B+1)$ (see Fig. 10).

In this design, a two-stage amplifier structure, as shown in Fig. 5, is adopted in the MDACs to provide a 2 V differential swing under a 2.5 V power supply. A unit capacitance of C_U is used in the MDAC. The value of C_U is defined by *kT/C* noise and matching requirements. As a result, the total sample and feedback capacitance in the MDAC is larger than the compensation capacitor used in the amplifier. Thus, the slew rate of a two-stage amplifier is limited by the output stage and can be expressed as: $\mathrm{SR} = I_2/(C_L + (1-\beta)\cdot C_{FB})$. Here I_2 is the total current in the second stage, $C_L = 2^B C_U$ is the load from next stage MDAC (also B-bit) and $C_{FB} = 2C_U$ is the feedback capacitor (see Fig. 10). Therefore, I_2 needs to satisfy (2) to provide enough slew rate:

$$I_2 = \left(2^B C_U + \left(1 - \frac{2}{2^B+1}\right)\cdot 2C_U\right)\frac{8V_{PP}}{MT_S}. \quad (2)$$

The GBW of a two-stage amplifier can be obtained as $GBW = \sqrt{I_1 K'}/2\pi C_C$, where I_1 is the tail current of the first stage differential pair, $K' = 2K_p\cdot W/L$ is the differential pair transistor

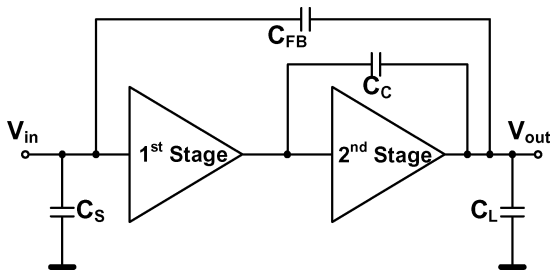


Fig. 5. MDAC circuit model with a two-stage amplifier.

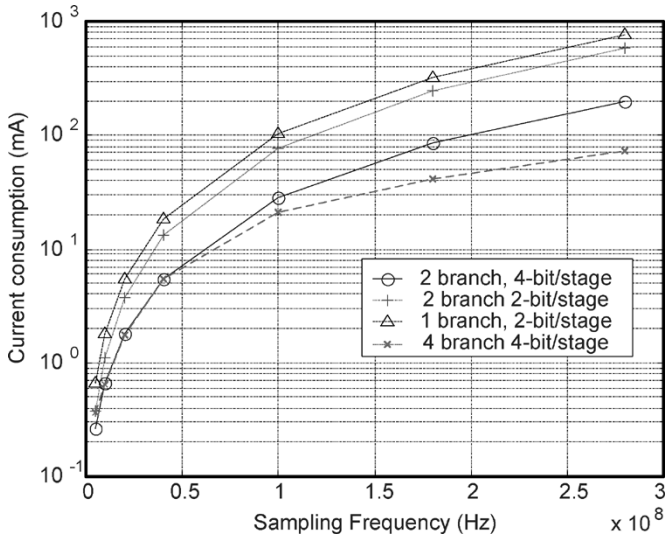


Fig. 6. Current consumption estimation of different pipeline ADC structures.

parameter and C_C is the value of the compensation capacitor. Hence, the requirement for I_1 can be derived as

$$I_1 = \left(\frac{(2^B+1)\cdot\ln\varepsilon_r}{MT_S}\right)^2\frac{16C_C^2}{K'}. \quad (3)$$

The total number of MDACs used in the 11-bit pipeline can be calculated as $11/(B-1)-1$. Therefore, the total current consumed in the MDACs, I_{MDACs}, can be derived as

$$I_{\mathrm{MDACs}} = \left(\frac{11}{B-1}-1\right)\cdot\left(\left(2^B C_U + \left(1-\frac{2}{2^B+1}\right)\cdot 2C_U\right)\times\frac{8V_{PP}}{MT_S} + \left(\frac{(2^B+1)\cdot\ln\varepsilon_r}{MT_S}\right)^2\frac{16C_C^2}{K'}\right). \quad (4)$$

Based on (4), the current consumption of several different ADC architectures is estimated as shown in Fig. 6. The proposed 2-branch 3/4-bit stage structure has the best power consumption performance for this particular application. Here 3 and 4 refer to the number of output bits in each stage, which includes 0.5 redundant bit for digital correction. In (4) it is assumed that all the stages use the same unit capacitor size. In the real implementation, the capacitor size can be scaled down in the LSB stages due to the loose *kT/C* and matching requirements. This even favors more the multi-bit stage pipeline structure because multi-bit MSB stages relax the requirements for the LSB stages and allow aggressive scaling of capacitors in the LSB stages. In the ADC branch design, the first 4-bit stages are loaded by lower

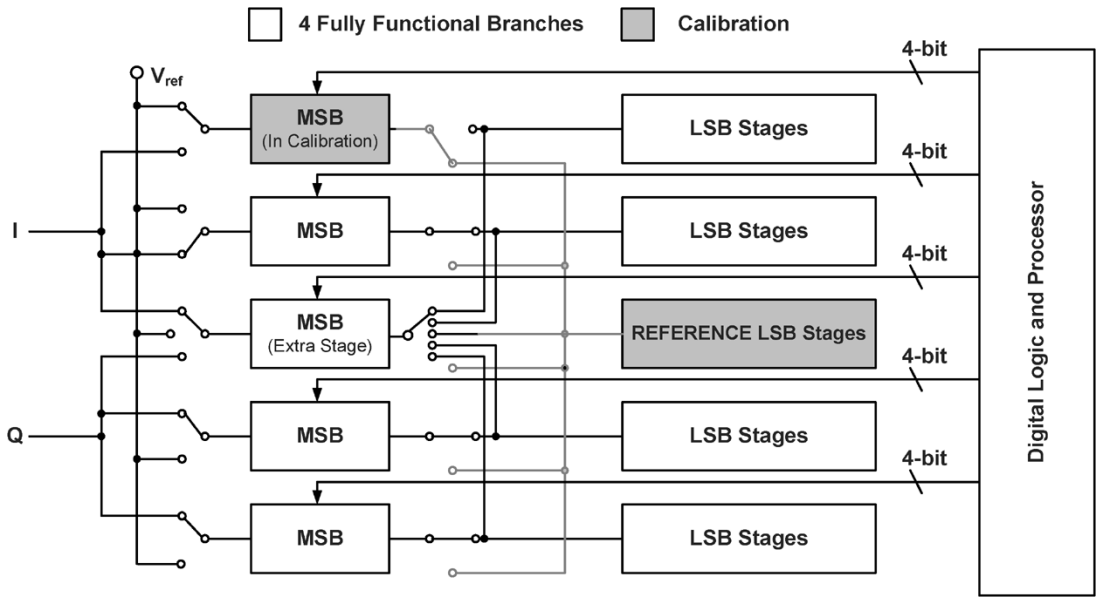


Fig. 7. On-line digital calibration mechanism.

bit (3-bit) stages to take advantage of the power saving without the disadvantage of the associated excessive load.

IV. Non-Idealities in a Time Interleaved Pipeline ADC and On-Line Digital Calibration

The proposed ADC faces the challenges of both, a time interleaved mechanism and a pipeline architecture. As a time-interleaved ADC, the mismatch among the ADC branches introduces offset error, gain error and timing skewing [6]. These nonidealities appear as tones at certain frequencies in the output spectrum and degrade the linearity of the ADC. Switched- capacitor techniques are adopted in this design. The mismatch among the capacitors contributes to the offset and gain error between the two ADC branches. An analysis through a Matlab macromodel shows that this 11-bit ADC can tolerate a maximum capacitor mismatch of 0.25%. A unit capacitor size of 200 fF is chosen to comply with this matching requirement under the given process characteristics and with a careful layout floorplan. The timing skewing is solved by using a front-end S&H circuit with an OpAmp sharing technique [12] as described in Section V.

The nonidealities in a pipeline ADC stage can be modeled as sub-ADC error, residue gain error, S&H offset and DAC nonlinearity. Since both the S&H and DAC functions are performed in the MDAC, the offset of each stage can be modeled together with the nonlinearity of the MDAC. The sub-ADC error is compensated by the digital correction in the pipeline ADC and hence is not a serious design concern. The residue is the difference between the input to the stage and the output of the sub-ADC, and it is detected and amplified by the MDAC so that it can be processed by the next stage. The residue gain error is a result of capacitor mismatch in the MDAC. As mentioned previously, the gain error requirement can be met by proper layout and selection of the capacitor size. The ADC linearity requirement in the 802.11b mode is 8-bit, careful layout for the MDAC in the first stage can yield better linearity than 8-bit in the current analog

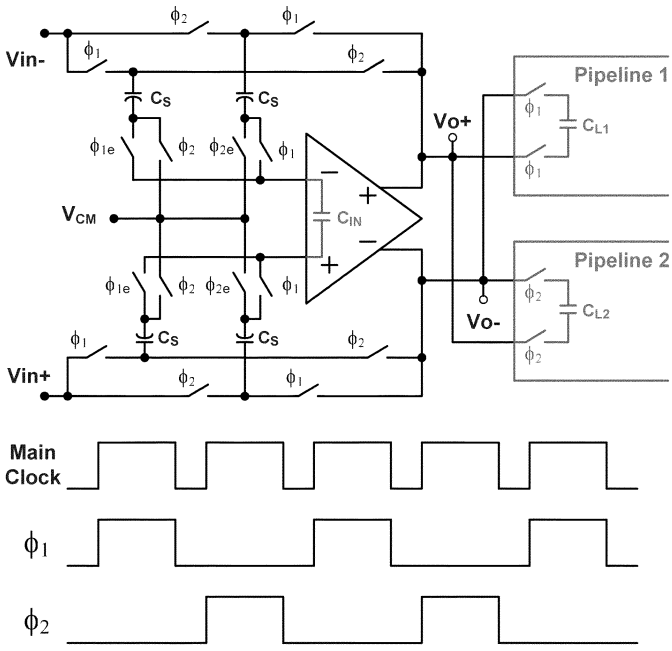


Fig. 8. Differential S&H with OpAmp sharing.

process. However, in the BT receiving mode, calibration is still needed in the first stage MDAC to guarantee the 11-bit linearity over process and temperature corners.

Fig. 7 depicts the online digital calibration scheme applied. The principle is to detect the error terms with respect to the first stage MDAC output and store them in digital domain during the calibration phase. In the normal operation phase, the error term is subtracted from the ADC output according to the first stage MDAC output. This common digital calibration scheme [13] requires no analog circuit and is simple in implementation. However, the calibration has to be performed offline, which is undesirable in a real-time receiver. In this design, the calibration

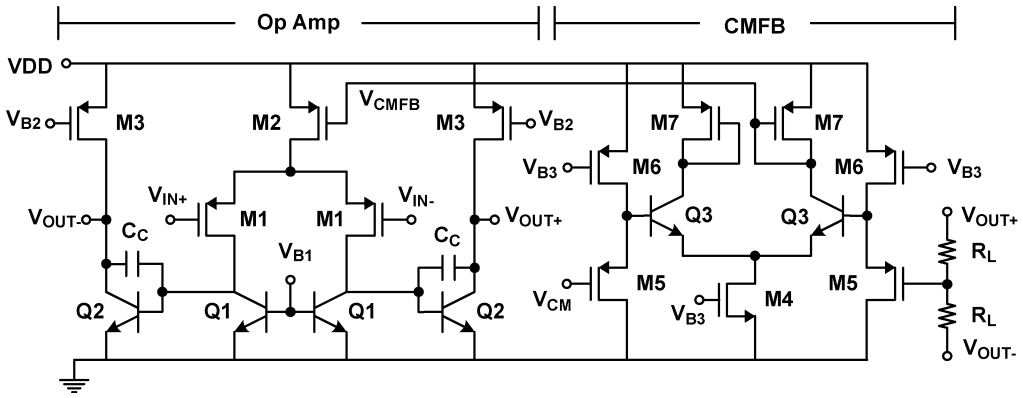


Fig. 9. BiCMOS OpAmp with CMFB circuit schematic.

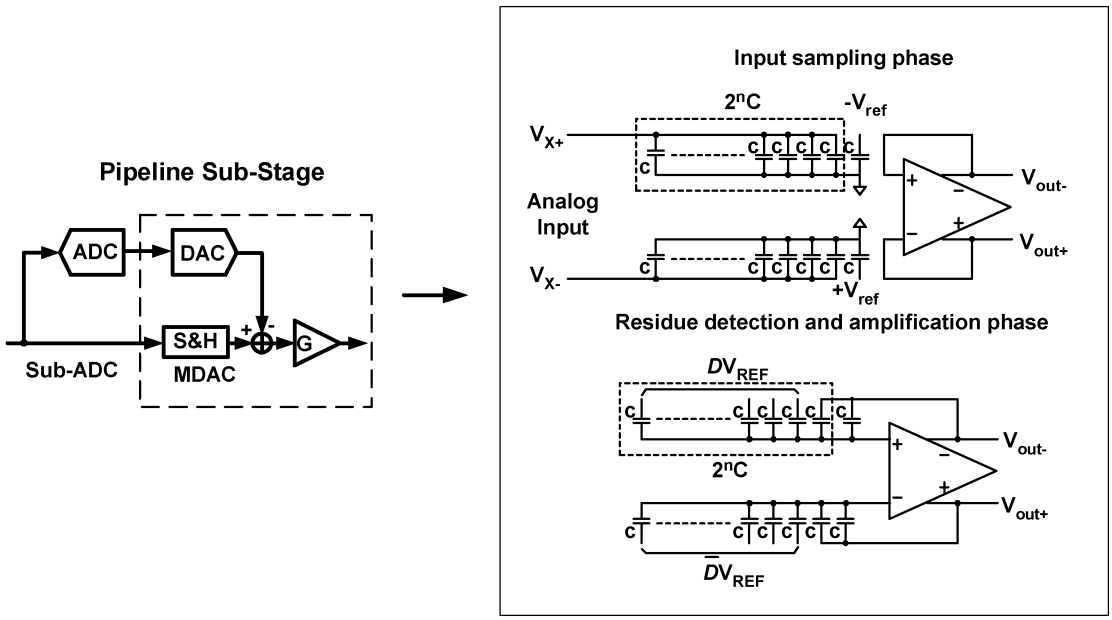


Fig. 10. MDAC schematic and operation mode.

is conducted online by adding an identical pipeline ADC branch to the existing four branches in the time-interleaved ADC. The first stage MDACs of all the five ADC branches are calibrated one by one in rotation with respect to the same LSB stages in the extra pipeline branch. When the first stage MDAC of any of the four pipeline branches in the time-interleaved ADC is under calibration, it is replaced by the first stage MDAC in the extra pipeline branch. Thus, at any time, there are always four fully functional pipeline branches available. This guarantees that both I/Q ADC channels are on all the time and makes the online calibration transparent to the rest of the receiver. Other online calibration schemes have been introduced before [14]. In this design, however, the process is improved by calibrating the first stage MDACs with respect to the same reference lower bits stages. All the first stage MDACs will therefore have identical performance after the calibration. Since the performance of the pipeline ADC branches is dominated by the MSB stage, this provides compensation to the mismatch between the branches. System wise, the mismatch between the I/Q channels is also alleviated through this scheme. The calibration is performed once every mille-second, which is a much lower speed compared to the normal operation speed of the time-interleaved ADC. In this way, the power consumption overhead is insignificant. As for the silicon area, there is a 20% increment due to the extra branch. Since the capacitor in the MDACs already occupies more than 50% of the total ADC area, employing larger capacitors for better matching may result in an even more significant area increment.

V. Circuit Implementation and Optimization

A. Sample-and-Hold (S&H)

The sample-and-hold (S&H) schematic and its clock diagram are shown in Fig. 8. The input samples are applied to the two parallel branches of the ADC in alternate clock phases (ϕ_1 and ϕ_2) using a single OpAmp. While convenient from the power consumption viewpoint, this configuration has the potential problem of introducing a correlation between consecutive samples [12]. Due to the finite gain of the OpAmp, a charge is injected every clock period in the parasitic capacitance C_{IN}, which is never reset. The output voltage then becomes a recursive function of the present and the previous sample.

The low-pass filtering effect of this phenomenon is minor and not harmful in this application. The associated nonlinearity, however, may degrade the SFDR of the ADC. To attain the 11 bits of resolution in the BT mode, the gain of the OpAmp in the S&H should be larger than 72 dB (2^{11+1}). If this gain is increased by another 6 dB, then the maximum error at the input of the OpAmp would be limited to LSB/4 and the correlation should be insignificant. Simulation results for the S&H with a gain of 75 dB in the OpAmp show a SFDR of 70 dB.

The circuit schematic of the proposed BiCMOS OpAmp for this ADC design is shown in Fig. 9. It is a two stage Miller compensated amplifier. pMOS transistors are used at the input to provide high input impedance and to allow employing NPN transistors for the next stage. The use of bipolar transistors results in a second stage with high transconductance and relatively low input capacitance. These features push the nondominant pole to high frequency and allow the optimization of the GBW and phase margin of the amplifier with respect to power consumption. Other BiCMOS OpAmps [15] have employed an emitter follower to drive the second stage to further increase the DC gain, which might be necessary in higher resolution ADC applications. In this design, the required gain (>75 dB) is achieved without an intermediate emitter follower. This reduces power consumption and provides additional voltage headroom for transistors M1 and M2. The simulated DC Gain, GBW and phase margin are 77 dB, 165 MHz and 67°.

The OpAmp core is the same for the amplifier in the S&H and the MDAC. For the later circuit, a SC CMFB is employed. Due to the clock arrangement, the use of a SC CMFB in the S&H would imply to sample the common mode voltage during the charging of one particular branch and to apply the correction during the charging of the other. In order to avoid any possible systematic error that this CMFB arrangement may cause, a continuous time CMFB is employed for the S&H OpAmp. Every time the S&H loads a sampled voltage into one of the MDAC capacitor banks, both, the common-mode and differential-mode voltages show a transient behavior. The pipeline stage that follows the S&H is fully differential and hence practically insensitive to common-mode errors. Nevertheless, in order to assure the overall stability, operating point, and gain of the S&H OpAmp it is desirable that its output settles in common mode as fast as in differential mode. This requires having similar GBW in both loops. In order to implement a relatively high DC gain (and therefore GBW) in the CMFB loop with low power consumption, a bipolar differential pair preceded by pMOS source followers is preferred over an nMOS pair.

B. Multiplying DAC (MDAC)

The MDAC is formed by an OpAmp and a capacitor bank. Fig. 10 describes its schematic and operation. To achieve better linearity, the capacitor bank in the MDAC uses thermometer control code. For the same random mismatch in the capacitor array, a thermometer code array and a binary array exhibit identical INL performance. However, the DNL is different. Given that the random process variation of each capacitor from its nominal value has a normal distribution of $\mathrm{N}(0,\sigma)$, the DNL of a thermometer code array is σ while the one of the binary code array is $\sigma\sqrt{2^N-1}$, where N is the number of the bits applied.

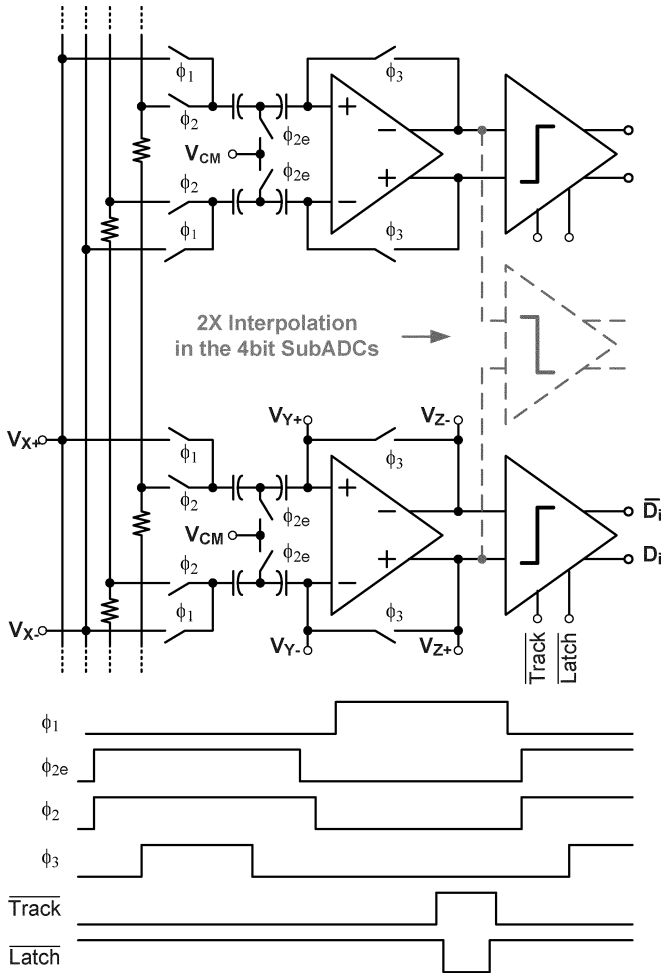


Fig. 11. Operation of preamp and comparator in the sub-ADC.

Therefore, the DNL of the thermometer code array is better by a factor of $\sqrt{2^N-1}$ [16]. Since the output of the sub-ADC is in the form of a thermometer code no encoder is needed between the sub-ADC and MDAC. As a result, any synchronization delay in the encoder is avoided.

C. Sub-ADCs

As shown in Fig. 4, each pipeline stage uses either a 3-bit or 4-bit sub-ADC. The 3-bit sub-ADCs employ a flash architecture with 6 preamps and 6 comparators. However, the last 3-bit stage is a full-flash ADC and uses 7 preamps and 7 comparators. The 4-bit sub-ADCs adopt a 2X flash interpolation structure using 14 comparators but only 8 preamps. Fig. 11 shows the block diagram and clock arrangement for the decision circuitry employed in the sub-ADCs as well as the interpolation arrangement in the 4-bit sub-ADCs. The decision circuit consists of a preamplifier and a latched comparator. The sampling circuit at the input of the preamp is designed to reduce offset and avoid loading the MDAC of the previous stage, thus significantly reducing the current consumed in capacitance charging. The transistor-level schematic of the preamp and comparator circuits is shown in Fig. 12. nMOS transistors are employed at the input of the preamp; they are operated in weak inversion to minimize both offset and bias current. The architecture of the comparator consists of input stage, a regenerative comparator, and an SR

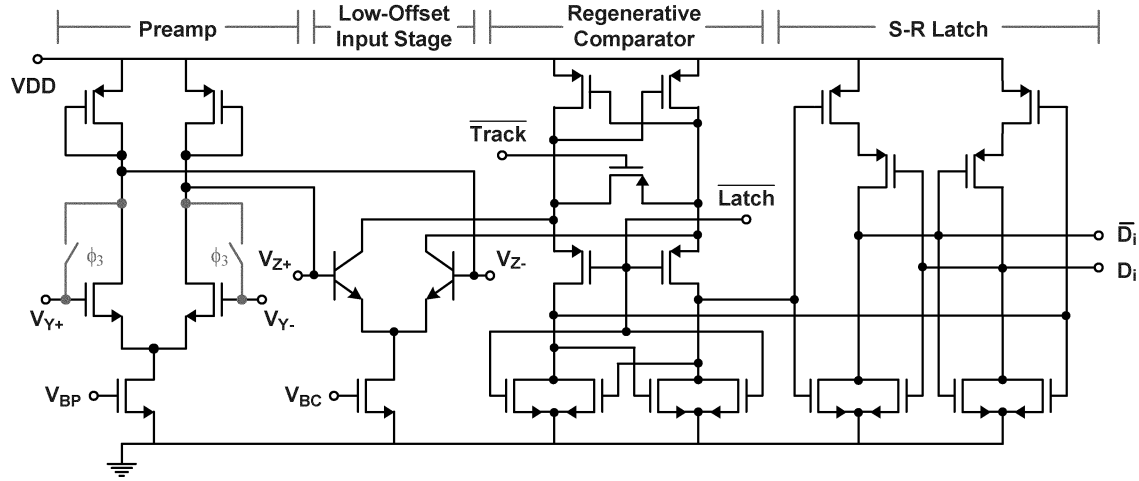


Fig. 12. Circuit schematic of preamp and comparator.

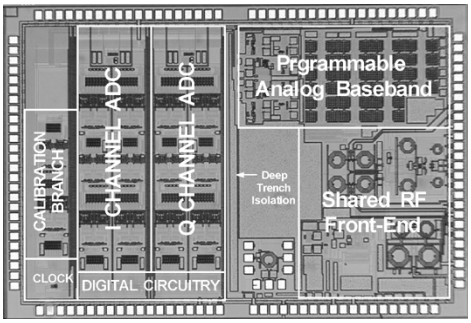


Fig. 13. Chip microphotograph of the 802.11b/Bluetooth dual-mode receiver.

latch [17]. Bipolar transistors are employed for the comparator to achieve the desired speed using minimum static current. The preamplifier improves the comparison sensitivity and reduces the negative effect of the kick-back noise.

VI. Measurement Results

The proposed time-interleaved pipeline ADC was fabricated along with the dual-mode receiver using 0.25 μm BiCMOS technology. Fig. 13 presents the chip microphotograph showing the ADCs for both I and Q channels, pads and the calibration circuit. The area for a single time-interleaved pipeline ADC is 2.1 mm^2.

In the test setup, 550 kHz and 5.5 MHz sinusoidal signals are applied to measure the ADC performance under the BT (11 MS/s) and 802.11b (44 MS/s) receiving modes, respectively. A 0 dB input power level corresponds to a 2.0 Vp-p sinusoidal signal. Fig. 14 shows the measured SNR in both receiving modes with respect to the input signal power. The ADC achieves a 60 dB SNR in the 802.11b mode without disabling the last 3 bit pipeline stage, and a 64 dB SNR in the BT mode. The effect of calibration scheme is tested in the DNL and INL measurement. Fig. 15(a) and Fig. 15(b) depict the DNL, INL of the ADC when the calibration is off and on, respectively. As it can be observed, the DNL improves from 1.34 LSB to 0.68 LSB; and INL improves from 1.14 LSB to 0.86 LSB. The ADC power consumption is 20.2 mW for the 801.11b mode and 14.8 mW for the BT mode. To place these results in perspective, it is worth to mention that the most recently

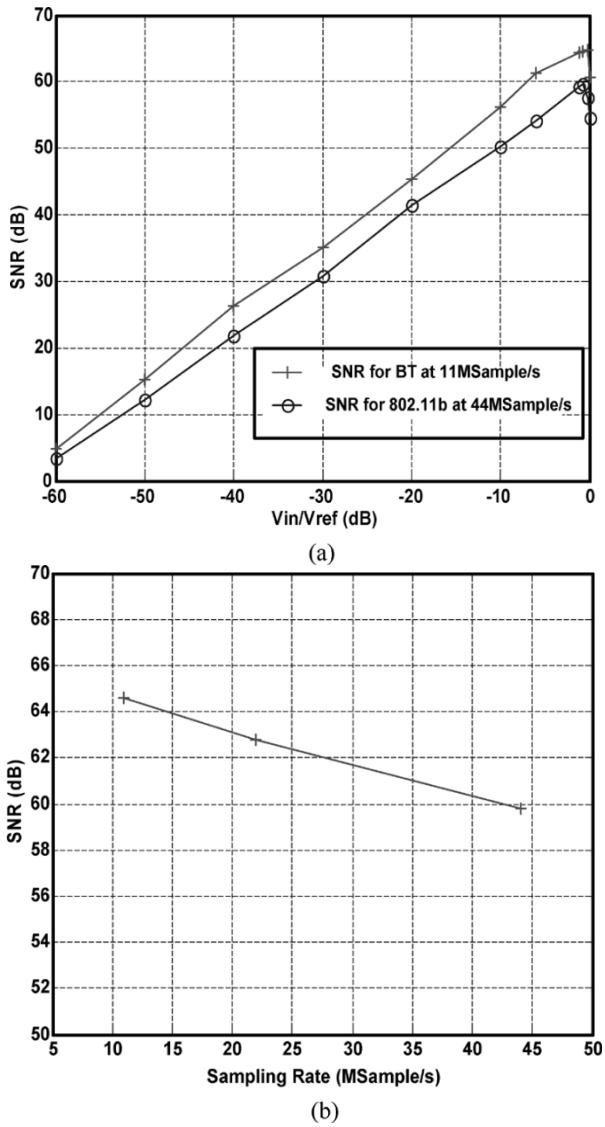
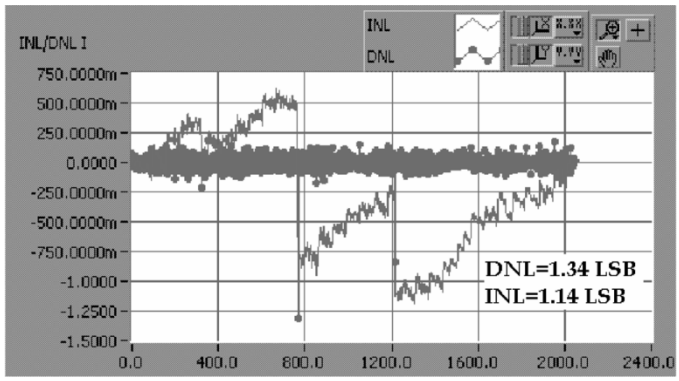
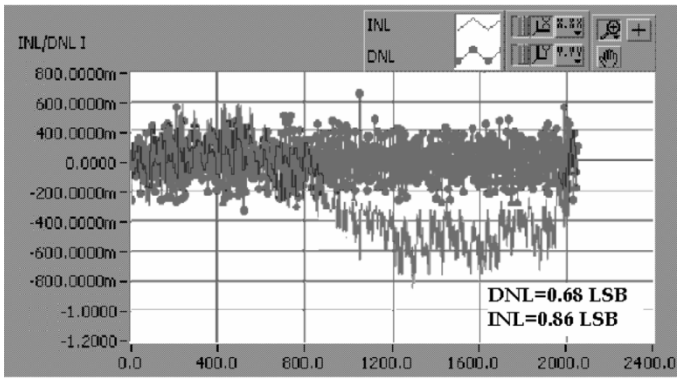


Fig. 14. Measured SNR under both receiving mode: (a) measured SNR of the ADC versus input signal power; (b) measured SNR of the ADC versus sampling rate.

reported pipeline ADC implementations with comparable performance (10 bit, 50 MS/s) using CMOS 0.18-μm technology



(a)



(b)

Fig. 15. Measured DNL and INL of the ADC, (a) without calibration, (b) with calibration.

TABLE II
ADC PERFORMANCE SUMMARY

Sample Rate	11 Ms/s	44 Ms/s
Signal Bandwidth	550 kHz	5.5 MHz
SNR	64 dB	60 dB
Current Consumption	5.9 mA	8.1 mA
Peak DNL @ 44Ms/s (Before/After Calibration)	1.34 / 0.68 LSB	
Peak INL @ 44Ms/s (Before/After Calibration)	1.14 / 0.86 LSB	
Supply Voltage	2.5V	
Process	0.25μm BiCMOS	
Total Area (I and Q channels) Including Pads	10.92mm^2	

have shown a power consumption of 29 mW [18] and 35 mW [19] occupying an area of 1.3 mm^2 and 1.2 mm^2, respectively. The performance of this ADC is summarized in Table II.

VII. CONCLUSION

A configurable time-interleaved pipeline ADC is proved to be an efficient ADC solution for the multi-mode wireless receivers that cover high data rate standards such as 802.11a/b/g. The proposed ADC has been demonstrated in an 802.11b/BT dual-mode receiver. The online digital calibration technique included in the implementation guarantees the conversion linearity without interrupting the receiver operation and adding insignificant power consumption overhead. Optimized circuit level design, the use of a BiCMOS process, and the time-interleaved architecture, yield low power dissipation and competitive area with respect to recently reported designs with comparable performance and technology [18], [19].

ACKNOWLEDGMENT

The authors thank the MOSIS service for the IC fabrication and the TI baseband group for technical discussions, as well as A. A. Emira, S. T. Moon, A. N. Mohieldin, A. Valero-Lopez, and C. Xin for their support.

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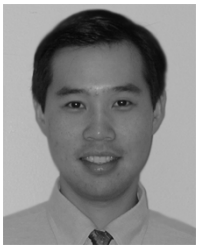

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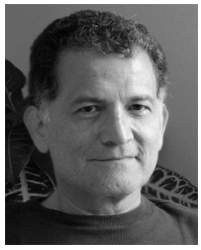

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