A Single Slope ADC With Row-Wise Noise Reduction Technique for CMOS Image Sensor

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***Abstract*— This paper presents a novel technique for single slope analog to digital converter (SSADC) to suppress the row-wise noise in CMOS image sensor. A sample switch is used in the current-steering DAC to reduce the noise introduced by bias circuits, which will deteriorate the characteristic of uniformity in the row direction. The sample switch can fix the voltage which biases the current source in the current-steering DAC when generating a ramp to avoid the ramp fluctuation in the time domain. The digital correlated double sampling is used to reduce the non-uniformity in column-level ADCs. The CMOS image sensor prototype is fabricated in 110nm 1P3M process. The 10-bit SSADC achieves DNL of −0.20 / +0.15 LSB and INL of −1.35 / +0.91 LSB at a sampling frequency of 29.2 KHz. It is proved that the row-wise noise is reduced from 764μV_{rms} to 163μV_{rms} at a frame rate of 228 fps using the proposed sample switch structure. The prototype photos taken by the sensor show that the row-wise noise is reduced under the low-illumination circumstance effectively.**

***Index Terms*— SSADC, CMOS image sensor, noise reduction.**

I. Introduction

CMOS image sensor is the crucial component in a visual system [1], which is widely used in mobile phones, safety-guard systems, and many other occasions. It is usually composed of pixel arrays, readout circuits and drive circuits [2]. The most important block in the readout circuits is analog-to-digital converters (ADCs), which are divided into pixel-level ADCs [3], column-level ADCs [4] and chip-level ADCs [5]. Among these architectures, the column-level ADCs are adopted in most cases because they can achieve appropriate tradeoff in readout speed and area. Single-slope ADC (SSADC) [6], successive-approximation-registers ADC (SAR ADC) [7] and cyclic ADC [8] are the most popular structures used in column-level ADC. The structure and operation process of SSADC are the simplest of the three ADCs above that contains a ramp generator, comparators and some digital circuits. By comparing the input voltage with a reference ramp voltage and then measuring the duration before the comparator toggles, the input voltage is transformed to digital numbers [9]. SSADC can achieve better uniformity compared with SAR ADC and cyclic ADC because all of the comparators share the same ramp reference voltage [10]. However, the offset among each comparator, the delay time of comparators' response and the delay time of counters' clock will deteriorate the uniformity and cause noise in output signals of the CMOS image sensor. In order to reduce these noises and non-ideal factors, the digital correlated double sampling (DCDS) technique is applied in most CMOS image sensors [11]. The error introduced by comparators will be recorded and removed during the process of quantifying the output of the pixel. Based on this technique, many other design and structures of SSADC were proposed to further improve the resolution, reduce the power consumption or suppress the noise. In [12], a new gain-adaptive column analog-to-digital converters to obtain input-referred dark random noise was proposed. The gain of slope can be adjusted according to the intensity of light signal to achieve low-noise readout. In [13], a double auto-zeroing scheme to address the high column fixed pattern noise (FPN) under bright illumination conditions was proposed. The auto-zeroing process was employed twice at reset and signal level respectively to suppress the column FPN. In [14], by operating the comparator with a bias current in the subthreshold region of 7.74–111 nA, it was successful to reduce the peak current when multiple ADCs triggering at one time. In combination with an ADC standby operation, the pixel-parallel ADC power consumption was reduced further. In [15], a column-parallel time stretcher was proposed. The time residue of the SSADC was expanded to 16 times and the conversion cycle of the SSADC was significantly reduced (only 80 cycles for 10-bit resolution). It used a lower clock frequency for column counters and reduced power significantly. In [16], a hybrid column-parallel time-to-digital-converter interpolated SSADC with a digital delay element feedback was proposed to solve the multiphase clock period matching problem in flash TDC-interpolation of SSADC without the use of a delay locked-loop. In [17], a low-noise CMOS image sensor based on a 14-bit two-step SSADC and a column self-calibration technique were proposed. It proposed an analog CDS structure which used a new 4-input comparator to deal with the difference in the slope ratio to achieve higher resolution of ADC. In [18], the proposed in-pixel comparing active pixel sensor used pixel transistors as a part of comparator for a SSADC instead of

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using them as a source follower (SF) to suppress nonlinearity, sensitivity degradation, and pixel readout noise.

Although it has been possible to deal with the noise and errors through CDS and DCDS introduced by readout circuits and pixel arrays in CMOS image sensors, there are still some kinds of noise can't be removed by these techniques, such as the noise caused by the bias source in CMOS image sensors. The bias source for the pixel array and readout circuits will induce row-wise noise in the image sensor. The noise will result in row stripes with different brightness appearing in imaging results, especially when imaging in the dark circumstance. In [19], the row temporal noise affected by voltage fluctuation of a pixel row select controlling voltage was decreased by adding a decoupling capacitor for that voltage. In [20], a novel readout architecture for CMOS image sensors based on switch biasing technique in order to reduce noisy pixel numbers induced by in-pixel source-follower transistor random telegraph signal noise was presented. There is another way to suppress the row-wise noise. Some reference dark pixels are arranged in every row of the pixel array and their average can be seen as the offset of each row. The row noise can be cancelled by subtracting the row offset from the output of imaging pixel outputs. In [21], the process of averaging and subtracting was completed in the digital domain and in [22] it was finished in the analog domain. But this method will make the size of pixel array larger and extend the row period of the image sensor. In this paper, a row-wise noise cancelling technique for SSADC combing with the DCDS technique is proposed.

The concept, design, and measurement results are presented as following sections. In section II, the architecture of CMOS image sensor and the proposed principle of noise-cancelling technique are described. In section III, the design of schematic including ramp generator, comparators and the low power design are discussed. In section IV, the experiment results and conclusions are demonstrated. Finally, in section V the conclusion is presented.

II. Proposed Technique

A typical architecture of CMOS image sensor with column-parallel SSADCs is shown in Fig. 1. It is consisted of a 4T active pixel array, a ramp generator formed by a current-steering digital-to-analog converter (DAC), column-parallel SSADCs, biased circuits, control circuits and readout interfaces. The ramp generator provides a column-shared ramp voltage for all of the column-parallel SSADCs. The key circuits of SSADC is a comparator which will be described in section Ø. All of the circuits are biased by a proportional to absolute temperature (PTAT) circuit.

A. Readout Circuits

The column-level schematic in CMOS image sensor and the timing diagram of DCDS is shown in Fig. 2. Initially, the signal RST are applied to charge the capacitance C_{FD}. The source-follower transistor will provide the potential of V_{rst} after the voltage of C_{FD} is steady. Then by comparing the ramp voltage V_{ramp} and the V_{rst}, the counter of SSADC

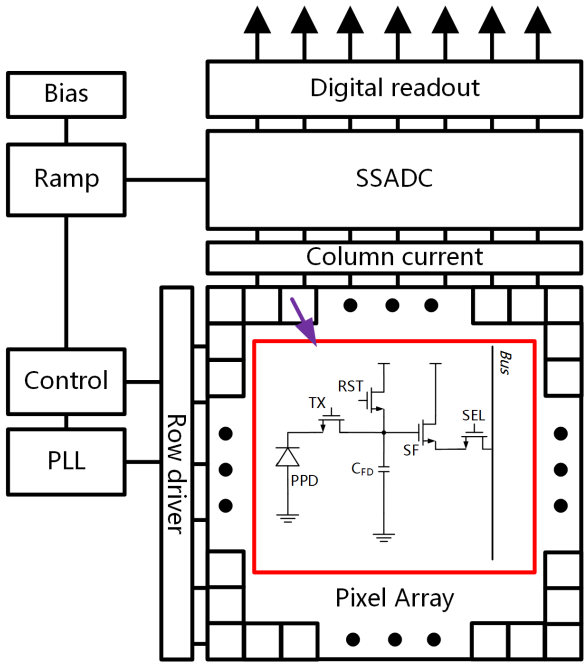


Fig. 1. A typical architecture of CMOS image sensor with column-parallel SSADCs.

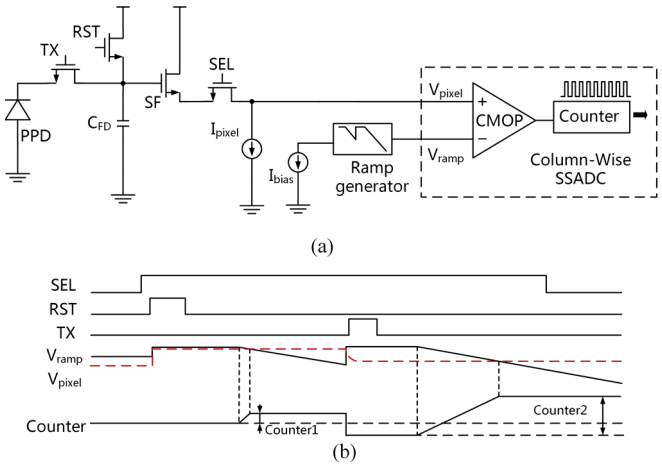


Fig. 2. The column readout schematic and timing diagram (a) the schematic of the column-level SSADC (b) the timing diagram of DCDS.

counts forward from 0 LSB to quantify the error voltage introduced by some non-ideal factors, such as the offset, response delay and charge injection of comparators and the time delay of the clock. The output of counter would be latched to *Counter*1 when the ramp reference voltage is equal to the error voltage:

$$Counter1 = \frac{V_{\mathrm{error}}}{T_{\mathrm{counter}} \cdot S} \tag{1}$$

where V_{error} is the error voltage introduced by non-ideal factors, S is the slope of the ramp (i.e., the speed of voltage falling down) and T_{counter} is the clock period of the counter.

Then the signal TX is applied to transfer the photo-generated electrons from PPD to C_{FD} after quantifying the V_{error}. At this time each bit of counter will invert to set the counter's value at the opposite value of *Counter*1.

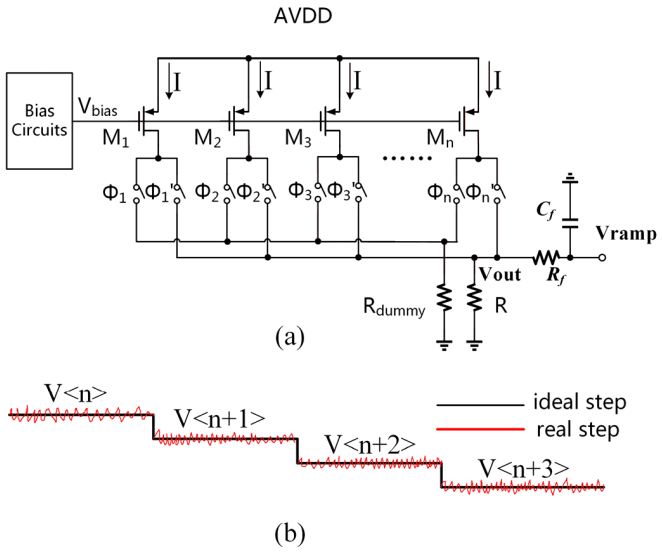


Fig. 3. A typical current-steering DAC (a) architecture (b) ramp diagram.

The voltage on C_{FD} will gradually descend because of electrons transference. The voltage of pixel will fall down by V_{rst}-V_{signal} and the counter of SSADCs will count forward to quantify it through

$$Counter2 = \frac{V_{error} + V_{rst} - V_{signal}}{T_{counter} \cdot S} \tag{2}$$

where $V_{rst} - V_{signal}$ is the voltage generated by photo-generated electrons. The final output is

$$Counter2 - Counter1 = \frac{V_{rst} - V_{signal}}{T_{counter} \cdot S} \tag{3}$$

which completes the correlated double sampling process to remove the noise caused by offset and charge injection of comparators and delay time of SSADC's clock.

B. The Structure of DAC and Row-Wise Noise Reduction Technique

A current-steering DAC is chosen as the ramp generator due to its high performance in speed of changing states. Fig. 3(a) demonstrates the conventional structure of current-steering DAC. By changing the number n and magnitude I of current source applying to the resistor R, a ramp voltage formed by different number of IR is generated. R_{dummy} is used to maintain the total current a constant in case of voltage drop caused by parasitic resistor. R_f and C_f are used to filter the voltage steps to a ramp. But this kind of structure would induce a random noise from bias circuits that can't be removed by DCDS as

$$V_n^2 = 4kT\left(\frac{2}{3} \cdot \frac{1}{g_{m0}}\right) + \frac{K}{C_{ox} W L} \cdot \frac{1}{f} \tag{4}$$

where k is Boltzmann constant, g_{m0} is the transconductance of the biased transistor in bias circuits, K is the process-dependent constant and f is the operation frequency. The noise seen from the current source is

$$I_n^2 = g_{m1}^2 \cdot \left[4kT\left(\frac{2}{3} \cdot \frac{1}{g_{m0}}\right) + \frac{K}{C_{ox} W L} \cdot \frac{1}{f}\right] \tag{5}$$

where g_{m1} is the transconductance of the current source. The noise current will apply to resistor R and make every step of ramp deviate from the ideal value, as shown in Fig. 3(b). The root-mean-square magnitude of noise appeared in slope is

$$\overline{V_{n,out^2}} = M \cdot \int_0^\infty I_n^2 R^2 \frac{1}{1 + 4\pi^2 R_f^2 C_f^2 f^2} df = M \cdot \overline{v_{noise,rms}^2} \tag{6}$$

where M is the number of current sources applied to resistor R and $v_{noise,rms}$ is the Root-Mean-Square (RMS) noise of one current source caused by the bias circuits. This noise will cause the random fluctuation on every step of the ramp as shown in Fig. 3 (b) and result in a random error on *Counter*1 and *Counter*2 respectively. So, the equation (1) and equation (2) would be corrected as:

$$Counter1 = \frac{V_{error} + v_{n1,rms}}{T_{counter} \cdot S} \tag{7}$$

$$Counter2 = \frac{V_{error} + V_{rst} - V_{sig} + v_{n2,rms}}{T_{counter} \cdot S} \tag{8}$$

where $v_{n1,rms}$ and $v_{n2,rms}$ are the RMS noise caused by bias circuits when quantifying V_{error} and $V_{rst} - V_{sig}$ respectively and

$$v_{n1,rms} = \sqrt{M} \cdot v_{noise,rms} \tag{9}$$

$$v_{n2,rms} = \sqrt{N} \cdot v_{noise,rms} \tag{10}$$

where M is the number of the current sources of the ramp when converting the V_{error} and N is the number of the current sources of the ramp when converting the V_{rst}-V_{sig}. Because the noise introduced by bias circuits is random, $v_{n1,rms}$ and $v_{n2,rms}$ is uncorrelated. After the DCDS, the total RMS noise caused by bias circuits can be described as:

$$v_{ntot1,rms} = \sqrt{\overline{v_{n1,rms^2}} + \overline{v_{n2,rms}^2}} = \sqrt{M + N} \cdot v_{noise,rms} \tag{11}$$

So the final output would be

$$Counter2 - Counter1 = \frac{V_{rst} - V_{sig} + v_{ntot1,rms}}{T_{counter} \cdot S} \tag{12}$$

Because one row of the comparators is utilizing a ramp as the input reference voltage in every row period, $v_{ntot1,rms}$ will infect all the output of comparators in a row. The worse thing is that $v_{ntot1,rms}$ is random so the influence caused by $v_{ntot1,rms}$ is different in different rows. Therefore, a row non-uniformity will be introduced and some horizontal stripes will appear in the sampled image, especially when imaging at the low-illumination circumstance.

In order to suppress the noise caused by bias circuits, we proposed a novel structure of current-steering DAC as shown in Fig. 4 (a). A sample switch Φ_{sample} is implemented between the bias circuits and the current source. During the period that the reset signal RST is applying, the sample switch is turned on first to make the current source biased on the proper operating points. At the same time, the output voltage will be mixed with noise caused by the biased circuits. Then the sample switch will be cut off. The bias voltage and the noise will be sampled and fixed on the sample capacitor like an error v_{error} and all of the current sources have the same error. The two ramps converting V_{error} and V_{rst}-V_{sig} respectively have

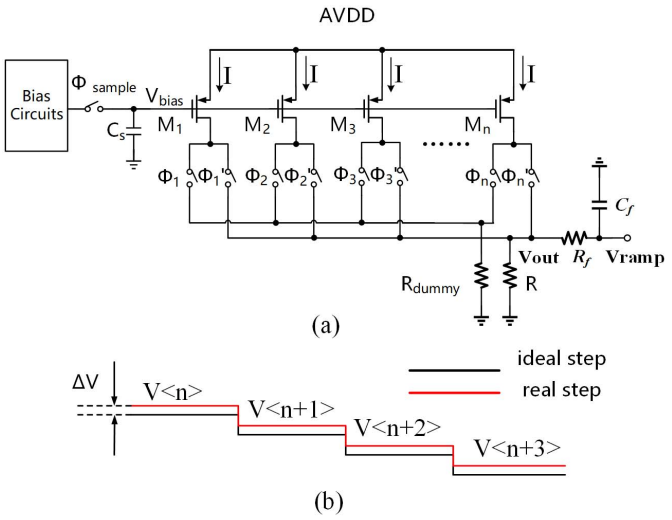


Fig. 4. The proposed current-steering DAC (a) architecture (b) ramp diagram.

the same error in every step of the ramp. So the RMS noise caused by the bias circuits when converting V_{error} is

$$v_{\text{n1}} = M \cdot v_{\text{error}} \tag{13}$$

And the RMS noise caused by the bias circuits when converting V_{rst}-V_{sig} is

$$v_{\text{n2}} = N \cdot v_{\text{error}} \tag{14}$$

So the RMS noise caused by the bias circuits of the ramp is

$$v_{\text{ntot2,rms}} = \sqrt{M - N} \cdot v_{\text{noise,rms}} \tag{15}$$

The diagram of the ramp voltage after sampling is shown in Fig. 4(b). Under the low-illumination condition, this operation ensures that v_{n1} and v_{n2} is close and $v_{\text{ntot2,rms}}$ is much smaller than $v_{\text{ntot1,rms}}$. The final output is

$$Counter2 - Counter1 = \frac{V_{\text{rst}} - V_{\text{signal}} + V_{\text{ntot2,rms}}}{T_{\text{counter}} \cdot S} \tag{16}$$

Therefore, the noise introduced by the bias circuits of the ramp is reduced significantly at low-illumination condition. If the illumination is high, this noise will become larger. However, at this condition the shot noise of the photons will be much larger, so the shot noise will be the dominant noise source. The effect of the row-wise noise reduction proposed in this manuscript become not obvious. So the analysis of the row-wise noise cancelling technique proposed in this manuscript is appropriate for the low–illumination condition.

III. Circuit Implementation

A. Current-Steering DAC

A structure of current-steering DAC described in section II is shown in Fig. 5. A cascode current mirror composed of PMOS is used for the current source because of its high output impedance. Besides, the common-gate transistor can prevent the current from being influenced by the fluctuation of the drain potential of itself when inverting the status of switch so as to reduce some non-ideal factors such as clock feedthrough affecting the magnitude of current source.

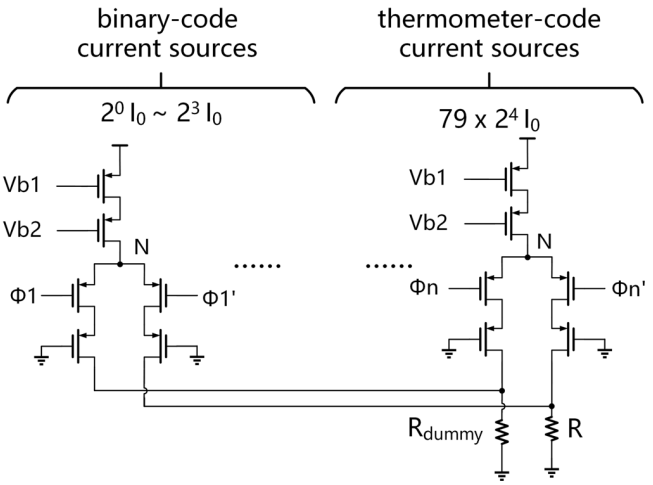


Fig. 5. A structure of current source.

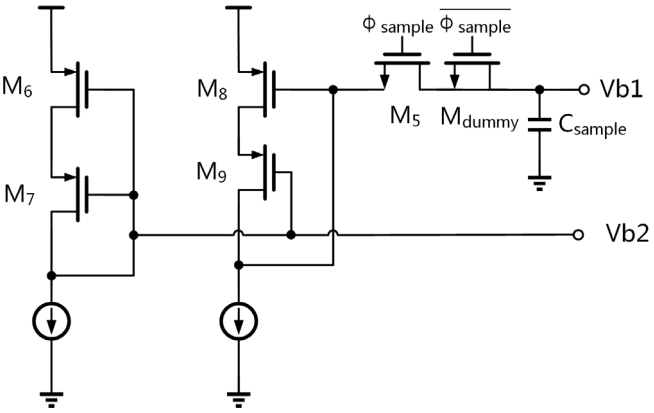


Fig. 6. Bias circuits of current source.

A cascode structure is also used for the switch circuits. Φ_{n} and Φ_{n}' are a pair of inverse signals provided by a latch that will be described in the following. At least one of them should be at low potential to make sure one side of the switch circuits is turned on. Otherwise the node N will be charged and produce a spike to deteriorate the DNL at the moment of switching. The common-gate transistors between the switch transistor and the resistor, operating in saturation region by connecting their gates to ground, protect the output nodes from being affected by clock feedthrough when Φ_{n} and Φ_{n}' changing their status.

In our design, the resolution of DAC is 11 bits in consideration of DCDS operation of 10-bit SSADC. We arranged 256 LSB redundant codes, and thus the input range of DAC is 0-1279LSB. In order to make a tradeoff among the circuits area, DNL and INL, the hybrid-code DAC is chosen for our design: the binary-code DAC is used for the low 4 bits and the thermometer-code DAC is used for the high 7 bits.

B. Bias Circuit for Current Source

The circuit that is used to maintain the bias point of current source is shown in Fig. 6. A switched-capacitor structure on the branch of output Vb1 is used. The Φ_{sample} is on when the V_{rst} is valid to charge the capacitor C_{sample}. Then the Φ_{sample}

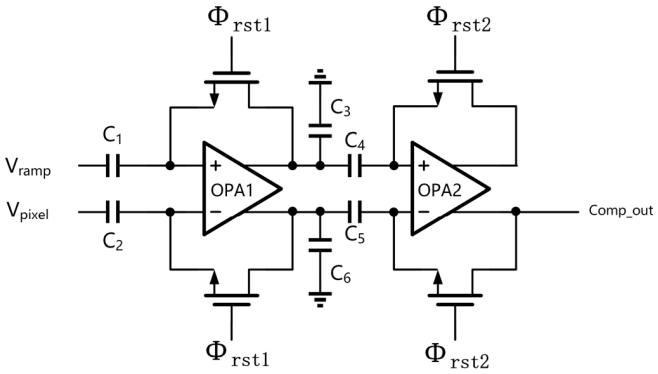


Fig. 7. The structure of two-stage comparator.

TABLE I
SIMULATION RESULTS OF OPA1 AND OPA2

ITEM	OPA1	OPA2
Gain	40.67dB	40.41dB
3dB bandwidth	990.38KHz	1.098MHz
Total current	7.4μA	1.6μA
Total rms noise	55.4μV	

will be cut off during the rest time of quantification period to ensure the voltage Vb1 is a constant. Even if there are some noise mixed into the output voltage, the noise from the bias circuit will be removed coordinating with DCDS. Vb2 can omit the switch-capacitor structure because the current noise caused by fluctuation of Vb2 is weak enough to be ignored. To suppress the effect of charge injection caused by M5, there is a dummy NMOS transistor whose drain and source are both connected to C_{sample} to compensate the charge injection.

C. Comparator

In order to implement a comparator with high gain, the two-stage OPA is chosen as shown in Fig. 7. The gain of each stage of the comparator should be greater than 30dB to ensure the resolution of the ADC reaches 10 bits. In the structure of the two-stage comparator, the noise of the second-stage comparator contributes very little to the input reference noise, so the bias current of the second-stage comparator can be relatively small. The noise of the first-stage comparator is the main source of noise, so the bias current of the first-stage comparator needs to be relatively large. In order to ensure that the response delay of the comparator is not too long, the 3dB bandwidth is set to around 1MHz. Before quantifying V_{error}, Φ_{rst1} and Φ_{rst2} are in high potential to charge the capacitor C_1, C_2, C_4 and C_5. Then Φ_{rst1} and Φ_{rst2} will be shut down in sequence to suppress the influence of charge injection and keep their states until the end of the current row period. C_3 and C_6 are load capacitors.

The structures of OPA1 and OPA2 and their simulation results are shown in Fig. 8 and Table I respectively.

D. Current Source Latch and Stable Switch Signal Design

Through the analysis in the section III (a), one of the branches of the switch circuits should be turned on to get rid of current spike appearing at the output nodes. Because PMOS transistors are served as the switches, the reversed control signal Φ_n and Φ_n' should cross at a lower voltage when they are inverting. Fig. 9 shows the circuit that can ensure the switch signal Φ_n and Φ_n' intersect at a low voltage by make the W/L of M2 and M6 much larger than that of M1 and M5. So the falling speed of Φ_n and Φ'_n is faster than the rising speed of Φ_n and Φ'_n. M3 and M4 are used to form a positive feedback to speed up the rising of both Φ_n and Φ'_n to prevent their rising speed from being too slow.

All of the current units in current-steering DAC are needed to be driven by clock because every unit is equipped with a latch. In order to enhance the drive ability of clock, the clock tree is used to ensure that they can drive the current unit. However, the clock tree would induce extra capacitor in nodes that will increase the dynamic power consumption. And the huge instant current will cause the IR drop problem in the power line and thus lead to the decrease of the current in the unit of the DAC. It will produce some spikes at the nodes of output. Besides, the toggle of CLK in Fig. 9 will couple to $V_{\text{switch\_n}}$ and $V_{\text{switch\_p}}$ and lead to some spikes in Φ_n and Φ_n'. These spikes will cause some current sources in the Fig. 5 wrongly apply to resistor R and lead fluctuations at the output nodes.

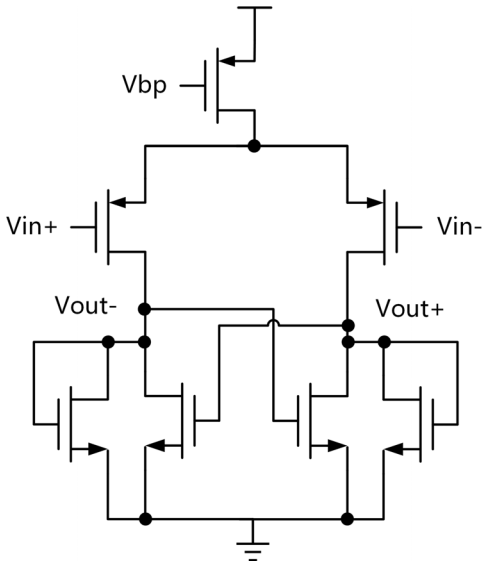


Fig. 8. Schematic of OPA1 and OPA2.

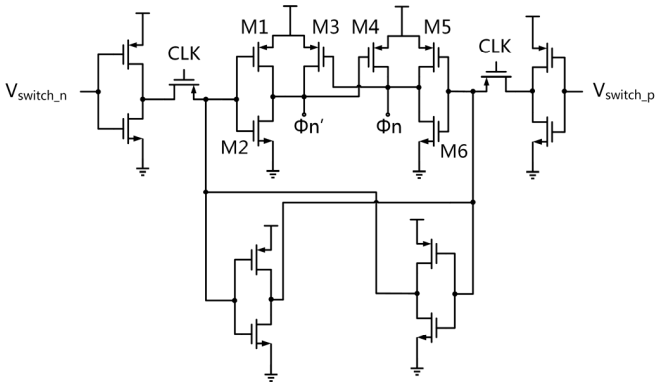


Fig. 9. The structure of current latch.

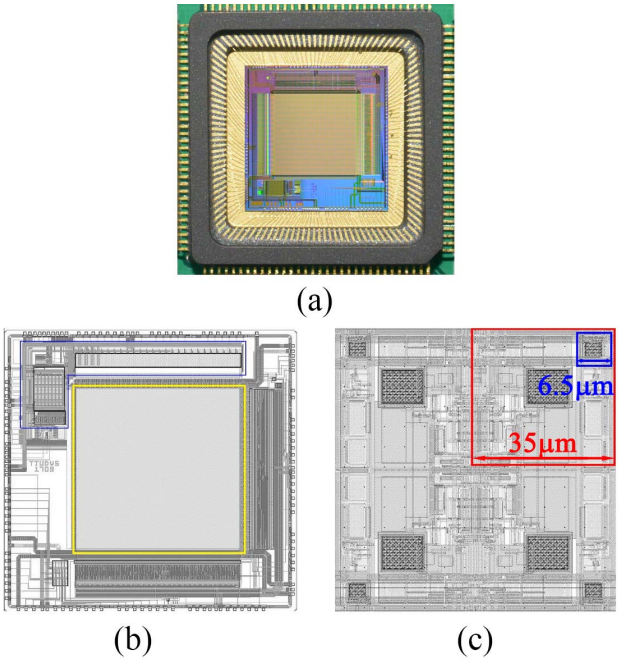


Fig. 10. The photograph of the CMOS image sensor (a) chip with package (b) chip layout (c) pixel layout.

In order to save the power consumption and reduce the spikes at the output nodes, a stable switch signal design is proposed. For the thermometer-code current sources, every unit only inverts one time when generating a ramp. So, the clocks of thermometer-code current latches are enabled in the period of switching. At the rest of time, they are latched to "0". The spikes at the output nodes can be removed and the dynamic power consumption is reduced compared with the clock of thermometer code enabled all the time.

IV. Experiment Results

A 128 × 128 image sensor prototype is fabricated in 110nm 1P3M process. Fig. 10(a) shows a die photograph of the implemented image sensor prototype with 128-pin package. The size of the active pixel is 6.5μm×6.5μm and the width of the column-level readout circuits is 6.5μm. Fig. 10(b) shows the layout of the image sensor. The yellow box is the pixel array and the blue box is the readout circuits used in this manuscript. Fig. 10(c) shows that the pixel with an active size of 6.5μm×6.5μm is placed with an average distance of 35μm. The space between columns of pixels or readout circuits is 35μm because there are some irrelevant circuits for other purpose in this chip. Therefore, with this special arrangement of pixels, the area of the whole chip reaches 8000μm(H) × 7900μm(V).

A. ADC Characteristics

The experiment results of DNL and INL at a sampling frequency f_s of 29.2 KHz are shown in Fig. 11. The frequency of input signal for the test of characteristics of ADC can be set at a lower level because the SSADC in CMOS image sensors mainly operates at low frequency when quantifying V_{error} and V_{rst}-V_{sig}. A sinusoidal signal with frequency

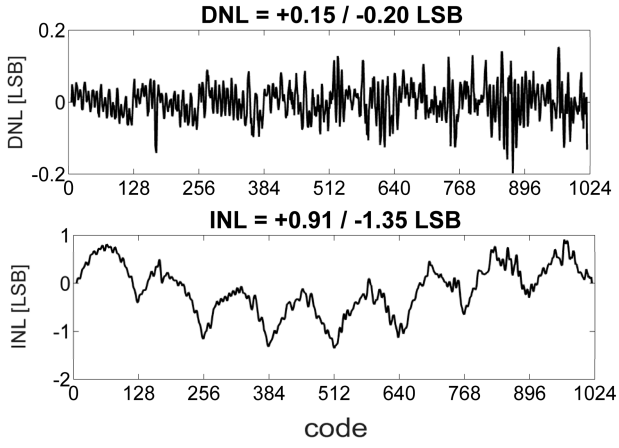


Fig. 11. DNL and INL of ADC.

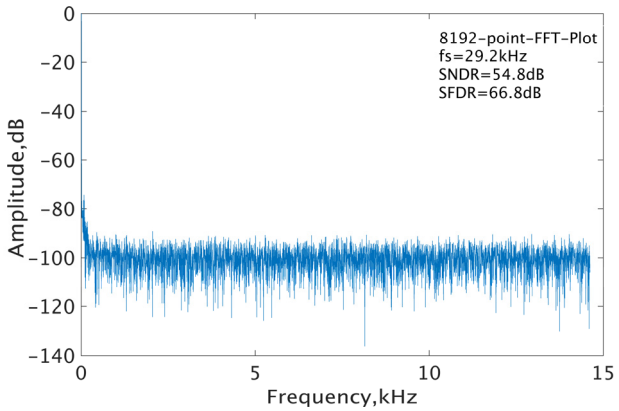


Fig. 12. Spectrum analysis with FFT.

of 0.05 Hz and $V_{peak-to-peak}$ of 1.3V is used as the input of ADC to measure its static characteristics. The 10-bit ADC achieves DNL of −0.20 / +0.15 LSB and the INL of −1.35 / +0.91 LSB after the DCDS operation.

To test the dynamic characteristics of the ADC, a sinusoidal signal with frequency of 3.57Hz and $V_{peak-to-peak}$ of 1.3V is used as the input signal. 8192 points of output data are sampled and then transformed to frequency domain by Fourier Transformation. Fig. 12 shows the result of Fast Fourier Transformation for the sampled points. The ADC achieves the SNR of 55.5 dB, THD of −63.2 dB, SNDR of 54.8 dB, SFDR of 66.8 dB and ENOB of 8.8bits. TABLE II summarizes the characteristics of the ADC.

B. The Light Response of CMOS Image Sensor

In order to test the light response of the image sensor, Gamma Scientific RS5 is used as the light source and the light intensity illuminating to the chip gradually increased from 0 lux when the exposure time are set to 205.2μs to prevent the light response from saturating too early. Fig. 13(a) shows the relationship between output numbers of the chip and the intensity of illumination. The noise at a certain light intensity is decided by the standard deviation of output of every pixel. Fig. 13(b) shows the measurement results of standard deviation at different light intensity. The curve falls down suddenly

TABLE II
ADC CHARACTERISTICS

Resolution	10-bit
Dynamic range	0-1V
*Sample frequency	29.2KHz
DNL	-0.20 / +0.15 LSB
INL	-1.35 / +0.91 LSB
SNR	55.5 dB
THD	-63.2 dB
SNDR	54.8 dB
SFDR	66.8 dB
ENOB	8.8 bits
Power(1 column)	56μW
**FOM1	4.3pJ/step

*Sample frequency=1/(1-row time)

** FOM1=P / $\{f_s \times 2^{\text{ENOB}}\}$

TABLE III
SUMMARIZES OF THE IMAGE SENSOR CHARACTERISTICS

Array format	128(V)×128(H)
Pixel pitch	6.5μm×6.5μm
Frame rate	228fps
ADC pitch	6.5μm
Sensitivity	9.536V/lux·s
Max SNR	49.2dB
Dynamic range	68.9dB
Dark current	0.016V/s
Power supply	3.3V(analog) / 1.5V(digital)
Power consumption	40mW

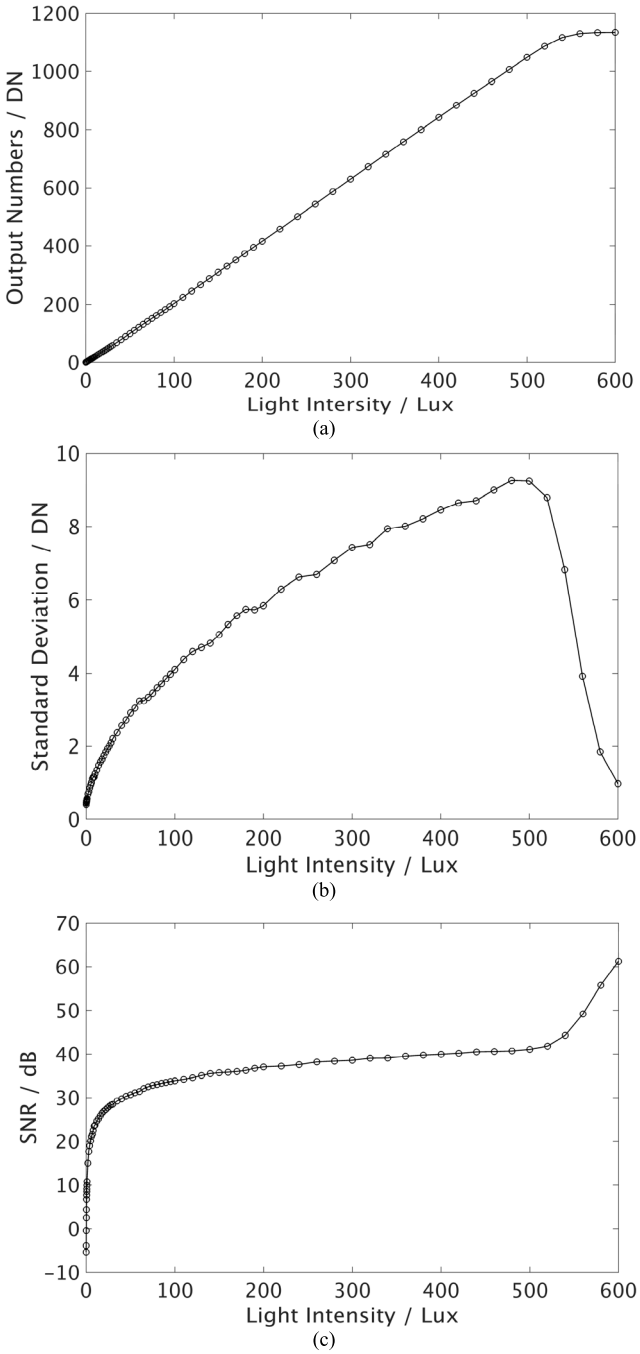


Fig. 13. The response of light incident (a) output numbers (b) noise (c) SNR.

at around 560lux because the output numbers have achieved the maximum value. The signal-to-noise ratio (SNR) can be calculated by divided output numbers from their standard deviation. Fig. 13(c) shows the variation trend of SNR when the light intensity is increasing. Table III presents the main characteristics of the CMOS image sensor.

C. Row-Wise Noise Reduction

In the analysis of section II, the sample switch implemented in DAC can reduce the row-wise noise effectively. In order to figure out the exact row-wise noise in CMOS image sensor, a $128 \times 128 \times P$ matrix is formed by the data of P frames. The FPN is removed by subtracting the matrix of first frame:

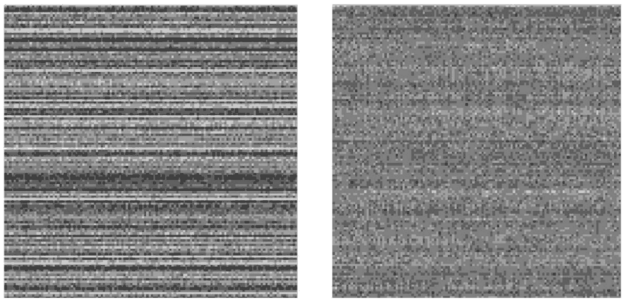
$$X_{i,j,k(1\le k\le P-1)} = D_{i,j,k(1<k\le P)} - D_{i,j,1} \tag{17}$$

where $D_{i,j,k}$ is the data in the row of i, column of j and frame of k. Then the column random noise is removed by the average operation:

$$A_{i,k} = \frac{\sum_{j=1}^{128} X_{i,j,k}}{128} \tag{18}$$

Next the standard deviation of $A_{i,k}$ in different frames represents the fluctuation of output digital numbers caused by bias circuits of DAC:

$$DN_{\text{row}} = \frac{1}{128 \times (P-1)} \sqrt{\sum_{k=1}^{P-1} \sum_{i=1}^{128} (A_{i,k} - \overline{A_m})^2} \tag{19}$$



(a) (b)

Fig. 14. Sample images captured in 0 lux (a) sample switch disabled in 25.5x digital gain (b) sample switch enabled in 25.5x digital gain.

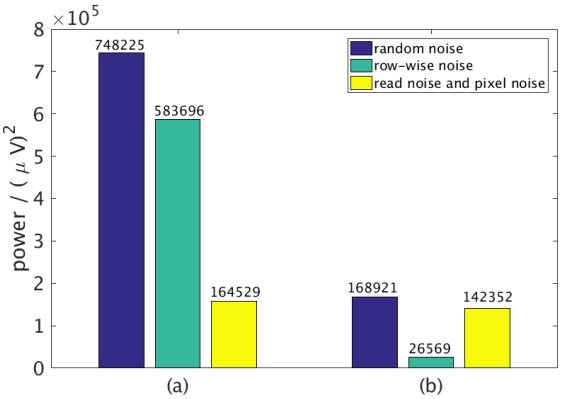


Fig. 15. The proportion of power between read noise and row-wise noise (a) sample switch disabled (b) sample switch enabled.

where

$$\overline{A_m} = \frac{\sum_{k=1}^{P-1}\sum_{i=1}^{128} A_{i,k}}{128 \times (P-1)} \tag{20}$$

Because in equation (17) the variance of $D_{i,j,k}$ is multiplied, the row-wise noise caused by bias circuits of DAC is

$$\overline{V_{\text{row-wise noise}}} = DN_{\text{row}}/\sqrt{2} \tag{21}$$

Fig. 14(a) and (b) show the pictures taken in a low-illumination circumstance when the sample switch is disabled and enabled respectively. The exposure time are set to 205.2μs to keep the test environment same to that when measuring the light response. The output data are multiplied by an integer Z to display the row-wise noise. Fig. 14(a) and (b) show the pictures that only display the grayscale from 0 to 10 that is equivalent to increasing the digital gain by 25.5 times after removing the FPN. The horizontal stripes in the left picture are more obvious because of influence by row-wise noise. The right picture proves that the switches can reduce the row-wise noise come from bias source effectively. The row-wise noise is suppressed from 764μV_{rms} to 163μV_{rms}.

Because the row-wise noise is suppressed by the operating of sample switch, the random noise, composed of read noise, row-wise noise and pixel noise, is also suppressed. The relationship among them can be described as

$$\overline{V_{\text{n,random}}} = \sqrt{\overline{V_{\text{n,read}}^2} + \overline{V_{\text{n,row}}^2} + \overline{V_{\text{n,pixel}}^2}} \tag{22}$$

TABLE IV

THE TEST RESULTS OF SENSOR'S NOISE

Sample switch	Disable	Enable
Row-wise noise	$\overline{764^2}$ μV_{rms}	$\overline{163^2}$ μV_{rms}
Random noise	$\overline{865^2}$ μV_{rms}	$\overline{411^2}$ μV_{rms}
Proportion	78.0%	15.7%

TABLE V

COMPARISON TABLE

	[13]	[14]	[16]	**This work**
Process	40nm	90nm CIS 65nm CMOS	130nm	**110nm**
Array size	-	1632(H)× 896(V)	1024(H)× 128(V)	**128(H)× 128(V)**
Pixel pitch	5.4μm	6.9μm	5.6μm	**6.5μm**
Resolution	12 bit	14 bit	12 bit	**10 bit**
DNL(LSB)	+0.32/-0.28	±0.29	+1.1/-0.4	**+0.15/-0.2**
INL(LSB)	+4.21/-0.94	-0.64%	+5.8/-8.2	**+0.91/-1.35**
1 Horizontal Time	6.02μs	0.928μs (pixel ADC)	4.4μs	**34.2μs**
*FOM2 (nJ/pixels•fps)	-	0.773	6.9	**10.7**
Random noise	216.5μV_{rms}	526.2μV_{rms}/ 309μV_{rms}	477μV_{rms}	**411 μV_{rms}**
Whether equipped with sample switch or not	no	no	no	**yes**

*FOM2 = (nJ/pixels·fps)

where $V_{\text{n,row}}$ is the row-wise noise caused by the bias circuit of the ramp generator, $V_{\text{n,read}}$ is the random noise caused by readout circuits except $V_{\text{n,row}}$, $V_{\text{n,pixel}}$ is the noise caused by the pixel including the pixel temporal noise of the source follower and the dark current shot noise. The random noise can be calculated by the standard deviation of all the output data

$$\overline{V_{\text{n,random}}} = [\text{standard\_deviation}\ (X_{i,j,k}) \times LSB]/\sqrt{2} \tag{23}$$

where $X_{i,j,k}$ is the matrix obtained by subtracting the gray value of the image of the first frame from the gray value of the image of other frames. It decreases from 865 μV_{rms} to 411 μV_{rms} due to the reduction of the row-wise noise. And the proportion of row-wise noise power in the random noise power is reduced from 78.8% to 15.8%, as shown in Fig. 15. Table IV summarizes the characteristics of noise variation when sample switch is disabled and enabled.

The simulation results show that the noise of the resistor in the ramp is 6.99μV, and the noise caused by current source is 0.33μV/unit and the intrinsic noise caused by the bias circuits is 0.41μV/unit. So the maximum noise caused by the current source is 11.8μV. However, the measurement results showed that the row-wise noise is 23.9μV/unit. This is because the power line, the ground line and the substrate will induce the noise to the Vb1 in the Fig.5. Besides, the noise caused by the digital circuits will also couple to Vb1 as well. So the measurement results of row-wise noise is larger than that of the simulation results. The row-wise noise reduction technique

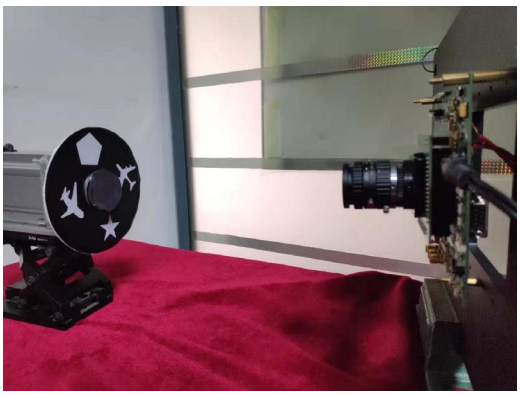


Fig. 16. The test platform of the image sensor.

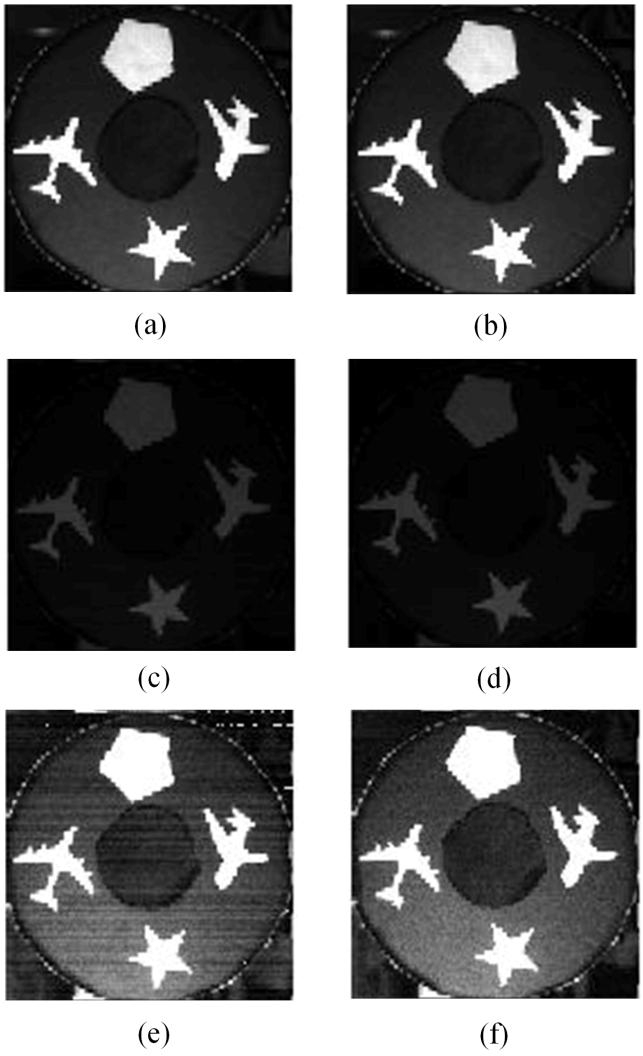


Fig. 17. Sampled images at 760 lux and 140 lux: (a) sample switch disabled at 760 lux (b) sample switch enabled at 760 lux (c) sample switch disabled at 140 lux (d) sample switch enabled at 140 lux (e) sample switch disabled at 140 lux with 10x digital gain (f) sample switch enabled at 140 lux with 10x digital gain.

proposed in the manuscript can suppress all the noise caused by the bias circuits.

Table V gives the comparison of characteristics of CMOS image sensors equipped with SSADCs in recently-proposed work.

To obtain visualized images, a test platform is designed as shown in Fig.16. A Direct Current light source is used to provide the stable background illuminant and a round black plate that contains four white simple figures on it is served as the object for imaging.

The sample images captured at 228 fps after the DCDS operation are shown in Fig. 17. Fig. 17 (a) and Fig. 17 (b) are the images captured at 760 lux when the sample switch is disabled and enabled respectively. The illumination is not over the saturation point because the lens above the sensor make the light recession. The effect of row-wise noise cancelling is not obvious because the shot noise of photon is dominant compared with the read noise of readout schematic in the environment of high illumination. Fig.17 (c) and Fig.17 (d) are the pictures captured at 140 lux when the sample switch is disabled and enabled respectively in order to verify the row-wise cancelling effect. To make this effect more obvious, the gray value of Fig. 17 (c) and (d) is multiplied by 10, as shown in Fig.17 (e) and Fig.17 (f). There are evident row-wise stripes in Fig. 17(e) because the readout noise is dominant in the dark circumstance and the row-wise non-uniformity caused by DAC is obvious due to the way of column-parallel readout. Fig. 17(f) is the image when the sample switch is enabled and it is evident that the row-wise stripes is suppressed successfully.

V. Conclusion

In this paper, we proposed a SSADC with row-wise noise reduction technique for CMOS image sensor. A current-steering DAC is served as the ramp generator and the sample switch is used to suppress the row-wise noise. Besides, CDS is implemented to remove the FPN from the pixel arrays and digital CDS is implemented to cancel the influence of response delay and offset in comparators. We fabricated a 128×128 CMOS image sensor prototype and tested the characteristics of the CMOS image sensor and the SSADC. It is proved that the sample switch can remove the row-wise noise introduced by the bias circuits efficiently. The row-wise noise is suppressed from $764\mu V_{rms}$ to $163\mu V_{rms}$.

References

[1] S. K. Mendis *et al.*, "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 187–197, Feb. 1997.

[2] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.

[3] Z. Huang *et al.*, "A 16-bit single-slope based pixel-level ADC for 15 μm-pitch 640×512 MWIR FPAs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Florence, Italy, May 2018, pp. 1–5.

[4] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 766–774, Apr. 2007.

[5] T. Kato, S. Kawahito, K. Kobayashi, H. Sasaki, T. Eki, and T. Hisanaga, "A binocular CMOS range image sensor with bit-serial block-parallel interface using cyclic pipelined ADCs," in *Symp. VLSI Circuits. Dig. Tech. Papers*, Honolulu, HI, USA, 2002, pp. 270–271.

[6] Y. Oike *et al.*, "An 8.3 M-pixel 480fps global-shutter CMOS image sensor with gain-adaptive column ADCs and 2-on-1 stacked device structure," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Honolulu, HI, USA, Jun. 2016, pp. 1–2.

[7] J. Deguchi *et al.*, "A 187.5 μVrms-read-noise 51 mW 1.4 Mpixel CMOS image sensor with PMOSCAP column CDS and 10b self-differential offset-cancelled pipeline SAR-ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 494–495.

[8] T. Arai *et al.*, "6.9 A 1.1 μm 33Mpixel 240fps 3D-stacked CMOS image sensor with 3-stage cyclic-based analog-to-digital converters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb.2016, pp. 126–127.

[9] S. Sukegawa *et al.*, "A 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 484–485.

[10] M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS imager with column-level ADC using dynamic column fixed-pattern noise reduction," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 3007–3015, Dec. 2006.

[11] Y. Nitta *et al.*, "High-speed digital double sampling with analog CDS on column parallel ADC architecture for low-noise active pixel sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 2024–2031.

[12] Y. Oike *et al.*, "8.3 M-pixel 480-fps global-shutter CMOS image sensor with gain-adaptive column ADCs and chip-on-chip stacked integration," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 985–993, Apr. 2017.

[13] Q. Liu, A. Edward, M. Kinyua, E. G. Soenen, and J. Silva-Martinez, "A low-power digitizer for back-illuminated 3-D-stacked CMOS image sensor readout with passing window and double auto-zeroing techniques," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1591–1604, Jun. 2017.

[14] M. Sakakibara *et al.*, "A 6.9-μm pixel-pitch back-illuminated global shutter CMOS image sensor with pixel-parallel 14-bit subthreshold ADC," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3017–3025, Nov. 2018.

[15] I. Park, C. Park, J. Cheon, and Y. Chae, "55.4 A 76 mW 500fps VGA CMOS image sensor with time-stretched single-slope ADCs achieving 1.95e$^-$ random noise," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 100–102.

[16] D. Levski, M. Wany, and B. Choubey, "A 1-μs ramp time 12-bit column-parallel flash TDC-interpolated single-slope ADC with digital delay-element calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 54–67, Jan. 2019.

[17] W. Lim, J. Hwang, D. Kim, S. Jeon, S. Son, and M. Song, "A low noise CMOS image sensor with a 14-bit two-step single-slope ADC and a column self-calibration technique," in *Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2014, pp. 48–51.

[18] D. Lee, K. Cho, D. Kim, and G. Han, "Low-noise in-pixel comparing active pixel sensor using column-level single-slope ADC," *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3383–3388, Dec. 2008.

[19] S. Matsuo *et al.*, "A very low column FPN and row temporal noise 8.9 M-pixel, 60 fps CMOS image sensor with 14bit column parallel SA- ADC," in *Proc. IEEE Symp. VLSI Circuits*, Honolulu, HI, Jun. 2008, pp. 138–139.

[20] P. Martin-Gonthier and P. Magnan, "Novel readout circuit architecture for CMOS image sensors minimizing RTS noise," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 776–778, Jun. 2011.

[21] Y. Mo and C. Xu, "Method and apparatus providing analog row noise correction and hot pixel filtering," U.S. Patent 8 077 227 B2, Dec. 13, 2011.

[22] B. Gove, S. Barna, S. Eikedal, S. Smith, M. Malone, and R. Panicacci, "Suppression of row-wise noise in an imager," U.S. Patent 0 243 193 A1, Nov. 3, 2005.

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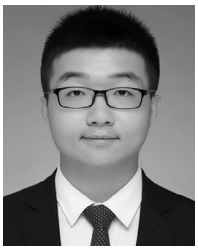

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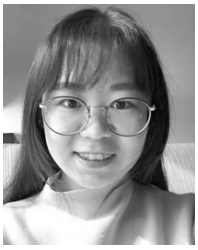

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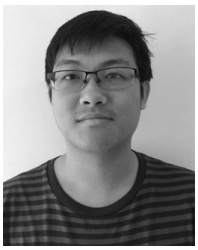

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