6.2 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs

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To realize next-generation highly realistic sensation broadcasting systems, the research and development of 8K ultrahigh-definition television (UHDTV) systems have been promoted. To realize 8K video cameras, 33Mpixel sensors [1-2] and a full-resolution camera system that uses three 33Mpixel sensors [3] have been reported. However, the weight of the camera with three sensors is over 40kg because the camera requires a large-format color-separation prism. To reduce the size of the camera, single-chip imaging is a promising approach, and a compact single-chip 8K camera that weighs only 2kg has already been developed using a color 33Mpixel CMOS image sensor [4]. However, a conventional single-chip camera has a lower image quality than a full-resolution camera because the total pixel count of the single-sensor camera is only one-third of that of the three-sensor camera, and pixel interpolation is required to configure a full-resolution image. In this paper, a 133Mpixel sensor that can be operated at 60fps to realize a full-resolution 8K single-chip camera is described. To achieve both high speed and suitable ADC resolution, 32-column multiplexing analog readout circuitry and 14b high-speed redundant successive approximation register (SAR) ADCs [5] are adopted. As a result, a full-size image with a data rate of 128.71Gb/s at 60fps has been captured.

Figure 6.2.1 shows the sensor block diagram. The total pixel array size is 15488(H) × 8776(V) including optical black pixels. The pixel design is a 2.45μm two-way vertically shared pinned photodiode. The readout of the array is addressed one physical pixel row at a time with 15,488 readout columns split between the top and bottom of the pixel array. The column readout circuit consists of a source-follower bias current (VLN), a programmable-gain amplifier (PGA), and two sets of sample-and-hold capacitor banks (SHCaps) for even-and-odd-row ping-pong operation. Analog data stored in the SHCaps are read out in parallel by 484 SAR-ADCs. Each SAR-ADC serially multiplexes 32 columns, and the resulting converter data are written into the SRAM line memory. Two banks of SRAM memory are used to provide pipelining of the ADC and SRAM readout to reduce the row time. The SRAM readout is further divided into 16 parallel ports to reduce the data rate. Each readout port outputs 960 columns, with the exception of the 4 edge corner ports that output an additional 32 optical black columns. CML output drivers are used to output 7b-wide data to a 574.56MHz DDR, achieving an aggregate data rate of 128.71Gb/s. The sensor block diagram is completed with distributed PLLs, SPI communication, and on-chip timing control logic.

Figure 6.2.2 shows a simplified block diagram of the signal readout path and timing control logic blocks. The PGA, SHCaps, CMR, and ADC are similar to those described in [5], which enables us to design a large-format sensor at 60fps that fits into a 1D stitching reticle. Front-end multiplexing of the columns is optimized for 32 columns per CMR and a 14b SAR-ADC with a conversion rate of 17.95Ms/s. To realize this conversion rate with 484 simultaneous ADCs operating in parallel, a 1.85-radix redundant SAR architecture with 12b resolution is chosen. This radix relaxes the ADC reference-settling requirement and also allows for sufficient digital redundancy in the output code to relax the capacitor-matching requirement. The signal readout path in Fig. 6.2.2 is repeated 16 times with 8 on the top and 8 on the bottom. In scaling up the readout architecture from [5], two critical design challenges need to be overcome: (1) the ADC reference and power supply distribution to meet the target performance, and (2) the timing control distribution across the chip for the SAR-ADC logic. The previous design [1] has an ADC reference and a power supply routed horizontally from left to right, thus relying on minimization of the routing resistance to meet the settling requirement. This approach is sufficient for <2MS/s ADC arrays but does not work for higher-speed ADC arrays at 17.95Ms/s. Here, our solution is to provide I/O pads in every port, thereby minimizing the resistive path to the off-chip low-ESR capacitors, which are required to supply the necessary large transient currents. This significantly reduces the horizontal routing height requirement to each port and enables scalability in the design. The reference and power are routed between the SRAM memory blocks and into the SAR-ADC array. The remaining reference and power for the lower-speed PGA, SHCaps, and CMR are distributed horizontally to each side of the sensor. The reference and supply layout busses are sized to meet supply drooping and settling requirements. The pixel sampling timing control block provides timing control to the pixel readout and ping-pong sample-and-hold operation. These signals are lower-speed timing signals; therefore, driving these controls from both the left and right sides of the chip is sufficient to reduce the RC propagation delay. However, the SAR-ADC logic and SRAM readout block require precise signal integrity to operate properly. These signals cannot tolerate degradation due to propagation across the chip. Our solution is to build a SAR control logic block in each ADC readout group. The HS timing control block provides only the 287.28MHz adc_clock, adc_sample pulse, and horizontal scanning logic. These signals are driven from the left side of the chip and are buffered periodically across the array to maintain quality. The ClkGen block retimes the adc_sample signal to adc_clock to generate the local timing.

Figure 6.2.3 shows the timing diagram for three horizontal-row periods. The conventional design approach for high-frame-rate sensors is to increase parallelism and read multiple rows within one row period. This results in multiple readout circuitries that increase area and power consumption. Here, our approach is to pipeline the row operation into three stages: pixel row readout, ADC conversion, and SRAM data output. Each readout operation takes 1.85185μs, achieving 60fps operation for the 133Mpixel sensor. Figure 6.2.3 also shows the detailed ADC readout operation. Within a row period, the ADC performs up to 33 conversions at a data rate of 17.95MS/s. The ADC timing is clocked with a 287.28MHz clock, requiring 16 clock cycles to perform the conversion. First, two clock cycles are reserved for the CMR, and the remaining 14 clock cycles are for the ADC bit cycle.

Figure 6.2.4 shows the measured DNL output code of a typical ADC at 60fps. At 12b resolution, there remain large spikes in the DNL code, which are typical in large arrays of SAR ADCs with reference settling issues. These spikes are significantly reduced with lower clock rates, indicating that refinements to the external sensor driver circuit can realize further improvements. The measured ADC readout noise at 60fps is $3.52e^-_{rms}$ at a PGA gain setting of 3× and $1.53e^-_{rms}$ at a PGA gain setting of 18×.

The image sensor specifications are summarized in Fig. 6.2.5. The sensor is fabricated using a 0.18μm 3.3V/1.8V 1P4M CIS process with 1D stitching. The standard metal thickness was used in place of the conventional thinned metal for the CIS process to minimize the pixel readout time. This is to reduce the IR drop in the horizontal and vertical pixel lines and to improve the quality of the power supply. The sensor has an effective resolution of 133Mpixels at 60fps, progressively scanned. The total random noise is measured to be $7.68e^-_{rms}$ (PGA gain 2×), and a saturation signal of $10005e^-$ results in a dynamic range of 62.3dB.

Figure 6.2.6 shows a reproduced full-size color image of a resolution chart at 60fps using a 35mm full-frame lens. Each pixel of the reproduced color image is composed of a combination of four pixels and two green signals in a Bayer CFA that are simply added. The magnified image in Fig. 6.2.6 shows that the sensor has a resolution of 4000 TV lines, which is 4× the number of current HDTV scanning lines. Figure 6.2.7 shows a chip micrograph of the 133Mpixel image sensor. The diagonal length of the active pixel area is 43.2mm, which is equivalent to the diameter of the image circle of 35mm full-frame lenses.

References:

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[4] H. Shimamoto, *et al.*, "Compact 120 Frames/sec UHDTV2 Camera with 35mm PL Mount Lens", *SMPTE Motion Imaging J.*, vol. 123, no. 4, pp. 21-28, May–June 2014.

[5] S. Huang, *et al.*, "Design of Analog Readout Circuitry with Front-End Multiplexing for Column Parallel Image Sensors", *IEEE Int. Image Sensor Workshop*, 7.08, June 2013.

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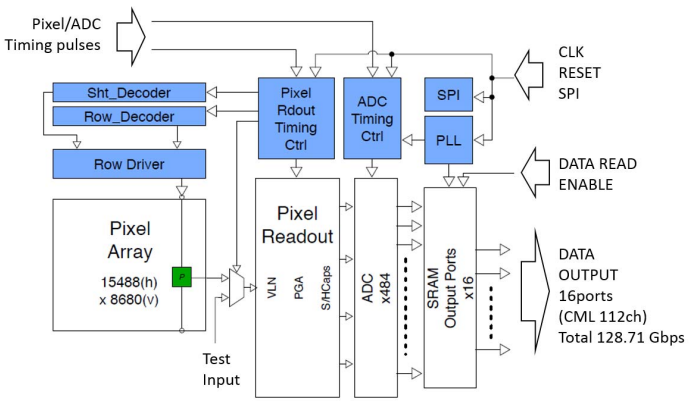

Figure 6.2.1: Block diagram.

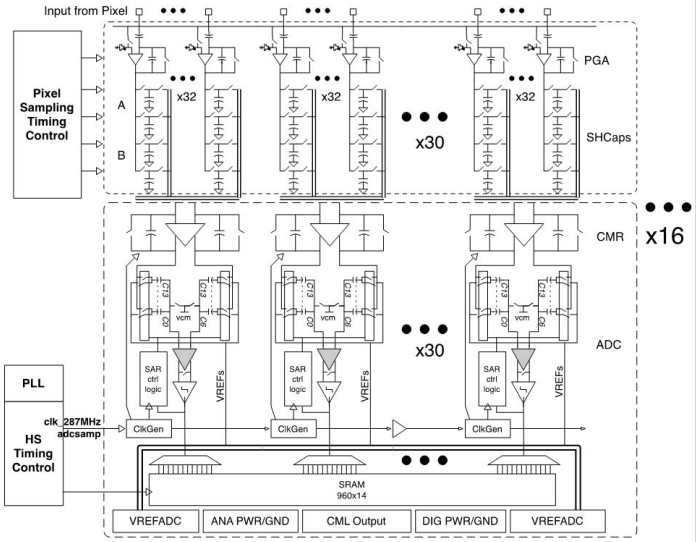

Figure 6.2.2: Signal readout path diagram.

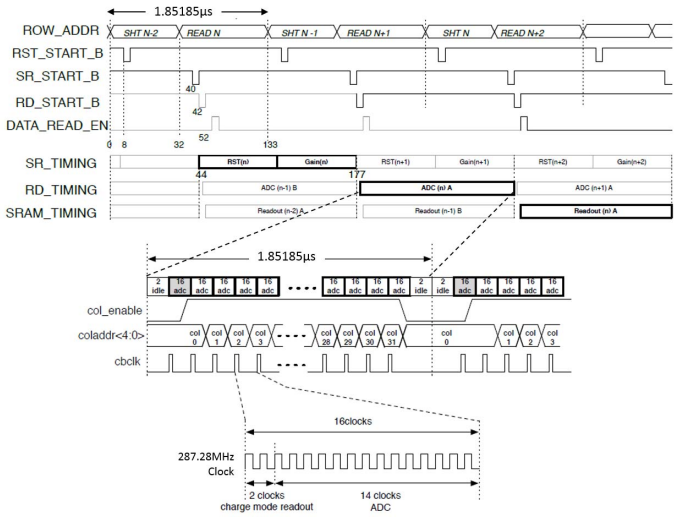

Figure 6.2.3: Timing diagram.

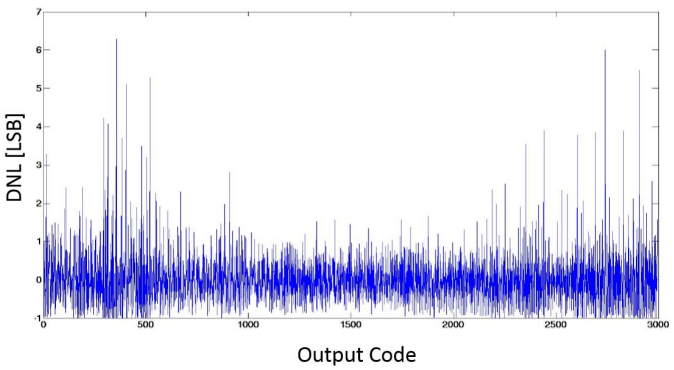

Figure 6.2.4: Measured DNL at 60fps.

Technology	0.18um 3.3V/1.8V CMOS	
Pixel size	2.45um (H) x 2.45um(V)	
Number of pixels	Total	15488(H) x 8776(V)
	Effective	15360(H) x 8640(V)
Active area	37.632mm (H) x 21.168mm(V)	
Max. frame rate	60 fps (progressive)	
Input clock	71.82 MHz @60fps	
Output data	112ch CML (1.14912 Gbps/ch @60fps)	
Total data rate	128.71 Gbps @60fps	
ADC conversion rate	17.955 Ms/s @60fps	
Number of I/O pads	1125 pads	
Color filter	Bayer CFA (G,G,B,R)	
Conversion gain	80 uV/e-	
Full well capacity	10005 e- @ PGA gain=2.0	
Dark current	50 e-/sec @ 42C	
Temporal noise	7.68 e- @60fps, PGA gain=2.0	
Dynamic range	62.3dB @60fps	
Power	11W @ 60fps	

Figure 6.2.5: Specification summary.

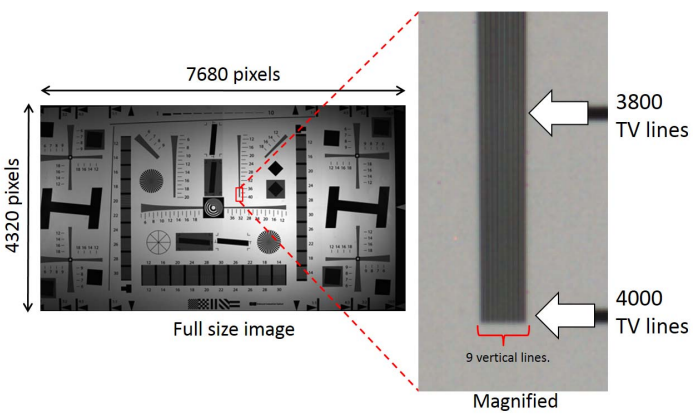

Figure 6.2.6: Reproduced full-size image.

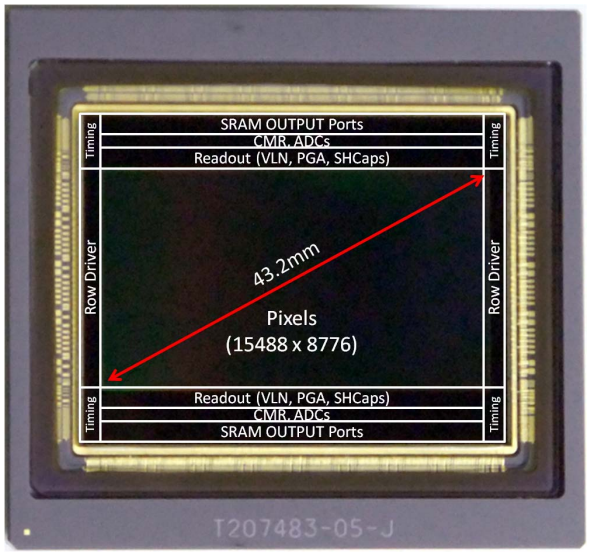

Figure 6.2.7: Die photograph.

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