SABYASACHI RATH

+91-9003353456 linkedin.com/in/essar006 rathsabyasachi08@gmail.com

I thrive in fast-paced environments and excel at tackling complex challenges with innovative solutions. With 3 years of experience my strong technical foundation allows me to quickly grasp new concepts and contribute meaningfully to the organisation.

EDUCATION

B.Tech in Electronics and Communication Engineering, VIT Vellore — CGPA: **8.26**, 2017-21
Class XII CBSE, Kendriya Vidyalaya Janakpuri, Delhi — Percentage: **80.6%**, 2015-17

SKILLS

Technical Skills Spring Boot, React.js, Data Structures and Algorithms, Databases, OOPs, UI/UX
Technologies Java, C++, Python(for automation), JavaScript, JQuery, MongoDB, MySQL, Figma

EXPERIENCE

Senior Software Engineer — **Mar 2023 – present**
Samsung Semiconductor India Research — *Bangalore, India*

- Spearheaded full-stack development initiatives, resulting in a 30% increase in project delivery efficiency:
  - Frontend: Architected and implemented responsive UIs using **React.js**, improving user engagement by 25%.
  - Backend: Engineered scalable solutions with Java **Spring Boot**, optimizing system performance by 40%.
  - Automated 15+ critical processes using **Python**, reducing manual effort by 50%.
  - Implemented **MongoDB** for data management, enhancing query performance by 30%.
- Co-worked with a group of interns to successfully deliver key projects, accelerating the productivity ramp-up.

Software Engineer — **Jan 2022 – Mar 2023**
Samsung Semiconductor India Research — *Bangalore, India*

- Designed and developed robust Java applications leveraging **Object-Oriented Programming (OOP)** principles and best practices for clean, maintainable code.
- Developed frontend user interfaces using **JavaScript** and integrated them with **SQL** databases to enhance functionality and data management

DFT Engineer — **Jul 2021 – Dec 2021**
Samsung Semiconductor India Research — *Bangalore, India*

- ATPG patterns verification with gate level simulation.
- Scan Architecture and insertion, and ATPG pattern generation.

DFT Intern — **Feb 2021 – Jul 2021**
Samsung Semiconductor India Research — *Bangalore, India*

- Acquired comprehensive understanding of DFT (Design for Testability) and its critical role in the semiconductor industry.
- Generated precise test and debug patterns to improve electronic component reliability and performance.

ACHIEVEMENTS

- **President Award** : Awarded by the Hon'ble President of India - Pranab Mukherjee.
- **Dev Hackathon at Samsung Research (March 2024)** : Designed and Developed Asset Tracking Portal (JavaScript, Spring Boot REST APIs) and qualified for final round and secured 3rd position.

EXTRA-CURRICULAR ACTIVITIES

- **Manager SPARK'19, International Society of Automation (ISA), VIT** : Led sponsorships & ensured accurate registration for SPARK'19 (ISA).
- **Professional Music Experience** : Have been a part of Samsung's and VIT's band, contributed as a vocalist.
- **Design Head** : Designed official Brochure, T-shirt for an 5th Pillar NGO.
- **Pro Badminton player** : Achieved 2nd place at an Inter-Corporate Tournament.