Assignment #11

Daniel Diaz

ID: 11656703

Computer Organization and Assembly Language Programming

CS-3350-002

Dr. Morshed

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Problem 2 (40%)

Assume that individual stages of the data-path have the following latencies (in ps) for two configurations of microprocessors (Microprocessor A & Microprocessor B):

	IF	ID	EX	MEM	WB
Microprocessor A	250	350	150	300	200
Microprocessor B	200	170	220	210	150

a. What are the clock cycle periods and frequencies in "Single Cycle" and in "Pipelined" microprocessors of A & B?

b. What are the total latencies of a single "lw" instruction in this single cycle and pipelined microprocessors of A & B?

c. What are the total latencies of 10 "lw" instructions in this single cycle and pipelined microprocessors of A & B? From the results, calculate the average time per instruction for each case.

d. If we can split one stage of the pipelined data path into two new stages, each with half the latency of the original stage, which stage would you split to achieve the minimum clock period and what is the new clock cycle periods and frequencies of the two microprocessors?

A)

a. Microprocessor A:
   i. Single Cycle = 250 + 350 + 150 + 300 + 200 = 1, 250 ps
   ii. F = 1/1250 = 0.8GHz
   iii. Pipeline = max{250,350,150,300, 200} = 350 ps
   iv. F = 1/350 = 2.86 Ghz
b. Microprocessor B:
   i. Single Cycle = 200 + 170 + 220 + 210 +150 = 950 ps
   ii. F = 1/950 = 1.10Ghz
   iii. Pipeline = max{200,170,220 210,150} = 220 ps
   iv. F = 1/220 = 4.54Ghz

B)

a. Microprocessor A:
   i. Single Cycle Latency = 1250ps
   ii. Pipeline Latency = 350 * 5 = 1750 ps
b. Microprocessor B:
   i. Single Cycle Latency = 950 ps
   ii. Pipeline Latency = 220 * 5 = 1100 ps

C)

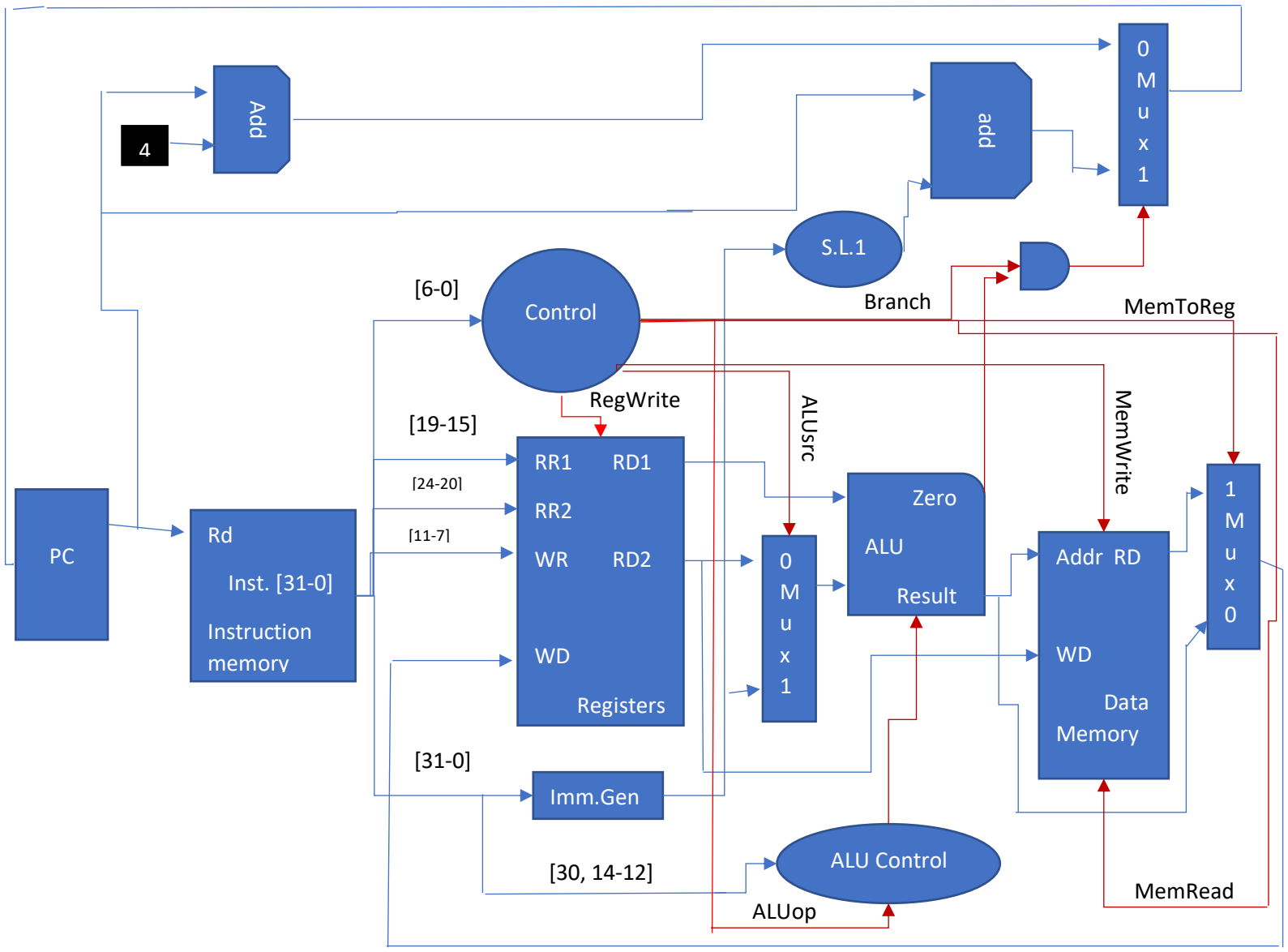
a. Microprocessor A:
   i. Single Cycle Latency = 1250 * 10 = 12500ps
   ii. Average Time = 12500 / 10 = 1250 ps
   iii. Pipeline Latency = 1750 + (350 * 9) = 4900ps
   iv. Average Time = 4900 / 10 = 490ps
b. Microprocessor B:
   i. Single Cycle Latency = 950 * 10 = 9500ps

ii. Average Time = 9500/10 = 950ps
iii. Pipeline Latency = 1100 + (220 * 9) = 3080ps
iv. Average Time = 3080 / 10 = 308ps

D) For both cases, splitting the stage that takes the longest time is going to be right call.
   a. Microprocessor A: I would split the Instruction decoding stage (ID), making the new clock cycle be 300ps, thus, making the frequency (f = 1/300) be 3.33Ghz
   b. Microprocessor B: Splitting the execution stage (EX) is the correct choice, making the new clock cycle be 210, thus, making the frequency (f = 1/210) be 4.76Ghz

Problem 1 (60%)

Draw a complete single cycle RISC V microprocessor clearly showing the hardware blocks, data path connections, the controllers, and the control signal connections.


4
Add
add
0
M
u
x
1
S.L.1
Branch
MemToReg
[6-0]
Control
RegWrite
ALUsrc
MemWrite
[19-15]
[24-20]
[11-7]
PC
Rd
Inst. [31-0]
Instruction
memory
RR1
RD1
RR2
WR
RD2
WD
Registers
Zero
ALU
Result
Addr
RD
WD
Data
Memory
1
M
u
x
0
[31-0]
Imm.Gen
[30, 14-12]
ALU Control
ALUop
MemRead