Hardware Design

**Lab 3 Report**

Sequential Circuits

**Team 01**

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# Advanced Q1. 4-bit ping pong counter

一張含有 螢幕擷取畫面 的圖片

自動產生的描述一張含有 螢幕擷取畫面, 正方形, 對稱, 黑色 的圖片

自動產生的描述

* 3 inputs: *a[7:0], b[7:0], cin*
* 2 outputs: *sum[7:0], cout*

To construct a **8-bit RCA**, we use eight Full Adders connecting each other to calculate each sum and carry. The first(rightmost), second, third, …, seventh Full Adders produce carry, for the next Full Adder to take as *cin*, and the eighth Full Adder produce the overall carry of the final answer. Each bit of sum is calculated by each Full Adder respectively. Additionally, due to the demand that we could only use NAND gates, so all the basic gates we are supposed to use are replaced by our hand-made modules, and so does following advanced question 3 and 4.

# Advanced Q2. Decode and execute

# Advanced Q3. 8-bit Carry Look-ahead Adder (CLA)

# Advanced Q4. 4-bit Multiplier

# Advanced Q5. Exhaustive testbench design

# FPGA: 7-Segment Display Control

# Testbenches

## A. 8-bit Ripple Carry Adder (RCA)

## B. Decode and execute

## C. 8-bit Carry Look-ahead Adder (CLA)

## D. 4-bit Multiplier

# What we have learned from Lab2?

# Contributions

謝佳晉：

wrote Verilog modules: Q1, Q2, Q4

wrote testbenches: Q1, Q2, Q4, Q5

performed simulation: Q1, Q2, Q4, Q5

drew diagram: basic Q1, Q2

wrote report: basic Q3, Q5, tbQ1, tbQ2, tbQ4

made FPGA demonstration

范升維：

wrote Verilog modules: Q1, Q2, Q3, Q4

wrote testbench: Q3

performed simulation: Q1, Q2, Q3, Q4 simulation on Vivado

drew diagram: ALL (basic Q1, Q1, Q2, Q3, Q4)

wrote report: basic Q1, basic Q3, Q1, Q2, Q3, Q4, tbQ3, what we learned

organized whole report

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | b-Q1 | b-Q3 | Q1 | Q2 | Q3 | Q4 | Q5 | FPGA | What we learned |
| wrote Verilog modules |  |  |  |  |  |  |  |  |  |
| wrote testbenches |  |  |  |  |  |  |  |  |  |
| performed simulation |  |  |  |  |  |  |  |  |  |
| drew diagram |  |  |  |  |  |  |  |  |  |
| wrote report |  |  |  |  |  |  |  |  |  |
| wrote report tb |  |  |  |  |  |  |  |  |  |

|  |
| --- |
| Both |
| 謝佳晉 |
| 范升維 |