**Lab 1 Report**

Gate-Level Verilog

Team 01

112062122 謝佳晉 112062144 范升維

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**Q1. 1x4\_4bit Dmux**

1. **1x2\_4bit Dmux**

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自動產生的描述

Figure 1.1

* Input: in[3:0]
* Control Signal: sel
* Output: a[3:0], b[3:0]

First, we construct module 1x2 Dmux. This module can route the input, in, to either a or b depending on the control signal, sel. When sel is 0, the upper four and gates have one of the input 1, so their outputs will be the same as input. Because the lower four have one of the input 0, so their outputs will all be 0. Vice versa.

1. **1x4\_4bit Dmux**

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自動產生的描述

Figure 1.2

* Input: in[3:0]
* Control Signal: sel[1:0]
* Output: a[3:0], b[3:0], c[3:0], d[3:0]

Now we have 1x2 Dmux, we can construct module 1x4 Dmux by combining three 1x2 Dmuxes. We can use the left one 1x2 Dmux with sel[1] to preliminarily route the input to a/b or c/d. Next, we use the right two 1x2 Dmux with sel[0] to route the input to a or b / c or d. Therefore, we get one of a/b/c/d to be the same as input, and three other outputs be 4’b0.

**Q2. 2x2\_4bit Crossbar Switch**

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自動產生的描述

Figure 2.1

* Input: in1[3:0], in2[3:0]
* Control Signal: control
* Output: out1[3:0], out2[3:0]

We use two 1x2 Dmuxes and two 2x1 Muxes to construct a 2x2 Crossbar Switch. When control is 0, in1->con1->out1, and in2->con4->out2, like parallel. When control is 1, in1->con2->out2, and in2->con3->out1, like cross.

**Q3. 4x4\_4bit Crossbar Switch**

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自動產生的描述

Figure 3.1

* Input: in1[3:0], in2[3:0], in3[3:0], in4[3:0]
* Control Signal: control[4:0]
* Output: out1[3:0], out2[3:0], out3[3:0], out4[3:0]

The 4x4 Crossbar Switch consists of five 2x2 Crossbar Switch. The function of it is something like 2x2 Crossbar Switch, but there exist a limit. Some routes of input to output is impossible. The following are the impossible routes:

[(in1, out3), (in2, out4), (in3, out1), (in4, out2)],

[(in1, out4), (in2, out3), (in3, out1), (in4, out2)],

[(in1, out3), (in2, out4), (in3, out2), (in4, out1)],

[(in1, out4), (in2, out3), (in3, out2), (in4, out1)].

Because this design is certain to route one of in1/in2 and in3/in4 to out1/out2 and out3/out4, so the limit will exist. To handle this problem, we can add an 2x2 Crossbar which takes con1 and con4 as input.

**Q4. Toggle Flip-Flop**

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自動產生的描述 一張含有 圖表, 文字, 方案, 行 的圖片

自動產生的描述**

Figure 4.1 Figure 4.1

Figure 4.1 shows how we construct the XOR gate. After we have the XOR gate and DFF, we can further get a Toggle Flip Flop. When rst\_n is 1, on the positive edge, q will be toggled into ~q if t is stably 1 at that time, and nothing happen if t is 0 or not stably 1.

**Testbenches**

1. **1x4\_4bit Dmux**

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自動產生的描述**一張含有 螢幕擷取畫面, 文字, 行 的圖片

自動產生的描述**

We can test this module by adding up sel’s value and see if the corresponding output port has changed. Changing input value shows that it’s flexible.

1. **2x2\_4bit Crossbar Switch**

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自動產生的描述一張含有 螢幕擷取畫面, 鍵盤, 電腦 的圖片

自動產生的描述**

We can test this module by keeping changing the value of control so that we can see if the inputs have been routed to the correct output ports. Same, changing input values shows that it’s flexible.

1. **4x4\_4bit Crossbar Switch**

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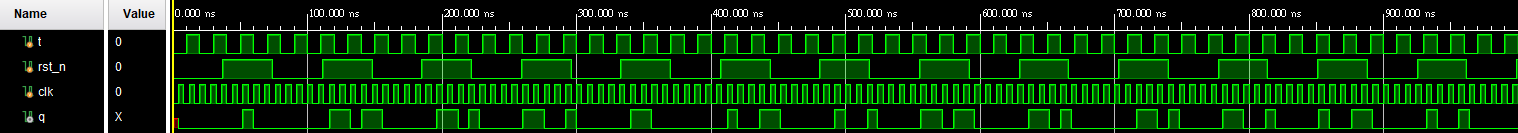
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自動產生的描述**

We can test this module by changing control’s value to see if the inputs have been routed to the correct output ports, just like 2x2\_4bit Crossbar Switch. Changing input values shows that it’s flexible. To find the impossible routes easily, we can set input values to be a, b, c, d and use $monitor command.

1. **Toggle Flip Flop**

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自動產生的描述**

We can test this module by properly setting the interval time between value changes so that it can simulate random cases that it may meet.

**What we have learned from Lab 1?**