Hardware Design

**Lab 3 Report**

Sequential Circuits

**Team 01**

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# Advanced Q1. 4-bit Ping-Pong Counter

一張含有 螢幕擷取畫面 的圖片

自動產生的描述一張含有 螢幕擷取畫面, 正方形, 對稱, 黑色 的圖片

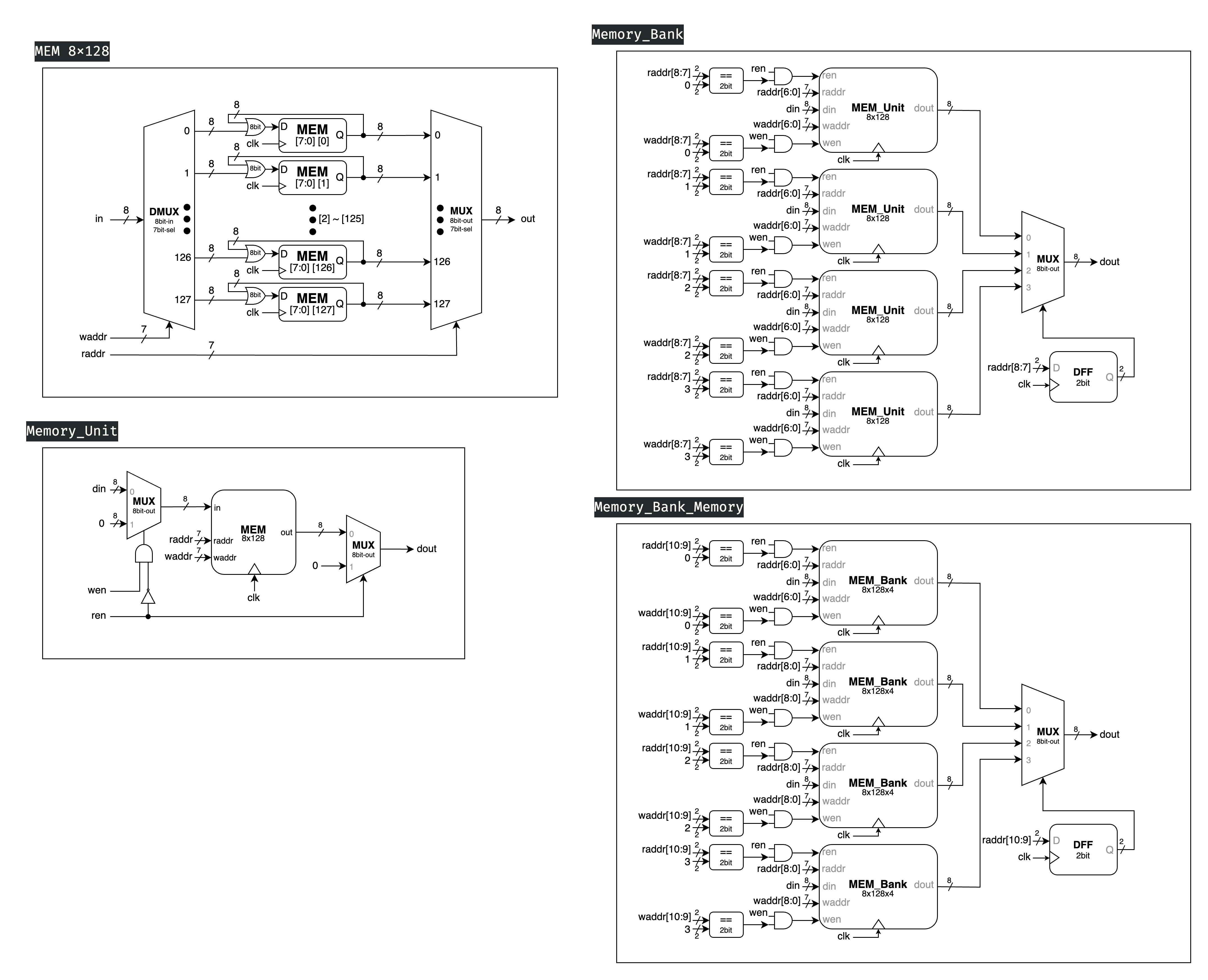
自動產生的描述

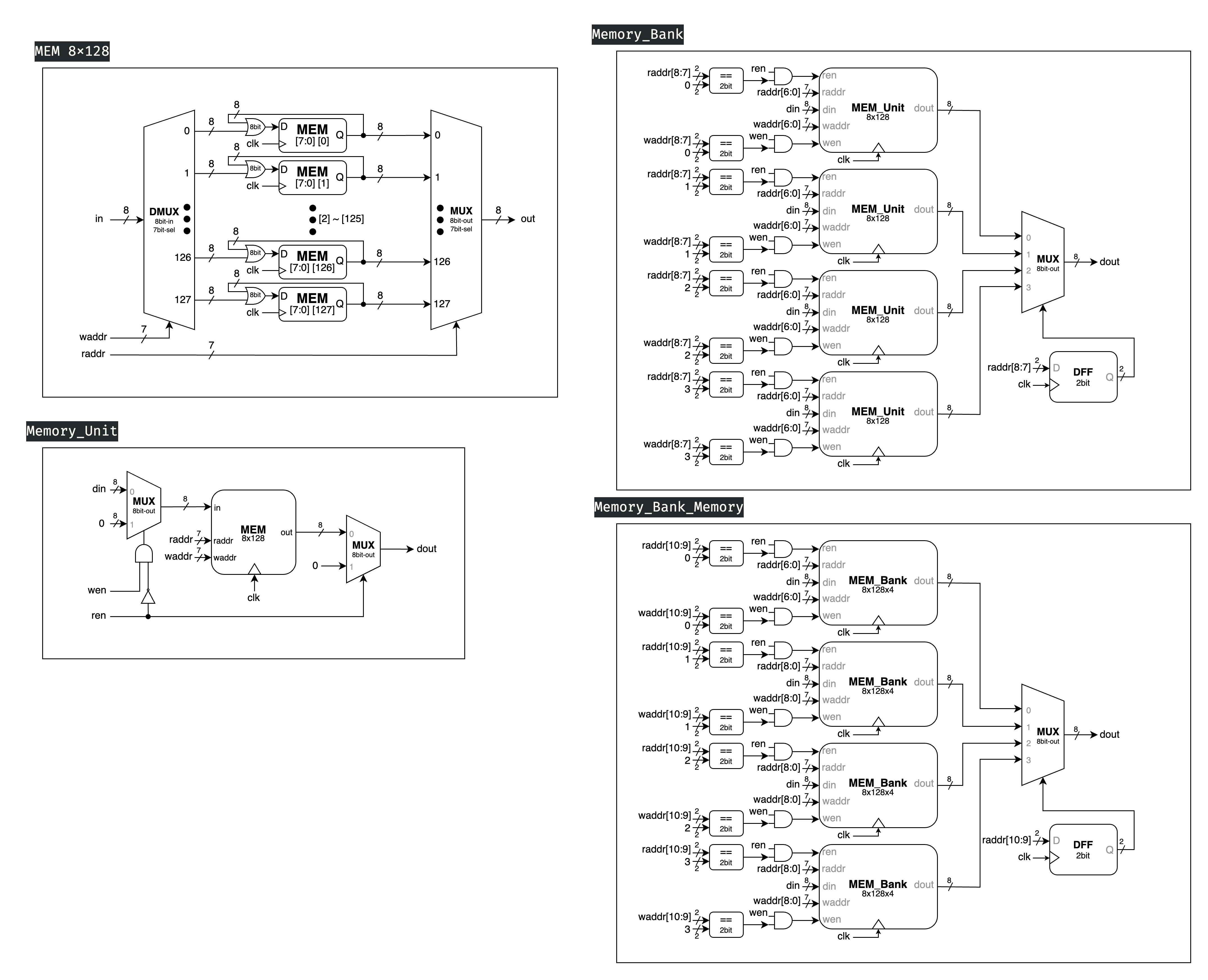
* 3 inputs: *a[7:0], b[7:0], cin*
* 2 outputs: *sum[7:0], cout*

To construct a **8-bit RCA**, we use eight Full Adders connecting each other to calculate each sum and carry. The first(rightmost), second, third, …, seventh Full Adders produce carry, for the next Full Adder to take as *cin*, and the eighth Full Adder produce the overall carry of the final answer. Each bit of sum is calculated by each Full Adder respectively. Additionally, due to the demand that we could only use NAND gates, so all the basic gates we are supposed to use are replaced by our hand-made modules, and so does following advanced question 3 and 4.

# Advanced Q2. First-In First Out (FIFO) Queue

# Advanced Q3. Multi-Bank Memory

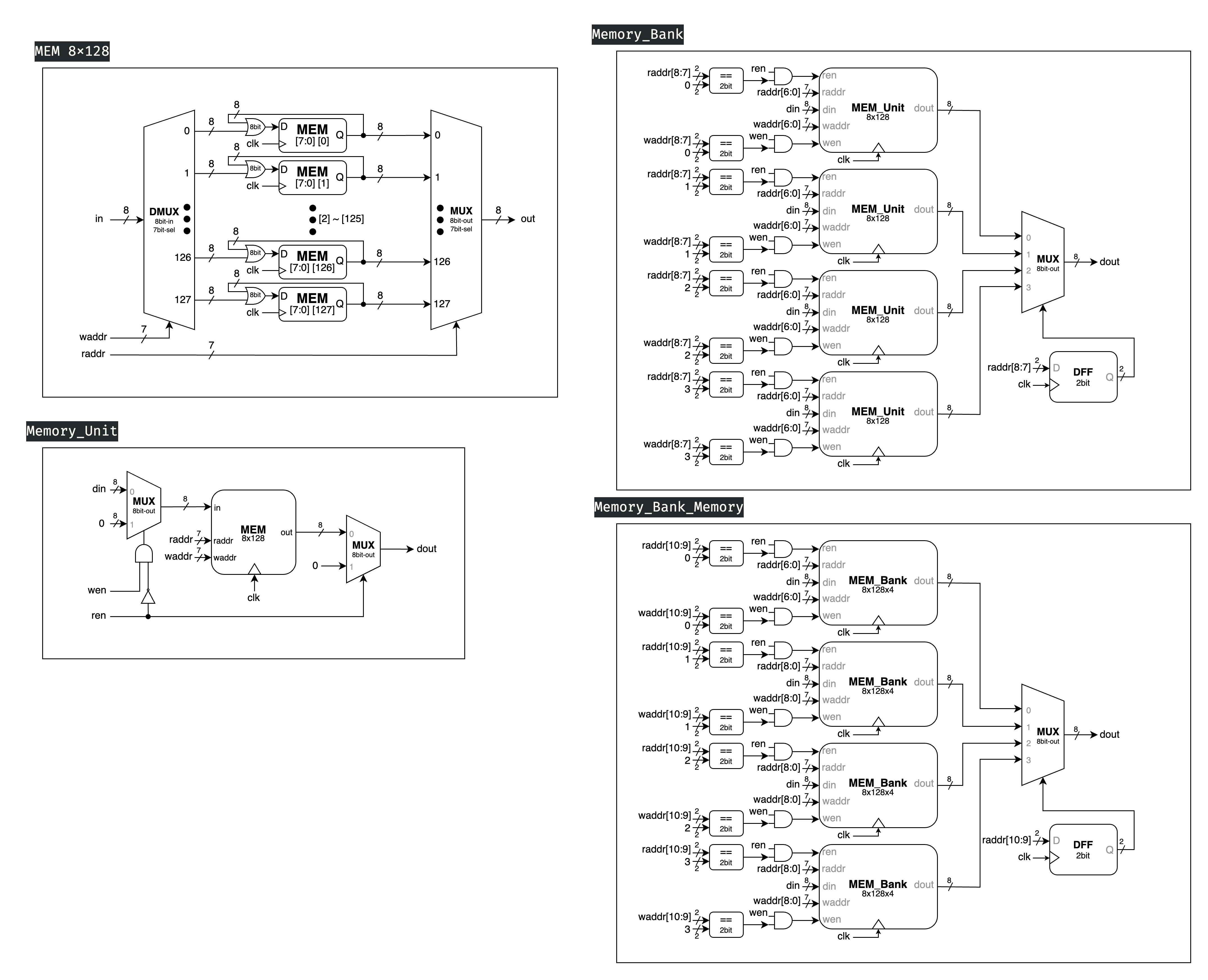
In Advanced Question 3, we are required to construct a multi-bank memory system consisting of 4 **Memory Banks**. Each bank comprises 4 **Memory Units**, and each Memory Unit is an 8-bit x 128 memory module, which we previously implemented in Basic Question 2.

▲ Figure 3.1: MEM 8x128

▲ Figure 3.2: Memory Unit (8bit x 128 memory module)

* 6 inputs: *clk, ren, wen, waddr[6:0], raddr[6:0], din[7:0]*
* 1 output: *dout[7:1]*

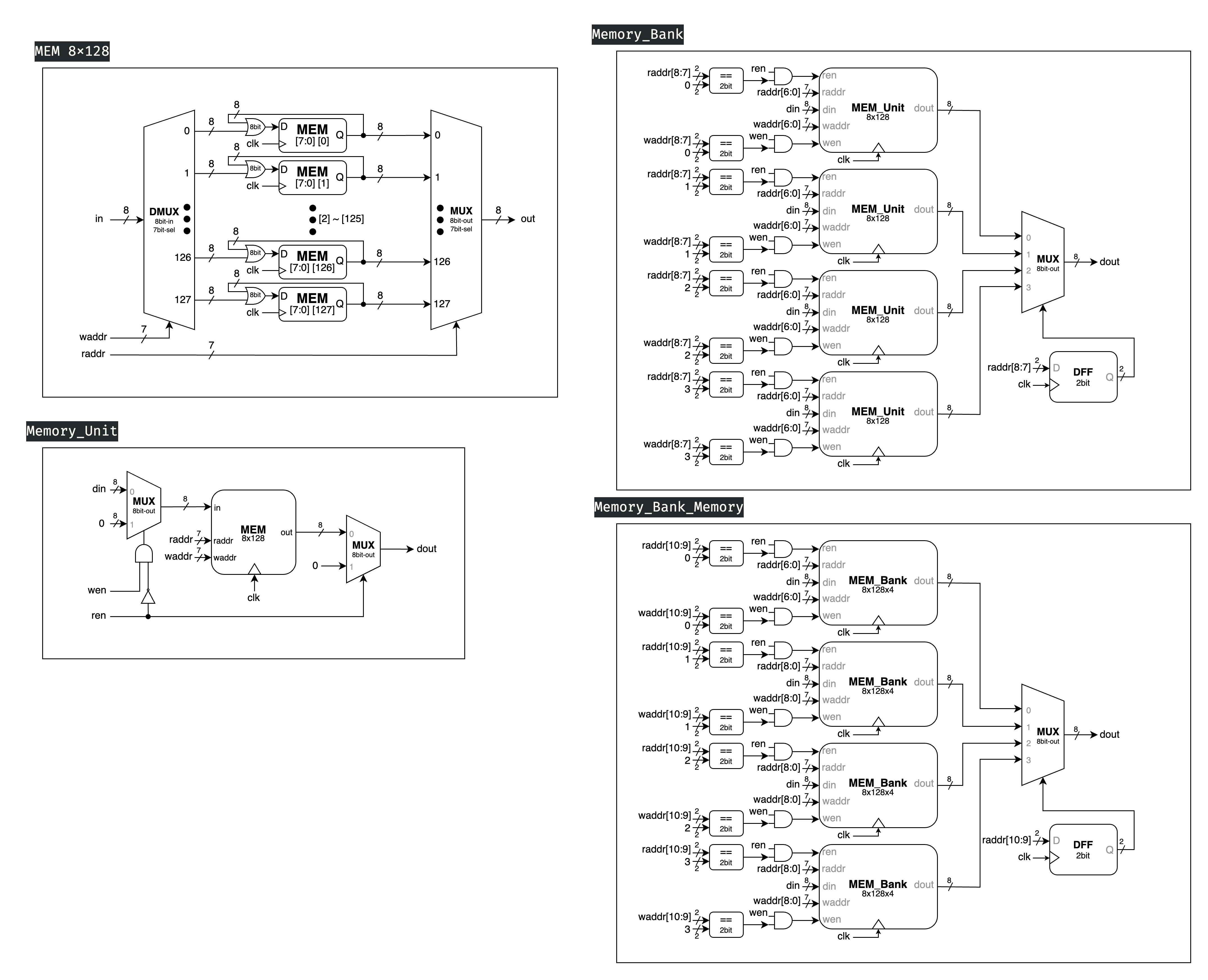
Figure 3.2 illustrates our implemented **Memory Unit**, which is an 8-bit x 128 memory module. This unit incorporates the **MEM 8x128** component shown in Figure 3.1. The MEM 8x128 is designed to store the input data (*din*) at the memory location specified by the write address (*waddr*). Each memory location within the MEM consists of a synchronized 8-bit register array, implemented with D Flip Flop. The output (*dout*) is determined by the value stored in the memory location designated by the read address (*raddr*).

Figure 3.2 illustrates the implementation that fulfills the specified requirements of the problem. The circuit is configured to output *dout[7:0]* only when the read enable signal (*ren*) is asserted to *1'b1*; otherwise, it outputs *8'b0*. Furthermore, the circuit permits data input operations under the condition that the input data (*din*) is stored in the memory location designated by the write address (*waddr*) exclusively when the write enable signal (*wen*) is asserted to *1'b1* and, concurrently, the read enable signal (*ren*) is de-asserted to *1'b0*. This control scheme ensures proper read and write operations while preventing potential conflicts between simultaneous read and write attempts.

▲ Figure 3.3: Memory Bank

* 6 inputs: *clk, ren, wen, waddr[8:0], raddr[8:0], din[7:0]*
* 1 output: *dout[7:1]*

Figure 3.3 depicts the circuit diagram of the **Memory Bank**, which integrates four Memory Units. The *waddr* and *raddr* signals have been expanded by two bits to specify the target Memory Unit. Consequently, the write enable (*wen*) and read enable (*ren*) signals for each Memory Unit are activated (set to *1'b1*) only when this module's *wen*/*ren* is *1'b1* and the two most significant bits of *waddr*/*raddr* correspond to that particular Memory Unit.

The output (*dout*) of this module utilizes a multiplexer (**MUX**) to select the *dout* from the Memory Unit indicated by the two most significant bits of *raddr*. It is important to note that the *select* signal for this MUX is not directly connected to *raddr*. Instead, it passes through a D flip-flop (**DFF**). This design choice ensures that fluctuations in the *raddr* signal between clock cycles do not inadvertently alter the Memory Unit connected to the module's *dout*, thereby maintaining signal integrity and preventing glitches in the output.

▲ Figure 3.4: Multi-Bank Memory

Figure 3.4 illustrates the **Multi-Bank Memory** module, which represents the final implementation of our design. The structure of this module bears a strong resemblance to that of the Memory Bank connected to four Memory Units, as previously discussed. The primary distinction lies in the further extension of *waddr* and *raddr* signals by an additional two bits. Given the structural similarities, an additional description of the design is deemed unnecessary.

# Advanced Q4. Round-Robin FIFO Arbiter

# Advanced Q5. Exhaustive testbench design

# FPGA: 4‑bit Parameterized Ping‑Pong Counter

# Testbenches

## A. 4-bit Ping-Pong Counter

## B. First-In First Out (FIFO) Queue

## C. Multi-Bank Memory

## D. Round-Robin FIFO Arbiter

## E. Exhaustive testbench design

# What have we learned from Lab 3?

# Contributions

謝佳晉：

wrote Verilog modules: Q1, Q2, Q4

wrote testbenches: Q1, Q2, Q4, Q5

performed simulation: Q1, Q2, Q4, Q5

drew diagram: basic Q1, Q2

wrote report: basic Q3, Q5, tbQ1, tbQ2, tbQ4

made FPGA demonstration

范升維：

wrote Verilog modules: Q1, Q2, Q3, Q4

wrote testbench: Q3

performed simulation: Q1, Q2, Q3, Q4 simulation on Vivado

drew diagram: ALL (basic Q1, Q1, Q2, Q3, Q4)

wrote report: basic Q1, basic Q3, Q1, Q2, Q3, Q4, tbQ3, what we learned

organized whole report

|  |  |  |  |  |  |  |  |  |  |
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|  | b-Q1 | b-Q3 | Q1 | Q2 | Q3 | Q4 | Q5 | FPGA | What we learned |
| wrote Verilog modules |  |  |  |  |  |  |  |  |  |
| wrote testbenches |  |  |  |  |  |  |  |  |  |
| performed simulation |  |  |  |  |  |  |  |  |  |
| drew diagram |  |  |  |  |  |  |  |  |  |
| wrote report |  |  |  |  |  |  |  |  |  |
| wrote report tb |  |  |  |  |  |  |  |  |  |

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