M3 Sensor and Timer (Version 3) Documentation (SNTv3)

Revision 1.0

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1 MBus Register File

1.1 MBus Register File Mapping

Table 1 shows MBus Register File mapping information. 'NR' indicates a non-retentive register.

Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 0 (0x00) Default: 24'h000020					
0x00	[9:6]	LDO_VREF_I_AMP	W/R	4'h0	
	[5:3]	LDO_SEL_VOUT	W/R	3'h4	
	[2]	LDO_EN_VREF	W/R	1'h0	
	[1]	LDO_EN_IREF	W/R	1'h0	
	[0]	LDO_EN_LDO	W/R	1'h0	
Register 1 (0x01) Default: 24'h000802					
0x01	[11]	TSNS_FORCE_CLR_IRQ_IF_EN_IRQ_0	W/R	1'h1	
	[10]	TSNS_EN_CLK_REF	W/R	1'h0	
	[9]	TSNS_EN_CLK_SENS	W/R	1'h0	
	[8]	TSNS_EN_IRQ	W/R	1'h0	
	[7]	TSNS_CONT_MODE	W/R	1'h0	
	[6]	TSNS_BURST_MODE	W/R	1'h0	
	[5]	TSNS_EN_SENSOR_LDO	W/R	1'h0	
	[4]	TSNS_EN_SENSOR_V1P2	W/R	1'h0	
	[3]	TSNS_SEL_LDO	W/R	1'h0	
	[2]	TSNS_SEL_V1P2	W/R	1'h0	
	[1]	TSNS_ISOLATE	W/R	1'h1	
	[0]	TSNS_RESETn	W/R	1'h0	
Register 2 (0x02) Default: 24'h200050					
0x02	[21:18]	TSNS_R_REF	W/R	4'h8	
	[17:14]	TSNS_I_BUF	W/R	4'h0	
	[13:10]	TSNS_I_BUF2	W/R	4'h0	
	[9:6]	TSNS_I_CMP	W/R	4'h1	
	[5:4]	TSNS_I_MIRROR	W/R	2'h1	
	[3:0]	TSNS_I_SOSC	W/R	4'h0	
Register 3 (0x03) Default: 24'h049CE6					
0x03	[18:16]	TSNS_MIM	W/R	3'h4	
	[15:13]	TSNS_MOM	W/R	3'h4	
	[12:9]	TSNS_SEL_VVDD	W/R	4'hE	
	[8:6]	TSNS_SEL_STB_TIME	W/R	3'h3	
	[5:4]	TSNS_SEL_REF_STB_TIME	W/R	2'h2	
	[3:0]	TSNS_SEL_CONV_TIME	W/R	4'h6	
Register 4 (0x04) Default: 24'h000200					
0x04	[14:0]	TSNS_PDIFF	W/R	15'h0200	
Register 5 (0x05) Default: 24'h004000					
0x05	[23:0]	TSNS_POLY	W/R	24'h004000	
Register 6 (0x06) Default: 24'h000000					
0x06	[23:0]	TSNS_DOUT	R	24'h000000	
Register 7 (0x07) Default: 24'h001000					
0x07	[15:8]	TSNS_INT_RPLY_SHORT_ADDR	W/R	8'h10	
	[7:0]	TSNS_INT_RPLY_REG_ADDR	W/R	8'h00	
Register 8 (0x08) Default: 24'h000060					
	[6]	TMR_SLEEP	W/R	1'h1	
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Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
	[5]	TMR_ISOLATE	W/R	1'h1	
	[4]	TMR_RESETB	W/R	1'h0	
	[3]	TMR_EN_OSC	W/R	1'h0	
	[2]	TMR_RESETB_DIV	W/R	1'h0	
	[1]	TMR_RESETB_DCDC	W/R	1'h0	
	[0]	TMR_EN_SELF_CLK	W/R	1'h0	
Register 9 (0x09) Default: 24'hE80813					
0x09	[23]	TMR_SEL_CLK_DIV	W/R	1'h1	
	[22]	TMR_SEL_CLK_OSC	W/R	1'h1	
	[21]	TMR_SELF_EN	W/R	1'h1	
	[20:17]	TMR_IBIAS_REF	W/R	4'h4	
	[16]	TMR_CASCODE_BOOST	W/R	1'h0	
	[15:8]	TMR_SEL_CAP	W/R	8'h08	
	[7:2]	TMR_SEL_DCAP	W/R	6'h04	
	[1]	TMR_EN_TUNE1	W/R	1'h1	
	[0]	TMR_EN_TUNE2	W/R	1'h1	
Register 10 (0x0A) Default: 24'h9FFDBC					
0x0A	[23:21]	TMR_S	W/R	3'h4	
	[20:7]	TMR_DIFF_CON	W/R	14'h3FFB	
	[5]	TMR_EN_TUNE1_RES	W/R	1'h1	
	[4]	TMR_EN_TUNE2_RES	W/R	1'h1	
	[3]	TMR_SAMPLE_EN	W/R	1'h1	
	[2:0]	TMR_AFC	W/R	3'h4	
Register 11 (0x0B) Default: 24'h00000F					
0x0B	[3:0]	TMR_TFR_CON	W/R	4'hF	
Register 23 (0x17) Default: 24'h601007					
0x17	[23]	WUP_ENABLE	W/R	1'h0	
	[22]	WUP_LC_IRQ_EN	W/R	1'h1	
	[21]	WUP_AUTO_RESET	W/R	1'h1	
	[20]	WUP_CLK_SEL	W/R	1'h0	
	[19]	WUP_ENABLE_CLK_SLP_OUT	W/R	1'h0	
	[15:8]	WUP_INT_RPLY_SHORT_ADDR	W/R	8'h10	
	[7:0]	WUP_INT_RPLY_REG_ADDR	W/R	8'h07	
Register 24 (0x18) Default: 24'h023002					
0x18	[23:0]	WUP_INT_RPLY_PAYLOAD	W/R	24'h023002	
Register 25 (0x19) Default: 24'h000000					
0x19	[7:0]	WUP_THRESHOLD_EXT	W/R	8'h00	
Register 26 (0x1A) Default: 24'h2DC6C0					
0x1A	[23:0]	WUP_THRESHOLD	W/R	24'h2DC6C0	
Register 27 (0x1B) Default: 24'h000000					
0x1B	[7:0]	WUP_CNT_VALUE_EXT	R	8'h00	
Register 28 (0x1C) Default: 24'h000000					
0x1C	[23:0]	WUP_CNT_VALUE	R	24'h000000	
Register 29 (0x1D) Default: 24'h000019					
0x1D	[5]	MBC_WAKEUP_ON_PEND_REQ	W/R	1'h0	
	[4]	MBC_IGNORE_RX_FAIL	W/R	1'h1	
	[3:2]	LC_CLK_DIV	W/R	2'h2	
	[1:0]	LC_CLK_RING	W/R	2'h1	

Table 1: SNTv3 MBus Register File Mapping

1.2 MBus Register Descriptions

1.2.1 Register 0 (0x00)

LDO_VREF_I_AMP Reg 0x00, Bit Field: [9:6], Default: 4'h0, W/R

LDO_SEL_VOUT Reg 0x00, Bit Field: [5:3], Default: 3'h4, W/R

LDO_EN_VREF Reg 0x00, Bit Field: [2], Default: 1'h0, W/R

LDO_EN_IREF Reg 0x00, Bit Field: [1], Default: 1'h0, W/R

LDO_EN_LDO Reg 0x00, Bit Field: [0], Default: 1'h0, W/R

1.2.2 Register 1 (0x01)

TSNS_FORCE_CLR_IRQ_IF_EN_IRQ_0 Reg 0x01, Bit Field: [11], Default: 1'h1, W/R

TSNS_EN_CLK_REF Reg 0x01, Bit Field: [10], Default: 1'h0, W/R

TSNS_EN_CLK_SENS Reg 0x01, Bit Field: [9], Default: 1'h0, W/R

TSNS_EN_IRQ Reg 0x01, Bit Field: [8], Default: 1'h0, W/R

TSNS_CONT_MODE Reg 0x01, Bit Field: [7], Default: 1'h0, W/R

TSNS_BURST_MODE Reg 0x01, Bit Field: [6], Default: 1'h0, W/R

TSNS_EN_SENSOR_LDO Reg 0x01, Bit Field: [5], Default: 1'h0, W/R

TSNS_EN_SENSOR_V1P2 Reg 0x01, Bit Field: [4], Default: 1'h0, W/R

TSNS_SEL_LDO Reg 0x01, Bit Field: [3], Default: 1'h0, W/R

TSNS_SEL_V1P2 Reg 0x01, Bit Field: [2], Default: 1'h0, W/R

TSNS_ISOLATE Reg 0x01, Bit Field: [1], Default: 1'h1, W/R

TSNS_RESETn Reg 0x01, Bit Field: [0], Default: 1'h0, W/R

1.2.3 Register 2 (0x02)

TSNS_R_REF Reg 0x02, Bit Field: [21:18], Default: 4'h8, W/R

TSNS_I_BUF Reg 0x02, Bit Field: [17:14], Default: 4'h0, W/R

TSNS_I_BUF2 Reg 0x02, Bit Field: [13:10], Default: 4'h0, W/R

TSNS_I_CMP Reg 0x02, Bit Field: [9:6], Default: 4'h1, W/R

TSNS_I_MIRROR Reg 0x02, Bit Field: [5:4], Default: 2'h1, W/R

TSNS_I_SOSC Reg 0x02, Bit Field: [3:0], Default: 4'h0, W/R

1.2.4 Register 3 (0x03)

TSNS_MIM Reg 0x03, Bit Field: [18:16], Default: 3'h4, W/R

TSNS_MOM Reg 0x03, Bit Field: [15:13], Default: 3'h4, W/R

TSNS_SEL_VVDD Reg 0x03, Bit Field: [12:9], Default: 4'hE, W/R

TSNS_SEL_STB_TIME Reg 0x03, Bit Field: [8:6], Default: 3'h3, W/R

TSNS_SEL_REF_STB_TIME Reg 0x03, Bit Field: [5:4], Default: 2'h2, W/R

TSNS_SEL_CONV_TIME Reg 0x03, Bit Field: [3:0], Default: 4'h6, W/R

1.2.5 Register 4 (0x04)

TSNS_PDIFF Reg 0x04, Bit Field: [14:0], Default: 15'h0200, W/R

1.2.6 Register 5 (0x05)

TSNS_POLY Reg 0x05, Bit Field: [23:0], Default: 24'h004000, W/R

1.2.7 Register 6 (0x06)

TSNS_DOUT Reg 0x06, Bit Field: [23:0], Default: 24'h000000, R

1.2.8 Register 7 (0x07)

TSNS_INT_RPLY_SHORT_ADDR Reg 0x07, Bit Field: [15:8], Default: 8'h10, W/R

TSNS_INT_RPLY_REG_ADDR Reg 0x07, Bit Field: [7:0], Default: 8'h00, W/R

1.2.9 Register 8 (0x08)

TMR_SLEEP Reg 0x08, Bit Field: [6], Default: 1'h1, W/R

TMR_ISOLATE Reg 0x08, Bit Field: [5], Default: 1'h1, W/R

TMR_RESETB Reg 0x08, Bit Field: [4], Default: 1'h0, W/R

TMR_EN_OSC Reg 0x08, Bit Field: [3], Default: 1'h0, W/R

TMR_RESETB_DIV Reg 0x08, Bit Field: [2], Default: 1'h0, W/R

TMR_RESETB_DCDC Reg 0x08, Bit Field: [1], Default: 1'h0, W/R

TMR_EN_SELF_CLK Reg 0x08, Bit Field: [0], Default: 1'h0, W/R

1.2.10 Register 9 (0x09)

TMR_SEL_CLK_DIV Reg 0x09, Bit Field: [23], Default: 1'h1, W/R

TMR_SEL_CLK_OSC Reg 0x09, Bit Field: [22], Default: 1'h1, W/R

TMR_SELF_EN Reg 0x09, Bit Field: [21], Default: 1'h1, W/R

TMR_IBIAS_REF Reg 0x09, Bit Field: [20:17], Default: 4'h4, W/R

TMR_CASCODE_BOOST Reg 0x09, Bit Field: [16], Default: 1'h0, W/R

TMR_SEL_CAP Reg 0x09, Bit Field: [15:8], Default: 8'h08, W/R

TMR_SEL_DCAP Reg 0x09, Bit Field: [7:2], Default: 6'h04, W/R

TMR_EN_TUNE1 Reg 0x09, Bit Field: [1], Default: 1'h1, W/R

TMR_EN_TUNE2 Reg 0x09, Bit Field: [0], Default: 1'h1, W/R

1.2.11 Register 10 (0x0A)

TMR_S Reg 0x0A, Bit Field: [23:21], Default: 3'h4, W/R

TMR_DIFF_CON Reg 0x0A, Bit Field: [20:7], Default: 14'h3FFB, W/R

TMR_EN_TUNE1_RES Reg 0x0A, Bit Field: [5], Default: 1'h1, W/R

TMR_EN_TUNE2_RES Reg 0x0A, Bit Field: [4], Default: 1'h1, W/R

TMR_SAMPLE_EN Reg 0x0A, Bit Field: [3], Default: 1'h1, W/R

TMR_AFC Reg 0x0A, Bit Field: [2:0], Default: 3'h4, W/R

1.2.12 Register 11 (0x0B)

TMR_TFR_CON Reg 0x0B, Bit Field: [3:0], Default: 4'hF, W/R

1.2.13 Register 23 (0x17)

WUP_ENABLE Reg 0x17, Bit Field: [23], Default: 1'h0, W/R

WUP_LC_IRQ_EN Reg 0x17, Bit Field: [22], Default: 1'h1, W/R

WUP_AUTO_RESET Reg 0x17, Bit Field: [21], Default: 1'h1, W/R

WUP_CLK_SEL Reg 0x17, Bit Field: [20], Default: 1'h0, W/R

WUP_ENABLE_CLK_SLP_OUT Reg 0x17, Bit Field: [19], Default: 1'h0, W/R

WUP_INT_RPLY_SHORT_ADDR Reg 0x17, Bit Field: [15:8], Default: 8'h10, W/R

WUP_INT_RPLY_REG_ADDR Reg 0x17, Bit Field: [7:0], Default: 8'h07, W/R

1.2.14 Register 24 (0x18)

WUP_INT_RPLY_PAYLOAD Reg 0x18, Bit Field: [23:0], Default: 24'h023002, W/R

1.2.15 Register 25 (0x19)

WUP_THRESHOLD_EXT Reg 0x19, Bit Field: [7:0], Default: 8'h00, W/R

1.2.16 Register 26 (0x1A)

WUP_THRESHOLD Reg 0x1A, Bit Field: [23:0], Default: 24'h2DC6C0, W/R

1.2.17 Register 27 (0x1B)

WUP_CNT_VALUE_EXT Reg 0x1B, Bit Field: [7:0], Default: 8'h00, R

1.2.18 Register 28 (0x1C)

WUP_CNT_VALUE Reg 0x1C, Bit Field: [23:0], Default: 24'h000000, R

1.2.19 Register 29 (0x1D)

MBC_WAKEUP_ON_PEND_REQ Reg 0x1D, Bit Field: [5], Default: 1'h0, W/R

MBC_IGNORE_RX_FAIL Reg 0x1D, Bit Field: [4], Default: 1'h1, W/R

LC_CLK_DIV Reg 0x1D, Bit Field: [3:2], Default: 2'h2, W/R

LC_CLK_RING Reg 0x1D, Bit Field: [1:0], Default: 2'h1, W/R