M3 Sensor and Timer (Version 4) Documentation (SNTv4)

Revision 1.0

Yejoong Kim [1], SeokHyeon Jeong[2], Inhee Lee[3] and Taekwang Jang[4]

Michigan Integrated Circuits Laboratory, University of Michigan, Ann Arbor

Last Updated: May 31, 2019

[1] yejoong@umich.edu
[2] seojeong@umich.edu
[3] inhee@umich.edu
[4] tkjang@umich.edu

Contents

I.   Revision History

A.   SNTv1
- First version

B.   SNTv2
- Added power gate to the Timer to fix sleep current issue

C.   SNTv3
- Poly resistor has been replaced with TFR (Timer)
- Pad Update (rev3)

D.   SNTv4
- Increased p+ diffusion resistance for better tuning range (Timer)
- Decreased # of s-oscillator stages (7->3) for better TC (Timer)
- Pad Update (rev4)
- P2 Registers

II. Layer Description

The Sensor and Timer Layer (SNTv4) (Figure II-i & Figure II-ii) contains Temperature Sensor, Timer, and Linear Regulator.

- Designed in TSMC180 tsmc18
- Tapedout on May 6th 2019
- Top-Level layout is located at:
  /afs/eecs.umich.edu/vlsida/projects/m3_hdk/virtuoso/TSMC180/SNTv4/layout
- Top-Level LVS CDL is located at:
  /afs/eecs.umich.edu/vlsida/projects/m3_hdk/layer/SNT/SNTv4/cdl/SNTv4.cdl
- Top-Level Finesim CDL is located at:
  /afs/eecs.umich.edu/vlsida/projects/m3_hdk/layer/SNT/SNTv4/ckt/SNTv4.ckt
- MBUS Long Address is 20'h23004

SNTv4

X: 1050um
Y: 1630um
Z: 150um

X: 1050um
Y: 1630um
Z: 150um

	V3P6	V1P2	V0P6	DIN	DOUT	VSS	CIN	COUT		CLK SLP	

SNTv4

PADS
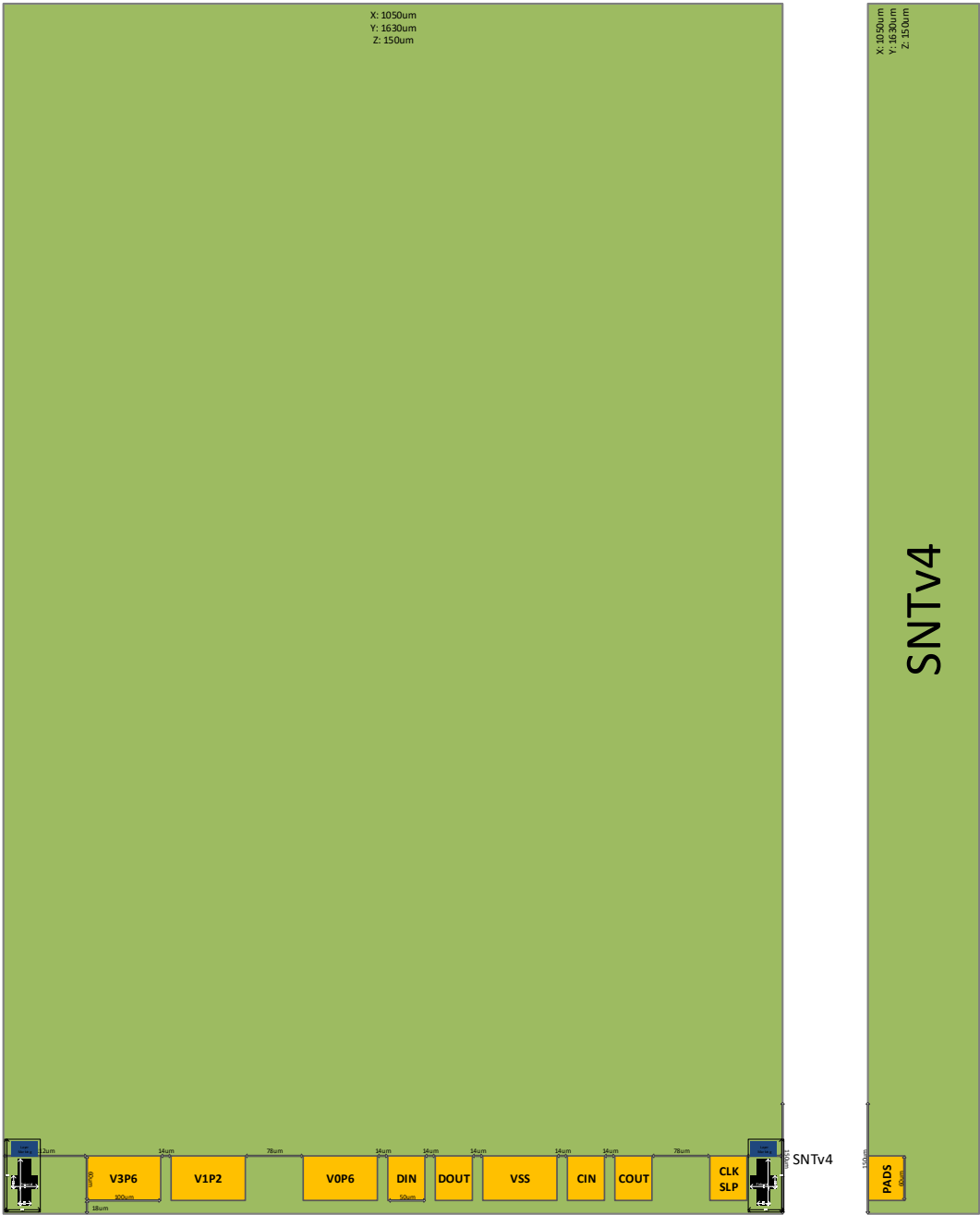
SNTv4

Figure II-i Sensor and Timer Layer (Version 4) (SNTv4) (1050um X 1630um)

5

SNTv4		
Pad	**Pin #**	**Pin Coord**
VBAT	4	C1
V1P2	5	D2
V0P6	7	E1
DIN	8	E2
DOUT	9	F1
VSS	10	F2
CIN	11	G1
COUT	12	G2
CLK_SLP	14	H2

Figure II-ii SNTv4 Wirebonding Diagram

III.   MBUS Register File

A.   Register File Mapping

Please see Table III-1.

Address	Register Name	W/R	Size & Reset	Bit Field	Module
0x00	LDO_ VREF_I_AMP	W/R	4'h0	[9:6]	LDO
	LDO_ SEL_VOUT	W/R	3'h4	[5:3]	
	LDO_EN_VREF	W/R	1'h0	[2]	
	LDO_EN_IREF	W/R	1'h0	[1]	
	LDO_EN_LDO	W/R	1'h0	[0]	
0x01	TSNS_FORCE_CLR_IRQ_IF_EN_IRQ_0	W/R	1'h0	[9]	TEMP_SENS OR
	TSNS_EN_IRQ	W/R	1'h0	[8]	
	TSNS_CONT_MODE	W/R	1'h0	[7]	
	TSNS_BURST_MODE	W/R	1'h0	[6]	
	TSNS_EN_SENSOR_LDO	W/R	1'h0	[5]	
	TSNS_EN_SENSOR_V1P2	W/R	1'h0	[4]	
	TSNS_SEL_LDO	W/R	1'h0	[3]	
	TSNS_SEL_V1P2	W/R	1'h0	[2]	
	TSNS_ISOLATE	W/R	1'h1	[1]	
	TSNS_RESETn	W/R	1'h0	[0]	
0x02	TSNS_R_REF	W/R	4'h8	[21:18]	
	TSNS_I_BUF	W/R	4'h0	[17:14]	
	TSNS_I_BUF2	W/R	4'h0	[13:10]	
	TSNS_I_CMP	W/R	4'h1	[9:6]	
	TSNS_I_MIRROR	W/R	2'h1	[5:4]	
	TSNS_I_SOSC	W/R	4'h0	[3:0]	
0x03	TSNS_MIM	W/R	3'h4	[18:16]	
	TSNS_MOM	W/R	3'h4	[15:13]	
	TSNS_SEL_VVDD	W/R	4'hE	[12:9]	
	TSNS_SEL_STB_TIME	W/R	3'h1	[8:6]	
	TSNS_SEL_REF_STB_TIME	W/R	2'h2	[5:4]	
	TSNS_SEL_CONV_TIME	W/R	4'h6	[3:0]	
0x04	TSNS_PDIFF	W/R	15'h0200	[14:0]	
0x05	TSNS_POLY	W/R	24'h004000	[23:0]	
0x06	TSNS _DOUT	R	24'hX	[23:0]	
0x07	TSNS_INT_RPLY_SHORT_ADDR	W/R	8'h10	[15:8]	
	TSNS_INT_RPLY_REG_ADDR	W/R	8'h00	[7:0]	
0x08	TMR_SLEEP	W/R	1'h1	[6]	Timer
	TMR_ISOLATE	W/R	1'h1	[5]	
	TMR_RESETB	W/R	1'h0	[4]	
	TMR_EN_OSC	W/R	1'h0	[3]	
	TMR_RESETB_DIV	W/R	1'h0	[2]	
	TMR_RESETB_DCDC	W/R	1'h0	[1]	

	TMR_EN_SELF_CLK	W/R	1'h0	[0]	
	TMR_SEL_CLK_DIV	W/R	1'h0	[23]	
	TMR_SEL_CLK_OSC	W/R	1'h1	[22]	
	TMR_SELF_EN	W/R	1'h1	[21]	
	TMR_IBIAS_REF	W/R	4'h4	[20:17]	
0x09	TMR_CASCODE_BOOST	W/R	1'h0	[16]	
	TMR_SEL_CAP	W/R	8'h80	[15:8]	
	TMR_SEL_DCAP	W/R	6'h3F	[7:2]	
	TMR_EN_TUNE1	W/R	1'h1	[1]	
	TMR_EN_TUNE2	W/R	1'h1	[0]	
	TMR_S	W/R	3'h1	[23:21]	
	TMR_DIFF_CON	W/R	14'h3FFF	[20:7]	
	TMR_EN_TUNE1_RES	W/R	1'h1	[5]	
0x0A	TMR_EN_TUNE2_RES	W/R	1'h1	[4]	
	TMR_SAMPLE_EN	W/R	1'h1	[3]	
	TMR_AFC	W/R	3'h4	[2:0]	
0x0B	TMR_TFR_CON	W/R	4'hF	[3:0]	
	WUP_ENABLE	W/R	1'h0	[23]	
	WUP_LC_IRQ_EN	W/R	1'h1	[22]	
	WUP_AUTO_RESET	W/R	1'h1	[21]	
0x17	WUP_CLK_SEL	W/R	1'h0	[20]	
	WUP_ENABLE_CLK_SLP_OUT	W/R	1'h0	[19]	
	WUP_INT_RPLY_SHORT_ADDR	W/R	8'h10	[15:8]	
	WUP_INT_RPLY_REG_ADDR	W/R	8'h07	[7:0]	
0x18	WUP_INT_RPLY_PAYLOAD	W/R	24'h023002	[23:0]	
0x19	WUP_THRESHOLD_EXT	W/R	8'h00	[7:0]	
0x1A	WUP_THRESHOLD	W/R	24'h2DC6C0	[23:0]	
0x1B	WUP_CNT_VALUE_EXT	R	8'hx	[7:0]	
0x1C	WUP_CNT_VALUE	R	24'hX	[23:0]	
	MBC_WAKEUP_ON_PEND_REQ	W/R	1'h0	[5]	
0x1D	LC_CLK_DIV	W/R	2'h2	[3:2]	
	LC_CLK_RING	W/R	2'h1	[2:1]	
0x20	RF2_ISOLATE	W/R	1'h0	[1]	
	RF2_SLEEP	W/R	1'h0	[0]	

Table III-1 Register File Mapping

B.   Register Descriptions

LDO_ VREF_I_AMP
Controls bias current of body buffers used in the voltage reference.

LDO_ SEL_VOUT
Controls output voltage level of the LDO.

LDO_EN_VREF
Enables voltage reference.

LDO_EN_IREF

Enables current reference.

LDO_EN_LDO

Controls power gate of the LDO (from VBAT).

TSNS_FORCE_CLR_IRQ_IF_EN_IRQ_0

Enables CLK_{REF} monitoring through debug pads.

TSNS_EN_CLK_REF

Enables CLK_{REF} monitoring through debug pads.

TSNS_EN_CLK_SENS

Enables CLK_{SENSE} monitoring through debug pads.

TSNS_EN_IRQ

Enables Interrupt for the temperature sensor.

TSNS_CONT_MODE

Enables TEMP_SENSOR's Continuous Mode. This mode eliminates startup time by keeping the sensor always-on (i.e., no power gating). Therefore, (TSNS_EN_SENSOR_LDO or TSNS_EN_SENSOR_V1P2) and (TSNS_SEL_LDO or TSNS_SEL_V1P2) should be kept high for this mode.

TSNS_BURST_MODE

Enables TEMP_SENSOR's Burst Mode. Requires TSNS_CONT_MODE=1'h1. In addition to TSNS_CONT_MODE, this mode starts conversion as soon as asserted CLR signal is cleared.

TSNS_EN_SENSOR_LDO

Power gate signal (Active low). Selects LDO as analog power source.

TSNS_EN_SENSOR_V1P2

Power gate signal (Active low). Selects V1P2 as analog power source.

TSNS_SEL_LDO

Power gate signal (Active low). Selects LDO as digital power source.

TSNS_SEL_V1P2

Power gate signal (Active low). Selects V1P2 as digital power source.

TSNS_ISOLATE

Isolates clock signals (CLK_{SENSE} and CLK_{REF}) from digital block.

TSNS_RESETn

Global reset. Starts conversion when released.

TSNS_R_REF

Adjusts resistance of the current source. Increasing this value will increase current.

TSNS_I_BUF

Adjusts the buffer bias current (Current REF). Increasing this value will increase current.

TSNS_I_BUF2

Adjusts the buffer bias current (Composite Resistor). Increasing this value will increase current.

TSNS_I_CMP

Adjusts the comparator bias current. Increasing bit increases comparator speed and thus improves temperature coefficient (TC) of the reference clock (CLK_{REF}) at the cost of higher power consumption. TC improves until comparator delay becomes negligible to the overall period.

TSNS_I_MIRROR

Adjusts main current. Increasing this value will increase current.

TSNS_I_SOSC

Adjusts speed of the start-up oscillator. Increasing this value will increase current which also increases the frequency of the oscillator.

TSNS_MIM

Adjusts MIM cap size. Increasing this value will decrease frequency.

TSNS_MOM

Adjusts MOM cap size. Increasing this value will decrease frequency.

TSNS_SEL_VVDD

Adjusts virtual VDD of the CLK_{SENS}. Increasing this value will increase CLK_{SENS}.

TSNS_SEL_STB_TIME

Controls the start-up time (tstartup, Time between TSNS_RESETn and internal start signal). Analog part of the temperature needs certain start-up time for its internal voltages to stabilize after a releasing its power gate (TSNS_EN_SENSOR_LDO or TSNS_EN_SENSOR_V1P2). This start-up time is controlled with a speed of the start-up oscillator (TSNS_I_SOSC) and asynchronous 10-bit counter (TSNS_SEL_STB_TIME). Higher bit results longer start-up time.

TSNS_SEL_STB_TIME	0	1	2	3	4	5	6	7
Counter bit	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}

Table III-2 Counter bit vs TSNS_SEL_STB_TIME

There are 2 parts that need to stabilize upon a power gate release; 1) a sensing clock (CLK_{SENSE}) and 2) a current reference inside the reference clock (CLK_{REF}). At low temperature (≤-10°C), sensing clock is a bottle neck. However, current reference becomes a bottle neck for higher temperatures.

Temp. (°C)	CLK_{SENSE}				CLK_{REF}							
	Time (ms)				Time (ms)				Number of Cycles			
	Mean	Std	Max	Min	Mean	Std	Max	Min	Mean	Std	Max	Min
-30	8.58	4.03	28.86	1.83	3.02	1.36	8.10	0.319	15.5	5.82	37	5
-10	2.65	1.12	7.94	0.7	2.79	1.26	7.39	0.257	16.3	6.15	37	5
10	0.99	0.40	2.95	0.28	2.67	1.14	6.81	0.0961	17.3	6.18	38	5
30	0.44	0.16	1.14	0.13	2.59	1.04	6.35	0.0608	18.5	6.19	40	5
50	0.22	0.074	0.55	0.067	2.57	0.928	5.98	0.0451	20.0	6.08	41	5
70	0.12	0.037	0.27	0.041	2.5	0.856	5.67	0.144	21.0	6.12	42	5

90	0.069	0.020	0.16	0.027	2.47	0.784	5.39	0.0649	22.5	6.10	45	5
110	0.043	0.012	0.089	0.017	2.47	0.759	5.26	0.126	24.3	6.39	54	5
130	0.028	0.007	0.054	0.011	2.81	0.799	5.55	0.0476	29.3	6.85	64	5

Table III-3 Stabilization time vs temperature (CLK_{SENS} and CLK_{REF})

TSNS_SEL_REF_STB_TIME

Controls the stabilization time (t_{stb}) of the reference clock (CLK_{REF}) after releasing internal start signal. Stabilization time is controlled with a speed of the reference clk (CLK_{REF}) and synchronous 4-bit counter (TSNS_SEL_REF_STB_TIME). Increasing control bit increases stabilization time. When designated value is reached, RST_Counter gets released and count starts.

TSNS_SEL_REF_STB_TIME	0	1	2	3
Counter bit	2^1	2^2	2^3	2^4

Table III-4 Counter bit vs TSNS_SEL_REF_STB_TIME

TSNS_SEL_CONV_TIME

Controls the conversion time (t_{conv}) of the temperature sensor. Increasing control bit increases conversion time. It will cause more energy consumption at the expense of better resolution.

Conversion Time = Counter bit / Frequency of CLK_{REF}

TSNS_SEL_CONV_TIME	0	1	2	3	4	5	6	7
Counter bit	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}
Conversion time(ms)	1.8	3.6	7.1	14.2	28.4	56.9	113.8	227.6

TSNS_SEL_CONV_TIME	8	9	10	11	12	13	14	15
Counter bit	2^{13}	2^{14}	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
Conversion time(s)	0.5	0.9	1.8	3.6	7.3	14.6	29.1	58.3

Table III-5 TSNS_SEL_CONV_TIME vs Conversion time (when $Freq_{CLK\_REF}$=18kHz)

TSNS_PDIFF

Adjusts P+ diffusion resistor size. Increasing the value (decreasing the resistance) will make period more CTAT.

TSNS_POLY

Adjusts P+ poly resistor size. Increasing the value (decreasing the resistance) will make period more PTAT.

TSNS _DOUT

Digital output of temperature.

TSNS_INT_RPLY_SHORT_ADDR

TSNS_INT_RPLY_REG_ADDR

TMR_SLEEP

Power gate signal (Active high).

TMR_ISOLATE

Isolates timer output.

TMR_RESETB

Global reset.

TMR_EN_OSC

Enables s-oscillator .

TMR_RESETB_DIV

Digital output of temperature.

TMR_RESETB_DCDC

Reset signal for DC-DC converter which generates bias voltages for the amplifier.

TMR_EN_SELF_CLK

Selects clock source for the DC-DC converter.

- 0: External clock. Source based on TMR_SEL_CLK_OSC
- 1: Self-clocking. Source based on TMR_SEL_CLK_DIV

TMR_SEL_CLK_DIV

Selects self-clocking division ratio. Effective only if TMR_EN_SELF_CLK = 1'h1.

- 0: No division (FVCO)
- 1: Divided by 2 (DIV)

TMR_SEL_CLK_OSC

Selects external clock source. Effective only if TMR_EN_SELF_CLK = 1'h0.

- *0: External clock (obsolete)*
- 1: S-oscillator.

TMR_SELF_EN

Selects current source for the amplifier bias voltage generator.

- 0 : Uses off-state MOS to generate current
- 1: Uses switched cap to generate current with the timer output clock (i.e. self-clocking). Output clock needs to be stabilized before enable this configuration.

TMR_IBIAS_REF

Controls current level in the amplifier bias voltage generator. Increasing this value will increase current level.

TMR_CASCODE_BOOST

Controls bias voltages in the amplifier bias voltage generator. Has been implemented mainly to cover different between the thick and thin model in TSMC180.

TMR_SEL_CAP

Controls capacitor size in the main switched-cap based resistor. Increasing this value will increase capacitance (i.e. decrease frequency). Effectiveness depends on TMR_EN_TUNE1 and TMR_EN_TUNE2. See below for details.

TMR_SEL_CAP	[0]	[1]	[2]	[3]
Capacitance	146.0fF	291.8fF	578.5fF	1.14pF
Effective only if	TMR_EN_TUNE2=1	TMR_EN_TUNE1=1	TMR_EN_TUNE2=1	N/A

TMR_SEL_CAP	[4]	[5]	[6]	[7]
Capacitance	2.28pF	4.67pF	8.96pF	17.9pF
Effective only if	TMR_EN_TUNE2=1			TMR_EN_TUNE1=1

Table III-6 Capacitance value and their dependence on TMR_EN_TUNE1 and TMR_EN_TUNE2

TMR_SEL_DCAP

Controls decoupling capacitance on the switched capacitor node. Increasing this value will increase decap. There is default decap of 2pF. Effectiveness depends on TMR_EN_TUNE1 and TMR_EN_TUNE2. See below for details.

TMR_SEL_DCAP	[0]	[1]	[2]
Capacitance	2pF	4pF	6pF
Effective only if	TMR_EN_TUNE1=1	TMR_EN_TUNE2=1	N/A

TMR_SEL_DCAP	[3]	[4]	[5]
Capacitance	16pF	32pF	Obsolete
Effective only if	TMR_EN_TUNE2=1		TMR_EN_TUNE1=1

Table III-7 Decap value and their dependence on TMR_EN_TUNE1 and TMR_EN_TUNE2

TMR_EN_TUNE1

Controls effective switching capacitance and decap along with TMR_SEL_CAP and TMR_SEL_DCAP. Refer to Table III-6 and Table III-7 for details.

TMR_EN_TUNE2

Controls effective switching capacitance and decap along with TMR_SEL_CAP and TMR_SEL_DCAP. Refer to Table III-6 and Table III-7 for details.

TMR_S

Control duty cycle ratio of the resistor. Increasing this value will increase effective resistance (i.e. decrease frequency).

TMR_S	0	1	2	3	4	5	6	7
Division Ratio	N/A	2	4	8	16	32	16	32
Duty cycle (%)	No duty cycle Always on	50	25	12.5	6.25	3.125	6.25	3.125

Table III-8 Division ratio vs S

TMR_DIFF_CON

Adjusts P+ diffusion resistor size. Increasing the value (increasing the resistance) will make period more PTAT.

TMR_EN_TUNE1_RES

Adds following leakage currents in the main current branch from the supply (active low).

- × 2 minimum size off-state PMOSsubthreshold leakage
- × 2 minimum size off-state PMOS body to drain/source leakage

TMR_EN_TUNE2_RES

Adds following leakage currents in the main current branch from the supply (active low).

- × 5 minimum size off-state PMOSsubthreshold leakage
- × 3 minimum size off-state PMOS body to drain/source leakage

TMR_SAMPLE_EN

Enables VCO control voltage sampling.

TMR_AFC

Controls VCO gain. Increasing this value will increase VCO gain.

TMR_TFR_CON

Adjusts thin film resistor (TFR) size. Increasing the value (decreasing the resistance) will make period more PTAT.

WUP_ENABLE

.

WUP_LC_IRQ_EN

.

WUP_AUTO_RESET

.

WUP_CLK_SEL

.

WUP_ENABLE_CLK_SLP_OUT

.

WUP_INT_RPLY_SHORT_ADDR

.

WUP_INT_RPLY_REG_ADDR

.

WUP_INT_RPLY_PAYLOAD

.

WUP_THRESHOLD_EXT

.

WUP_THRESHOLD

.

WUP_CNT_VALUE_EXT

.

WUP_CNT_VALUE

.

MBC_WAKEUP_ON_PEND_REQ

.

LC_CLK_DIV

Layer Controller's Clock Divider. See Table III-9. Used in conjunction with **Error! Not a valid bookmark self-reference.**.

Value	Clock Division
2'h0	8
2'h1	4
2'h2	2
2'h3	0

Table III-9 LC_CLK_DIV Register

LC_CLK_RING

Layer Controller's Ring Oscillator's Speed. See Table III-10 & Table III-11 for post-pex simulation results. Use in conjunction with LC_CLK_DIV.

27°C LC_CLK_DIV: 2'h3						
V0P6 (V)	0.45	0.50	0.55	0.60	0.65	0.70
V1P2 (V)	0.90	1.00	1.10	1.20	0.30	1.40
LC_CLK_RING: 2'h3						
Frequency (KHz)	38.6	64.7	95.4	129	166	204
V0P6 Power (nW)	7.64	17.2	33.3	58.0	93.2	141
V1P2 Power (nW)	3.78	6.62	12.0	19.6	29.7	43.0
V0P6 Leakage (pW)	94.0	107	121	135	150	166
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h2						
Frequency (KHz)	31.8	53.3	78.6	107	137	169
V0P6 Power (nW)	6.30	14.2	27.5	47.8	76.8	116
V1P2 Power (nW)	2.60	5.60	9.90	16.0	24.4	35.5
V0P6 Leakage (pW)	96.8	110	125	140	154	171
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h1						
Frequency (KHz)	27.1	45.4	67.0	90.8	116	144
V0P6 Power (nW)	5.4	12.1	23.5	40.8	65.6	99.2

V1P2 Power (nW)	2.4	4.7	8.6	13.6	20.9	30.3
V0P6 Leakage (pW)	96.8	110	125	140	155	171
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h0						
Frequency (KHz)	24.1	40.4	59.7	80.9	104	128
V0P6 Power (nW)	4.9	10.8	20.9	36.3	58.4	88.4
V1P2 Power (nW)	2.0	4.2	7.5	12.1	18.7	27.0
V0P6 Leakage (pW)	99.4	114	129	144	159	177
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0

Table III-10 LC_CLK_RING Register Post-Pex Results (27°C) (TT)[5]

40°C **LC_CLK_DIV: 2'h3**						
V0P6 (V)	0.45	0.50	0.55	0.60	0.65	0.70
V1P2 (V)	0.90	1.00	1.10	1.20	0.30	1.40
LC_CLK_RING: 2'h3						
Frequency (KHz)	43.4	70.0	100	134	170	207
V0P6 Power (nW)	8.9	19.2	36.2	61.6	97.5	145
V1P2 Power (nW)	3.7	7.3	12.7	20.4	30.7	43.9
V0P6 Leakage (pW)	189	216	244	273	303	335
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h2						
Frequency (KHz)	35.7	57.6	83.0	111	140	171
V0P6 Power (nW)	7.4	15.9	29.9	50.9	80.4	120
V1P2 Power (nW)	3.0	6.0	10.6	16.8	25.3	36.2
V0P6 Leakage (pW)	196	223	252	282	313	346
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h1						
Frequency (KHz)	30.4	49.1	70.8	94.3	119	145
V0P6 Power (nW)	6.4	13.6	25.5	44.5	68.7	103
V1P2 Power (nW)	2.5	5.2	8.9	14.4	21.7	31.1
V0P6 Leakage (pW)	195	220	252	282	313	346
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0
LC_CLK_RING: 2'h0						
Frequency (KHz)	27.1	43.7	63.0	83.9	106	129
V0P6 Power (nW)	5.7	12.1	22.8	38.7	61.2	91.3
V1P2 Power (nW)	2.4	4.6	8.1	12.8	19.3	27.7
V0P6 Leakage (pW)	202	230	260	291	323	357
V1P2 Leakage (pW)	≈0	≈0	≈0	≈0	≈0	≈0

Table III-11 LC_CLK_RING Register Post-Pex Results (40°C) (TT)[6]

RF2_ISOLATE

.

---

[5] Leakage Power does not include power-gating
[6] Leakage Power does not include power-gating

RF2_SLEEP

.

IV. TEMP_SENSOR

This is a temperature Sensor designed by SeokHyeon Jeong. The sensor has been designed for -30°C to 130°C temperature range and consumes ~250nW at 25°C when active.

Figure IV-i shows the TEMP_SENSOR block diagram. It consists of analog and digital block where analog block consists of sensing clock and reference clock while digital block consists of a start-up circuit and a digital processing backend. The sensor can be power gated to minimize power consumption when not being used. Calibration and post processing are required to translate the output code into temperature (See "Calibration and Post-processing" for details).
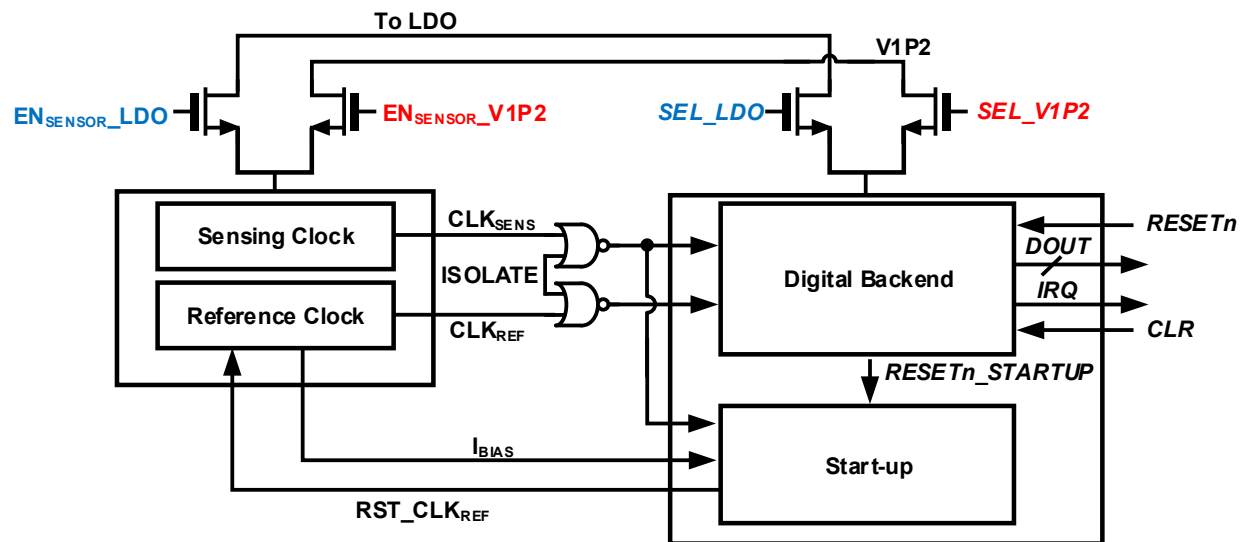
Figure IV-i TEMP_SENSOR Block Diagram

A.   Power Domains

Temperature sensor has been designed to operate from a supply voltage ranging from 1.0V to 1.4V. It can choose to operate either from VDD_1P2 generated from PMU for VDD_LDO generated from LDO. See "LDO" for details regarding the block itself. As LDO provides regulated output voltage, running off of LDO provides better supply sensitivity compared to PMU VDD_1P2.

- VDD_1P2 (from PMU)
- VDD_LDO (from LDO)

B.   Interrupt Considerations

Interrupts when request is serviced (after ≈ 0.5s)

C.   Power Draw / Current Draw / Energy Consumption

Mode	V1P2 (1.2V)
Active	210nA
Standby	

Table IV-1 TEMP_SENSOR Current Draw

D.   Operation

- **Startup sequence**
    - o **Using PMU V1P2 as a power source**
        1. Un-powergate digital block
            TSNS_SEL_V1P2   -> 1'h1

        2. Un-powergate analog block
            TSNS_EN_SENSOR_V1P2   -> 1'h1

        3. Start TEMP_SENSOR
            TSNS_ISOLATE   -> 1'h0
            TSNS_RESETn   -> 1'h1

    - o **Using LDO as a power source**
        1. Un-powergate voltage reference in LDO. Voltage reference consumes only tens of pA so it requires some stabilization time (~30ms)
            LDO_EN_VREF   -> 1'h1

        2. Un-powergate the current reference and the main amplifier in LDO
            LDO_EN_IREF   -> 1'h1
            LDO_EN_LDO   -> 1'h1

        3. Un-powergate digital block
            TSNS_SEL_LDO   -> 1'h1

        4. Un-powergate analog block
            TSNS_EN_SENSOR_LDO   -> 1'h1

        5. Start TEMP_SENSOR
            TSNS_ISOLATE   -> 1'h0
            TSNS_RESETn   -> 1'h1

- **Timing diagram**

    TEMP_SENSOR has 3 different operating modes. See following diagrams for details. Related parameters that effect timing are as follows.

    TSNS_SEL_STB_TIME ($t_{startup}$)
    TSNS_SEL_REF_STB_TIME (t_{stb})
    TSNS_SEL_CONV_TIME (t_{conv})
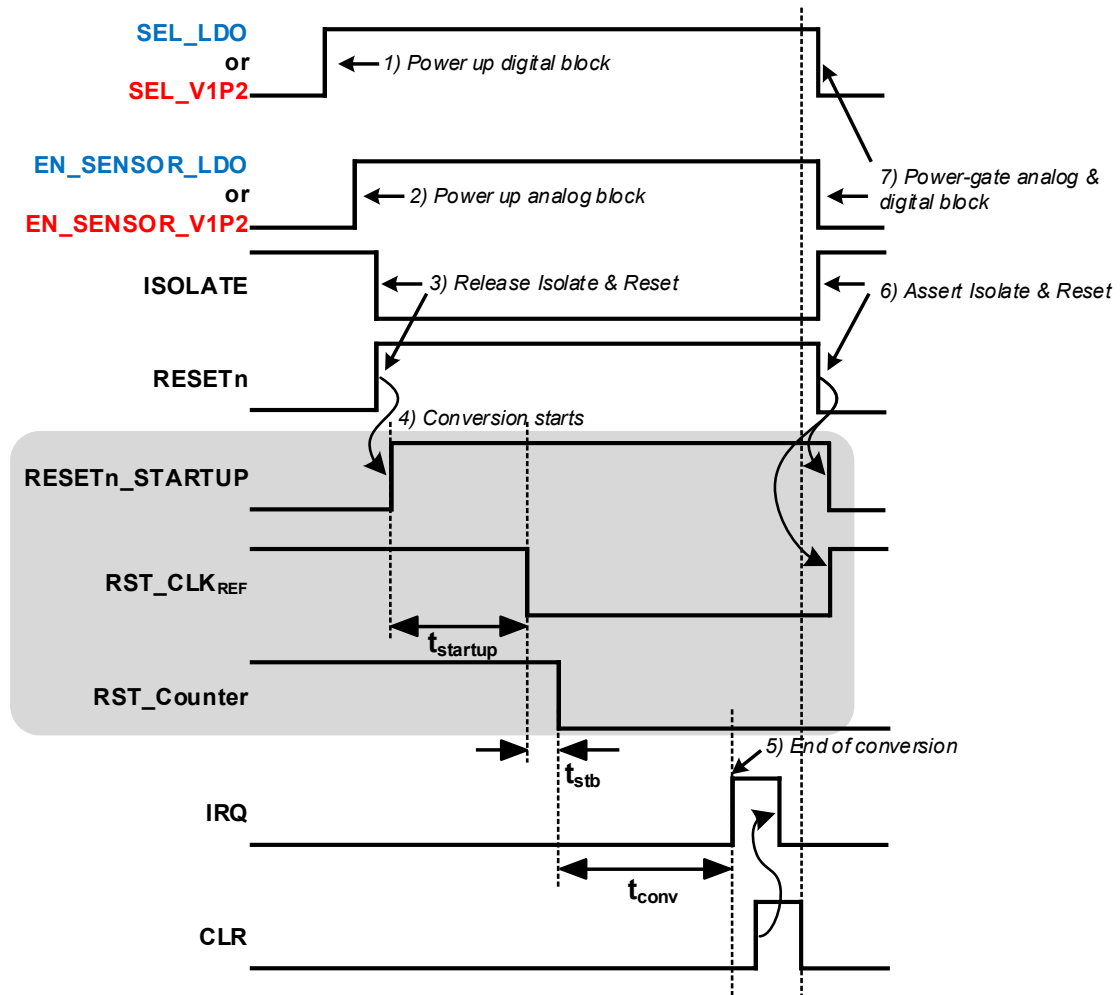
A. Normal operation

Figure IV-ii TEMP_SENSOR Timing Diagram (Normal operation, i.e., TSNS_CONT_MODE=0 & TSNS_BURST_MODE = 0)
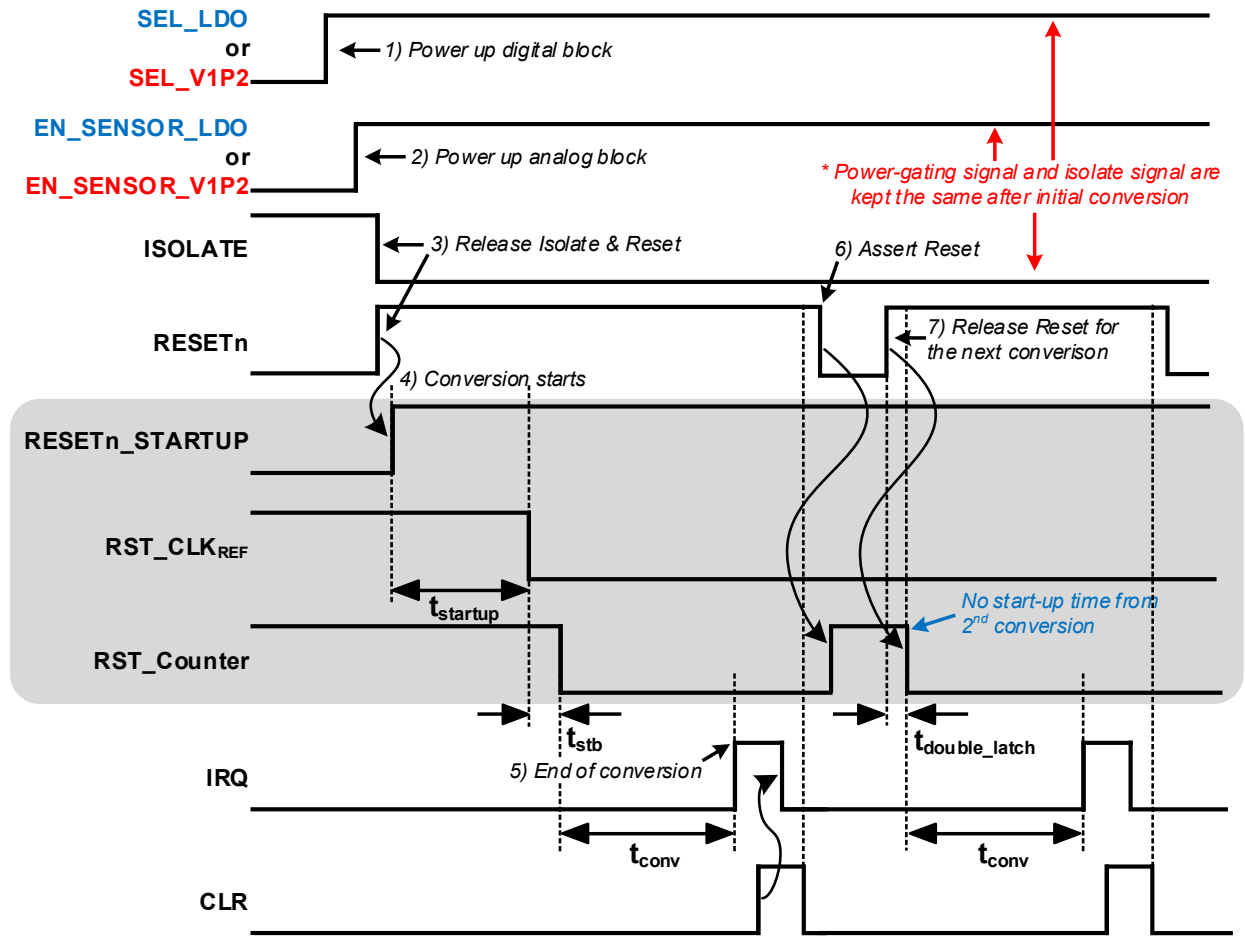
B. Continuous Mode

Figure IV-iii TEMP_SENSOR Timing Diagram (Continuous mode operation, i.e., TSNS_CONT_MODE=1 & TSNS_BURST_MODE = 0)
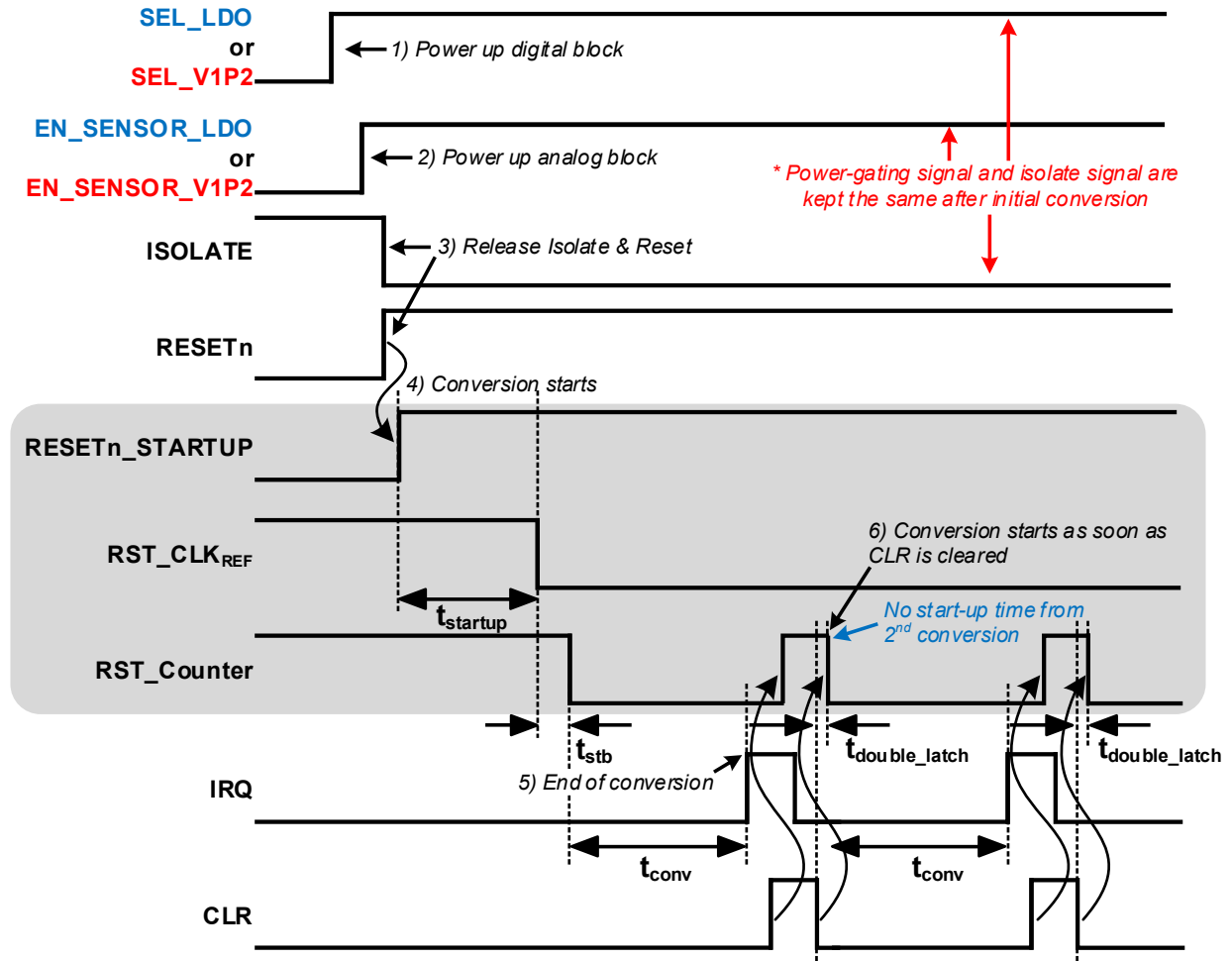
C. Burst Mode

Figure IV-iv TEMP_SENSOR Timing Diagram (Burst mode operation, i.e., TSNS_CONT_MODE=1 & TSNS_BURST_MODE = 1)

E.   Calibration and Post-processing

Output code requires post-processing in order to get linear relationship between output code (TSNS _DOUT) and temperature. Following equation shows aforementioned post-processing.

$$Code_{Post-processing} = \ln\left(\frac{\text{TSNS\_DOUT} \times f_{CLK\_REF}}{2^{(\text{TSNS\_SEL\_CONV\_TIME}+5)}}\right) \times [Temperature(°C) + 273]$$

$$where\ f_{CLK_{REF}} = 17.5kHz$$

Calibration can be done using the post-processed codes ($Code_{Post-processing}$).

- **Two-point calibration**
  Use two post-processed codes to get first order coefficient **a** and **b** (**a**T+**b**).

  ex) Code$_{post-prcessing}$= 1140 @ 20°C & Code$_{post-prcessing}$= 1707 @ 80°C

  a = (1707-1140)/(80-20) = 9.45

  b= 1140 − (20+273)×9.45 = -1628.85

- **One-point calibration**
  Get offset **b** using predetermined slope **a**.

After getting coefficients (**a** and **b**) with the calibration, use following equation to get temperature from the code.

$$Temperature(°C) = \frac{-b}{a - \ln\left(\frac{\text{TSNS\_DOUT} \times f_{CLK\_REF}}{2^{(\text{TSNS\_SEL\_CONV\_TIME}+5)}}\right)} - 273$$

Figure IV-v (left) shows measurement error across 26 chips after 2-pt calibration. Figure IV-v (right) shows error after 3rd order batch calibration. Batch calibration is based on an average error resulting from 2-pt calibration.
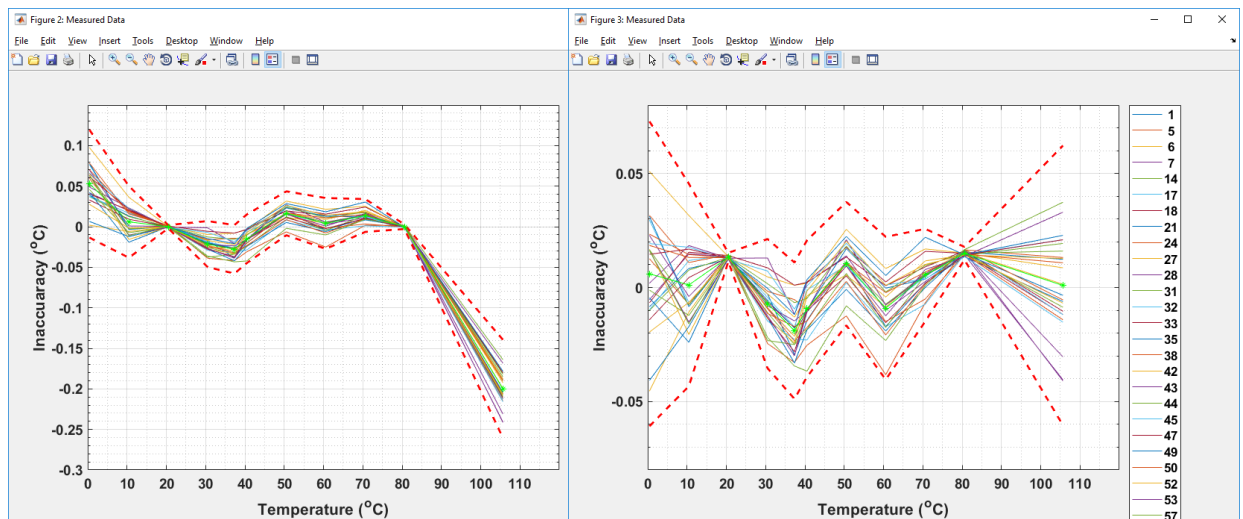
Figure IV-v Sensor accuracy after 2-pt calibration (left) and after 2pt + batch calibration (right)

V. Timer

This is a wakeup timer originally designed by Taekwang Jang. The timer has been designed for -25°C to 85°C temperature range and outputs 1-2kHz frequency.

Figure IV-i shows the block diagram of the wakeup timer.
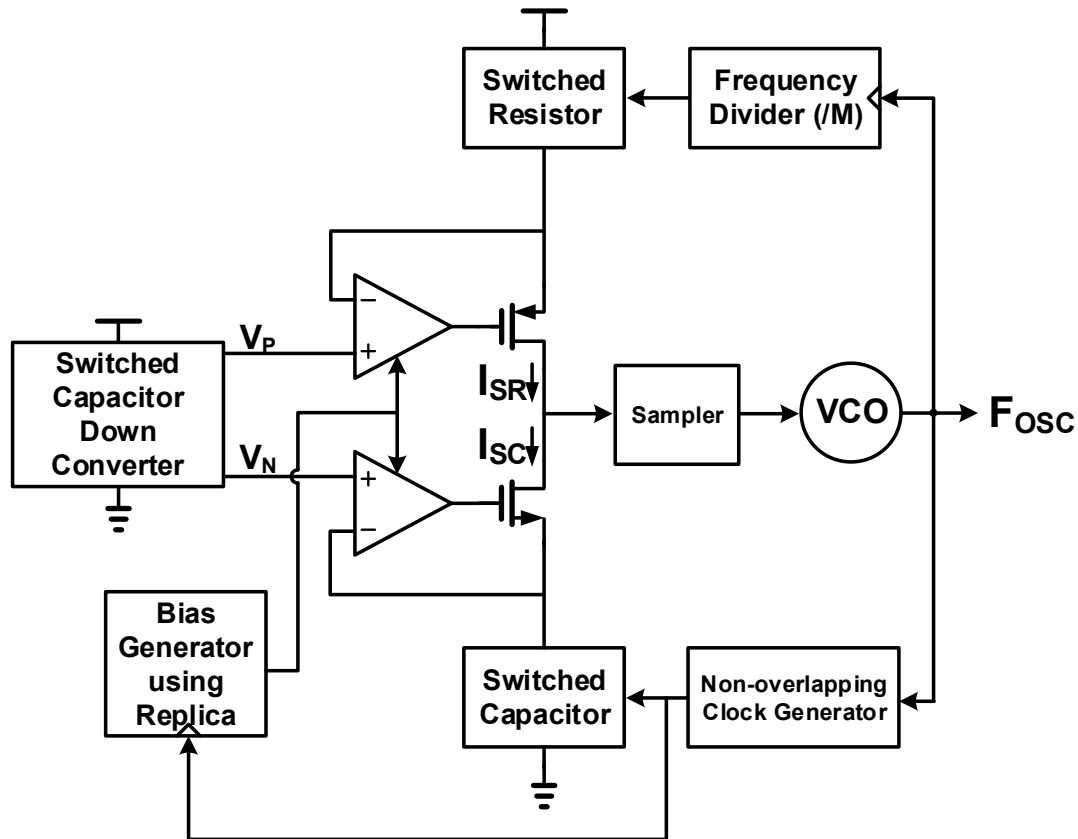
Figure V-i Timer Block Diagram

A. Power Domains

- VDD_1P2 (from PMU)

B. Power Draw / Current Draw / Energy Consumption

Mode	V1P2 (1.2V)
Active	5nA
Standby	

Table V-1 TEMP_SENSOR Current Draw

C. Operation

- **Startup sequence**
  1. Un-powergate timer and release isolate
     TMR_SLEEP   -> 1'h0
     TMR_ISOLATE   -> 1'h0

2. Start s-oscillator
   TMR_EN_OSC   -> 1'h1

3. Release reset
   TMR_RESETB   -> 1'h1
   TMR_RESETB_DIV   -> 1'h1
   TMR_RESETB_DCDC   -> 1'h1

4. Enable self-clocking
   TMR_EN_SELF_CLK   -> 1'h1
   TMR_SELF_EN   -> 1'h1

5. Disable s-oscillator
   TMR_EN_OSC   -> 1'h0

- Temperature Coefficient (TC)
  Temperature coefficient of the output frequency can be tuned with following parameters. Refer to their descriptions for usage.
  TMR_DIFF_CON
  TMR_TFR_CON

- Frequency Tuning
  Output frequency can be tuned with following parameters. Refer to their descriptions for usage.
  TMR_SEL_CAP
  TMR_S

  *Although TMR_DIFF_CON / TMR_TFR_CON can adjust frequency, it is not recommended as they will affect TC.

VI.   LDO

This is a Linear Regulator used to regulate VDD of TEMP_SENSOR, originally designed by Inhee Lee. See Figure VI-i & Figure VI-ii.

A.   Power Domains

- VDD_3P6
- VDD_1P2
- TEMP_SENSOR's VDD

B.   Operation

- Select desired output voltage via LDO_ SEL_VOUT.
- Select desired amplifier current via LDO_ VREF_I_AMP.

Enable LDO's Reference via LDO_ VREF_I_AMP

Controls bias current of body buffers used in the voltage reference.

LDO_ SEL_VOUT

Controls output voltage level of the LDO.

- LDO_EN_VREF (Active High).
- Enable LDO IREF & output via LDO_ VREF_I_AMP & LDO_ SEL_VOUT (Active High).

Figure VI-i LDO_TOP Block Diagram
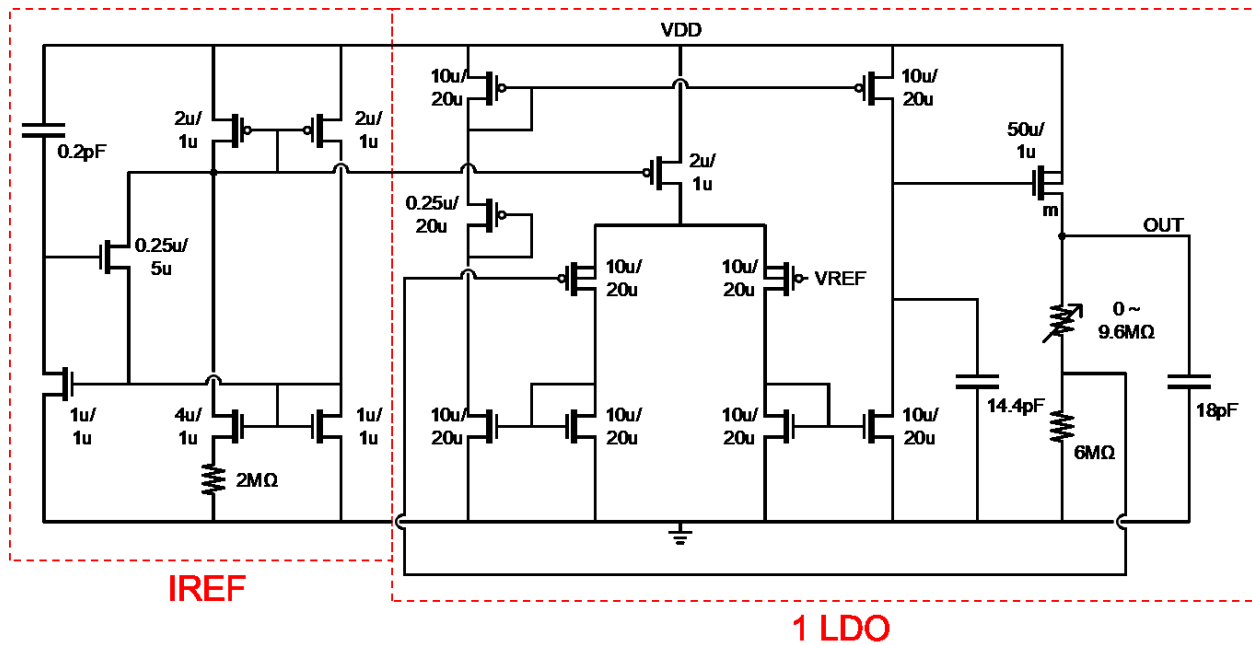
Figure VI-ii IREF+1 LDO

VDD_3P6 Drop at LDO ON

- Transient Simulation
- Connected 5kohm between VDD_3P6 & circuits
- Connected 1nF to supply of the circuits (VDD_3P6x)
- Measured the maximum voltage drop of VDD_3P6x

VDD_3P6 Voltage Drop [V]

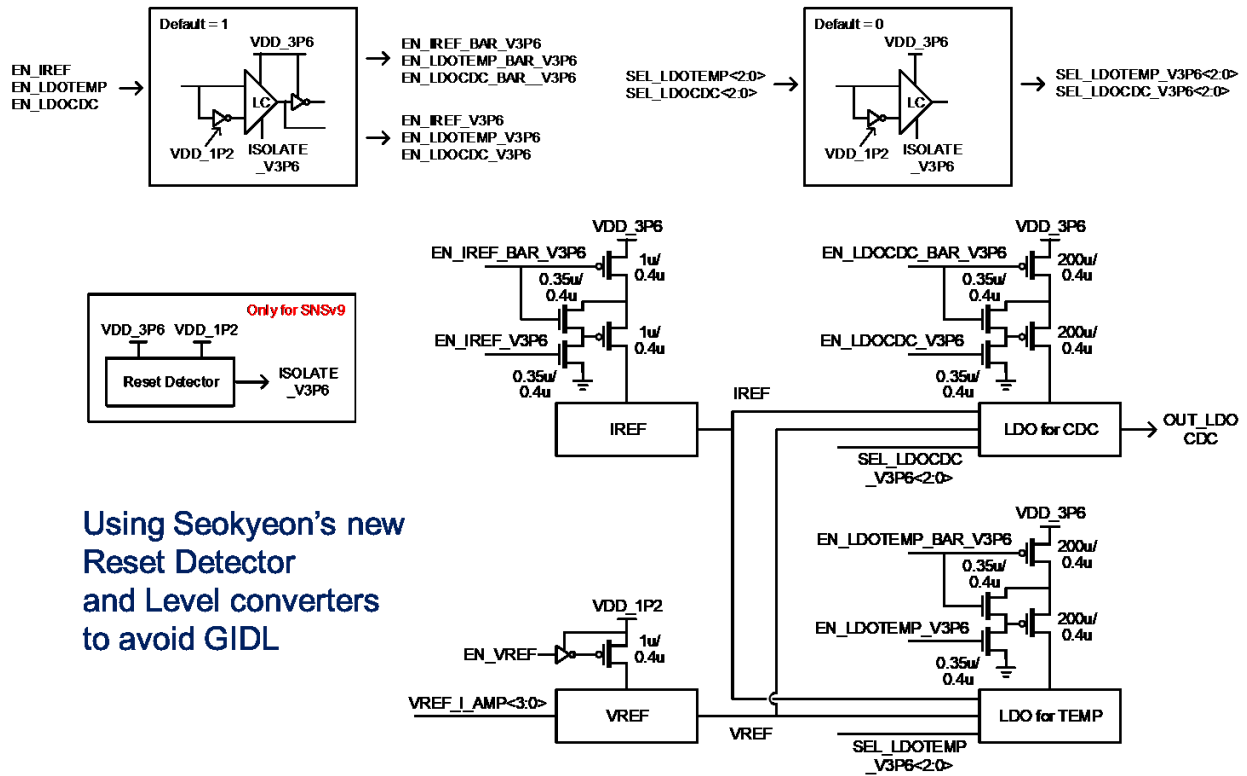| Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	7.51E-03	7.71E-03	7.32E-03	7.51E-03	7.51E-03
27	1.1	2.5	5.28E-03	5.49E-03	5.11E-03	5.28E-03	5.29E-03
27	1.1	4.2	5.29E-03	5.49E-03	5.11E-03	5.28E-03	5.30E-03
27	1.4	2.5	1.00E-02	1.02E-02	9.87E-03	1.00E-02	1.00E-02
27	1.4	4.2	1.00E-02	1.02E-02	9.87E-03	1.00E-02	1.00E-02
-40	1.1	2.5	5.18E-03	5.39E-03	4.99E-03	5.18E-03	5.17E-03
-40	1.1	4.2	5.18E-03	5.39E-03	5.00E-03	5.18E-03	5.18E-03
-40	1.4	2.5	9.92E-03	1.01E-02	9.70E-03	9.91E-03	9.91E-03
-40	1.4	4.2	9.91E-03	1.01E-02	9.69E-03	9.92E-03	9.90E-03
130	1.1	2.5	5.47E-03	5.66E-03	5.27E-03	5.47E-03	5.46E-03
130	1.1	4.2	5.47E-03	5.66E-03	5.27E-03	5.47E-03	5.46E-03
130	1.4	2.5	1.02E-02	1.03E-02	1.00E-02	1.02E-02	1.02E-02
130	1.4	4.2	1.02E-02	1.03E-02	1.00E-02	1.02E-02	1.02E-02

Charge Loss from VDD_3P6 at LDO ON

- Transient Simulation
- Measured charge loss from VDD_3P6 when 'IREF + 2 LDOs' are turned on
- I(VDD_3P6) < 1uA @ outside of the integration window

Charge Loss from VDD_3P6 [C]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	8.14E-12	8.29E-12	8.00E-12	8.13E-12	8.15E-12
27	1.1	2.5	5.75E-12	5.96E-12	5.57E-12	5.75E-12	5.76E-12
27	1.1	4.2	1.08E-11	1.09E-11	1.07E-11	1.08E-11	1.08E-11
27	1.4	2.5	5.75E-12	5.96E-12	5.58E-12	5.75E-12	5.76E-12
27	1.4	4.2	1.08E-11	1.09E-11	1.07E-11	1.08E-11	1.08E-11
-40	1.1	2.5	5.38E-12	5.85E-12	4.87E-12	5.66E-12	5.15E-12
-40	1.1	4.2	1.04E-11	1.08E-11	1.02E-11	1.05E-11	1.03E-11
-40	1.4	2.5	5.38E-12	5.85E-12	4.87E-12	5.67E-12	5.15E-12
-40	1.4	4.2	1.04E-11	1.08E-11	1.02E-11	1.05E-11	1.03E-11
130	1.1	2.5	6.04E-12	6.21E-12	5.85E-12	6.06E-12	6.02E-12
130	1.1	4.2	1.11E-11	1.12E-11	1.10E-11	1.11E-11	1.11E-11
130	1.4	2.5	6.04E-12	6.22E-12	5.85E-12	6.06E-12	6.03E-12
130	1.4	4.2	1.11E-11	1.12E-11	1.10E-11	1.11E-11	1.11E-11

Charge Loss from VDD_1P2 at VREF ON

- Transient Simulation
- Measured charge loss from VDD_1P2 when VREF is turned on
- I(VDD_3P6) < 1uA @ outside of the integration window

Charge Loss from VDD_3P6 [C]

Temp	1P2	TT	FF	SS	FS	SF
27	1.2	4.55E-12	5.56E-12	3.40E-12	5.68E-12	3.53E-12
27	1.1	4.32E-12	5.31E-12	3.19E-12	5.45E-12	3.30E-12
27	1.4	5.02E-12	5.90E-12	3.88E-12	6.20E-12	3.93E-12
-40	1.1	3.03E-12	3.98E-12	2.04E-12	4.05E-12	2.15E-12
-40	1.4	3.59E-12	4.60E-12	2.55E-12	4.63E-12	2.70E-12
130	1.1	6.31E-12	7.12E-12	5.15E-12	7.57E-12	5.09E-12
130	1.4	6.55E-12	7.34E-12	5.51E-12	7.91E-12	5.27E-12

LDO Start-Up Time at LDO ON

- Transient Simulation
- Measured 1% settling time after 'IREF + LDO' are turned on

Start-Up Time of LDO [s]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	3.87E-02	7.95E-03	1.83E-01	2.63E-02	5.71E-02
27	1.1	2.5	3.89E-02	8.07E-03	1.85E-01	2.64E-02	5.74E-02
27	1.1	4.2	3.88E-02	7.95E-03	1.85E-01	2.60E-02	5.70E-02
27	1.4	2.5	3.85E-02	8.00E-03	1.82E-01	2.62E-02	5.68E-02
27	1.4	4.2	3.84E-02	7.88E-03	1.84E-01	2.60E-02	5.71E-02
-40	1.1	2.5	2.77E+00	3.74E-01	5.66E+00	1.67E+00	4.32E+00
-40	1.1	4.2	2.68E+00	3.66E-01	5.48E+00	1.61E+00	4.22E+00
-40	1.4	2.5	2.74E+00	3.69E-01	5.68E+00	1.65E+00	4.28E+00
-40	1.4	4.2	2.65E+00	3.62E-01	5.48E+00	1.58E+00	4.17E+00
130	1.1	2.5	1.18E-03	6.13E-04	3.18E-03	8.64E-04	1.47E-03
130	1.1	4.2	1.13E-03	4.47E-04	3.09E-03	8.92E-04	1.40E-03
130	1.4	2.5	1.18E-03	6.14E-04	3.17E-03	8.64E-04	1.46E-03
130	1.4	4.2	1.12E-03	4.48E-04	3.07E-03	8.84E-04	1.40E-03

VREF Start-Up Time at VREF ON

- Transient Simulation
- Measured 1% settling time after VREF is turned on
- Safe to turn on VREF one sleep cycle before

Start-Up Time of VREF [s]

Temp	1P2	TT	FF	SS	FS	SF
27	1.2	3.96E-02	7.13E-03	2.05E-01	2.60E-02	5.88E-02
27	1.1	3.98E-02	7.24E-03	2.08E-01	2.58E-02	5.97E-02
27	1.4	3.87E-02	6.89E-03	2.00E-01	2.54E-02	5.75E-02
-40	1.1	2.74E+00	3.17E-01	1.39E+01	1.56E+00	4.52E+00
-40	1.4	2.65E+00	3.10E-01	1.39E+01	1.56E+00	4.32E+00
130	1.1	9.89E-04	2.42E-04	3.71E-03	6.08E-04	1.45E-03
130	1.4	9.60E-04	2.37E-04	3.66E-03	5.84E-04	1.42E-03

Sleep Mode Current

- DC Simulation

I(VDD_3P6) @ Sleep Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	3.08E-12	1.37E-11	1.20E-12	2.55E-12	4.34E-12
27	1.1 - 1.4	2.5	2.54E-12	1.23E-11	8.18E-13	2.00E-12	3.78E-12
27	1.1 - 1.4	4.2	1.33E-11	3.34E-11	6.89E-12	1.24E-11	1.51E-11
-40	1.1 - 1.4	2.5	3.12E-13	3.37E-13	2.97E-13	3.16E-13	3.09E-13
-40	1.1 - 1.4	4.2	7.21E-12	1.29E-11	4.28E-12	6.96E-12	7.50E-12
130	1.1 - 1.4	2.5	1.64E-09	5.19E-09	6.97E-10	1.30E-09	2.21E-09
130	1.1 - 1.4	4.2	1.85E-09	5.88E-09	7.93E-10	1.53E-09	2.42E-09

I(VDD_1P2) @ Sleep Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	6.61E-14	6.21E-13	1.03E-14	1.19E-13	5.23E-14
27	1.1 - 1.4	2.5	6.61E-14	6.21E-13	1.03E-14	1.19E-13	5.23E-14
27	1.1 - 1.4	4.2	6.61E-14	6.21E-13	1.03E-14	1.19E-13	5.23E-14
-40	1.1 - 1.4	2.5	1.71E-15	3.50E-15	1.55E-15	1.81E-15	1.71E-15
-40	1.1 - 1.4	4.2	1.71E-15	3.50E-15	1.55E-15	1.81E-15	1.71E-15
130	1.1 - 1.4	2.5	3.65E-11	1.36E-10	1.79E-11	4.62E-11	3.43E-11
130	1.1 - 1.4	4.2	3.65E-11	1.36E-10	1.79E-11	4.62E-11	3.43E-11

Active Mode Current - 1 LDO ON

- DC Simulation

I(VDD_3P6) @ Active Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	2.25E-07	2.72E-07	1.92E-07	2.35E-07	2.16E-07
27	1.1 - 1.4	2.5	2.19E-07	2.63E-07	1.86E-07	2.28E-07	2.09E-07
27	1.1 - 1.4	4.2	2.49E-07	3.02E-07	2.11E-07	2.58E-07	2.40E-07
-40	1.1 - 1.4	2.5	1.86E-07	2.25E-07	1.58E-07	1.95E-07	1.78E-07
-40	1.1 - 1.4	4.2	2.10E-07	2.55E-07	1.77E-07	2.18E-07	2.02E-07
130	1.1 - 1.4	2.5	2.74E-07	3.31E-07	2.34E-07	2.85E-07	2.64E-07
130	1.1 - 1.4	4.2	3.19E-07	3.88E-07	2.70E-07	3.29E-07	3.10E-07

I(VDD_1P2) @ Active Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	3.01E-10	1.35E-09	6.99E-11	7.91E-10	1.21E-10
27	1.1 - 1.4	2.5	3.15E-10	1.46E-09	7.18E-11	7.99E-10	1.48E-10
27	1.1 - 1.4	4.2	3.15E-10	1.46E-09	7.18E-11	7.99E-10	1.48E-10
-40	1.1 - 1.4	2.5	3.65E-12	2.52E-11	6.07E-13	1.23E-11	1.44E-12
-40	1.1 - 1.4	4.2	3.65E-12	2.52E-11	6.07E-13	1.23E-11	1.44E-12
130	1.1 - 1.4	2.5	1.69E-08	5.22E-08	5.84E-09	3.23E-08	9.78E-09
130	1.1 - 1.4	4.2	1.69E-08	5.22E-08	5.84E-09	3.23E-08	9.78E-09

Active Mode Current - 2 LDOs ON

- DC Simulation

I(VDD_3P6) @ Active Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	3.55E-07	4.29E-07	3.02E-07	3.74E-07	3.37E-07
27	1.1 - 1.4	2.5	3.47E-07	4.18E-07	2.95E-07	3.66E-07	3.28E-07
27	1.1 - 1.4	4.2	3.83E-07	4.65E-07	3.24E-07	4.01E-07	3.65E-07
-40	1.1 - 1.4	2.5	3.03E-07	3.66E-07	2.57E-07	3.20E-07	2.85E-07
-40	1.1 - 1.4	4.2	3.31E-07	4.02E-07	2.79E-07	3.48E-07	3.14E-07
130	1.1 - 1.4	2.5	4.20E-07	5.06E-07	3.58E-07	4.40E-07	3.99E-07
130	1.1 - 1.4	4.2	4.73E-07	5.74E-07	4.01E-07	4.93E-07	4.54E-07

I(VDD_1P2) @ Active Mode [A]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.1 - 1.4	3.3	3.02E-10	1.36E-09	7.01E-11	7.92E-10	1.23E-10
27	1.1 - 1.4	2.5	3.02E-10	1.36E-09	7.01E-11	7.92E-10	1.23E-10
27	1.1 - 1.4	4.2	3.02E-10	1.36E-09	7.01E-11	7.92E-10	1.23E-10
-40	1.1 - 1.4	2.5	3.51E-12	2.34E-11	5.96E-13	1.22E-11	1.11E-12
-40	1.1 - 1.4	4.2	3.51E-12	2.34E-11	5.96E-13	1.22E-11	1.11E-12
130	1.1 - 1.4	2.5	1.62E-08	4.93E-08	5.69E-09	3.19E-08	8.72E-09
130	1.1 - 1.4	4.2	1.62E-08	4.93E-08	5.69E-09	3.19E-08	8.72E-09

PSRR - LDO

- AC Simulation from 1uHz to 1GHz
- Assigned AC input signals both to VDD_3P6 and VDD_1P2

Max. PSRR of LDO [dB]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	-43.60	-43.43	-44.09	-44.08	-41.58
27	1.1	2.5	-45.30	-43.83	-46.36	-44.05	-43.35
27	1.1	4.2	-41.15	-40.34	-41.97	-42.03	-39.37
27	1.4	2.5	-45.68	-44.00	-46.34	-44.49	-43.88
27	1.4	4.2	-41.55	-40.66	-42.41	-42.45	-39.72
-40	1.1	2.5	-44.23	-43.24	-44.71	-43.78	-43.27
-40	1.1	4.2	-41.20	-39.70	-42.56	-42.62	-39.45
-40	1.4	2.5	-44.77	-43.83	-44.97	-44.11	-43.92
-40	1.4	4.2	-41.62	-40.10	-43.04	-43.05	-39.87
130	1.1	2.5	-45.31	-44.24	-46.15	-44.79	-44.87
130	1.1	4.2	-40.99	-40.35	-41.84	-41.36	-40.51
130	1.4	2.5	-45.37	-44.29	-46.20	-45.13	-45.24
130	1.4	4.2	-41.28	-40.63	-42.15	-41.70	-40.77

PSRR Example

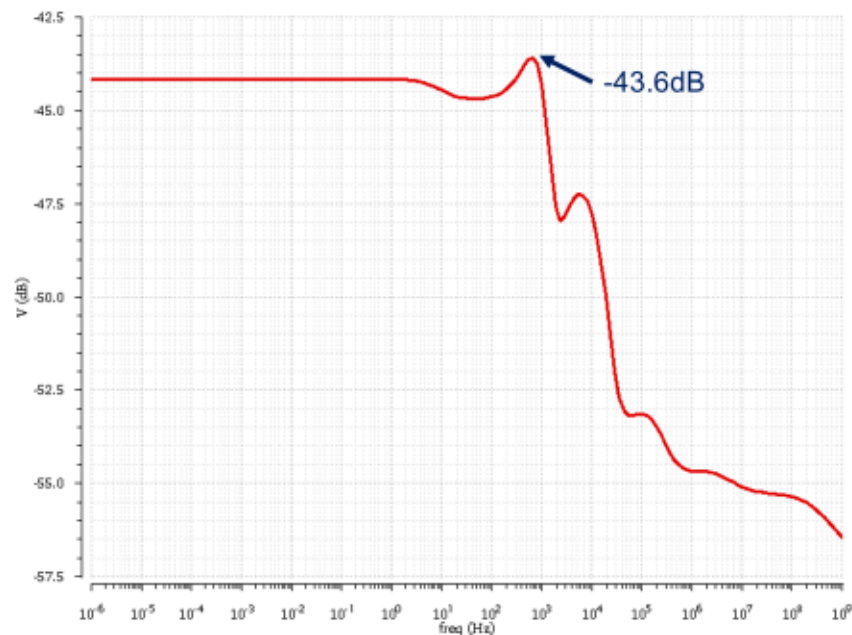- VDD_1P2 = 1.2V, VDD_3P6 = 3.3V, Temp = 27°C

PSRR - VREF

- AC Simulation from 1uHz to 1GHz
- Assigned AC input signals both to VDD_3P6 and VDD_1P2

Max. PSRR of VREF [dB]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	-49.36	-47.90	-50.61	-49.31	-48.42
27	1.1	2.5	-49.11	-47.65	-50.35	-49.07	-48.51
27	1.1	4.2	-48.48	-47.05	-49.83	-49.33	-46.91
27	1.4	2.5	-49.31	-47.85	-50.54	-49.28	-48.99
27	1.4	4.2	-48.91	-47.50	-50.27	-49.55	-47.30
-40	1.1	2.5	-49.07	-47.63	-50.33	-49.03	-48.24
-40	1.1	4.2	-48.91	-47.31	-50.36	-49.30	-46.90
-40	1.4	2.5	-49.27	-47.83	-50.53	-49.25	-48.83
-40	1.4	4.2	-49.41	-47.79	-50.79	-49.52	-47.41
130	1.1	2.5	-48.78	-46.82	-50.17	-48.56	-48.87
130	1.1	4.2	-47.81	-46.07	-49.15	-48.33	-46.81
130	1.4	2.5	-48.97	-46.99	-50.37	-48.73	-49.09
130	1.4	4.2	-48.24	-46.39	-49.60	-48.98	-47.22

LDO Output Variation – Default Setting

- DC Simulation w/ Default setting (3'b100)
- MC Simulation (1k samples) for each parameter set

LDO Output Voltage [V]

Temp	1P2	3P6	MIN	MAX	AVG	STD
27	1.2	3.3	1.137	1.357	1.248	0.033
27	1.1	2.5	1.136	1.356	1.247	0.033
27	1.1	4.2	1.138	1.358	1.248	0.033
27	1.4	2.5	1.138	1.358	1.248	0.033
27	1.4	4.2	1.139	1.359	1.250	0.033
-40	1.1	2.5	1.135	1.353	1.245	0.033
-40	1.1	4.2	1.136	1.355	1.246	0.033
-40	1.4	2.5	1.136	1.355	1.246	0.033
-40	1.4	4.2	1.138	1.356	1.248	0.033
130	1.1	2.5	1.136	1.357	1.247	0.033
130	1.1	4.2	1.139	1.359	1.249	0.033
130	1.4	2.5	1.138	1.358	1.249	0.033
130	1.4	4.2	1.140	1.361	1.251	0.033

VREF Variation – Default Setting

- DC Simulation w/ Default setting (4'b0000)
- MC Simulation (1k samples) for each parameter set

VREF Output Voltage [V]

Temp	1P2	3P6	MIN	MAX	AVG	STD
27	1.2	3.3	0.577	0.688	0.633	0.017
27	1.1	2.5	0.576	0.688	0.632	0.017
27	1.1	4.2	0.576	0.688	0.632	0.017
27	1.4	2.5	0.577	0.689	0.633	0.017
27	1.4	4.2	0.577	0.689	0.633	0.017
-40	1.1	2.5	0.576	0.686	0.631	0.017
-40	1.1	4.2	0.576	0.686	0.631	0.017
-40	1.4	2.5	0.576	0.687	0.632	0.017
-40	1.4	4.2	0.576	0.687	0.632	0.017
130	1.1	2.5	0.576	0.688	0.632	0.017
130	1.1	4.2	0.576	0.688	0.632	0.017
130	1.4	2.5	0.577	0.689	0.633	0.017
130	1.4	4.2	0.577	0.689	0.633	0.017

LDO Output Variation – Default Setting

- DC Simulation w/ Default setting (3'b100)
- No load current

LDO Output Voltage [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	1.249	1.293	1.206	1.358	1.140
27	1.1	2.5	1.248	1.291	1.205	1.358	1.139
27	1.1	4.2	1.249	1.293	1.207	1.359	1.140
27	1.4	2.5	1.249	1.293	1.207	1.359	1.141
27	1.4	4.2	1.251	1.295	1.209	1.361	1.142
-40	1.1	2.5	1.246	1.289	1.205	1.355	1.137
-40	1.1	4.2	1.247	1.291	1.206	1.356	1.139
-40	1.4	2.5	1.247	1.291	1.206	1.356	1.139
-40	1.4	4.2	1.249	1.292	1.208	1.358	1.140
130	1.1	2.5	1.248	1.291	1.208	1.359	1.138
130	1.1	4.2	1.250	1.293	1.209	1.360	1.140
130	1.4	2.5	1.250	1.294	1.210	1.361	1.141
130	1.4	4.2	1.252	1.295	1.212	1.363	1.142

LDO Output Voltage Drop - Default

- DC Simulation w/ Default setting (3'b100)
- 100uA load current

LDO Output Voltage Drop [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	0.0004	0.0004	0.0004	0.0004	0.0004
27	1.1	2.5	0.0004	0.0004	0.0005	0.0005	0.0004
27	1.1	4.2	0.0004	0.0004	0.0005	0.0005	0.0004
27	1.4	2.5	0.0005	0.0005	0.0005	0.0005	0.0005
27	1.4	4.2	0.0005	0.0005	0.0005	0.0005	0.0005
-40	1.1	2.5	0.0004	0.0004	0.0004	0.0004	0.0004
-40	1.1	4.2	0.0004	0.0004	0.0004	0.0004	0.0004
-40	1.4	2.5	0.0004	0.0004	0.0004	0.0004	0.0004
-40	1.4	4.2	0.0004	0.0004	0.0004	0.0004	0.0004
130	1.1	2.5	0.0007	0.0006	0.0007	0.0007	0.0007
130	1.1	4.2	0.0007	0.0006	0.0007	0.0007	0.0007
130	1.4	2.5	0.0007	0.0007	0.0008	0.0007	0.0008
130	1.4	4.2	0.0007	0.0007	0.0008	0.0007	0.0008

LDO Output Variation – Max Setting

- DC Simulation w/ Default setting (3'b000)
- No load current

LDO Output Voltage [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	1.646	1.704	1.590	1.791	1.502
27	1.1	2.5	1.644	1.702	1.588	1.788	1.500
27	1.1	4.2	1.646	1.704	1.590	1.791	1.502
27	1.4	2.5	1.647	1.705	1.591	1.792	1.503
27	1.4	4.2	1.649	1.707	1.593	1.794	1.505
-40	1.1	2.5	1.641	1.699	1.587	1.785	1.499
-40	1.1	4.2	1.643	1.701	1.589	1.787	1.501
-40	1.4	2.5	1.644	1.702	1.590	1.788	1.501
-40	1.4	4.2	1.646	1.704	1.592	1.790	1.503
130	1.1	2.5	1.644	1.701	1.591	1.790	1.500
130	1.1	4.2	1.646	1.703	1.593	1.792	1.502
130	1.4	2.5	1.648	1.705	1.595	1.794	1.503
130	1.4	4.2	1.650	1.707	1.597	1.796	1.505

LDO Output Voltage Drop – Max Setting

- DC Simulation w/ Default setting (3'b000)
- 100uA load current

LDO Output Voltage Drop [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	0.0007	0.0007	0.0007	0.0008	0.0006
27	1.1	2.5	0.0010	0.0010	0.0011	0.0029	0.0008
27	1.1	4.2	0.0010	0.0010	0.0011	0.0028	0.0008
27	1.4	2.5	0.0007	0.0007	0.0007	0.0008	0.0007
27	1.4	4.2	0.0007	0.0007	0.0007	0.0008	0.0007
-40	1.1	2.5	0.0010	0.0010	0.0011	0.0048	0.0007
-40	1.1	4.2	0.0010	0.0010	0.0011	0.0051	0.0007
-40	1.4	2.5	0.0006	0.0006	0.0006	0.0007	0.0006
-40	1.4	4.2	0.0006	0.0006	0.0006	0.0007	0.0006
130	1.1	2.5	0.0012	0.0012	0.0013	0.0020	0.0010
130	1.1	4.2	0.0013	0.0012	0.0013	0.0021	0.0010
130	1.4	2.5	0.0010	0.0010	0.0011	0.0011	0.0010
130	1.4	4.2	0.0010	0.0009	0.0010	0.0011	0.0010

LDO Output Variation – Min Setting

- DC Simulation w/ Default setting (3'b111)
- No load current

LDO Output Voltage [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	0.951	0.984	0.918	1.034	0.868
27	1.1	2.5	0.950	0.983	0.918	1.034	0.867
27	1.1	4.2	0.951	0.984	0.919	1.035	0.868
27	1.4	2.5	0.951	0.985	0.919	1.035	0.868
27	1.4	4.2	0.952	0.986	0.920	1.036	0.869
-40	1.1	2.5	0.948	0.981	0.917	1.031	0.866
-40	1.1	4.2	0.949	0.982	0.918	1.032	0.867
-40	1.4	2.5	0.949	0.983	0.918	1.032	0.867
-40	1.4	4.2	0.950	0.984	0.919	1.033	0.868
130	1.1	2.5	0.950	0.983	0.920	1.035	0.867
130	1.1	4.2	0.952	0.984	0.921	1.036	0.868
130	1.4	2.5	0.952	0.985	0.921	1.036	0.869
130	1.4	4.2	0.953	0.986	0.923	1.038	0.870

LDO Output Voltage Drop – Min Setting

- DC Simulation w/ Default setting (3'b111)
- 100uA load current

LDO Output Voltage Drop [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	0.0003	0.0003	0.0003	0.0003	0.0003
27	1.1	2.5	0.0003	0.0003	0.0003	0.0003	0.0003
27	1.1	4.2	0.0003	0.0003	0.0003	0.0003	0.0003
27	1.4	2.5	0.0004	0.0004	0.0004	0.0004	0.0004
27	1.4	4.2	0.0004	0.0004	0.0004	0.0004	0.0004
-40	1.1	2.5	0.0003	0.0003	0.0003	0.0003	0.0003
-40	1.1	4.2	0.0003	0.0003	0.0003	0.0003	0.0003
-40	1.4	2.5	0.0003	0.0003	0.0003	0.0003	0.0003
-40	1.4	4.2	0.0003	0.0003	0.0003	0.0003	0.0003
130	1.1	2.5	0.0005	0.0005	0.0005	0.0005	0.0005
130	1.1	4.2	0.0005	0.0005	0.0005	0.0005	0.0005
130	1.4	2.5	0.0006	0.0006	0.0006	0.0006	0.0006
130	1.4	4.2	0.0006	0.0006	0.0006	0.0006	0.0006

LDO Output Tuning

- DC Simulation @ 1.2V, 3.3V, 27°C

LDO Output Voltage [V]

Tuning Bits	TT	FF	SS	FS	SF
0	1.646	1.704	1.590	1.791	1.502
1	1.547	1.601	1.494	1.683	1.412
2	1.448	1.498	1.398	1.575	1.321
3	1.348	1.396	1.302	1.467	1.231
4	1.249	1.293	1.206	1.358	1.140
5	1.149	1.190	1.110	1.250	1.049
6	1.050	1.087	1.014	1.142	0.958
7	0.951	0.984	0.918	1.034	0.868

DC Loop Gain

- Stability Simulation w/ Default setting (3'b100)

DC Loop Gain [dB]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	57.79	57.83	57.74	57.82	57.71
27	1.1	2.5	57.60	57.65	57.54	57.54	57.61
27	1.1	4.2	57.60	57.65	57.54	57.53	57.61
27	1.4	2.5	56.30	56.28	56.31	56.54	56.01
27	1.4	4.2	56.31	56.29	56.32	56.55	56.02
-40	1.1	2.5	58.13	58.18	58.08	57.98	58.20
-40	1.1	4.2	58.13	58.18	58.08	57.98	58.20
-40	1.4	2.5	57.20	57.19	57.21	57.34	56.98
-40	1.4	4.2	57.20	57.19	57.21	57.34	56.99
130	1.1	2.5	55.53	55.70	55.35	55.55	55.49
130	1.1	4.2	55.53	55.70	55.35	55.55	55.49
130	1.4	2.5	53.95	54.01	53.88	54.27	53.59
130	1.4	4.2	53.95	54.02	53.89	54.28	53.60

Phase Margin w/ 20pF Load Cap.

- Stability Simulation w/ Default setting (3'b100)

Phase Margin [°]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	81.28	80.29	82.00	81.71	80.79
27	1.1	2.5	81.65	80.70	82.34	82.04	81.19
27	1.1	4.2	81.66	80.71	82.35	82.05	81.20
27	1.4	2.5	80.23	79.09	81.07	80.73	79.64
27	1.4	4.2	80.23	79.10	81.07	80.74	79.65
-40	1.1	2.5	83.15	82.31	83.75	83.45	82.79
-40	1.1	4.2	83.15	82.31	83.76	83.46	82.80
-40	1.4	2.5	82.04	81.03	82.78	82.43	81.58
-40	1.4	4.2	82.05	81.03	82.79	82.44	81.59
130	1.1	2.5	79.31	77.90	80.27	79.77	78.73
130	1.1	4.2	79.31	77.91	80.27	79.78	78.74
130	1.4	2.5	77.37	75.75	78.51	77.99	76.64
130	1.4	4.2	77.38	75.76	78.52	78.00	76.65

Unity-Gain Bandwidth w/ 20pF

- Stability Simulation w/ Default setting (3'b100)

Unity-Gain Bandwidth [Hz]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	1.62E+04	1.98E+04	1.36E+04	1.68E+04	1.56E+04
27	1.1	2.5	1.59E+04	1.93E+04	1.33E+04	1.65E+04	1.52E+04
27	1.1	4.2	1.59E+04	1.93E+04	1.33E+04	1.65E+04	1.52E+04
27	1.4	2.5	1.73E+04	2.11E+04	1.45E+04	1.79E+04	1.67E+04
27	1.4	4.2	1.73E+04	2.12E+04	1.45E+04	1.79E+04	1.67E+04
-40	1.1	2.5	1.66E+04	2.01E+04	1.39E+04	1.72E+04	1.59E+04
-40	1.1	4.2	1.66E+04	2.01E+04	1.39E+04	1.72E+04	1.59E+04
-40	1.4	2.5	1.80E+04	2.19E+04	1.51E+04	1.86E+04	1.73E+04
-40	1.4	4.2	1.80E+04	2.19E+04	1.51E+04	1.86E+04	1.73E+04
130	1.1	2.5	1.49E+04	1.82E+04	1.25E+04	1.55E+04	1.43E+04
130	1.1	4.2	1.49E+04	1.82E+04	1.25E+04	1.55E+04	1.43E+04
130	1.4	2.5	1.64E+04	2.00E+04	1.37E+04	1.70E+04	1.57E+04
130	1.4	4.2	1.64E+04	2.00E+04	1.37E+04	1.70E+04	1.58E+04

LDO VOUT Recovery Time – 0 → 100uA

- Transient Simulation w/ 5pF load cap
- load current : 0 to 100uA

5% Recovery Time [s]

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	4.02E-04	2.84E-04	5.40E-04	4.00E-04	4.02E-04
27	1.1	2.5	4.27E-04	3.02E-04	5.78E-04	4.27E-04	4.30E-04
27	1.1	4.2	3.40E-04	2.38E-04	4.62E-04	3.41E-04	3.39E-04
27	1.4	2.5	4.27E-04	3.02E-04	5.78E-04	4.27E-04	4.30E-04
27	1.4	4.2	3.40E-04	2.38E-04	4.62E-04	3.41E-04	3.39E-04
-40	1.1	2.5	4.83E-04	3.41E-04	6.54E-04	4.83E-04	4.84E-04
-40	1.1	4.2	3.85E-04	2.69E-04	5.24E-04	3.86E-04	3.83E-04
-40	1.4	2.5	4.83E-04	3.41E-04	6.54E-04	4.83E-04	4.84E-04
-40	1.4	4.2	3.85E-04	2.69E-04	5.24E-04	3.86E-04	3.83E-04
130	1.1	2.5	3.69E-04	2.58E-04	5.02E-04	3.68E-04	3.72E-04
130	1.1	4.2	2.89E-04	2.00E-04	3.99E-04	2.90E-04	2.90E-04
130	1.4	2.5	3.69E-04	2.58E-04	5.02E-04	3.68E-04	3.72E-04
130	1.4	4.2	2.89E-04	2.00E-04	3.99E-04	2.90E-04	2.90E-04

LDO VOUT Recovery Time –100uA → 0

- Transient Simulation w/ 5pF load cap
- load current : 100uA to 0

<div align="center">5% Recovery Time [s]</div>

Temp	1P2	3P6	TT	FF	SS	FS	SF
27	1.2	3.3	4.73E-04	3.30E-04	6.44E-04	4.72E-04	4.74E-04
27	1.1	2.5	5.06E-04	3.53E-04	6.88E-04	5.03E-04	5.08E-04
27	1.1	4.2	3.96E-04	2.74E-04	5.45E-04	3.98E-04	3.96E-04
27	1.4	2.5	5.06E-04	3.53E-04	6.88E-04	5.03E-04	5.08E-04
27	1.4	4.2	3.96E-04	2.74E-04	5.45E-04	3.98E-04	3.96E-04
-40	1.1	2.5	5.69E-04	3.98E-04	7.76E-04	5.68E-04	5.72E-04
-40	1.1	4.2	4.51E-04	3.10E-04	6.19E-04	4.52E-04	4.47E-04
-40	1.4	2.5	5.69E-04	3.98E-04	7.76E-04	5.68E-04	5.72E-04
-40	1.4	4.2	4.51E-04	3.10E-04	6.19E-04	4.52E-04	4.47E-04
130	1.1	2.5	4.40E-04	3.03E-04	6.03E-04	4.36E-04	4.40E-04
130	1.1	4.2	3.39E-04	2.31E-04	4.70E-04	3.39E-04	3.39E-04
130	1.4	2.5	4.40E-04	3.02E-04	6.03E-04	4.36E-04	4.40E-04
130	1.4	4.2	3.39E-04	2.31E-04	4.70E-04	3.39E-04	3.39E-04

LDO w/ nwell/psub diode model

- DC Simulation w/ Default setting (3'b100)
- No load current

<div align="center">LDO Output Voltage w/ nwell/psub diode model [V]</div>

Temp	1P2	3P6	TT	FF	SS	FS	SF	FF_dioS	SS_dioF
130	1.1	2.5	1.246	1.290	1.203	1.358	1.135	1.291	1.201
130	1.1	4.2	1.249	1.293	1.206	1.360	1.138	1.293	1.203
130	1.4	2.5	1.248	1.292	1.205	1.359	1.137	1.292	1.203
130	1.4	4.2	1.250	1.295	1.207	1.362	1.140	1.295	1.205

<div align="center">LDO Output Voltage w/o nwell/psub diode model [V]</div>

Temp	1P2	3P6	TT	FF	SS	FS	SF	FF_dioS	SS_dioF
130	1.1	2.5	1.247	1.291	1.205	1.358	1.137	1.291	1.205
130	1.1	4.2	1.250	1.293	1.208	1.360	1.140	1.293	1.208
130	1.4	2.5	1.249	1.292	1.207	1.360	1.138	1.292	1.207
130	1.4	4.2	1.251	1.295	1.209	1.362	1.141	1.295	1.209

VREF w/ nwell/psub diode model

- DC Simulation w/ Default setting (4'b0000)
- No load current

VREF Output Voltage w/ nwell/psub diode model [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF	FF_dioS	SS_dioF
130	1.1	2.5	0.632	0.654	0.610	0.689	0.576	0.655	0.609
130	1.1	4.2	0.632	0.654	0.610	0.689	0.576	0.655	0.609
130	1.4	2.5	0.633	0.655	0.611	0.689	0.577	0.655	0.610
130	1.4	4.2	0.633	0.655	0.611	0.689	0.577	0.655	0.610

VREF Output Voltage w/o nwell/psub diode model [V]

Temp	1P2	3P6	TT	FF	SS	FS	SF	FF_dioS	SS_dioF
130	1.1	2.5	0.632	0.655	0.611	0.689	0.577	0.655	0.611
130	1.1	4.2	0.632	0.655	0.611	0.689	0.577	0.655	0.611
130	1.4	2.5	0.633	0.655	0.612	0.690	0.577	0.655	0.612
130	1.4	4.2	0.633	0.655	0.612	0.690	0.577	0.655	0.612