M3 Power Management Unit (Version 10) Documentation (PMUv10)

Revision 1.0

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1.1 MBus Register File Mapping

Table 1 shows MBus Register File mapping information. 'NR' indicates a non-retentive register.

Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 0 (0x00) Default: 24'h000000					
0x00	[0]	PMU_READ_ADDR	W	1'h0	
Register 1 (0x01) Default: 24'h000000					
0x01	[0]	PMU_EN_ADC_CONFIG	W	1'h0	
Register 2 (0x02) Default: 24'h000000					
0x02	[0]	PMU_EN_ADC_CONFIG_OVERRIDE	W	1'h0	
Register 3 (0x03) Default: 24'h000000					
0x03	[0]	PMU_EN_ADC_STORED_OUT	W	1'h0	
Register 4 (0x04) Default: 24'h000000					
0x04	[0]	PMU_EN_SAR_RATIO	W	1'h0	
Register 5 (0x05) Default: 24'h000000					
0x05	[0]	PMU_EN_SAR_RATIO_OVERRIDE	W	1'h0	
Register 6 (0x06) Default: 24'h000000					
0x06	[0]	PMU_EN_SAR_RATIO_OFFSET_DOWN_SLEEP	W	1'h0	
Register 7 (0x07) Default: 24'h000000					
0x07	[0]	PMU_EN_SAR_RATIO_OFFSET_DOWN_ACTIVE	W	1'h0	
Register 8 (0x08) Default: 24'h000000					
0x08	[0]	PMU_EN_SAR_RATIO_OFFSET_UP_SLEEP	W	1'h0	
Register 9 (0x09) Default: 24'h000000					
0x09	[0]	PMU_EN_SAR_RATIO_OFFSET_UP_ACTIVE	W	1'h0	
Register 10 (0x0A) Default: 24'h000000					
0x0A	[0]	PMU_EN_SAR_RATIO_MINIMUM	W	1'h0	
Register 11 (0x0B) Default: 24'h000000					
0x0B	[0]	PMU_EN_VOLTAGE_CLAMP_OUT	W	1'h0	
Register 12 (0x0C) Default: 24'h000000					
0x0C	[0]	PMU_EN_REFERENCE_TRIM_SLEEP	W	1'h0	
Register 13 (0x0D) Default: 24'h000000					
0x0D	[0]	PMU_EN_REFERENCE_TRIM_ACTIVE	W	1'h0	
Register 14 (0x0E) Default: 24'h000000					
0x0E	[0]	PMU_EN_VOLTAGE_CLAMP_TRIM	W	1'h0	
Register 15 (0x0F) Default: 24'h000000					
0x0F	[0]	PMU_EN_SAR_TRIM_SLEEP	W	1'h0	
Register 16 (0x10) Default: 24'h000000					
0x10	[0]	PMU_EN_SAR_TRIM_ACTIVE	W	1'h0	
Register 17 (0x11) Default: 24'h000000					
0x11	[0]	PMU_EN_UPCONVERTER_TRIM_SLEEP	W	1'h0	
Register 18 (0x12) Default: 24'h000000					
0x12	[0]	PMU_EN_UPCONVERTER_TRIM_ACTIVE	W	1'h0	
Register 19 (0x13) Default: 24'h000000					
0x13	[0]	PMU_EN_DOWNCONVERTER_TRIM_SLEEP	W	1'h0	
Register 20 (0x14) Default: 24'h000000					
0x14	[0]	PMU_EN_DOWNCONVERTER_TRIM_ACTIVE	W	1'h0	

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Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 21 (0x15) Default: 24'h000000					
0x15	[0]	PMU_EN_SAR_TRIM_V3_SLEEP	W	1'h0	
Register 22 (0x16) Default: 24'h000000					
0x16	[0]	PMU_EN_SAR_TRIM_V3_ACTIVE	W	1'h0	
Register 23 (0x17) Default: 24'h000000					
0x17	[0]	PMU_EN_UPCONVERTER_TRIM_V3_SLEEP	W	1'h0	
Register 24 (0x18) Default: 24'h000000					
0x18	[0]	PMU_EN_UPCONVERTER_TRIM_V3_ACTIVE	W	1'h0	
Register 25 (0x19) Default: 24'h000000					
0x19	[0]	PMU_EN_DOWNCONVERTER_TRIM_V3_SLEEP	W	1'h0	
Register 26 (0x1A) Default: 24'h000000					
0x1A	[0]	PMU_EN_DOWNCONVERTER_TRIM_V3_ACTIVE	W	1'h0	
Register 27 (0x1B) Default: 24'h000000					
0x1B	[0]	PMU_EN_SAR_TRIM_V3_STARTUP	W	1'h0	
Register 28 (0x1C) Default: 24'h000000					
0x1C	[0]	PMU_EN_UPCONVERTER_TRIM_V3_STARTUP	W	1'h0	
Register 29 (0x1D) Default: 24'h000000					
0x1D	[0]	PMU_EN_DOWNCONVERTER_TRIM_V3_STARTUP	W	1'h0	
Register 30 (0x1E) Default: 24'h000000					
0x1E	[0]	PMU_EN_SAR_TRIM_V3_OUTPUT	W	1'h0	
Register 31 (0x1F) Default: 24'h000000					
0x1F	[0]	PMU_EN_UPCONVERTER_TRIM_V3_OUTPUT	W	1'h0	
Register 32 (0x20) Default: 24'h000000					
0x20	[0]	PMU_EN_DOWNCONVERTER_TRIM_V3_OUTPUT	W	1'h0	
Register 33 (0x21) Default: 24'h000000					
0x21	[0]	PMU_EN_TICK_SAR_SCN_RESET	W	1'h0	
Register 34 (0x22) Default: 24'h000000					
0x22	[0]	PMU_EN_TICK_SAR_SCN_POST_RESET	W	1'h0	
Register 35 (0x23) Default: 24'h000000					
0x23	[0]	PMU_EN_TICK_SAR_SCN_RST_STABILIZE	W	1'h0	
Register 36 (0x24) Default: 24'h000000					
0x24	[0]	PMU_EN_TICK_SAR_SCN_STABILIZE	W	1'h0	
Register 37 (0x25) Default: 24'h000000					
0x25	[0]	PMU_EN_TICK_SAR_SCN_POST_STABILIZE	W	1'h0	
Register 38 (0x26) Default: 24'h000000					
0x26	[0]	PMU_EN_TICK_REFGEN_ON	W	1'h0	
Register 39 (0x27) Default: 24'h000000					
0x27	[0]	PMU_EN_TICK_UPCONVERTER_ON	W	1'h0	
Register 40 (0x28) Default: 24'h000000					
0x28	[0]	PMU_EN_TICK_UPCONVERTER_RST_STABILIZE	W	1'h0	
Register 41 (0x29) Default: 24'h000000					
0x29	[0]	PMU_EN_TICK_UPCONVERTER_STABILIZE	W	1'h0	
Register 42 (0x2A) Default: 24'h000000					
0x2A	[0]	PMU_EN_TICK_UPCONVERTER_POST_STABILIZE	W	1'h0	
Register 43 (0x2B) Default: 24'h000000					
0x2B	[0]	PMU_EN_TICK_DOWNCONVERTER_ON	W	1'h0	
Register 44 (0x2C) Default: 24'h000000					
0x2C	[0]	PMU_EN_TICK_DOWNCONVERTER_RST_STABILIZE	W	1'h0	

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Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 45 (0x2D) Default: 24'h000000					
0x2D	[0]	PMU_EN_TICK_DOWNCONVERTER_STABILIZE	W	1'h0	
Register 46 (0x2E) Default: 24'h000000					
0x2E	[0]	PMU_EN_TICK_DOWNCONVERTER_POST_STABILIZE	W	1'h0	
Register 47 (0x2F) Default: 24'h000000					
0x2F	[0]	PMU_EN_TICK_OUTPUT_PRE_3P6_ON	W	1'h0	
Register 48 (0x30) Default: 24'h000000					
0x30	[0]	PMU_EN_TICK_OUTPUT_POST_3P6_ON	W	1'h0	
Register 49 (0x31) Default: 24'h000000					
0x31	[0]	PMU_EN_TICK_OUTPUT_POST_1P2_ON	W	1'h0	
Register 50 (0x32) Default: 24'h000000					
0x32	[0]	PMU_EN_TICK_OUTPUT_WEAK	W	1'h0	
Register 51 (0x33) Default: 24'h000000					
0x33	[0]	PMU_EN_TICK_ADC_RESET	W	1'h0	
Register 52 (0x34) Default: 24'h000000					
0x34	[0]	PMU_EN_TICK_ADC_CLK	W	1'h0	
Register 53 (0x35) Default: 24'h000000					
0x35	[0]	PMU_EN_TICK_CONTROLLER_CLK	W	1'h0	
Register 54 (0x36) Default: 24'h000000					
0x36	[0]	PMU_EN_TICK_REPEAT_VBAT_ADJUST	W	1'h0	
Register 55 (0x37) Default: 24'h000000					
0x37	[0]	PMU_EN_TICK_WAKEUP_WAIT	W	1'h0	
Register 56 (0x38) Default: 24'h000000					
0x38	[0]	PMU_EN_TICK_SLEEP_WAIT	W	1'h0	
Register 57 (0x39) Default: 24'h000000					
0x39	[0]	PMU_EN_CONTROLLER_STALL_SLEEP	W	1'h0	
Register 58 (0x3A) Default: 24'h000000					
0x3A	[0]	PMU_EN_CONTROLLER_STALL_ACTIVE	W	1'h0	
Register 59 (0x3B) Default: 24'h000000					
0x3B	[0]	PMU_EN_CONTROLLER_DESIRED_STATE_SLEEP	W	1'h0	
Register 60 (0x3C) Default: 24'h000000					
0x3C	[0]	PMU_EN_CONTROLLER_DESIRED_STATE_ACTIVE	W	1'h0	
Register 61 (0x3D) Default: 24'h000000					
0x3D	[0]	PMU_EN_CONTROLLER_STATE_MAIN	W	1'h0	
Register 62 (0x3E) Default: 24'h000000					
0x3E	[0]	PMU_EN_CONTROLLER_STATE_SAR	W	1'h0	
Register 63 (0x3F) Default: 24'h000000					
0x3F	[0]	PMU_EN_CONTROLLER_STATE_UPCONVERTER	W	1'h0	
Register 64 (0x40) Default: 24'h000000					
0x40	[0]	PMU_EN_CONTROLLER_STATE_DOWNCONVERTER	W	1'h0	
Register 65 (0x41) Default: 24'h000000					
0x41	[0]	PMU_EN_CONTROLLER_STATE_ADC	W	1'h0	
Register 66 (0x42) Default: 24'h000000					
0x42	[0]	PMU_EN_CONTROLLER_STATE_TICKCOUNT	W	1'h0	
Register 67 (0x43) Default: 24'h000000					
0x43	[0]	PMU_EN_CONTROLLER_STATE_OUTPUT	W	1'h0	
Register 68 (0x44) Default: 24'h000000					
0x44	[0]	PMU_EN_RESERVED_1	W	1'h0	

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Reg Addr	**Bit Field**	**Reg Name**	**Property**	**Size & Reset**	**Remark**
Register 69 (0x45) Default: 24'h000000					
0x45	[0]	PMU_EN_RESERVED_2	W	1'h0	
Register 70 (0x46) Default: 24'h000000					
0x46	[0]	PMU_EN_RESERVED_3	W	1'h0	
Register 71 (0x47) Default: 24'h000000					
0x47	[0]	PMU_EN_RESERVED_4	W	1'h0	
Register 72 (0x48) Default: 24'h000000					
0x48	[0]	PMU_EN_RESERVED_5	W	1'h0	
Register 80 (0x50) Default: 24'h000000					
0x50	[23:0]	IRQ_PAYLOAD	R	24'h000000	
Register 81 (0x51) Default: 24'h00009D					
0x51	[7]	MBUS_IGNORE_RX_FAIL	W/R	1'h1	
	[6]	EN_GLITCH_FILT	W/R	1'h0	
	[5]	PMU_CHECK_WRITE	W/R	1'h0	
	[4]	PMU_IRQ_EN	W/R	1'h1	
	[3:2]	LC_CLK_DIV	W/R	2'h3	
	[1:0]	LC_CLK_RING	W/R	2'h1	
Register 82 (0x52) Default: 24'h001000					
0x52	[15:8]	INT_RPLY_SHORT_ADDR	W/R	8'h10	
	[7:0]	INT_RPLY_REG_ADDR	W/R	8'h00	
Register 83 (0x53) Default: 24'h000000					
0x53	[23]	VCO_CNT_ENABLE	W/R	1'h0	
	[22]	VCO_CNT_MODE	W/R	1'h0	
	[21:0]	VCO_CNT_THRESHOLD	W/R	22'h000000	

Table 1: PMUv10 MBus Register File Mapping

1.2 PMUv10 Register Write/Read Operation

1.2.1 Register 0x00: PMU_READ_ADDR

Using a typical MBus Register Write message, writing 8-bit data into this register triggers PMU Register Read operation. The 8-bit data is treated as an address of the register that will be read.

For example, writing 0x01 into this register initiates a READ from register 0x01, which corresponds to PMU_ADC_CONFIG. Then, PMUv10 sends an MBus message containing this PMU_ADC_CONFIG data. This reply message uses addresses specified in INT_RPLY_SHORT_ADDR and INT_RPLY_REG_ADDR.

Similarly, writing 0x42 into this register 0x00 initiates a READ from register 0x42, which corresponds to PMU_CONTROLLER_STATE_TICKCOUNT.

For this purpose, the valid 8-bit data range is 0x01 $\sim$ 0x48. See Table 1 for the register names.

There is one more valid 8-bit data, which is 0xFF. Writing 0xFF into this register 0x00 resets the interface controller inside PMUv10. This controller (pmuv10_ctrl) is an interface between the Layer Controller (pmuv10_layer_ctrl) and the PMU itself (pmuv10_top). It does NOT reset the PMU itself (pmuv10_top). This reset signal is effective for one clock cycle (i.e., one Layer Ctrl clock cycle), and then will be released automatically.

Using a typical MBus Register Read message, reading from this register 0x00 returns pmu_reg_en signal in the controller (pmuv10_ctrl), which is a previously accessed register address.

1.2.2 Register 0x01 $\sim$ 0x48

Register 0x01 $\sim$ 0x48 are mapped to internal PMU registers.

Using a typical MBus Register Write message, writing 24-bit data into one of the registers initiates a WRITE into the corresponding register.

For example, writing 0xFFFFFF into the register 0x38 will write 0xFFFFFF into PMU_TICK_SLEEP_WAIT. Once the write operation is done, PMUv10 will send a reply if PMU_IRQ_EN is set to 1, using the addresses specified in INT_RPLY_SHORT_ADDR and INT_RPLY_REG_ADDR. This reply message contains the write data.

Using a typical MBus Register Read message, reading from one of these registers will return zero.

1.2.3 Register 0x50 $\sim$ 0x53

Register 0x50 $\sim$ 0x53 can be treated as typical MBus Register File; user can use the standard MBus Register Write/Read messages to access those registers.

1.3 MBus Register Descriptions

1.3.1 Register 0 (0x00)

PMU_READ_ADDR Reg 0x00, Bit Field: [0], Default: 1'h0, W

1.3.2 Register 1 (0x01)

PMU_EN_ADC_CONFIG Reg 0x01, Bit Field: [0], Default: 1'h0, W

1.3.3 Register 2 (0x02)

PMU_EN_ADC_CONFIG_OVERRIDE Reg 0x02, Bit Field: [0], Default: 1'h0, W

1.3.4 Register 3 (0x03)

PMU_EN_ADC_STORED_OUT Reg 0x03, Bit Field: [0], Default: 1'h0, W

1.3.5 Register 4 (0x04)

PMU_EN_SAR_RATIO Reg 0x04, Bit Field: [0], Default: 1'h0, W

1.3.6 Register 5 (0x05)

PMU_EN_SAR_RATIO_OVERRIDE Reg 0x05, Bit Field: [0], Default: 1'h0, W

1.3.7 Register 6 (0x06)

PMU_EN_SAR_RATIO_OFFSET_DOWN_SLEEP Reg 0x06, Bit Field: [0], Default: 1'h0, W

1.3.8 Register 7 (0x07)

PMU_EN_SAR_RATIO_OFFSET_DOWN_ACTIVE Reg 0x07, Bit Field: [0], Default: 1'h0, W

1.3.9 Register 8 (0x08)

PMU_EN_SAR_RATIO_OFFSET_UP_SLEEP Reg 0x08, Bit Field: [0], Default: 1'h0, W

1.3.10 Register 9 (0x09)

PMU_EN_SAR_RATIO_OFFSET_UP_ACTIVE Reg 0x09, Bit Field: [0], Default: 1'h0, W

1.3.11 Register 10 (0x0A)

PMU_EN_SAR_RATIO_MINIMUM Reg 0x0A, Bit Field: [0], Default: 1'h0, W

1.3.12 Register 11 (0x0B)

PMU_EN_VOLTAGE_CLAMP_OUT Reg 0x0B, Bit Field: [0], Default: 1'h0, W

1.3.13 Register 12 (0x0C)

PMU_EN_REFERENCE_TRIM_SLEEP Reg 0x0C, Bit Field: [0], Default: 1'h0, W

1.3.14 Register 13 (0x0D)

PMU_EN_REFERENCE_TRIM_ACTIVE Reg 0x0D, Bit Field: [0], Default: 1'h0, W

1.3.15 Register 14 (0x0E)

PMU_EN_VOLTAGE_CLAMP_TRIM Reg 0x0E, Bit Field: [0], Default: 1'h0, W

1.3.16 Register 15 (0x0F)

PMU_EN_SAR_TRIM_SLEEP Reg 0x0F, Bit Field: [0], Default: 1'h0, W

1.3.17 Register 16 (0x10)

PMU_EN_SAR_TRIM_ACTIVE Reg 0x10, Bit Field: [0], Default: 1'h0, W

1.3.18 Register 17 (0x11)

PMU_EN_UPCONVERTER_TRIM_SLEEP Reg 0x11, Bit Field: [0], Default: 1'h0, W

1.3.19 Register 18 (0x12)

PMU_EN_UPCONVERTER_TRIM_ACTIVE Reg 0x12, Bit Field: [0], Default: 1'h0, W

1.3.20 Register 19 (0x13)

PMU_EN_DOWNCONVERTER_TRIM_SLEEP Reg 0x13, Bit Field: [0], Default: 1'h0, W

1.3.21 Register 20 (0x14)

PMU_EN_DOWNCONVERTER_TRIM_ACTIVE Reg 0x14, Bit Field: [0], Default: 1'h0, W

1.3.22 Register 21 (0x15)

PMU_EN_SAR_TRIM_V3_SLEEP Reg 0x15, Bit Field: [0], Default: 1'h0, W

1.3.23 Register 22 (0x16)

PMU_EN_SAR_TRIM_V3_ACTIVE Reg 0x16, Bit Field: [0], Default: 1'h0, W

1.3.24 Register 23 (0x17)

PMU_EN_UPCONVERTER_TRIM_V3_SLEEP Reg 0x17, Bit Field: [0], Default: 1'h0, W

1.3.25 Register 24 (0x18)

PMU_EN_UPCONVERTER_TRIM_V3_ACTIVE Reg 0x18, Bit Field: [0], Default: 1'h0, W

1.3.26 Register 25 (0x19)

PMU_EN_DOWNCONVERTER_TRIM_V3_SLEEP Reg 0x19, Bit Field: [0], Default: 1'h0, W

1.3.27 Register 26 (0x1A)

PMU_EN_DOWNCONVERTER_TRIM_V3_ACTIVE Reg 0x1A, Bit Field: [0], Default: 1'h0, W

1.3.28 Register 27 (0x1B)

PMU_EN_SAR_TRIM_V3_STARTUP Reg 0x1B, Bit Field: [0], Default: 1'h0, W

1.3.29 Register 28 (0x1C)

PMU_EN_UPCONVERTER_TRIM_V3_STARTUP Reg 0x1C, Bit Field: [0], Default: 1'h0, W

1.3.30 Register 29 (0x1D)

PMU_EN_DOWNCONVERTER_TRIM_V3_STARTUP Reg 0x1D, Bit Field: [0], Default: 1'h0, W

1.3.31 Register 30 (0x1E)

PMU_EN_SAR_TRIM_V3_OUTPUT Reg 0x1E, Bit Field: [0], Default: 1'h0, W

1.3.32 Register 31 (0x1F)

PMU_EN_UPCONVERTER_TRIM_V3_OUTPUT Reg 0x1F, Bit Field: [0], Default: 1'h0, W

1.3.33 Register 32 (0x20)

PMU_EN_DOWNCONVERTER_TRIM_V3_OUTPUT Reg 0x20, Bit Field: [0], Default: 1'h0, W

1.3.34 Register 33 (0x21)

PMU_EN_TICK_SAR_SCN_RESET Reg 0x21, Bit Field: [0], Default: 1'h0, W

1.3.35 Register 34 (0x22)

PMU_EN_TICK_SAR_SCN_POST_RESET Reg 0x22, Bit Field: [0], Default: 1'h0, W

1.3.36 Register 35 (0x23)

PMU_EN_TICK_SAR_SCN_RST_STABILIZE Reg 0x23, Bit Field: [0], Default: 1'h0, W

1.3.37 Register 36 (0x24)

PMU_EN_TICK_SAR_SCN_STABILIZE Reg 0x24, Bit Field: [0], Default: 1'h0, W

1.3.38 Register 37 (0x25)

PMU_EN_TICK_SAR_SCN_POST_STABILIZE Reg 0x25, Bit Field: [0], Default: 1'h0, W

1.3.39 Register 38 (0x26)

PMU_EN_TICK_REFGEN_ON Reg 0x26, Bit Field: [0], Default: 1'h0, W

1.3.40 Register 39 (0x27)

PMU_EN_TICK_UPCONVERTER_ON Reg 0x27, Bit Field: [0], Default: 1'h0, W

1.3.41 Register 40 (0x28)

PMU_EN_TICK_UPCONVERTER_RST_STABILIZE Reg 0x28, Bit Field: [0], Default: 1'h0, W

1.3.42 Register 41 (0x29)

PMU_EN_TICK_UPCONVERTER_STABILIZE Reg 0x29, Bit Field: [0], Default: 1'h0, W

1.3.43 Register 42 (0x2A)

PMU_EN_TICK_UPCONVERTER_POST_STABILIZE Reg 0x2A, Bit Field: [0], Default: 1'h0, W

1.3.44 Register 43 (0x2B)

PMU_EN_TICK_DOWNCONVERTER_ON Reg 0x2B, Bit Field: [0], Default: 1'h0, W

1.3.45 Register 44 (0x2C)

PMU_EN_TICK_DOWNCONVERTER_RST_STABILIZE Reg 0x2C, Bit Field: [0], Default: 1'h0, W

1.3.46 Register 45 (0x2D)

PMU_EN_TICK_DOWNCONVERTER_STABILIZE Reg 0x2D, Bit Field: [0], Default: 1'h0, W

1.3.47 Register 46 (0x2E)

PMU_EN_TICK_DOWNCONVERTER_POST_STABILIZE Reg 0x2E, Bit Field: [0], Default: 1'h0, W

1.3.48 Register 47 (0x2F)

PMU_EN_TICK_OUTPUT_PRE_3P6_ON Reg 0x2F, Bit Field: [0], Default: 1'h0, W

1.3.49 Register 48 (0x30)

PMU_EN_TICK_OUTPUT_POST_3P6_ON Reg 0x30, Bit Field: [0], Default: 1'h0, W

1.3.50 Register 49 (0x31)

PMU_EN_TICK_OUTPUT_POST_1P2_ON Reg 0x31, Bit Field: [0], Default: 1'h0, W

1.3.51 Register 50 (0x32)

PMU_EN_TICK_OUTPUT_WEAK Reg 0x32, Bit Field: [0], Default: 1'h0, W

1.3.52 Register 51 (0x33)

PMU_EN_TICK_ADC_RESET Reg 0x33, Bit Field: [0], Default: 1'h0, W

1.3.53 Register 52 (0x34)

PMU_EN_TICK_ADC_CLK Reg 0x34, Bit Field: [0], Default: 1'h0, W

1.3.54 Register 53 (0x35)

PMU_EN_TICK_CONTROLLER_CLK Reg 0x35, Bit Field: [0], Default: 1'h0, W

1.3.55 Register 54 (0x36)

PMU_EN_TICK_REPEAT_VBAT_ADJUST Reg 0x36, Bit Field: [0], Default: 1'h0, W

1.3.56 Register 55 (0x37)

PMU_EN_TICK_WAKEUP_WAIT Reg 0x37, Bit Field: [0], Default: 1'h0, W

1.3.57 Register 56 (0x38)

PMU_EN_TICK_SLEEP_WAIT Reg 0x38, Bit Field: [0], Default: 1'h0, W

1.3.58 Register 57 (0x39)

PMU_EN_CONTROLLER_STALL_SLEEP Reg 0x39, Bit Field: [0], Default: 1'h0, W

1.3.59 Register 58 (0x3A)

PMU_EN_CONTROLLER_STALL_ACTIVE Reg 0x3A, Bit Field: [0], Default: 1'h0, W

1.3.60 Register 59 (0x3B)

PMU_EN_CONTROLLER_DESIRED_STATE_SLEEP Reg 0x3B, Bit Field: [0], Default: 1'h0, W

1.3.61 Register 60 (0x3C)

PMU_EN_CONTROLLER_DESIRED_STATE_ACTIVE Reg 0x3C, Bit Field: [0], Default: 1'h0, W

1.3.62 Register 61 (0x3D)

PMU_EN_CONTROLLER_STATE_MAIN Reg 0x3D, Bit Field: [0], Default: 1'h0, W

1.3.63 Register 62 (0x3E)

PMU_EN_CONTROLLER_STATE_SAR Reg 0x3E, Bit Field: [0], Default: 1'h0, W

1.3.64 Register 63 (0x3F)

PMU_EN_CONTROLLER_STATE_UPCONVERTER Reg 0x3F, Bit Field: [0], Default: 1'h0, W

1.3.65 Register 64 (0x40)

PMU_EN_CONTROLLER_STATE_DOWNCONVERTER Reg 0x40, Bit Field: [0], Default: 1'h0, W

1.3.66 Register 65 (0x41)

PMU_EN_CONTROLLER_STATE_ADC Reg 0x41, Bit Field: [0], Default: 1'h0, W

1.3.67 Register 66 (0x42)

PMU_EN_CONTROLLER_STATE_TICKCOUNT Reg 0x42, Bit Field: [0], Default: 1'h0, W

1.3.68 Register 67 (0x43)

PMU_EN_CONTROLLER_STATE_OUTPUT Reg 0x43, Bit Field: [0], Default: 1'h0, W

1.3.69 Register 68 (0x44)

PMU_EN_RESERVED_1 Reg 0x44, Bit Field: [0], Default: 1'h0, W

1.3.70 Register 69 (0x45)

PMU_EN_RESERVED_2 Reg 0x45, Bit Field: [0], Default: 1'h0, W

1.3.71 Register 70 (0x46)

PMU_EN_RESERVED_3 Reg 0x46, Bit Field: [0], Default: 1'h0, W

1.3.72 Register 71 (0x47)

PMU_EN_RESERVED_4 Reg 0x47, Bit Field: [0], Default: 1'h0, W

1.3.73 Register 72 (0x48)

PMU_EN_RESERVED_5 Reg 0x48, Bit Field: [0], Default: 1'h0, W

1.3.74 Register 80 (0x50)

IRQ_PAYLOAD Reg 0x50, Bit Field: [23:0], Default: 24'h000000, R

1.3.75 Register 81 (0x51)

MBUS_IGNORE_RX_FAIL Reg 0x51, Bit Field: [7], Default: 1'h1, W/R

EN_GLITCH_FILT Reg 0x51, Bit Field: [6], Default: 1'h0, W/R

PMU_CHECK_WRITE Reg 0x51, Bit Field: [5], Default: 1'h0, W/R

PMU_IRQ_EN Reg 0x51, Bit Field: [4], Default: 1'h1, W/R

LC_CLK_DIV Reg 0x51, Bit Field: [3:2], Default: 2'h3, W/R

LC_CLK_RING Reg 0x51, Bit Field: [1:0], Default: 2'h1, W/R

1.3.76 Register 82 (0x52)

INT_RPLY_SHORT_ADDR Reg 0x52, Bit Field: [15:8], Default: 8'h10, W/R

INT_RPLY_REG_ADDR Reg 0x52, Bit Field: [7:0], Default: 8'h00, W/R

1.3.77 Register 83 (0x53)

VCO_CNT_ENABLE Reg 0x53, Bit Field: [23], Default: 1'h0, W/R

VCO_CNT_MODE Reg 0x53, Bit Field: [22], Default: 1'h0, W/R

VCO_CNT_THRESHOLD Reg 0x53, Bit Field: [21:0], Default: 22'h000000, W/R