M3 Light Sensor and Timer (Version 1B) Documentation (LNTv1B)

Revision 1.0

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1 MBus Register File

1.1 MBus Register File Mapping

Table 1 shows MBus Register File mapping information. 'NR' indicates a non-retentive register.

Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 0 (0x00) Default: 24'h00000B					
0x00	[6]	WAKEUP_WHEN_DONE	W/R	1'h0	
	[5]	MODE_CONTINUOUS	W/R	1'h0	
	[4]	DBE_ENABLE	W/R	1'h0	
	[3]	RESET_AFE	W/R	1'h1	
	[2]	RESETN_DBE	W/R	1'h0	
	[1]	LDC_ISOLATE	W/R	1'h1	
	[0]	LDC_PG	W/R	1'h1	
Register 1 (0x01) Default: 24'h003778					
0x01	[14:12]	CTRL_CAPSIZE	W/R	3'h3	
	[11:9]	CTRL_ICOMP	W/R	3'h3	
	[8]	CTRL_VOFS_CANCEL	W/R	1'h1	
	[7:4]	CTRL_IBIAS_VBIAS	W/R	4'h7	
	[3:0]	CTRL_IBIAS_I	W/R	4'h8	
Register 2 (0x02) Default: 24'h0001E7					
0x02	[8:7]	CTRL_VREF_COMP_V	W/R	2'h3	
	[6:0]	CTRLB_VREF_COMP_I	W/R	7'h67	
Register 3 (0x03) Default: 24'h000258					
0x03	[23:0]	TIME_COUNTING	W/R	24'h000258	
Register 4 (0x04) Default: 24'h00000A					
0x04	[23:12]	TIME_MONITOR_HOLD	W/R	12'h000	
	[11:0]	TIME_MONITORING	W/R	12'h00A	
Register 5 (0x05) Default: 24'h028014					
0x05	[23:12]	THRESHOLD_HIGH	W/R	12'h028	
	[11:0]	THRESHOLD_LOW	W/R	12'h014	
Register 6 (0x06) Default: 24'h000000					
0x06	[0]	OBSEN_AFEOUT	W/R	1'h0	
Register 7 (0x07) Default: 24'h000000					
0x07	[1:0]	OBSSEL_ABUF	W/R	2'h0	
Register 8 (0x08) Default: 24'h000000					
0x08	[1]	OVSEL_IBIAS_VBIAS	W/R	1'h0	
	[0]	OVSEL_VREF_COMP	W/R	1'h0	
Register 9 (0x09) Default: 24'h000000					
0x09	[1]	OVVAL_DIN	W/R	1'h0	
	[0]	OVSEL_DIN	W/R	1'h0	
Register 10 (0x0A) Default: 24'h000000					
0x0A	[1]	OVVAL_CLK	W/R	1'h0	
	[0]	OVSEL_CLK	W/R	1'h0	
Register 11 (0x0B) Default: 24'h000000					
0x0B	[5:1]	OVVAL_CONFIG	W/R	5'h00	
	[0]	OVSEL_CONFIG	W/R	1'h0	
Register 12 (0x0C) Default: 24'h000000					
0x0C	[3:1]	OVVAL_MONITOR_STATE	W/R	3'h0	

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Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
	[0]	OVSEL_MONITOR_STATE	W/R	1'h0	
Register 13 (0x0D) Default: 24'h000000					
0x0D	[3:1]	OVVAL_COUNTER_STATE	W/R	3'h0	
	[0]	OVSEL_COUNTER_STATE	W/R	1'h0	
Register 14 (0x0E) Default: 24'h000000					
0x0E	[13:7]	OVVAL_CTRLB_ICHARGE_MUL	W/R	7'h00	
	[6:2]	OVVAL_CTRLB_ICHARGE_DIV	W/R	5'h00	
	[1]	OVVAL_CTRL_ICHARGE_MUL_LOWLEAK	W/R	1'h0	
	[0]	OVVAL_CTRL_ICHARGE_DIV_LOWLEAK	W/R	1'h0	
Register 15 (0x0F) Default: 24'h000000					
0x0F	[3]	OVSEL_CTRLB_ICHARGE_MUL	W/R	1'h0	
	[2]	OVSEL_CTRLB_ICHARGE_DIV	W/R	1'h0	
	[1]	OVSEL_CTRL_ICHARGE_MUL_LOWLEAK	W/R	1'h0	
	[0]	OVSEL_CTRL_ICHARGE_DIV_LOWLEAK	W/R	1'h0	
Register 16 (0x10) Default: 24'h000000					
0x10	[23:0]	DOUT_LOWER	R	24'h000000	
Register 17 (0x11) Default: 24'h000000					
0x11	[23]	DOUT_OVERFLOW	R	1'h0	
	[22:0]	DOUT_UPPER	R	23'h000000	
Register 18 (0x12) Default: 24'h000000					
0x12	[4:0]	LDC_CONFIG	R	5'h00	
Register 19 (0x13) Default: 24'h000000					
0x13	[13:7]	CTRLB_ICHARGE_MUL	R	7'h00	
	[6:2]	CTRLB_ICHARGE_DIV	R	5'h00	
	[1]	CTRL_ICHARGE_MUL_LOWLEAK	R	1'h0	
	[0]	CTRL_ICHARGE_DIV_LOWLEAK	R	1'h0	
Register 20 (0x14) Default: 24'h000000					
0x14	[12]	MONITOR_OVERFLOW	R	1'h0	
	[11:0]	MONITOR	R	12'h000	
Register 21 (0x15) Default: 24'h000000					
0x15	[2:0]	MONITOR_STATE	R	3'h0	
Register 22 (0x16) Default: 24'h000000					
0x16	[2:0]	COUNTER_STATE	R	3'h0	
Register 23 (0x17) Default: 24'h000000					
0x17	[4:1]	FDIV_CTRL_FREQ	W/R	4'h0	
	[0]	FDIV_RESETN	W/R	1'h0	
Register 32 (0x20) Default: 24'h000060					
0x20	[6]	TMR_SLEEP	W/R	1'h1	
	[5]	TMR_ISOLATE	W/R	1'h1	
	[4]	TMR_RESETB	W/R	1'h0	
	[3]	TMR_EN_OSC	W/R	1'h0	
	[2]	TMR_RESETB_DIV	W/R	1'h0	
	[1]	TMR_RESETB_DCDC	W/R	1'h0	
	[0]	TMR_EN_SELF_CLK	W/R	1'h0	
Register 33 (0x21) Default: 24'hE80813					
0x21	[23]	TMR_SEL_CLK_DIV	W/R	1'h1	
	[22]	TMR_SEL_CLK_OSC	W/R	1'h1	
	[21]	TMR_SELF_EN	W/R	1'h1	
	[20:17]	TMR_IBIAS_REF	W/R	4'h4	
	[16]	TMR_CASCODE_BOOST	W/R	1'h0	

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Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
	[15:8]	TMR_SEL_CAP	W/R	8'h08	
	[7:2]	TMR_SEL_DCAP	W/R	6'h04	
	[1]	TMR_EN_TUNE1	W/R	1'h1	
	[0]	TMR_EN_TUNE2	W/R	1'h1	
Register 34 (0x22) Default: 24'h9FFDFC					
0x22	[23:21]	TMR_S	W/R	3'h4	
	[20:7]	TMR_DIFF_CON	W/R	14'h3FFB	
	[6]	TMR_POLY_CON	W/R	1'h1	
	[5]	TMR_EN_TUNE1_RES	W/R	1'h1	
	[4]	TMR_EN_TUNE2_RES	W/R	1'h1	
	[3]	TMR_SAMPLE_EN	W/R	1'h1	
	[2:0]	TMR_AFC	W/R	3'h4	
Register 48 (0x30) Default: 24'h000019					
0x30	[5]	WAKEUP_ON_PEND_REQ	W/R	1'h0	
	[4]	MBUS_IGNORE_RX_FAIL	W/R	1'h1	
	[3:2]	CLKGEN_DIV	W/R	2'h2	
	[1:0]	CLKGEN_RING	W/R	2'h1	
Register 49 (0x31) Default: 24'h001000					
0x31	[15:8]	LDC_IRQ_SHORT_ADDR	W/R	8'h10	
	[7:0]	LDC_IRQ_REG_ADDR	W/R	8'h00	
Register 50 (0x32) Default: 24'h001001					
0x32	[15:8]	LDC_IRQ_START_REG_ADDR	W/R	8'h10	
	[7:0]	LDC_IRQ_NUM_REG_1	W/R	8'h01	
Register 64 (0x40) Default: 24'h600000					
0x40	[23]	WUP_ENABLE	W/R	1'h0	
	[22]	WUP_LC_IRQ_EN	W/R	1'h1	
	[21]	WUP_AUTO_RESET	W/R	1'h1	
	[19]	WUP_ENABLE_CLK_SLP_OUT	W/R	1'h0	
Register 65 (0x41) Default: 24'h000000					
0x41	[7:0]	WUP_THRESHOLD_EXT	W/R	8'h00	
Register 66 (0x42) Default: 24'h2DC6C0					
0x42	[23:0]	WUP_THRESHOLD	W/R	24'h2DC6C0	
Register 67 (0x43) Default: 24'h000000					
0x43	[7:0]	WUP_CNT_VALUE_EXT	R	8'h00	
Register 68 (0x44) Default: 24'h000000					
0x44	[23:0]	WUP_CNT_VALUE	R	24'h000000	
Register 69 (0x45) Default: 24'h025001					
0x45	[23:0]	WUP_IRQ_PAYLOAD	W/R	24'h025001	
Register 70 (0x46) Default: 24'h001000					
0x46	[15:8]	WUP_IRQ_SHORT_ADDR	W/R	8'h10	
	[7:0]	WUP_IRQ_REG_ADDR	W/R	8'h00	
Register 71 (0x47) Default: 24'h003500					
0x47	[15:8]	WUP_IRQ_START_REG_ADDR	W/R	8'h35	
	[7:0]	WUP_IRQ_NUM_REG_1	W/R	8'h00	

Table 1: LNTv1B MBus Register File Mapping

1.2 MBus Register Descriptions

1.2.1 Register 0 (0x00)

WAKEUP_WHEN_DONE Reg 0x00, Bit Field: [6], Default: 1'h0, W/R

MODE_CONTINUOUS Reg 0x00, Bit Field: [5], Default: 1'h0, W/R

DBE_ENABLE Reg 0x00, Bit Field: [4], Default: 1'h0, W/R

RESET_AFE Reg 0x00, Bit Field: [3], Default: 1'h1, W/R

RESETN_DBE Reg 0x00, Bit Field: [2], Default: 1'h0, W/R

LDC_ISOLATE Reg 0x00, Bit Field: [1], Default: 1'h1, W/R

LDC_PG Reg 0x00, Bit Field: [0], Default: 1'h1, W/R

1.2.2 Register 1 (0x01)

CTRL_CAPSIZE Reg 0x01, Bit Field: [14:12], Default: 3'h3, W/R

CTRL_ICOMP Reg 0x01, Bit Field: [11:9], Default: 3'h3, W/R

CTRL_VOFS_CANCEL Reg 0x01, Bit Field: [8], Default: 1'h1, W/R

CTRL_IBIAS_VBIAS Reg 0x01, Bit Field: [7:4], Default: 4'h7, W/R

CTRL_IBIAS_I Reg 0x01, Bit Field: [3:0], Default: 4'h8, W/R

1.2.3 Register 2 (0x02)

CTRL_VREF_COMP_V Reg 0x02, Bit Field: [8:7], Default: 2'h3, W/R

CTRLB_VREF_COMP_I Reg 0x02, Bit Field: [6:0], Default: 7'h67, W/R

1.2.4 Register 3 (0x03)

TIME_COUNTING Reg 0x03, Bit Field: [23:0], Default: 24'h000258, W/R

1.2.5 Register 4 (0x04)

TIME_MONITOR_HOLD Reg 0x04, Bit Field: [23:12], Default: 12'h000, W/R

TIME_MONITORING Reg 0x04, Bit Field: [11:0], Default: 12'h00A, W/R

1.2.6 Register 5 (0x05)

THRESHOLD_HIGH Reg 0x05, Bit Field: [23:12], Default: 12'h028, W/R

THRESHOLD_LOW Reg 0x05, Bit Field: [11:0], Default: 12'h014, W/R

1.2.7 Register 6 (0x06)

OBSEN_AFEOUT Reg 0x06, Bit Field: [0], Default: 1'h0, W/R

1.2.8 Register 7 (0x07)

OBSSEL_ABUF Reg 0x07, Bit Field: [1:0], Default: 2'h0, W/R

1.2.9 Register 8 (0x08)

OVSEL_IBIAS_VBIAS Reg 0x08, Bit Field: [1], Default: 1'h0, W/R

OVSEL_VREF_COMP Reg 0x08, Bit Field: [0], Default: 1'h0, W/R

1.2.10 Register 9 (0x09)

OVVAL_DIN Reg 0x09, Bit Field: [1], Default: 1'h0, W/R

OVSEL_DIN Reg 0x09, Bit Field: [0], Default: 1'h0, W/R

1.2.11 Register 10 (0x0A)

OVVAL_CLK Reg 0x0A, Bit Field: [1], Default: 1'h0, W/R

OVSEL_CLK Reg 0x0A, Bit Field: [0], Default: 1'h0, W/R

1.2.12 Register 11 (0x0B)

OVVAL_CONFIG Reg 0x0B, Bit Field: [5:1], Default: 5'h00, W/R

OVSEL_CONFIG Reg 0x0B, Bit Field: [0], Default: 1'h0, W/R

1.2.13 Register 12 (0x0C)

OVVAL_MONITOR_STATE Reg 0x0C, Bit Field: [3:1], Default: 3'h0, W/R

OVSEL_MONITOR_STATE Reg 0x0C, Bit Field: [0], Default: 1'h0, W/R

1.2.14 Register 13 (0x0D)

OVVAL_COUNTER_STATE Reg 0x0D, Bit Field: [3:1], Default: 3'h0, W/R

OVSEL_COUNTER_STATE Reg 0x0D, Bit Field: [0], Default: 1'h0, W/R

1.2.15 Register 14 (0x0E)

OVVAL_CTRLB_ICHARGE_MUL Reg 0x0E, Bit Field: [13:7], Default: 7'h00, W/R

OVVAL_CTRLB_ICHARGE_DIV Reg 0x0E, Bit Field: [6:2], Default: 5'h00, W/R

OVVAL_CTRL_ICHARGE_MUL_LOWLEAK Reg 0x0E, Bit Field: [1], Default: 1'h0, W/R

OVVAL_CTRL_ICHARGE_DIV_LOWLEAK Reg 0x0E, Bit Field: [0], Default: 1'h0, W/R

1.2.16 Register 15 (0x0F)

OVSEL_CTRLB_ICHARGE_MUL Reg 0x0F, Bit Field: [3], Default: 1'h0, W/R

OVSEL_CTRLB_ICHARGE_DIV Reg 0x0F, Bit Field: [2], Default: 1'h0, W/R

OVSEL_CTRL_ICHARGE_MUL_LOWLEAK Reg 0x0F, Bit Field: [1], Default: 1'h0, W/R

OVSEL_CTRL_ICHARGE_DIV_LOWLEAK Reg 0x0F, Bit Field: [0], Default: 1'h0, W/R

1.2.17 Register 16 (0x10)

DOUT_LOWER Reg 0x10, Bit Field: [23:0], Default: 24'h000000, R

1.2.18 Register 17 (0x11)

DOUT_OVERFLOW Reg 0x11, Bit Field: [23], Default: 1'h0, R

DOUT_UPPER Reg 0x11, Bit Field: [22:0], Default: 23'h000000, R

1.2.19 Register 18 (0x12)

LDC_CONFIG Reg 0x12, Bit Field: [4:0], Default: 5'h00, R

1.2.20 Register 19 (0x13)

CTRLB_ICHARGE_MUL Reg 0x13, Bit Field: [13:7], Default: 7'h00, R

CTRLB_ICHARGE_DIV Reg 0x13, Bit Field: [6:2], Default: 5'h00, R

CTRL_ICHARGE_MUL_LOWLEAK Reg 0x13, Bit Field: [1], Default: 1'h0, R

CTRL_ICHARGE_DIV_LOWLEAK Reg 0x13, Bit Field: [0], Default: 1'h0, R

1.2.21 Register 20 (0x14)

MONITOR_OVERFLOW Reg 0x14, Bit Field: [12], Default: 1'h0, R

MONITOR Reg 0x14, Bit Field: [11:0], Default: 12'h000, R

1.2.22 Register 21 (0x15)

MONITOR_STATE Reg 0x15, Bit Field: [2:0], Default: 3'h0, R

1.2.23 Register 22 (0x16)

COUNTER_STATE Reg 0x16, Bit Field: [2:0], Default: 3'h0, R

1.2.24 Register 23 (0x17)

FDIV_CTRL_FREQ Reg 0x17, Bit Field: [4:1], Default: 4'h0, W/R

FDIV_RESETN Reg 0x17, Bit Field: [0], Default: 1'h0, W/R

1.2.25 Register 32 (0x20)

TMR_SLEEP Reg 0x20, Bit Field: [6], Default: 1'h1, W/R

TMR_ISOLATE Reg 0x20, Bit Field: [5], Default: 1'h1, W/R

TMR_RESETB Reg 0x20, Bit Field: [4], Default: 1'h0, W/R

TMR_EN_OSC Reg 0x20, Bit Field: [3], Default: 1'h0, W/R

TMR_RESETB_DIV Reg 0x20, Bit Field: [2], Default: 1'h0, W/R

TMR_RESETB_DCDC Reg 0x20, Bit Field: [1], Default: 1'h0, W/R

TMR_EN_SELF_CLK Reg 0x20, Bit Field: [0], Default: 1'h0, W/R

1.2.26 Register 33 (0x21)

TMR_SEL_CLK_DIV Reg 0x21, Bit Field: [23], Default: 1'h1, W/R

TMR_SEL_CLK_OSC Reg 0x21, Bit Field: [22], Default: 1'h1, W/R

TMR_SELF_EN Reg 0x21, Bit Field: [21], Default: 1'h1, W/R

TMR_IBIAS_REF Reg 0x21, Bit Field: [20:17], Default: 4'h4, W/R

TMR_CASCODE_BOOST Reg 0x21, Bit Field: [16], Default: 1'h0, W/R

TMR_SEL_CAP Reg 0x21, Bit Field: [15:8], Default: 8'h08, W/R

TMR_SEL_DCAP Reg 0x21, Bit Field: [7:2], Default: 6'h04, W/R

TMR_EN_TUNE1 Reg 0x21, Bit Field: [1], Default: 1'h1, W/R

TMR_EN_TUNE2 Reg 0x21, Bit Field: [0], Default: 1'h1, W/R

1.2.27 Register 34 (0x22)

TMR_S Reg 0x22, Bit Field: [23:21], Default: 3'h4, W/R

TMR_DIFF_CON Reg 0x22, Bit Field: [20:7], Default: 14'h3FFB, W/R

TMR_POLY_CON Reg 0x22, Bit Field: [6], Default: 1'h1, W/R

TMR_EN_TUNE1_RES Reg 0x22, Bit Field: [5], Default: 1'h1, W/R

TMR_EN_TUNE2_RES Reg 0x22, Bit Field: [4], Default: 1'h1, W/R

TMR_SAMPLE_EN Reg 0x22, Bit Field: [3], Default: 1'h1, W/R

TMR_AFC Reg 0x22, Bit Field: [2:0], Default: 3'h4, W/R

1.2.28 Register 48 (0x30)

WAKEUP_ON_PEND_REQ Reg 0x30, Bit Field: [5], Default: 1'h0, W/R

MBUS_IGNORE_RX_FAIL Reg 0x30, Bit Field: [4], Default: 1'h1, W/R

CLKGEN_DIV Reg 0x30, Bit Field: [3:2], Default: 2'h2, W/R

CLKGEN_RING Reg 0x30, Bit Field: [1:0], Default: 2'h1, W/R

1.2.29 Register 49 (0x31)

LDC_IRQ_SHORT_ADDR Reg 0x31, Bit Field: [15:8], Default: 8'h10, W/R

LDC_IRQ_REG_ADDR Reg 0x31, Bit Field: [7:0], Default: 8'h00, W/R

1.2.30 Register 50 (0x32)

LDC_IRQ_START_REG_ADDR Reg 0x32, Bit Field: [15:8], Default: 8'h10, W/R

LDC_IRQ_NUM_REG_1 Reg 0x32, Bit Field: [7:0], Default: 8'h01, W/R

1.2.31 Register 64 (0x40)

WUP_ENABLE Reg 0x40, Bit Field: [23], Default: 1'h0, W/R

WUP_LC_IRQ_EN Reg 0x40, Bit Field: [22], Default: 1'h1, W/R

WUP_AUTO_RESET Reg 0x40, Bit Field: [21], Default: 1'h1, W/R

WUP_ENABLE_CLK_SLP_OUT Reg 0x40, Bit Field: [19], Default: 1'h0, W/R

1.2.32 Register 65 (0x41)

WUP_THRESHOLD_EXT Reg 0x41, Bit Field: [7:0], Default: 8'h00, W/R

1.2.33 Register 66 (0x42)

WUP_THRESHOLD Reg 0x42, Bit Field: [23:0], Default: 24'h2DC6C0, W/R

1.2.34 Register 67 (0x43)

WUP_CNT_VALUE_EXT Reg 0x43, Bit Field: [7:0], Default: 8'h00, R

1.2.35 Register 68 (0x44)

WUP_CNT_VALUE Reg 0x44, Bit Field: [23:0], Default: 24'h000000, R

1.2.36 Register 69 (0x45)

WUP_IRQ_PAYLOAD Reg 0x45, Bit Field: [23:0], Default: 24'h025001, W/R

1.2.37 Register 70 (0x46)

WUP_IRQ_SHORT_ADDR Reg 0x46, Bit Field: [15:8], Default: 8'h10, W/R

WUP_IRQ_REG_ADDR Reg 0x46, Bit Field: [7:0], Default: 8'h00, W/R

1.2.38 Register 71 (0x47)

WUP_IRQ_START_REG_ADDR Reg 0x47, Bit Field: [15:8], Default: 8'h35, W/R

WUP_IRQ_NUM_REG_1 Reg 0x47, Bit Field: [7:0], Default: 8'h00, W/R