M3 Resistance-to-Digital Conversion (Version 3) Documentation (RDCv3)

Revision 1.0

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March 16, 2019

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1 MBus Register File

1.1 MBus Register File Mapping

Table 1 shows MBus Register File mapping information. 'NR' indicates a non-retentive register.

Reg Addr	Bit Field	Reg Name	Property	Size & Reset	Remark
Register 0 (0x00) Default: 24'h000019					
0x00	[6]	WAKEUP_UPON_RDC_IRQ	W/R	1'h0	
	[5]	MBC_WAKEUP_ON_PEND_REQ	W/R	1'h0	
	[4]	MBC_IGNORE_RX_FAIL	W/R	1'h1	
	[3:2]	LC_CLK_DIV	W/R	2'h2	
	[1:0]	LC_CLK_RING	W/R	2'h1	
Register 1 (0x01) Default: 24'h001007					
0x01	[15:8]	IRQ_RPLY_SHORT_ADDR	W/R	8'h10	
	[7:0]	IRQ_RPLY_REG_ADDR	W/R	8'h07	
Register 2 (0x02) Default: 24'h001100					
0x02	[15:8]	IRQ_RPLY_PYLD_REG_ADDR	W/R	8'h11	
	[7:0]	IRQ_RPLY_PYLD_LENGTH_1	W/R	8'h00	
Register 16 (0x10) Default: 24'h022003					
0x10	[23:0]	RDC_SIGNATURE	W/R	24'h022003	
Register 17 (0x11) Default: 24'h000000					
0x11	[16:0]	RDC_DOUT_OS	R	17'h00000	
Register 32 (0x20) Default: 24'h021419					
0x20	[17]	RDC_ISOLATE	W/R	1'h1	
	[15]	RDC_RESETn_FSM	W/R	1'h0	
	[14:6]	RDC_CNT_INIT	W/R	9'h050	
	[5:1]	RDC_CNT_AMP1	W/R	5'h0C	
	[0]	RDC_EN_AZ	W/R	1'h1	
Register 33 (0x21) Default: 24'h011106					
0x21	[18:15]	RDC_CNT_AZ_RESETB	W/R	4'h2	
	[14:10]	RDC_CNT_STORE	W/R	5'h04	
	[9:5]	RDC_CNT_REDIS	W/R	5'h08	
	[4:0]	RDC_CNT_AMP2	W/R	5'h06	
Register 34 (0x22) Default: 24'h000488					
0x22	[12:9]	RDC_CNT_IDLE	W/R	4'h2	
	[8:7]	RDC_CNT_SKIP	W/R	2'h1	
	[6:0]	RDC_OSR	W/R	7'h08	
Register 35 (0x23) Default: 24'h0000B6					
0x23	[12:8]	RDC_VREF_I_AMP_LC	W/R	5'h00	
	[7:2]	RDC_VCM_R_SEL_LC	W/R	6'h2D	
	[1:0]	RDC_I_VCM_GEN_n_LC	W/R	2'h2	
Register 36 (0x24) Default: 24'h016476					
0x24	[17:14]	RDC_SEL_DLY	W/R	4'h5	
	[13]	RDC_SEL_STORE	W/R	1'h1	
	[12:8]	RDC_SEL_VB2_LC	W/R	5'h04	
	[7:5]	RDC_SEL_VB3b_LC	W/R	3'h3	
	[4:0]	RDC_SEL_GAIN_LC	W/R	5'h16	
Register 37 (0x25) Default: 24'h00164B					
0x25	[12:8]	RDC_OFFSET_P_LC	W/R	5'h16	
	[7:3]	RDC_OFFSET_PB_LC	W/R	5'h09	

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Reg Addr	**Bit Field**	**Reg Name**	**Property**	**Size & Reset**	**Remark**
	[2:0]	RDC_I_AMP_BIASGEN	W/R	3'h3	
Register 38 (0x26) Default: 24'h0000FC					
0x26	[7:5]	RDC_OFFSET_SELN_B_LC	W/R	3'h7	
	[4:2]	RDC_OFFSET_SELP_B_LC	W/R	3'h7	
	[1]	RDC_SEL_ADC_MODE	W/R	1'h0	
	[0]	RDC_ENb_DWA	W/R	1'h0	
Register 39 (0x27) Default: 24'h000005					
0x27	[2:0]	RDC_I_BUF_VH_n_LC	W/R	3'h5	
Register 40 (0x28) Default: 24'h060005					
0x28	[18]	RDC_RESET_RC_OSC	W/R	1'h1	
	[17:14]	RDC_R_REF	W/R	4'h8	
	[13:10]	RDC_I_BUF	W/R	4'h0	
	[9:6]	RDC_I_BUF2	W/R	4'h0	
	[5:2]	RDC_I_CMP	W/R	4'h1	
	[1:0]	RDC_I_MIRROR	W/R	2'h1	
Register 41 (0x29) Default: 24'h000200					
0x29	[14:0]	RDC_PDIFF	W/R	15'h0200	
Register 42 (0x2A) Default: 24'h004000					
0x2A	[23:0]	RDC_POLY	W/R	24'h004000	
Register 43 (0x2B) Default: 24'h000049					
0x2B	[6:4]	RDC_MIM	W/R	3'h4	
	[3:1]	RDC_MOM	W/R	3'h4	
	[0]	RDC_CLK_ISOLATE	W/R	1'h1	
Register 44 (0x2C) Default: 24'h0007C4					
0x2C	[10]	RDC_EN_PG_FSM	W/R	1'h1	
	[9]	RDC_EN_PG_AMP_V1P2	W/R	1'h1	
	[8]	RDC_EN_PG_ADC_V1P2	W/R	1'h1	
	[7]	RDC_EN_PG_BUF_VH_V1P2	W/R	1'h1	
	[6]	RDC_EN_PG_RC_OSC	W/R	1'h1	
	[5]	RDC_ENb_PG_VREF	W/R	1'h0	
	[4]	RDC_ENb_PG_AMP_VBAT	W/R	1'h0	
	[3]	RDC_ENb_PG_ADC_VBAT	W/R	1'h0	
	[2]	RDC_ENb_MIRROR_LDO	W/R	1'h1	
	[1]	RDC_ENb_PG_BUF_VCM	W/R	1'h0	
	[0]	RDC_ENb_PG_BUF_VH_VBAT	W/R	1'h0	

Table 1: RDCv3 MBus Register File Mapping

1.2 MBus Register Descriptions

1.2.1 Register 0 (0x00)

WAKEUP_UPON_RDC_IRQ Reg 0x00, Bit Field: [6], Default: 1'h0, W/R

MBC_WAKEUP_ON_PEND_REQ Reg 0x00, Bit Field: [5], Default: 1'h0, W/R

MBC_IGNORE_RX_FAIL Reg 0x00, Bit Field: [4], Default: 1'h1, W/R

LC_CLK_DIV Reg 0x00, Bit Field: [3:2], Default: 2'h2, W/R

LC_CLK_RING Reg 0x00, Bit Field: [1:0], Default: 2'h1, W/R

1.2.2 Register 1 (0x01)

IRQ_RPLY_SHORT_ADDR Reg 0x01, Bit Field: [15:8], Default: 8'h10, W/R

IRQ_RPLY_REG_ADDR Reg 0x01, Bit Field: [7:0], Default: 8'h07, W/R

1.2.3 Register 2 (0x02)

IRQ_RPLY_PYLD_REG_ADDR Reg 0x02, Bit Field: [15:8], Default: 8'h11, W/R

IRQ_RPLY_PYLD_LENGTH_1 Reg 0x02, Bit Field: [7:0], Default: 8'h00, W/R

1.2.4 Register 16 (0x10)

RDC_SIGNATURE Reg 0x10, Bit Field: [23:0], Default: 24'h022003, W/R

1.2.5 Register 17 (0x11)

RDC_DOUT_OS Reg 0x11, Bit Field: [16:0], Default: 17'h00000, R

1.2.6 Register 32 (0x20)

RDC_ISOLATE Reg 0x20, Bit Field: [17], Default: 1'h1, W/R

RDC_RESETn_FSM Reg 0x20, Bit Field: [15], Default: 1'h0, W/R

RDC_CNT_INIT Reg 0x20, Bit Field: [14:6], Default: 9'h050, W/R

RDC_CNT_AMP1 Reg 0x20, Bit Field: [5:1], Default: 5'h0C, W/R

RDC_EN_AZ Reg 0x20, Bit Field: [0], Default: 1'h1, W/R

1.2.7 Register 33 (0x21)

RDC_CNT_AZ_RESETB Reg 0x21, Bit Field: [18:15], Default: 4'h2, W/R

RDC_CNT_STORE Reg 0x21, Bit Field: [14:10], Default: 5'h04, W/R

RDC_CNT_REDIS Reg 0x21, Bit Field: [9:5], Default: 5'h08, W/R

RDC_CNT_AMP2 Reg 0x21, Bit Field: [4:0], Default: 5'h06, W/R

1.2.8 Register 34 (0x22)

RDC_CNT_IDLE Reg 0x22, Bit Field: [12:9], Default: 4'h2, W/R

RDC_CNT_SKIP Reg 0x22, Bit Field: [8:7], Default: 2'h1, W/R

RDC_OSR Reg 0x22, Bit Field: [6:0], Default: 7'h08, W/R

1.2.9 Register 35 (0x23)

RDC_VREF_I_AMP_LC Reg 0x23, Bit Field: [12:8], Default: 5'h00, W/R

RDC_VCM_R_SEL_LC Reg 0x23, Bit Field: [7:2], Default: 6'h2D, W/R

RDC_I_VCM_GEN_n_LC Reg 0x23, Bit Field: [1:0], Default: 2'h2, W/R

1.2.10 Register 36 (0x24)

RDC_SEL_DLY Reg 0x24, Bit Field: [17:14], Default: 4'h5, W/R

RDC_SEL_STORE Reg 0x24, Bit Field: [13], Default: 1'h1, W/R

RDC_SEL_VB2_LC Reg 0x24, Bit Field: [12:8], Default: 5'h04, W/R

RDC_SEL_VB3b_LC Reg 0x24, Bit Field: [7:5], Default: 3'h3, W/R

RDC_SEL_GAIN_LC Reg 0x24, Bit Field: [4:0], Default: 5'h16, W/R

1.2.11 Register 37 (0x25)

RDC_OFFSET_P_LC Reg 0x25, Bit Field: [12:8], Default: 5'h16, W/R

RDC_OFFSET_PB_LC Reg 0x25, Bit Field: [7:3], Default: 5'h09, W/R

RDC_I_AMP_BIASGEN Reg 0x25, Bit Field: [2:0], Default: 3'h3, W/R

1.2.12 Register 38 (0x26)

RDC_OFFSET_SELN_B_LC Reg 0x26, Bit Field: [7:5], Default: 3'h7, W/R

RDC_OFFSET_SELP_B_LC Reg 0x26, Bit Field: [4:2], Default: 3'h7, W/R

RDC_SEL_ADC_MODE Reg 0x26, Bit Field: [1], Default: 1'h0, W/R

RDC_ENb_DWA Reg 0x26, Bit Field: [0], Default: 1'h0, W/R

1.2.13 Register 39 (0x27)

RDC_I_BUF_VH_n_LC Reg 0x27, Bit Field: [2:0], Default: 3'h5, W/R

1.2.14 Register 40 (0x28)

RDC_RESET_RC_OSC Reg 0x28, Bit Field: [18], Default: 1'h1, W/R

RDC_R_REF Reg 0x28, Bit Field: [17:14], Default: 4'h8, W/R

RDC_I_BUF Reg 0x28, Bit Field: [13:10], Default: 4'h0, W/R

RDC_I_BUF2 Reg 0x28, Bit Field: [9:6], Default: 4'h0, W/R

RDC_I_CMP Reg 0x28, Bit Field: [5:2], Default: 4'h1, W/R

RDC_I_MIRROR Reg 0x28, Bit Field: [1:0], Default: 2'h1, W/R

1.2.15 Register 41 (0x29)

RDC_PDIFF Reg 0x29, Bit Field: [14:0], Default: 15'h0200, W/R

1.2.16 Register 42 (0x2A)

RDC_POLY Reg 0x2A, Bit Field: [23:0], Default: 24'h004000, W/R

1.2.17 Register 43 (0x2B)

RDC_MIM Reg 0x2B, Bit Field: [6:4], Default: 3'h4, W/R

RDC_MOM Reg 0x2B, Bit Field: [3:1], Default: 3'h4, W/R

RDC_CLK_ISOLATE Reg 0x2B, Bit Field: [0], Default: 1'h1, W/R

1.2.18 Register 44 (0x2C)

RDC_EN_PG_FSM Reg 0x2C, Bit Field: [10], Default: 1'h1, W/R

RDC_EN_PG_AMP_V1P2 Reg 0x2C, Bit Field: [9], Default: 1'h1, W/R

RDC_EN_PG_ADC_V1P2 Reg 0x2C, Bit Field: [8], Default: 1'h1, W/R

RDC_EN_PG_BUF_VH_V1P2 Reg 0x2C, Bit Field: [7], Default: 1'h1, W/R

RDC_EN_PG_RC_OSC Reg 0x2C, Bit Field: [6], Default: 1'h1, W/R

RDC_ENb_PG_VREF Reg 0x2C, Bit Field: [5], Default: 1'h0, W/R

RDC_ENb_PG_AMP_VBAT Reg 0x2C, Bit Field: [4], Default: 1'h0, W/R

RDC_ENb_PG_ADC_VBAT Reg 0x2C, Bit Field: [3], Default: 1'h0, W/R

RDC_ENb_MIRROR_LDO Reg 0x2C, Bit Field: [2], Default: 1'h1, W/R

RDC_ENb_PG_BUF_VCM Reg 0x2C, Bit Field: [1], Default: 1'h0, W/R

RDC_ENb_PG_BUF_VH_VBAT Reg 0x2C, Bit Field: [0], Default: 1'h0, W/R