M3 Medium Range Radio (Version 10) Documentation

(MRRv10)

Revision 2.0

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# Revision History

## MRRv7

* Power oscillator's transistor size increased

Version A : 2µm to 8µm   
Version B : 2µm to 16 µm

## MRRv8

* Chip width increased for sideway step back
* Double size ANT pads
* MBUS change
* Has Version A only

## MRRv9

* ANTP and ANTN Pad (100µm -> 50µm) (M1~M6 -> M3~M6)
* Has Version A and C

Version C : 5µm transistor size in the power oscillator

## MRRv10

* Added Voltage Clamp to fix chirp/settling
* Fixed floating S/D in the Power Oscillator tuning cap
* Increased division ratio in the RF Counter
* Has Version A, B and C

# Layer Description

The Medium Range Radio (MRRv10) (Figure II‑i & Figure II‑ii) contains TRX Radio, on-chip clock gen, and Linear Regulator.

* Designed in TSMC180 tsmc18rf
* Tapedout on May 6th 2019
* Top-Level layout is located at:  
  /afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/virtuoso/TSMC180/MRRv10A/layout

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/virtuoso/TSMC180/MRRv10B/layout

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/virtuoso/TSMC180/MRRv10C/layout

* Top-Level LVS CDL is located at:  
  /afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10A/cdl/MRRv10A.cdl

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10B/cdl/MRRv10B.cdl

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10C/cdl/MRRv10C.cdl

* Top-Level Finesim CDL is located at:  
  /afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10A/ckt/MRRv10A.ckt

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10B/ckt/MRRv10B.ckt

/afs/eecs.umich.edu/vlsida/projects/ m3\_hdk/layer/MRR/MRRv10C/ckt/MRRv10C.ckt

* MBUS Long Address is 20’h23004



Figure ‑ Medium Range Radio Layer (Version 10) (MRRv10) (1050um X 1630um)



Figure ‑ MRRv10 Wirebonding Diagram (MBUS only)

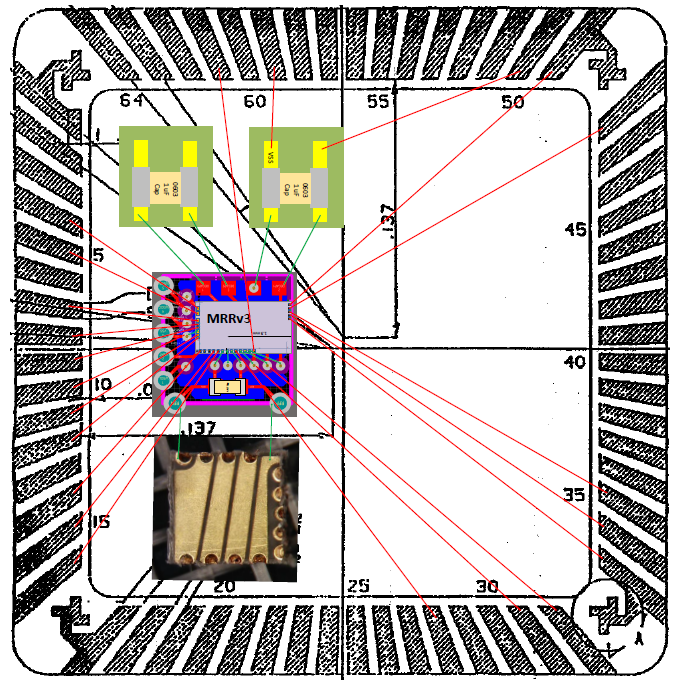


Figure II-iii MRR Wirebonding diagram w/ antenna example

# MBUS Register File

## Register File Mapping

Please see Table III‑1.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address | Register Name | W/R | Size & Reset | Bit Field |
| 0x00 | MRR\_TRX\_DIV\_RESETN | W/R | 1’h0 | [22] |
| MRR\_TRX\_DIV\_EN | W/R | 1’h0 | [21] |
| MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE | W/R | 10’h000 | [16:7] |
| MRR\_CL\_CTRL | W/R | 6’h08 | [6:1] |
| MRR\_CL\_EN | W/R | 1’h0 | [0] |
| 0x01 | MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE | W/R | 6’h00 | [21:16] |
| MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE | W/R | 6’h00 | [15:10] |
| MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE | W/R | 10’h000 | [9:0] |
| 0x02 | MRR\_TX\_PULSE\_FINE\_TUNE | W/R | 4’h7 | [18:15] |
| MRR\_TX\_PULSE\_FINE | W/R | 1’h0 | [14] |
| MRR\_TX\_EN\_OW | W/R | 1’h0 | [13] |
| MRR\_TX\_BIAS\_TUNE | W/R | 13’h1FFF | [12:0] |
| 0x03 | MRR\_RX\_AMP\_OW\_EN | W/R | 1’h0 | [21] |
| MRR\_TRX\_ISOLATEN | W/R | 1’h0 | [20] |
| MRR\_CAP\_P\_OW | W/R | 1’h0 | [19] |
| MRR\_CAP\_S\_OW | W/R | 1’h0 | [18] |
| MRR\_RX\_SAMPLE\_CAP | W/R | 3’h0 | [17:15] |
| MRR\_TRX\_MODE\_EN | W/R | 1’h0 | [14] |
| MRR\_RX\_EN\_OW | W/R | 1’h0 | [13] |
| MRR\_RX\_BIAS\_TUNE | W/R | 13’h0801 | [12:0] |
| 0x04 | LDO\_ VREF\_I\_AMP | W/R | 4’h0 | [19:16] |
| LDO\_ SEL\_VOUT | W/R | 3’h4 | [15:13] |
| LDO\_EN\_VREF | W/R | 1’h0 | [12] |
| LDO\_EN\_IREF | W/R | 1’h0 | [11] |
| LDO\_EN\_LDO | W/R | 1’h0 | [10] |
| RO\_EN\_MONITOR | W/R | 1’h0 | [9] |
| RO\_SEL\_DIV | W/R | 2’h0 | [8:7] |
| RO\_SEL\_EXT\_CLK | W/R | 1’h0 | [6] |
| RO\_EN\_CLK | W/R | 1’h0 | [5] |
| RO\_ISOLATE\_CLK | W/R | 1’h1 | [4] |
| RO\_RESET | W/R | 1’h1 | [3] |
| RO\_EN\_RO\_LDO | W/R | 1’h0 | [2] |
| RO\_EN\_RO\_V1P2\_PRE | W/R | 1’h0 | [1] |
| RO\_EN\_RO\_V1P2 | W/R | 1’h0 | [0] |
| 0x05 | RO\_R\_REF | W/R | 4’h8 | [23:20] |
| RO\_I\_BUF | W/R | 4’h0 | [19:16] |
| RO\_I\_BUF2 | W/R | 4’h0 | [15:12] |
| RO\_I\_CMP | W/R | 4’h1 | [11:8] |
| RO\_I\_MIRROR | W/R | 2’h1 | [7:6] |
| RO\_I\_MIRROR2 | W/R | 2’h1 | [5:4] |
| RO\_I\_MIRRb | W/R | 4’hD | [3:0 |
| 0x06 | RO\_PDIFF | W/R | 15’h1000 | [14:0] |
| 0x07 | RO\_MIM | W/R | 7’h10 | [13:7] |
| RO\_MOM | W/R | 7’h10 | [6:0] |
| 0x08 | RO\_POLY | W/R | 24’h400000 | [23:0] |
| 0x09 | MRR\_RAD\_FSM\_TX\_DATA\_0 | W/R | 24’h000000 | [23:0] |
| 0x0A | MRR\_RAD\_FSM\_TX\_DATA\_1 | W/R | 24’h000000 | [23:0] |
| 0x0B | MRR\_RAD\_FSM\_TX\_DATA\_2 | W/R | 24’h000000 | [23:0] |
| 0x0C | MRR\_RAD\_FSM\_TX\_DATA\_3 | W/R | 24’h000000 | [23:0] |
| 0x0D | MRR\_RAD\_FSM\_TX\_DATA\_4 | W/R | 24’h000000 | [23:0] |
| 0x0E | MRR\_RAD\_FSM\_TX\_DATA\_5 | W/R | 24’h000000 | [23:0] |
| 0x0F | MRR\_RAD\_FSM\_TX\_DATA\_6 | W/R | 24’h000000 | [23:0] |
| 0x10 | MRR\_RAD\_FSM\_TX\_DATA\_7 | W/R | 24’h000000 | [23:0] |
| 0x11 | MRR\_RAD\_FSM\_TX\_D\_LEN | W/R | 8’hC0 | [15:8] |
| MRR\_RAD\_FSM\_TX\_H\_LEN | W/R | 5’h0 | [7:3] |
| MRR\_RAD\_FSM\_EN | W/R | 1’h0 | [2] |
| MRR\_RAD\_FSM\_RSTN | W/R | 1’h0 | [1] |
| MRR\_RAD\_FSM\_SLEEP | W/R | 1’h0 | [0] |
| 0x12 | MRR\_RAD\_FSM\_ TX\_PR\_LEN | W/R | 3’h0 | [22:20] |
| MRR\_RAD\_FSM\_ TX\_PS\_LEN | W/R | 10’h031 | [19:10] |
| MRR\_RAD\_FSM\_TX\_LW\_LEN | W/R | 10’h018 | [9:0 |
| 0x13 | MRR\_RAD\_FSM\_TX\_MODE | W/R | 3’h3 | [23:21] |
| MRR\_RAD\_FSM\_SEED | W/R | 6’h01 | [20:15] |
| MRR\_RAD\_FSM\_TX\_C\_LEN | W/R | 15’h064 | [14:0] |
| 0x14 | MRR\_RAD\_FSM\_RX\_SAMPLE\_LEN | W/R | 3’h0 | [23:21] |
| MRR\_RAD\_FSM\_RX\_POWERON\_LEN | W/R | 2’h0 | [20:19] |
| MRR\_RAD\_FSM\_TX\_POWERON\_LEN | W/R | 3’h0 | [18:16] |
| MRR\_RAD\_FSM\_GUARD\_LEN | W/R | 14’h0 | [15:2] |
| MRR\_RAD\_FSM\_TX\_CNST\_LEN | W/R | 2’h0 | [1:0] |
| 0x15 | MRR\_RAD\_FSM\_TX\_HDR\_CNST | W/R | 4’h8 | [23:20] |
| MRR\_EN\_DIG\_MONITOR | W/R | 1’h0 | [19] |
| MRR\_RAD\_FSM\_RX\_DATA\_BITS | W/R | 7’h20 | [18:12] |
| MRR\_RAD\_FSM\_RX\_HDR\_TH | W/R | 6’h08 | [11:6] |
| MRR\_RAD\_FSM\_RX\_HDR\_BITS | W/R | 6’h08 | [5:0] |
| 0x16 | MRR\_RAD\_FSM\_CONT\_PULSE\_MODEb | W/R | 1’h1 | [12] |
| MRR\_DIG\_MONITOR\_SEL3 | W/R | 4’h0 | [11:8] |
| MRR\_DIG\_MONITOR\_SEL2 | W/R | 4’h0 | [7:4] |
| MRR\_DIG\_MONITOR\_SEL1 | W/R | 4’h0 | [3:0] |
| 0x17 | MRR\_RAD\_FSM\_SYNC\_SUC | R | 1’h0 | [11] |
| MRR\_RAD\_FSM\_LFSR | R | 6’h00 | [10:5] |
| MRR\_RAD\_FSM\_STATE | R | 5’h00 | [4:0] |
| 0x18 | MRR\_RAD\_FSM\_RX\_HDR\_0 | R | 24’hX | [23:0] |
| 0x19 | MRR\_RAD\_FSM\_RX\_HDR\_1 | R | 24’hX | [23:0] |
| 0x1A | MRR\_RAD\_FSM\_RX\_DATA\_0 | R | 24’hX | [23:0] |
| 0x1B | MRR\_RAD\_FSM\_RX\_DATA\_1 | R | 24’hX | [23:0] |
| 0x1C | MRR\_RAD\_FSM\_RX\_DATA\_2 | R | 24’hX | [23:0] |
| 0x1D | MRR\_RAD\_FSM\_RX\_DATA\_3 | R | 24’hX | [23:0] |
| 0x1E | MRR\_RAD\_FSM\_IRQ\_REPLY\_PACKET | W/R | 24’h001002 | [23:0] |
| 0x1F | IRQ packet to PRC  WAKEUP\_ON\_PEND\_REQ | W/R | 1’h0 | [5] |
| FIX ME  LC\_CLK\_LOAD | W/R | 1’h0 | [4] |
| LC\_CLK\_DIV | W/R | 2’h3 | [3:2] |
| LC\_CLK\_RING | W/R | 2’h3 | [1:0] |
| 0x20 | MRR\_TRX\_CNT\_OUT | R | 24’hX | [23:0] |
| 0x21 | MRR\_TRX\_RC\_IRQ\_EN | W/R | 1’h0 | [14] |
| MRR\_TRX\_SEL\_VCLAMP\_SLP | W/R | 2’h0 | [13:12] |
| MRR\_TRX\_EN\_SLP\_VCLAMP | W/R | 1’h0 | [11] |
| MRR\_TRX\_ENb\_CONT\_RC | W/R | 1’h1 | [10] |
| MRR\_TRX\_SEL\_VCLAMP | W/R | 6’h11 | [9:4] |
| MRR\_TRX\_RESETn\_RC\_CNT | W/R | 1’h0 | [3] |
| MRR\_TRX\_ISOLn\_COMP | W/R | 1’h0 | [2] |
| MRR\_TRX\_ENb\_COMP | W/R | 1’h1 | [1] |
| MRR\_TRX\_EN\_DIV | W/R | 1’h0 | [0] |
| 0x22 | MRR\_TRX\_RC\_CNT | R | 24’hX | [23:0] |
| 0x23 | MRR\_TRX\_RC\_IRQ\_REPLY\_PACKET | W/R | 24’h001003 | [23:0] |

Table ‑ Register File Mapping

## Register Descriptions

##### MRR\_TRX\_DIV\_RESETN

Resets CFO counter.

##### MRR\_TRX\_DIV\_EN

Controls CFO clock gating which is fed into a divider.

##### MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE

Controls CFO frequency by adjusting capacitance. Thermometer code with 100fF step size. Increasing this value will increase capacitance and thus decrease frequency. It has been designed to cover ~100MHz range. Note that ideally (assuming no mismatch) MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE should have same value as MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE to be symmetric. Also note that tuning range varies with center frequency. At lower center frequency, tuning range will be narrower while at high center frequency, tuning range will be wider. Following table shows simulated (after PEX) CFO for each code. See Table VII‑1/Table VII‑2 for expected CFO frequency with different configurations.

|  |  |
| --- | --- |
| MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE | Capacitance (fF) |
| 10’h000 | 0 |
| 10’h001 | 100 |
| 10’h003 | 200 |
| 10‘h007 | 300 |
| 10’h00F | 400 |
| 10’h01F | 500 |
| 10’h03F | 600 |
| 10’h07F | 700 |
| 10’h0FF | 800 |
| 10’h1FF | 900 |
| 10’h3FF | 1000 |

Table III‑2 Code vs Capacitance Values

##### MRR\_CL\_CTRL

Controls current limiter strength. Refer to following table for details. Detailed circuit is shown in “Figure IV-vi MRR Current Limiter.”

|  |  |  |  |
| --- | --- | --- | --- |
| MRR\_CL\_CTRL | Switch (Ω) | Resistor(Ω) | Total(Ω) |
| 0 | 26.5 | 0.0 | 26.5 |
| 1 | 26.5 | 112.1 | 138.7 |
| 2 | 133.0 | 1.09k | 1.22k |
| 3 | 672.6 | 10.85k | 11.52k |
| 4 | 3.7k | 106.7k | 110.4k |
| 5 | 35.6k | 1.14M | 1.18M |

Table III‑3 Current limiter strength vs code (simulated)

##### MRR\_CL\_EN

Enables current limiter (i.e. supplies current). Note that with addition of voltage limiter (in v10), current limiter can be controlled by the voltage limiter. Please refer to following table for right configuration.

|  |  |  |  |
| --- | --- | --- | --- |
| MRR\_CL\_EN | MRR\_TRX\_ISOLn\_COMP | MRR\_TRX\_ENb\_CONT\_RC | Current Limiter Configuration |
| 1’h0 | 1’hx | 1’hx | Always OFF |
| 1’h1 | 1’h0 | 1’hx | Always ON |
| 1’h1 | 1’h1 | 1’h0 | Controlled by Voltage clamp  Can be ON during TX |
| 1’h1 | 1’h1 | 1’h1 | Controlled by Voltage clamp  OFF during TX |

Table III‑4 Current limiter configurations

##### MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE

Controls CFO frequency by adjusting capacitance. Binary code with 5fF step size. Increasing this value will increase capacitance and thus decrease frequency. It has been designed to cover ~20MHz range. Note that ideally (assuming no mismatch) MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE should have same value as MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE to be symmetric. Also note that tuning range varies with center frequency. At lower center frequency, tuning range will be narrower while at high center frequency, tuning range will be wider. See Table VII‑1/Table VII‑2 for expected CFO frequency with different configurations.

##### MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE

Controls CFO frequency by adjusting capacitance. Binary code with 5fF step size. Refer to MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE for details. See Table VII‑1/Table VII‑2 for expected CFO frequency with different configurations.

##### MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE

Controls CFO frequency by adjusting capacitance. Thermometer code with 100fF step size. Refer to MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE for details. See Table VII‑1/Table VII‑2 for expected CFO frequency with different configurations.

##### MRR\_TX\_PULSE\_FINE\_TUNE (Reserved for other use)

Controls pulse width in TX mode. Effective only when MRR\_TX\_PULSE\_FINE = 1’h1.

##### MRR\_TX\_PULSE\_FINE (Reserved for other use)

Selects pulse control method in TX mode.

* 1’h0 : Pulse width set by FSM. Minimum pulse width is limited by FSM clock speed. Pulse width can be controlled at the integer multiple of the min value. <- need to check
* 1’h1: Pulse width set by internal pulse generator. Allows fine control using MRR\_TX\_PULSE\_FINE\_TUNE.

##### MRR\_TX\_EN\_OW

Overwrite signal for TX mode. Always transmitting when enabled (i.e. Power oscillator runs continuously).

##### MRR\_TX\_BIAS\_TUNE

Controls bias current of the Power Oscillator in TX mode. Thermometer code. Increasing this value will increase current consumption. See following table for the current consumption.

|  |  |  |
| --- | --- | --- |
| MRR\_TX\_BIAS\_TUNE | Current Consumption (µA) | |
| **Minimum cap**  MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE = 10’h0  MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE=10’h0  MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE=6’h0  MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE =6’h0 | **Maximum Cap**  MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE = 10’h3FF  MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE=10’h3FF  MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE=6’h3F  MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE =6’h3F |
| 13’h0001 | 41.6 | 41.5 |
| 13’h0003 | 75.7 | 75.5 |
| 13’h0007 | 109.7 | 109.8 |
| 13’h000F | 143.2 | 143.3 |
| 13’h001F | 274.2 | 275.6 |
| 13’h003F | 398.6 | 402.0 |
| 13’h007F | 485.0 | 507.3 |
| 13’h00FF | 535.0 | 570.5 |
| 13’h01FF | 572.6 | 613.7 |
| 13’h03FF | 604.0 | 648.0 |
| 13’h07FF | 631.9 | 677.3 |
| 13’h0FFF | 656.2 | 703.4 |
| 13’h1FFF | 678.5 | 726.2 |

Table III‑5 Code vs Current Consumption in the Power Oscillator (after PEX)

##### MRR\_RX\_AMP\_OW\_EN (Reserved for debug)

Enables voltage overwriting for controlling RX amplifier current. Overwrite voltage can be provided by from pads (either RX\_AMP\_PW or RX\_AMP\_PMOS, i.e. two pads on the bottom right).

##### MRR\_TRX\_ISOLATEN

Isolate signal.

##### MRR\_CAP\_P\_OW

Overwrite signal for decap configuration. Enabling this signal (=1’h1) will always put external decaps in parallel. See “Figure IV-i TRX Radio front-end of MRR” for configuration details.

##### MRR\_CAP\_S\_OW

Overwrite signal for decap configuration. Enabling this signal (=1’h1) will always put external decaps in series. See “Figure IV-i TRX Radio front-end of MRR” for configuration details.

##### MRR\_RX\_SAMPLE\_CAP

Controls sampling capacitance in RX mode. Thermometer code. Increasing this value will increase sampling capacitance which will help to reduce noise. See following table for capacitance values.

|  |  |
| --- | --- |
| MRR\_RX\_SAMPLE\_CAP | Sampling Capacitance (pF) |
| 3’h0 | 0.5 |
| 3’h1 | 1 (Default) |
| 3’h3 | 1.5 |
| 3’h7 | 2 |

Table III‑6 Code vs Sampling Capacitance (pF)

##### MRR\_TRX\_MODE\_EN

Enables RX. See “Figure IV-i TRX Radio front-end of MRR” for configuration details.

##### MRR\_RX\_EN\_OW (Reserved for debug)

Overwrite signal for RX mode. Always receiving when enabled (i.e. Power oscillator runs continuously). Effective only when MRR\_TRX\_MODE\_EN = 1’h1.

##### MRR\_RX\_BIAS\_TUNE

Controls bias current of the Power Oscillator in RX mode. Thermometer code. Increasing this value will increase bias current.

##### LDO\_ VREF\_I\_AMP

Controls bias current of body buffers used in the voltage reference.

##### LDO\_ SEL\_VOUT

Controls output voltage level of the LDO.

##### LDO\_EN\_VREF

Enables voltage reference.

##### LDO\_EN\_IREF

Enables current reference.

##### LDO\_EN\_LDO

Controls power gate of the LDO (from VBAT).

##### RO\_EN\_MONITOR

Enables monitoring of output frequency of on-chip clock gen through pad (CLK MON, second pad in the top left corner)

##### RO\_SEL\_DIV

Selects division ratio of the on-chip clock gen. See below table for details. Also, refer to Table VII‑3 for details on clock frequency values.

|  |  |  |
| --- | --- | --- |
| RO\_SEL\_DIV | Division ratio | Clock frequency (kHz) |
| 0 | 1 | 240 |
| 1 | 2 | 120 |
| 2 | 4 | 60 |
| 3 | 8 | 30 |

Table III‑7 Code vs Division ratio based on simulation results (TT after PEX)

##### RO\_SEL\_EXT\_CLK

Selects clock source for the RADIO FSM.

* 1’h0 : on-chip clock gen
* 1’h1 : External clock (EXT CLK, first pad in the top left corner)

##### RO\_EN\_CLK

Enables Radio FSM clock.

##### RO\_ISOLATE\_CLK

Isolates clock output.

##### RO\_RESET

Resets on-chip clock.

##### RO\_EN\_RO\_LDO

Resets on-chip clock.

##### RO\_EN\_RO\_V1P2\_PRE

Resets on-chip clock.

##### RO\_EN\_RO\_V1P2

Resets on-chip clock.

##### RO\_R\_REF

Controls resistance of the current source.

##### RO\_I\_BUF

Adjust the buffer bias current (Current REF).

##### RO\_I\_BUF2

Adjusts the buffer bias current (Composite resistor).

##### RO\_I\_CMP

Adjusts the comparator bias current. Increasing bit increases comparator speed and thus improves temperature coefficient (TC) of the reference clock (CLKREF) at the cost of higher power consumption. TC improves until comparator delay becomes negligible to the overall period.

##### RO\_I\_MIRROR

Adjusts main current.

##### RO\_I\_MIRROR2

Adjusts current level of the bias voltage generator used in the wide-swing current mirror.

##### RO\_I\_MIRRb

Adjusts bias voltages in the main current mirror.

##### RO\_PDIFF

Adjusts P+ diffusion resistor size. Increasing the value (decreasing the resistance) will make period more CTAT.

##### RO\_MIM

Adjusts MIM cap size. Increasing the value decreases clock frequency. See Table VII‑3 for details.

##### RO\_MOM

Adjusts MOM cap size. Increasing the value decreases clock frequency. See Table VII‑3 for details.

##### RO\_POLY

Adjust P+ poly resistor size. Increasing the value (decreasing the resistance) will make period more PTAT.

##### MRR\_RAD\_FSM\_TX\_DATA\_0

TX Data buffer (Bits: 0-23)

##### MRR\_RAD\_FSM\_TX\_DATA\_1

TX Data buffer (Bits: 24-47)

##### MRR\_RAD\_FSM\_TX\_DATA\_2

TX Data buffer (Bits: 48-71)

##### MRR\_RAD\_FSM\_TX\_DATA\_3

TX Data buffer (Bits: 72-95)

##### MRR\_RAD\_FSM\_TX\_DATA\_4

TX Data buffer (Bits: 96-119)

##### MRR\_RAD\_FSM\_TX\_DATA\_5

TX Data buffer (Bits: 120-143)

##### MRR\_RAD\_FSM\_TX\_DATA\_6

TX Data buffer (Bits: 144-167)

##### MRR\_RAD\_FSM\_TX\_DATA\_7

TX Data buffer (Bits: 168-191)

##### MRR\_RAD\_FSM\_TX\_D\_LEN

Set the number of transmitted bits

##### MRR\_RAD\_FSM\_TX\_H\_LEN (Reserved)

Set the number of transmitted header bits (not used typically)

##### MRR\_RAD\_FSM\_EN

Start the radio FSM

##### MRR\_RAD\_FSM\_RSTN

Reset the radio FSM

##### MRR\_RAD\_FSM\_SLEEP

Power gated the FSM

##### MRR\_RAD\_FSM\_ TX\_PR\_LEN

Set pulse repetition rate. See “Figure IV-iii MRR TX Pulse Configuration” for detailed explanation.

##### MRR\_RAD\_FSM\_ TX\_PS\_LEN

Set pulse spacing (ex: conventional 2PPM 🡪 PS\_LEN=PW\_LEN). See “Figure IV-iii MRR TX Pulse Configuration” for detailed explanation.

##### MRR\_RAD\_FSM\_TX\_PW\_LEN

Set pulse width. See “Figure IV-iii MRR TX Pulse Configuration” for detailed explanation.

##### MRR\_RAD\_FSM\_TX\_MODE (Reserved for other use, use code rate = 1 for default setting)

TX convolutional coding -- code rate **0**:4 **1**:3 **2**:2 **3**:1(baseline) **4**:1/2 **5**:1/3 **6**:1/4

When code rate (M) is greater than 1, TX will use 2M PPM modulation for enhanced data rate

##### MRR\_RAD\_FSM\_SEED (Reserved)

Set seed for TX header LFSR (not used typically)

##### MRR\_RAD\_FSM\_TX\_C\_LEN

Decap recharging time respect to PW\_LEN (ex: C\_LEN=32 if (PW\_LEN+1):C\_LEN=1:32). See “Figure IV-iii MRR TX Pulse Configuration” for detailed explanation.

##### MRR\_RAD\_FSM\_RX\_SAMPLE\_LEN

Set RX sample cap time (integration time, i.e. RX data rate). See “Figure IV-iv MRR RX Timing” and “Figure IV-v MRR RX Sampling Circuits Details.”

##### MRR\_RAD\_FSM\_RX\_POWERON\_LEN

Set RX power on time. See “Figure IV-ii MRR Packet Timing Register Controls” for detailed explanation.

##### MRR\_RAD\_FSM\_TX\_POWERON\_LEN

Set TX power on time. See “Figure IV-ii MRR Packet Timing Register Controls” for detailed explanation.

##### MRR\_RAD\_FSM\_GUARD\_LEN

Set TX power on time. See “Figure IV-ii MRR Packet Timing Register Controls” for detailed explanation.

##### MRR\_RAD\_FSM\_TX\_CNST\_LEN (Reserved)

TX convolutional code constraint length (https://en.wikipedia.org/wiki/Convolutional\_code)

##### MRR\_RAD\_FSM\_TX\_HDR\_CNST (Reserved)

TX LFSR shift due to different pulse width setting (not used typically)

##### MRR\_EN\_DIG\_MONITOR (Reserved for debug)

Enable digital monitor pad output

##### MRR\_RAD\_FSM\_RX\_DATA\_BITS

Set the number of RX bits

##### MRR\_RAD\_FSM\_RX\_HDR\_TH (Reserved, default should be 0)

RX PN-code check threshold, 0 🡪 don’t check

##### MRR\_RAD\_FSM\_RX\_HDR\_BITS (Reserved for debug)

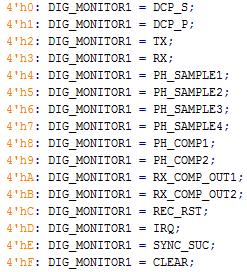
Set the number of RX header bits

##### MRR\_RAD\_FSM\_CONT\_PULSE\_MODEb

FIX ME

##### MRR\_DIG\_MONITOR\_SEL3 (Reserved for debug)

Selection of different FSM control signal monitoring



##### MRR\_DIG\_MONITOR\_SEL2 (Reserved for debug)

Selection of different FSM control signal monitoring

##### MRR\_DIG\_MONITOR\_SEL1 (Reserved for debug)

Selection of different FSM control signal monitoring

##### MRR\_RAD\_FSM\_SYNC\_SUC (Reserved for debug)

Indicator of FSM RX sync success (Read-only)

##### MRR\_RAD\_FSM\_LFSR (Reserved for debug)

FSM LFSR value (Read-only)

##### MRR\_RAD\_FSM\_STATE (Reserved for debug)

FSM state (Read-only)

##### MRR\_RAD\_FSM\_RX\_HDR\_0 (Reserved for debug)

RX header bits

##### MRR\_RAD\_FSM\_RX\_HDR\_1 (Reserved for debug)

RX header bits

##### MRR\_RAD\_FSM\_RX\_DATA\_0

RX data

##### MRR\_RAD\_FSM\_RX\_DATA\_1

RX data

##### MRR\_RAD\_FSM\_RX\_DATA\_2

RX data

##### MRR\_RAD\_FSM\_RX\_DATA\_3

RX data

##### MRR\_RAD\_FSM\_IRQ\_REPLY\_PACKET

Set the correct MBus IRQ packet configuration to PRC

##### WAKEUP\_ON\_PEND\_REQ

FIX ME

##### LC\_CLK\_LOAD

FIX ME

##### LC\_CLK\_DIV

Layer Controller’s Clock Divider. See Table III‑8. Used in conjunction with LC\_CLK\_RING.

|  |  |
| --- | --- |
| Value | Clock Division |
| 2’h0 | 8 |
| 2’h1 | 4 |
| 2’h2 | 2 |
| 2’h3 | 0 |

Table ‑ LC\_CLK\_DIV Register

##### LC\_CLK\_RING

Layer Controller’s Ring Oscillator’s Speed. See Table III‑9 & Table III‑10 for post-pex simulation results. Use in conjunction with LC\_CLK\_DIV.

|  |
| --- |
| 27°C  LC\_CLK\_DIV: 2’h3 |
| V0P6 (V) | 0.45 | 0.50 | 0.55 | 0.60 | 0.65 | 0.70 |
| V1P2 (V) | 0.90 | 1.00 | 1.10 | 1.20 | 0.30 | 1.40 |
| LC\_CLK\_RING: 2’h3 |
| Frequency (KHz) | 38.6 | 64.7 | 95.4 | 129 | 166 | 204 |
| V0P6 Power (nW) | 7.64 | 17.2 | 33.3 | 58.0 | 93.2 | 141 |
| V1P2 Power (nW) | 3.78 | 6.62 | 12.0 | 19.6 | 29.7 | 43.0 |
| V0P6 Leakage (pW) | 94.0 | 107 | 121 | 135 | 150 | 166 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h2 |
| Frequency (KHz) | 31.8 | 53.3 | 78.6 | 107 | 137 | 169 |
| V0P6 Power (nW) | 6.30 | 14.2 | 27.5 | 47.8 | 76.8 | 116 |
| V1P2 Power (nW) | 2.60 | 5.60 | 9.90 | 16.0 | 24.4 | 35.5 |
| V0P6 Leakage (pW) | 96.8 | 110 | 125 | 140 | 154 | 171 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h1 |
| Frequency (KHz) | 27.1 | 45.4 | 67.0 | 90.8 | 116 | 144 |
| V0P6 Power (nW) | 5.4 | 12.1 | 23.5 | 40.8 | 65.6 | 99.2 |
| V1P2 Power (nW) | 2.4 | 4.7 | 8.6 | 13.6 | 20.9 | 30.3 |
| V0P6 Leakage (pW) | 96.8 | 110 | 125 | 140 | 155 | 171 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h0 |
| Frequency (KHz) | 24.1 | 40.4 | 59.7 | 80.9 | 104 | 128 |
| V0P6 Power (nW) | 4.9 | 10.8 | 20.9 | 36.3 | 58.4 | 88.4 |
| V1P2 Power (nW) | 2.0 | 4.2 | 7.5 | 12.1 | 18.7 | 27.0 |
| V0P6 Leakage (pW) | 99.4 | 114 | 129 | 144 | 159 | 177 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |

Table ‑ LC\_CLK\_RING Register Post-Pex Results (27°C) (TT)[[4]](#footnote-4)

|  |
| --- |
| 40°C  LC\_CLK\_DIV: 2’h3 |
| V0P6 (V) | 0.45 | 0.50 | 0.55 | 0.60 | 0.65 | 0.70 |
| V1P2 (V) | 0.90 | 1.00 | 1.10 | 1.20 | 0.30 | 1.40 |
| LC\_CLK\_RING: 2’h3 |
| Frequency (KHz) | 43.4 | 70.0 | 100 | 134 | 170 | 207 |
| V0P6 Power (nW) | 8.9 | 19.2 | 36.2 | 61.6 | 97.5 | 145 |
| V1P2 Power (nW) | 3.7 | 7.3 | 12.7 | 20.4 | 30.7 | 43.9 |
| V0P6 Leakage (pW) | 189 | 216 | 244 | 273 | 303 | 335 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h2 |
| Frequency (KHz) | 35.7 | 57.6 | 83.0 | 111 | 140 | 171 |
| V0P6 Power (nW) | 7.4 | 15.9 | 29.9 | 50.9 | 80.4 | 120 |
| V1P2 Power (nW) | 3.0 | 6.0 | 10.6 | 16.8 | 25.3 | 36.2 |
| V0P6 Leakage (pW) | 196 | 223 | 252 | 282 | 313 | 346 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h1 |
| Frequency (KHz) | 30.4 | 49.1 | 70.8 | 94.3 | 119 | 145 |
| V0P6 Power (nW) | 6.4 | 13.6 | 25.5 | 44.5 | 68.7 | 103 |
| V1P2 Power (nW) | 2.5 | 5.2 | 8.9 | 14.4 | 21.7 | 31.1 |
| V0P6 Leakage (pW) | 195 | 220 | 252 | 282 | 313 | 346 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |
| LC\_CLK\_RING: 2’h0 |
| Frequency (KHz) | 27.1 | 43.7 | 63.0 | 83.9 | 106 | 129 |
| V0P6 Power (nW) | 5.7 | 12.1 | 22.8 | 38.7 | 61.2 | 91.3 |
| V1P2 Power (nW) | 2.4 | 4.6 | 8.1 | 12.8 | 19.3 | 27.7 |
| V0P6 Leakage (pW) | 202 | 230 | 260 | 291 | 323 | 357 |
| V1P2 Leakage (pW) | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 | ≈0 |

Table ‑ LC\_CLK\_RING Register Post-Pex Results (40°C) (TT)[[5]](#footnote-5)

##### MRR\_TRX\_CNT\_OUT

Count for CFO. Counter gets CFO/128 as an input.

##### MRR\_TRX\_RC\_IRQ\_EN

Enables RC\_IRQ. This is a mask signal for RC\_IRQ

##### MRR\_TRX\_SEL\_VCLAMP\_SLP

Adjusts clamped voltage of a sleep mode voltage clamp. See Figure III‑i for voltage levels.



Figure ‑ Clamped voltage vs temperature w.r.t different VBAT and MRR\_TRX\_SEL\_VCLAMP. Simulated at TT corner with 15nA decap leakage.

##### MRR\_TRX\_EN\_SLP\_VCLAMP

Enables sleep mode voltage clamp

##### MRR\_TRX\_ENb\_CONT\_RC

Enables or disables voltage clamp during TX. See Table III‑4 for detailed configurations.

##### MRR\_TRX\_SEL\_VCLAMP

Adjusts clamped voltage level. Clamped voltage level can be calculated as follows.

Clamped Voltage (V) = VREF/0.69 × (MRR\_TRX\_SEL\_VCLAMP × 0.05 + 2.7)

VREF level can be found in Table III‑11.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | TT | FF | SS | SF | FS |
| VREF (V) | 0.690 | 0.768 | 0.614 | 0.563 | 0.820 |

Table ‑ Simulated VREF values across corners.

If this value is set too high, VRAD won’t be able to recharge within time, i.e. does not reach plateau. If this value is too low, TX distance will degrade due to low VRAD. Proper value can be found by monitoring MRR\_TRX\_RC\_CNT.

##### MRR\_TRX\_RESETn\_RC\_CNT

Reset signal for recharge counter. See Table III‑4 for detailed configurations.

##### MRR\_TRX\_ISOLn\_COMP

Isolates voltage clamp output.

##### MRR\_TRX\_ENb\_COMP

Power gate signal for a comparator used in the voltage clamp.

##### MRR\_TRX\_EN\_DIV

Power gate signal for divider used in the voltage clamp

##### MRR\_TRX\_RC\_CNT

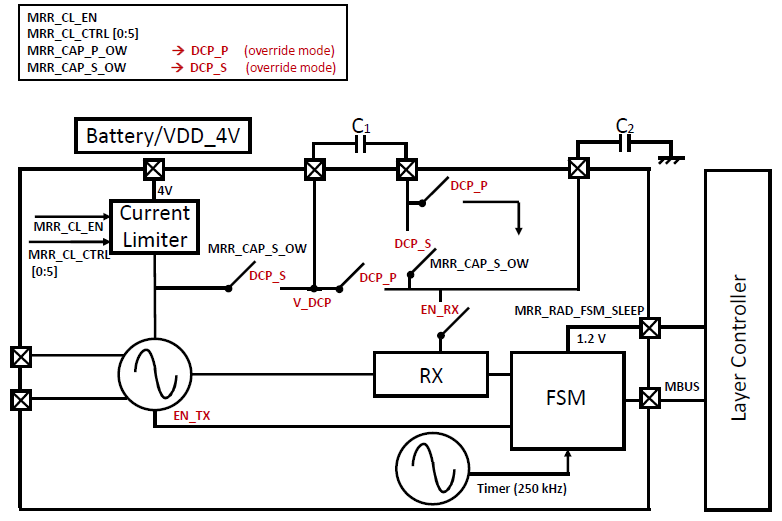
Represents number of successful recharge event. Count per pulse is binary, i.e. either 0 (VRAD did not reach target voltage) or 1 (VRAD reached target voltage and clamped). When MRR\_TRX\_SEL\_VCLAMP is set too high, count value will be 0 while when it is set too low, count will be same as number of pulses in the packet. Therefore, ideal MRR\_TRX\_SEL\_VCLAMP can be found by decreasing its value from maximum while monitoring the count. As MRR\_TRX\_SEL\_VCLAMP decrease, MRR\_TRX\_RC\_CNT will start to increase and then saturate. MRR\_TRX\_SEL\_VCLAMP value at that knee corresponds to an ideal value.

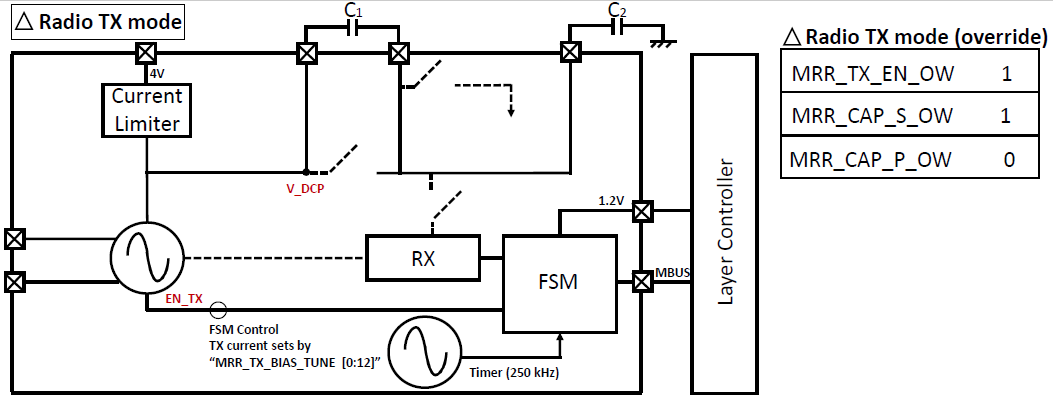
##### MRR\_TRX\_RC\_IRQ\_REPLY\_PACKET

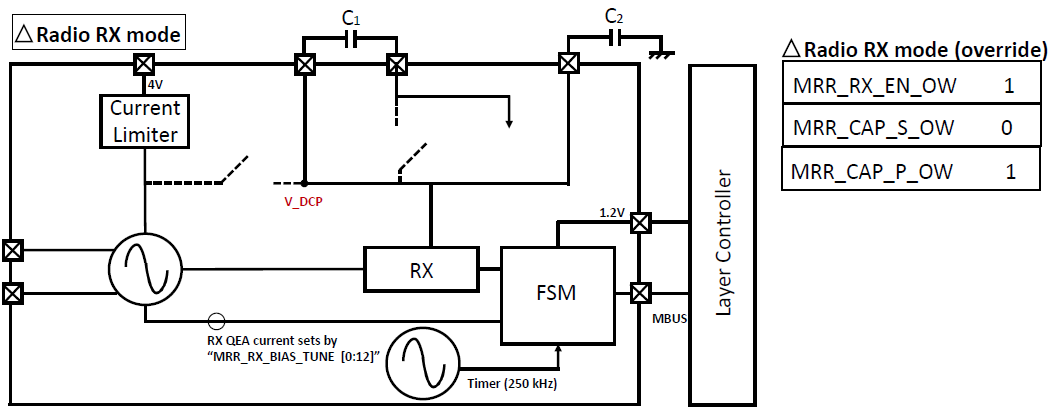
FIX ME

# TRX Radio

This is a TRX Radio designed by Li-Xuan Chuo. Figure IV‑i shows the block diagram of the TRX front-end of MRR. The transmitter and receiver are co-designed with the loop antenna. The carrier frequency is set by the antenna impedance and off-chip/on-chip capacitor.







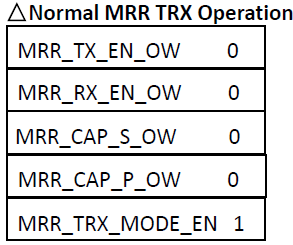


Figure IV‑i TRX Radio front-end of MRR

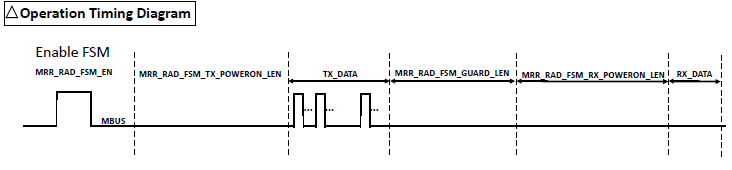


Figure IV-ii MRR Packet Timing Register Controls

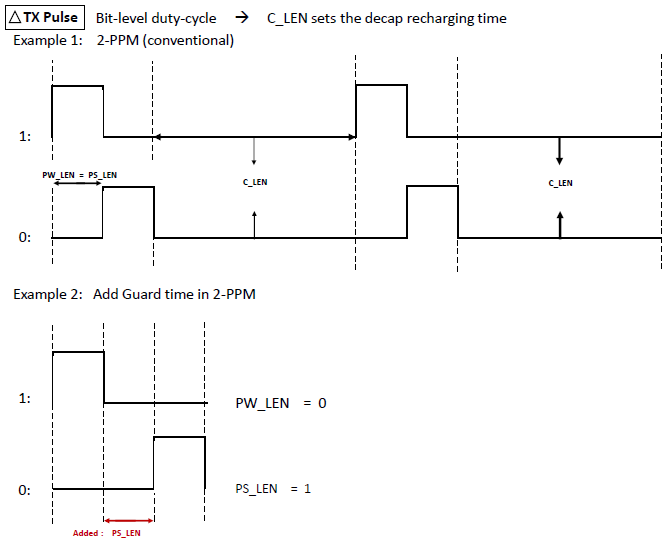


Figure IV-iii MRR TX Pulse Configuration

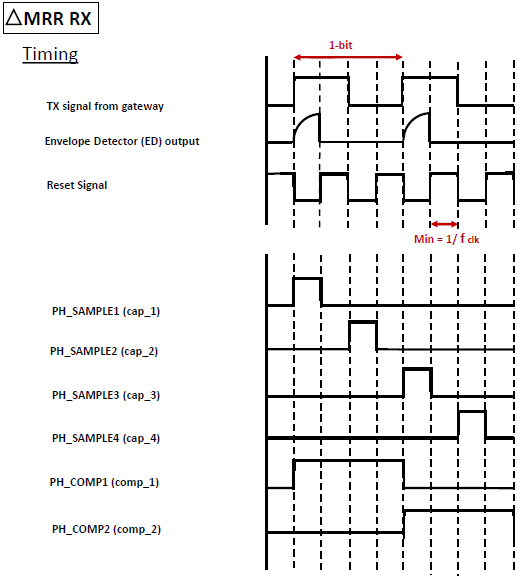


Figure IV-iv MRR RX Timing

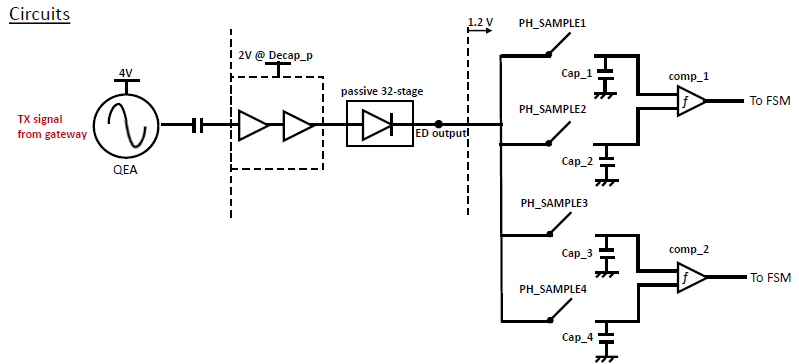


Figure IV-v MRR RX Sampling Circuits Details

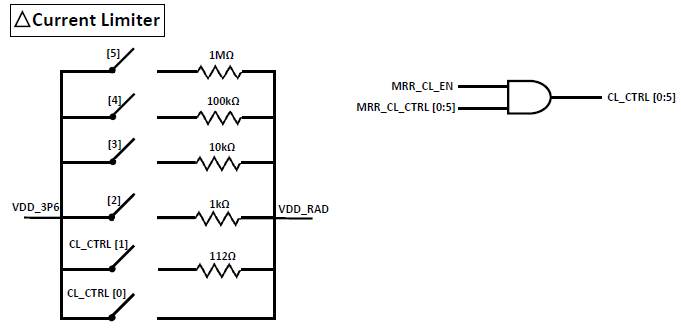


Figure IV-vi MRR Current Limiter

## Power Domains

The radio portion mainly works out of off-chip decaps. Those decaps need to be recharged periodically by a 4V-battery (through current limiter) or by PMU VDD\_3P6. The radio is at 4V in TX mode and at 2V in RX mode. The radio block has a switching structure to generate 2V from decaps. It is always TX first then RX. The FSM portion works at 1.2V which is generated by PMU.

## Interrupt Considerations

TRX radio will send out an interrupt signal when it finishes the received operation, followed by the demodulated signal.

## Power Draw / Current Draw / Energy Consumption

|  |  |  |
| --- | --- | --- |
| Mode | V3P6  (3.6V) | V1P2  (1.2V) |
| Active |  |  |
| Standby |  |  |

Table ‑ TEMP\_SENSOR Current Draw

## Operation

* **Initial TRX radio settings**
* Need to first setup the register correctly (TRX data bits, data rate, decap recharge time, etc.)
* Need to enable the current limiter
* Normal operation is to set the current limiter in a tiny current mode and trickle charge decaps (in series, by setting MRR\_CAP\_S\_OW = 1) in the beginning. Before starting the FSM, the MRR\_CAP\_S\_OW register should be set to 0.
* Decaps need to be periodically configured in parallel to equalize the floating node voltage.

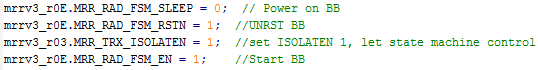
(MRR\_CAP\_P\_OW = 1, MRR\_CAP\_S\_OW = 0)

* **Q-Enhanced Amplifier (QEA) setting for the receiver**
* TRX RX uses a QEA as the front-end first stage RF amplifier, the bias current setting should base on the LC tank (antenna/cap) Q value. This is a one-time calibration value for the same system. Use MRR\_RX\_BIAS\_TUNE register to sweep the current from VBAT and monitor the envelope detector output to make sure the power oscillator does not oscillate (no DC shift at ED output). Usually the bias current value is 10’s of µA for a Q of 150-200 antenna.
* **FSM Start sequence**

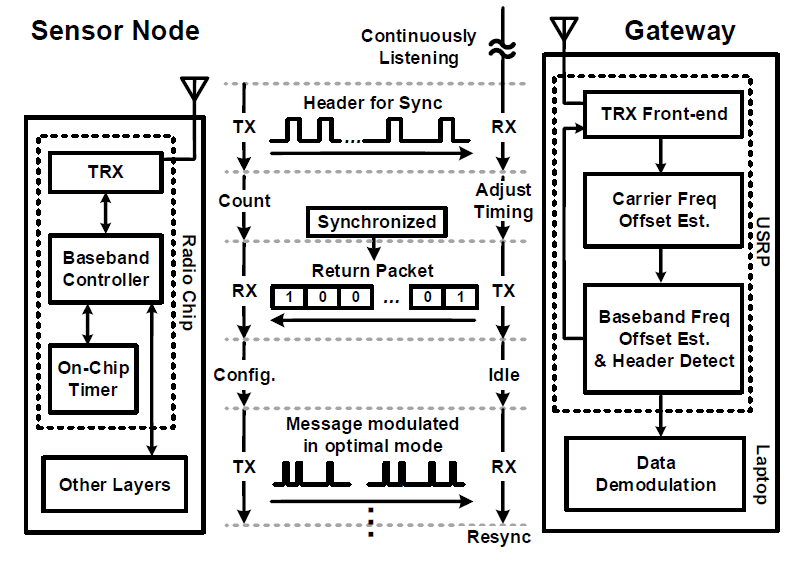
Before starting the FSM, make sure the on-chip timer already has a stable frequency. FSM will send out **ALL** the data in the TX\_DATA register specified by # of data to send in the configuration register.

* Power on the FSM
* Unreset the FSM
* Set ISOLATEN to high to give state machine control
* Enable the FSM

Following is the TX sequence in C code:



* **MRR TRX radio always does TX 🡪 RX (default operation)**
* Can be modified to TX only in setting MRR\_TRX\_MODE\_EN register
* **The RX power domain is 2V, which is coming from the internal DC-DC converter (DCP\_S, DCP\_P) and decaps**
* **The Full MRR TX 🡪 RX operation timing with the gateway can be found below.**



## Block Diagrams

1. Power Oscillator/Q-enhanced Amplifier  
   

Figure IV‑ii Power Oscillator block diagram

Power oscillator/ Q-enhanced Amplifier is based on a back-to-back inverter with tunable cap array on each node (ANTP and ANTN). Its current level is controlled by adjusting the footer configuration with MRR\_TX\_BIAS\_TUNE (for TX) or MRR\_RX\_BIAS\_TUNE (for RX). Tunable cap array are controlled with MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE, MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE, MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE, and MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE. Refer to Table VII‑1/Table VII‑2 for expected CFO frequency with different configurations. Note that switches in the cap array connect capacitor to VRAD when they are OFF. This provides high impedance connection to VRAD and prevents floating nodes which causes the settling issue.

1. Voltage Clamp



Figure IV‑iiiiii Voltage Clamp Block Diagram

Voltage clamp presets VRAD voltage before TX to prevent settling issue due to finite PMU strength. Voltage clamp has 2 modes, sleep and active mode. During sleep mode, voltage clamp uses divided V3P6 to charge/hold VRAD to a fixed voltage. To enable sleep mode, MRR\_TRX\_EN\_SLP\_VCLAMP should be set high and target voltage level can be controlled with MRR\_TRX\_SEL\_VCLAMP\_SLP (Detailed voltage level can be found in the register description). During active mode, voltage clamps controls current limiter (CL) to charge VRAD by turning it ON and clamps VRAD when it reaches target voltage by turning it off. To enable active mode, the clamp should be un-power gated (MRR\_TRX\_ENb\_COMP & MRR\_TRX\_EN\_DIV) and un-isolated (MRR\_TRX\_ISOLn\_COMP). Active mode voltage clamp level can be controlled by MRR\_TRX\_SEL\_VCLAMP. Note that active voltage clamp operation can either enabled or disabled during TX by controlling MRR\_TRX\_ENb\_CONT\_RC. Disabling active voltage clamp during TX is preferred as enabling CL introduces spike on VRAD which affects CFO. Active mode voltage clamp output (Recharge) can be monitored through MRR\_TRX\_RC\_CNT to figure out optimal MRR\_TRX\_SEL\_VCLAMP. Refer to register description of MRR\_TRX\_RC\_CNT for finding optimal MRR\_TRX\_SEL\_VCLAMP.

# On-chip Clock Generator

This is an on-chip clock generator designed by Seokhyeon Jeong. The clock generator has been mainly designed to be used as a TRX Radio FSM clock. It has been designed for -30°C to 130°C temperature range with 240kHz output frequency.

Figure V‑i shows the block diagram of the on-chip clock generator.



Figure V‑i Timer Block Diagram

## Power Domains

Clock genenerator has been designed to operate from a supply voltage ranging from 1.0V to 1.4V. It can choose to operate either from VDD\_1P2 generated from PMU for VDD\_LDO generated from LDO. See Section VI for details regarding the block itself. As LDO provides regulated output voltage, running off of LDO provides better supply sensitivity compared to PMU VDD\_1P2.

* VDD\_1P2 (from PMU)
* VDD\_LDO (from LDO)

## Power Draw / Current Draw / Energy Consumption

|  |  |
| --- | --- |
| Mode | V1P2  (1.2V) |
| Active | 1μA |
| Standby |  |

Table V‑1 On-chip Clock gen Current Draw

## Operation

* **Startup sequence** 
  + **Using PMU V1P2 as a power source**

1. Un-powergate clock gen

RO\_EN\_RO\_V1P2-> 1’h1

\*Include following step before step #1 if startup current is too high.

RO\_EN\_RO\_V1P2\_PRE **-**> 1’h1

1. Release isolation

RO\_ISOLATE\_CLK -> 1’h0

RO\_EN\_CLK -> 1’h1

1. Start Clock

RO\_RESET **-**> 1’h0

* + **Using LDO as a power source**

1. Un-powergate voltage reference in LDO. Voltage reference consumes only tens of pA so it requires some stabilization time (~30ms)  
   MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE -> 1’h1
2. Un-powergate the current reference and the main amplifier in LDO  
   MRR\_CL\_CTRL -> 1’h1  
   MRR\_CL\_EN -> 1’h1
3. Un-powergate clock gen

RO\_EN\_RO\_LDO-> 1’h1

1. Release isolation

RO\_ISOLATE\_CLK -> 1’h0

RO\_EN\_CLK -> 1’h1

1. Start Clock

RO\_RESET **-**> 1’h0

* **Temperature Coefficient (TC)**

Temperature coefficient of the output frequency can be tuned with following parameters. Refer to their description for usage.

RO\_POLY

RO\_PDIFF

* **Frequency Tuning**

Output frequency can be tuned by adjusting RO\_MIM or RO\_MOM. It is recommended to adjust them simultaneously (i.e. RO\_MOM=RO\_MIM) as they affect temperature coefficient. This will give 5kHz tuning step while tuning them individually will give 2.5kHz step. See Table VII‑3 for tuning range. Note that although RO\_POLY/ RO\_PDIFF can adjust frequency, it is not recommended as they will affect temperature coefficient.

# LDO

This is a Linear Regulator used to regulate VDD of On-chip clock generator, originally designed by Inhee Lee. See Figure VI‑i & Figure VI‑ii.

## Power Domains

* VDD\_3P6
* VDD\_1P2
* On-chip clock generator’s VDD

## Operation

* Select desired output voltage via LDO\_ SEL\_VOUT

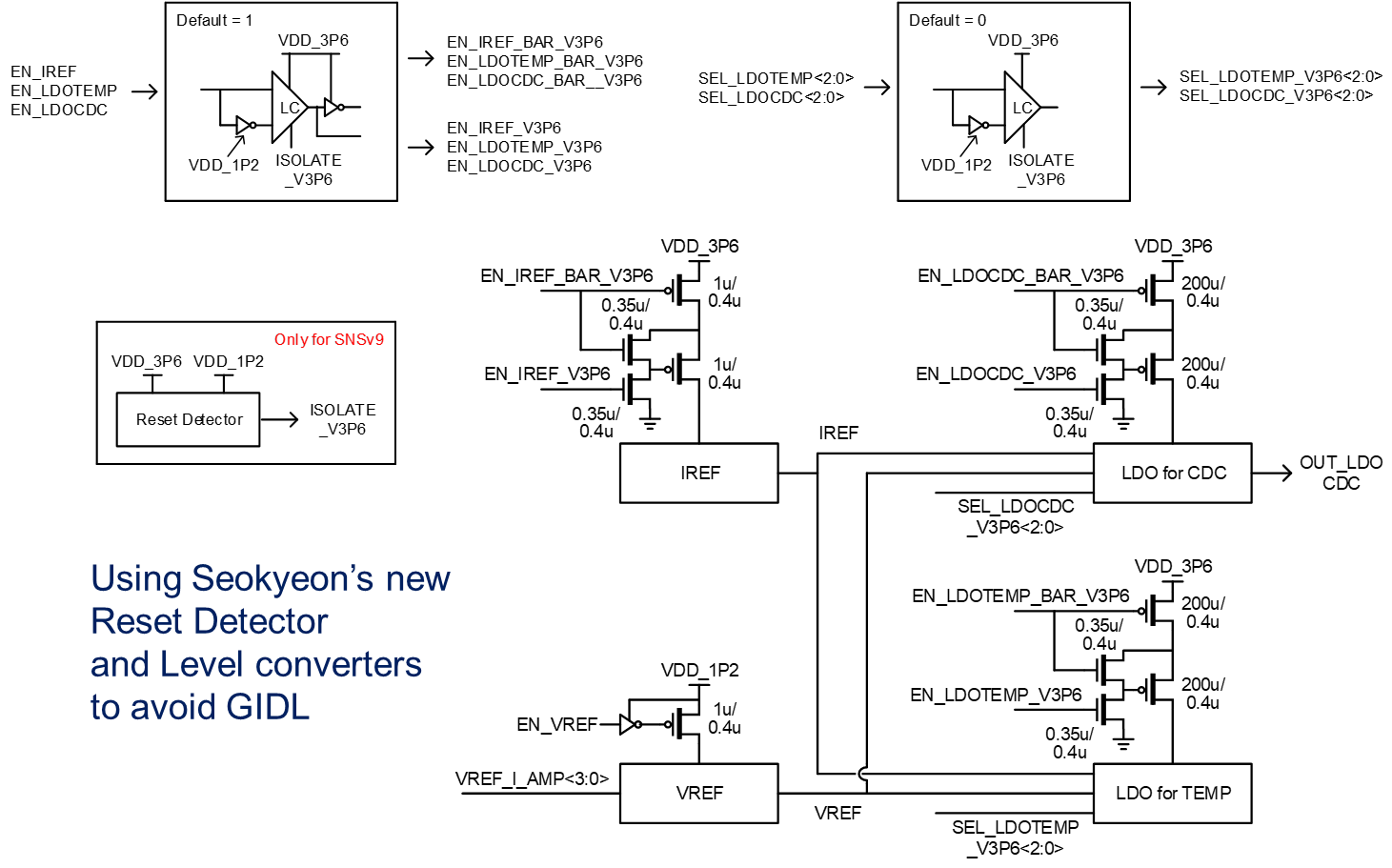


Figure ‑ LDO\_TOP Block Diagram

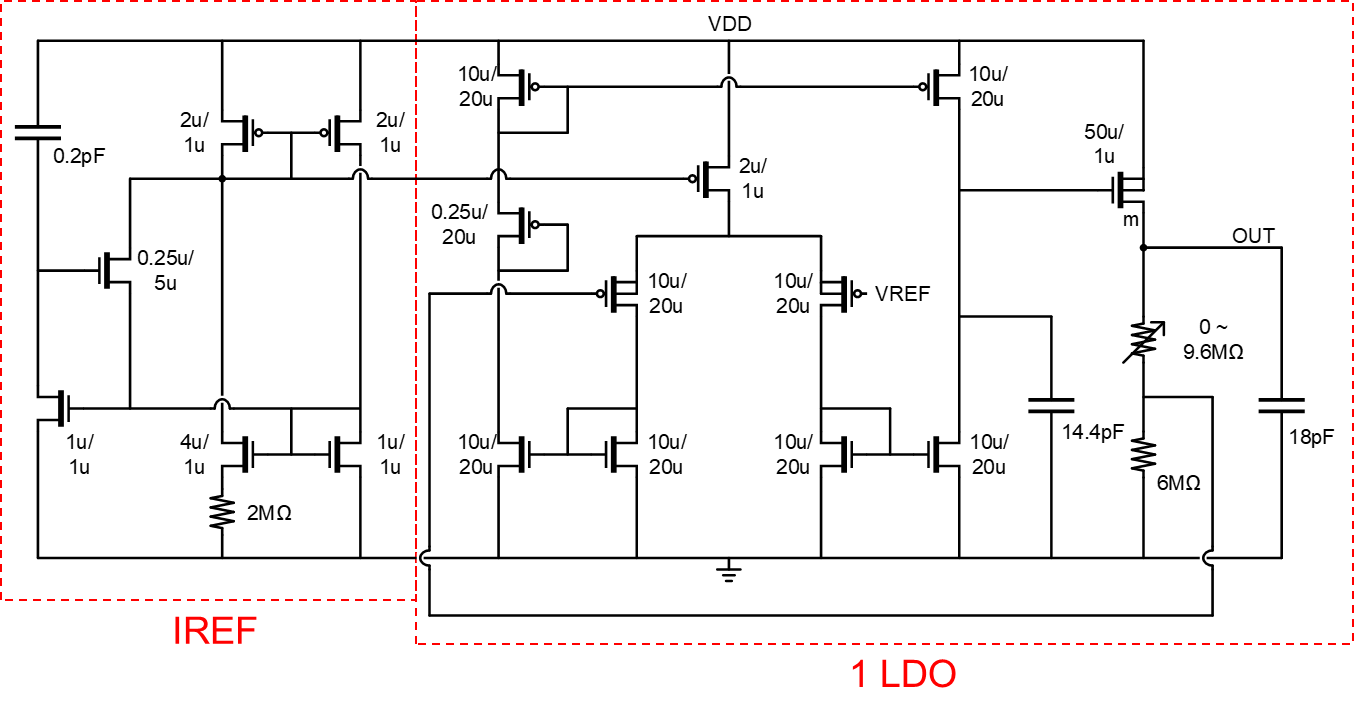
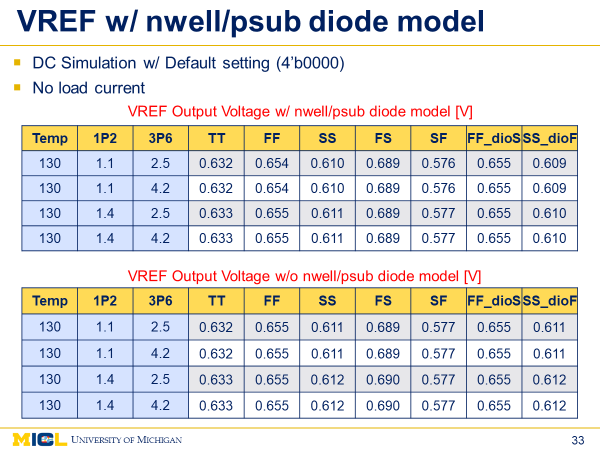
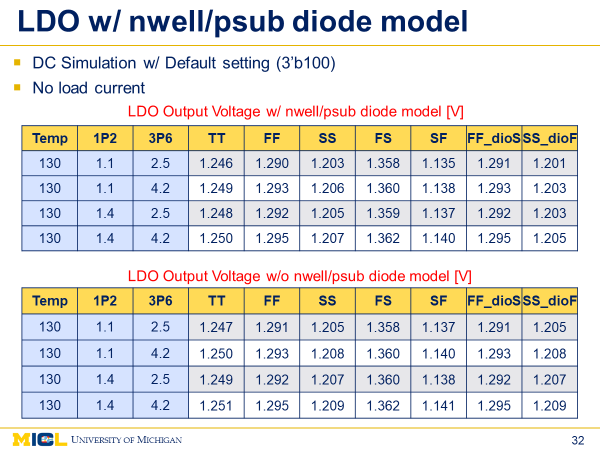
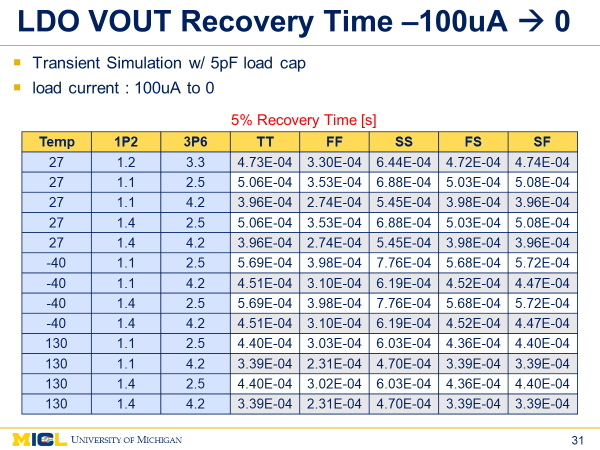
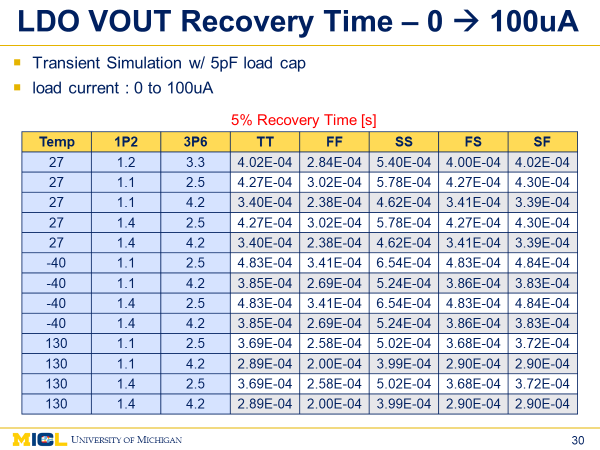
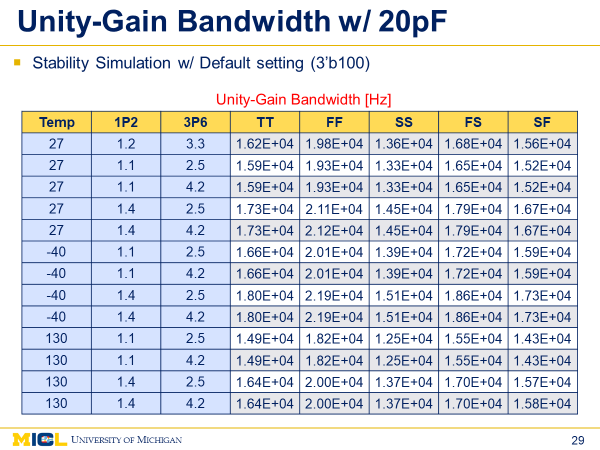
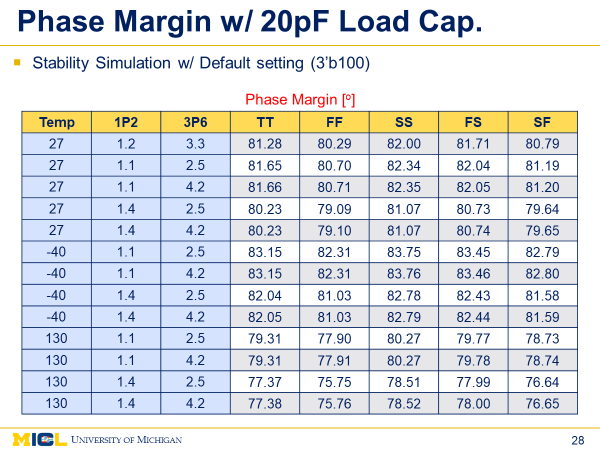
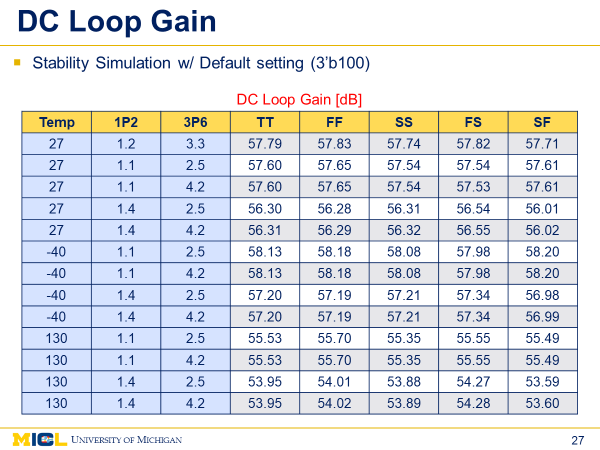
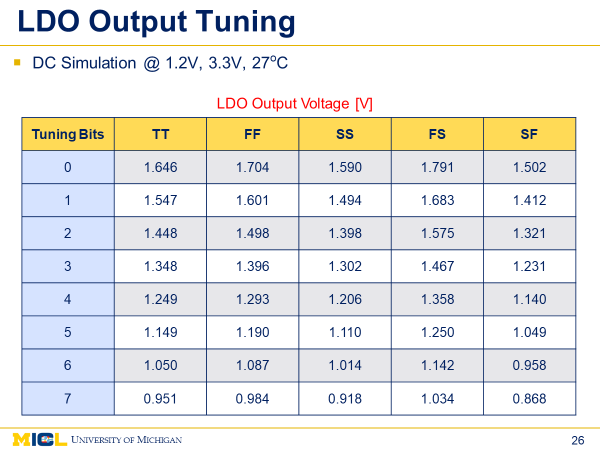
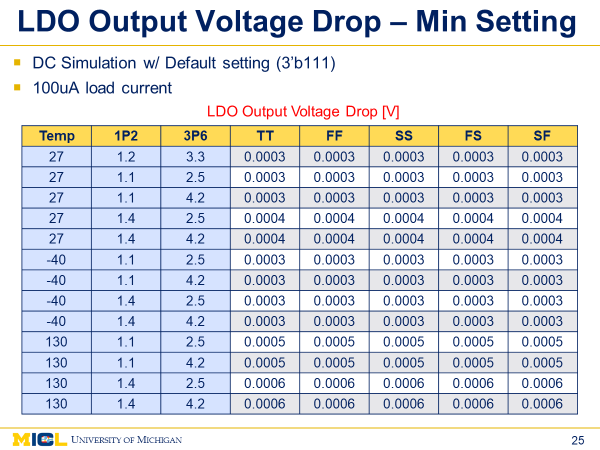
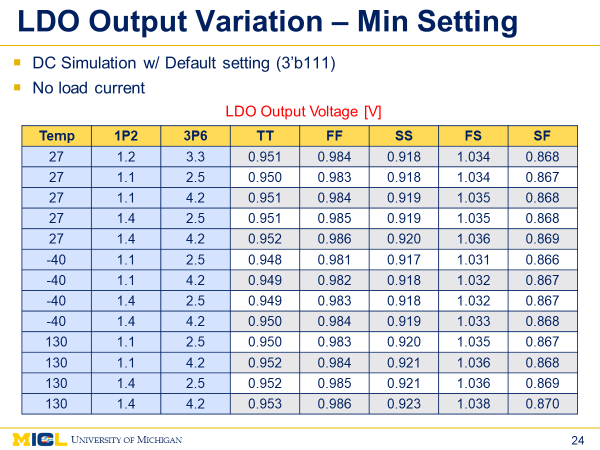
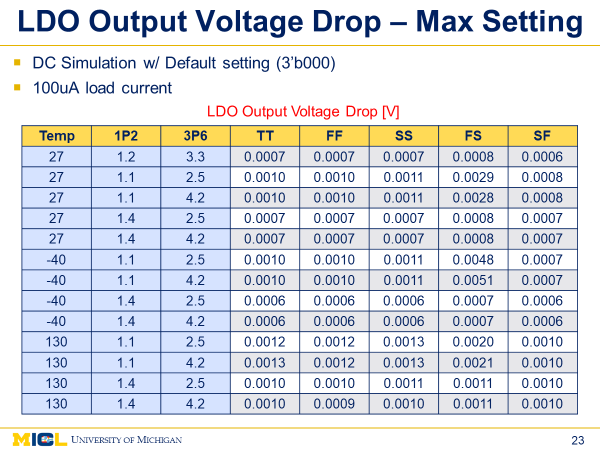
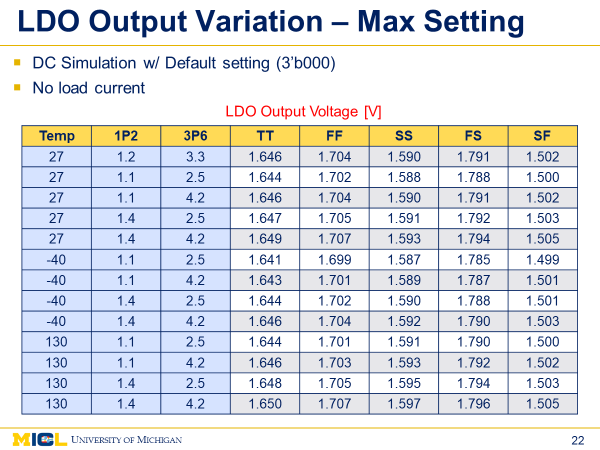
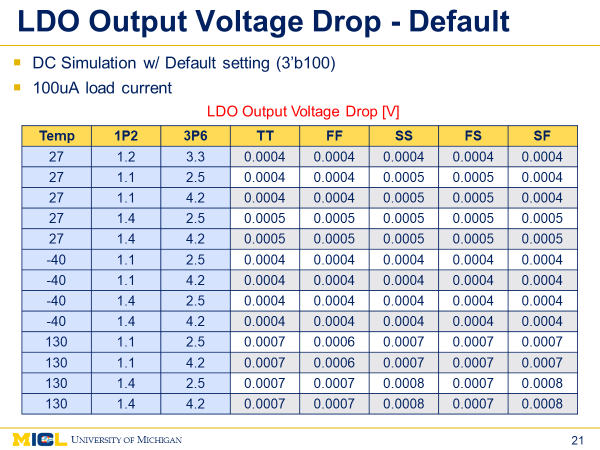
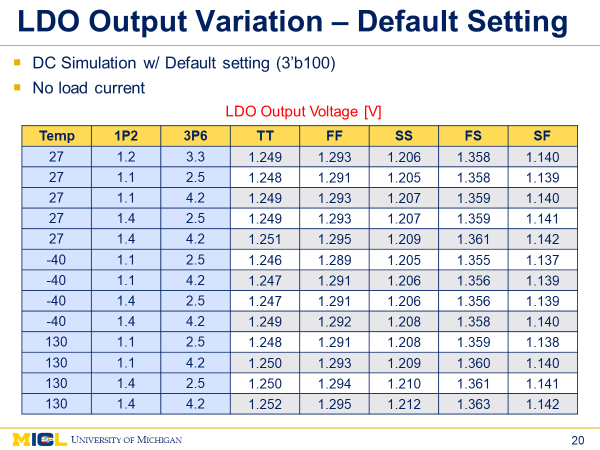
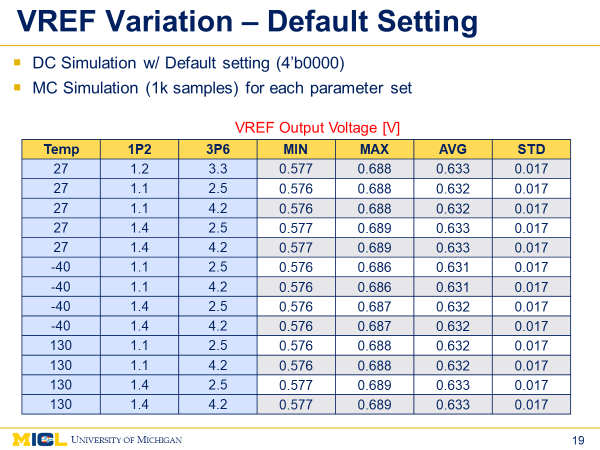
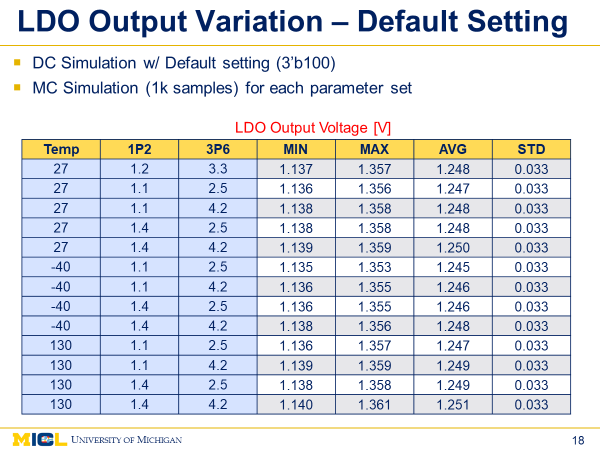
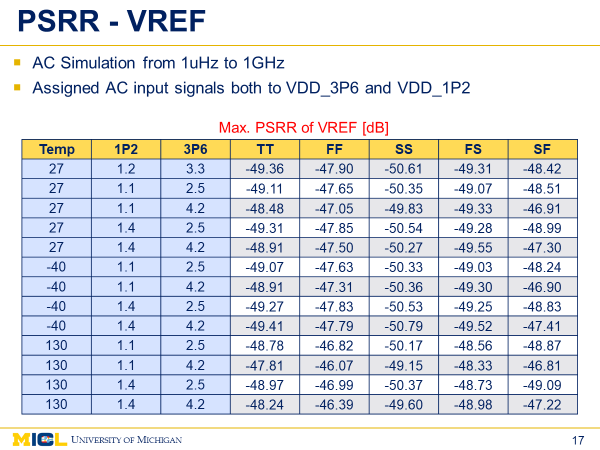
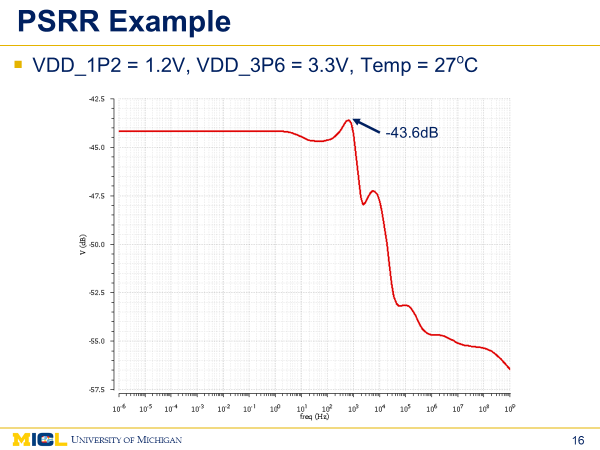
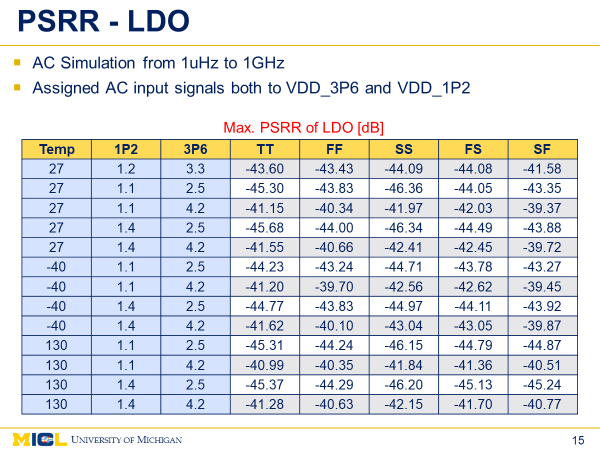
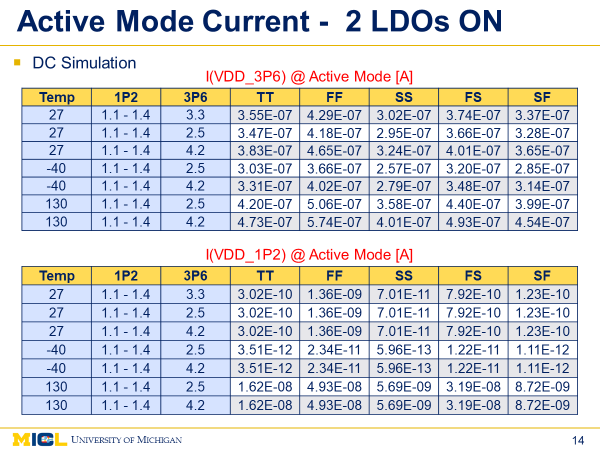
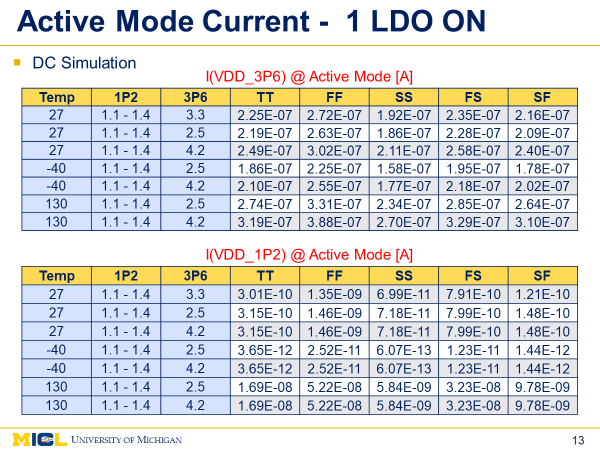
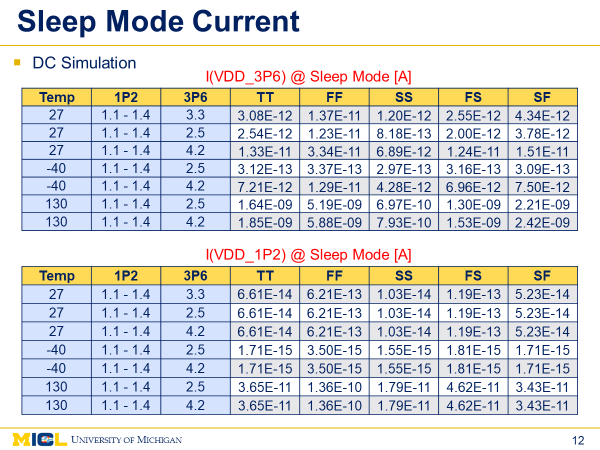
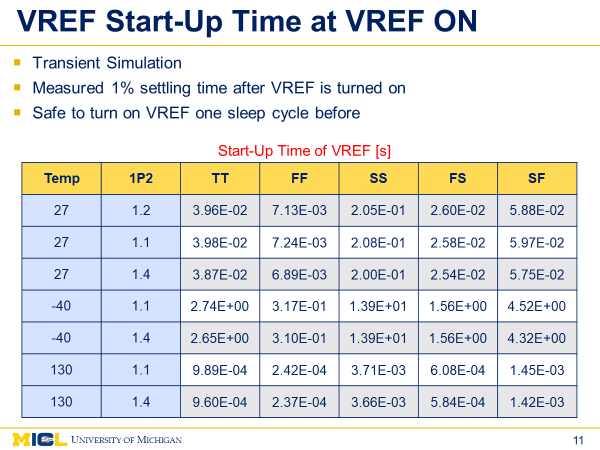
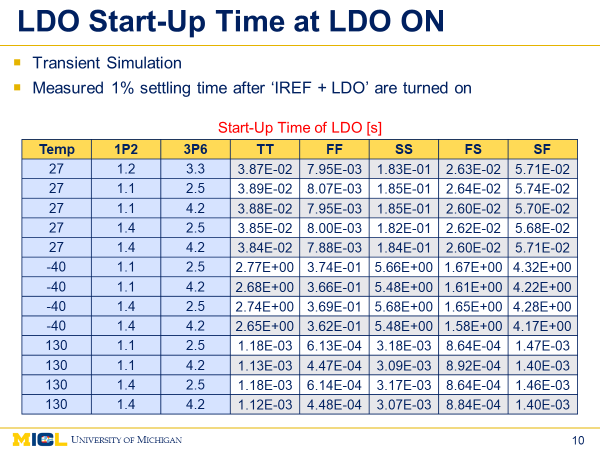
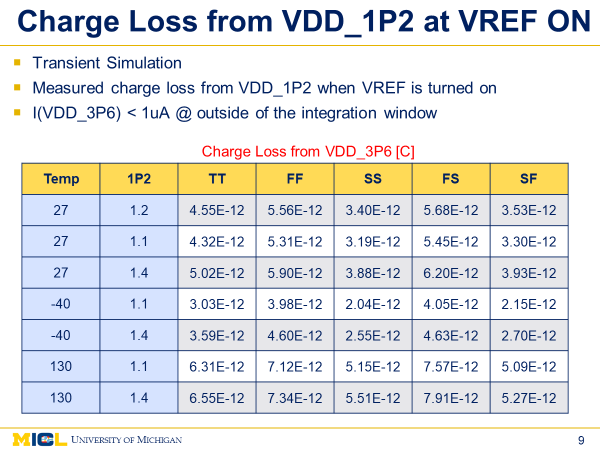
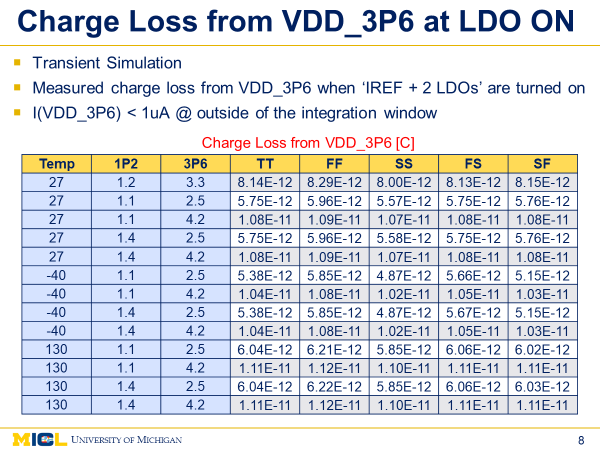
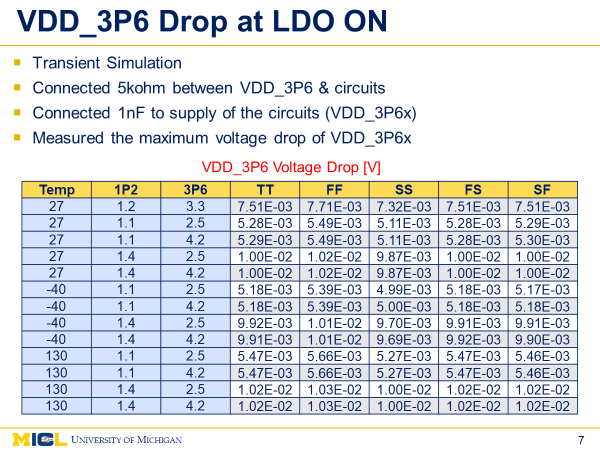


Figure ‑ IREF+1 LDO

## Post-PEX Simulation Results



## Measurement Results

# Appendix

## Power Oscillator Frequency Range

Following tables show simulated power oscillator frequency depending on different tuning values as well as the external antenna cap. Simulation includes parasitic extraction and uses extracted antenna model (AHv4.1\_rev1) from HFSS.

As mentioned before, frequency tuning can be done by adjusting MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE / MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE and MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE / MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE. In the table, coarse tuning values are shown in column and fine tuning values are shown in row.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Power Oscillator Frequency (MHz) | | | | | | | | | | |
| **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| 0 | 944.93 | 934.33 | 923.71 | 913.60 | 903.96 | 894.38 | 885.29 | 876.40 | 867.68 | 859.40 | 851.17 |
| 1 | 944.61 | 933.87 | 923.62 | 913.39 | 903.67 | 894.18 | 885.01 | 876.07 | 867.55 | 859.18 | 850.46 |
| 2 | 944.34 | 933.53 | 923.08 | 912.93 | 903.32 | 893.78 | 884.64 | 875.71 | 867.27 | 858.83 | 850.70 |
| 3 | 944.14 | 933.46 | 923.10 | 912.72 | 903.10 | 893.65 | 884.50 | 875.74 | 867.09 | 858.57 | 850.47 |
| 4 | 943.23 | 932.50 | 922.08 | 912.10 | 902.42 | 892.88 | 883.83 | 875.08 | 866.46 | 858.07 | 849.94 |
| 5 | 942.89 | 932.17 | 921.83 | 911.93 | 902.19 | 892.76 | 883.60 | 874.70 | 866.17 | 857.78 | 849.76 |
| 6 | 942.53 | 932.01 | 921.64 | 911.57 | 901.93 | 892.53 | 883.32 | 874.38 | 866.04 | 857.61 | 849.50 |
| 7 | 942.19 | 931.64 | 921.26 | 911.19 | 901.57 | 892.14 | 883.27 | 874.18 | 865.61 | 857.30 | 849.55 |
| 8 | 941.26 | 930.57 | 920.23 | 910.36 | 900.58 | 891.23 | 882.21 | 873.44 | 864.79 | 856.57 | 848.45 |
| 9 | 940.97 | 930.35 | 920.21 | 910.10 | 900.33 | 890.98 | 882.03 | 873.14 | 864.52 | 856.38 | 848.29 |
| 10 | 940.53 | 929.91 | 919.61 | 909.56 | 900.03 | 890.59 | 881.61 | 872.82 | 864.30 | 856.02 | 847.93 |
| 11 | 940.24 | 929.65 | 919.48 | 909.50 | 899.73 | 890.45 | 881.36 | 872.53 | 864.04 | 855.81 | 847.84 |
| 12 | 939.45 | 929.08 | 918.71 | 908.79 | 899.18 | 889.77 | 880.84 | 871.95 | 863.66 | 855.15 | 847.18 |
| 13 | 939.17 | 928.61 | 918.41 | 908.53 | 898.87 | 889.53 | 880.65 | 871.81 | 863.35 | 855.02 | 847.08 |
| 14 | 938.73 | 928.22 | 918.01 | 908.07 | 898.45 | 889.14 | 880.24 | 871.38 | 862.99 | 854.84 | 846.84 |
| 15 | 938.56 | 928.15 | 919.15 | 907.90 | 898.30 | 889.21 | 880.00 | 871.33 | - | 854.72 | 846.51 |
| 16 | 937.10 | 926.58 | 916.39 | 906.54 | 896.89 | 887.75 | 878.76 | 870.08 | 861.56 | 853.47 | 845.50 |
| 17 | 936.81 | 926.50 | 916.10 | 906.25 | 896.82 | 887.48 | 878.45 | 869.77 | 861.41 | 853.24 | 845.28 |
| 18 | 936.55 | 925.93 | 915.83 | 905.93 | 896.33 | 887.26 | 878.23 | 869.63 | 861.16 | 852.94 | 844.98 |
| 19 | 936.06 | 925.58 | 915.52 | 905.60 | 896.11 | 886.95 | 877.98 | 869.24 | - | 852.67 | 844.80 |
| 20 | 935.36 | 924.85 | 914.81 | 904.92 | 895.41 | 886.32 | 877.31 | 868.64 | 860.35 | 852.16 | 844.19 |
| 21 | 935.22 | 924.86 | 914.59 | 904.71 | 895.23 | 886.01 | - | 868.53 | 860.12 | 851.93 | 844.09 |
| 22 | 934.80 | 924.29 | 914.14 | 904.38 | 894.88 | 885.66 | 876.74 | 868.13 | 859.75 | 851.69 | 843.73 |
| 23 | 934.38 | 924.19 | 913.94 | 904.16 | 894.65 | 885.52 | 876.64 | - | 859.51 | 851.40 | 843.70 |
| 24 | 933.77 | 923.23 | 913.39 | 903.26 | 893.99 | 884.84 | 875.94 | 867.28 | 858.79 | 850.80 | 843.05 |
| 25 | 933.39 | 922.96 | 912.81 | 903.13 | 893.86 | 884.54 | 875.70 | 867.09 | 858.74 | 850.57 | 842.71 |
| 26 | 932.93 | 922.63 | 912.57 | 902.74 | 893.34 | 884.20 | 875.24 | 866.75 | 858.35 | 850.21 | 842.37 |
| 27 | 932.65 | 922.29 | 912.30 | 902.45 | 893.20 | - | 875.05 | 866.55 | 858.12 | 850.11 | 842.18 |
| 28 | 931.98 | 921.61 | 911.66 | 901.88 | 892.47 | 883.28 | 874.50 | 865.86 | 857.49 | 849.49 | 841.68 |
| 29 | 931.65 | 943.80 | 911.31 | 901.62 | 892.17 | 883.12 | 874.25 | 865.68 | 857.36 | 849.30 | 841.43 |
| 30 | 931.38 | 921.04 | 910.87 | 901.23 | 891.95 | 882.85 | 873.69 | 865.45 | 857.04 | 849.23 | 841.16 |
| 31 | 930.98 | 920.72 | 910.66 | - | 891.61 | 882.59 | 873.70 | - | 856.80 | 848.79 | 841.07 |
| 32 | 929.93 | 919.62 | 943.86 | 900.03 | 890.68 | 881.64 | 872.83 | 864.32 | 856.02 | 847.96 | 840.17 |
| 33 | 929.68 | 919.43 | 909.57 | 899.80 | 890.50 | 881.80 | - | 864.09 | 855.87 | 847.85 | 840.04 |
| 34 | 929.37 | 919.02 | 909.09 | 899.39 | 890.11 | 881.17 | 872.29 | 863.79 | 855.59 | 847.52 | 839.68 |
| 35 | 929.22 | 918.78 | 908.79 | 899.19 | 889.97 | 880.82 | 872.08 | 863.57 | 855.34 | 847.35 | 839.54 |
| 36 | 928.30 | 918.03 | 908.19 | 898.49 | 889.22 | 880.26 | 871.51 | 863.03 | 854.73 | 846.81 | 838.95 |
| 37 | 927.98 | 917.76 | 907.93 | 898.36 | 889.10 | 880.11 | 871.42 | 862.81 | 854.60 | 846.53 | 838.79 |
| 38 | 927.68 | 917.42 | 907.50 | 897.92 | 888.70 | 879.70 | 870.95 | 862.60 | 854.25 | 846.21 | 838.54 |
| 39 | 927.42 | 917.14 | - | - | 888.48 | 879.53 | 870.75 | 862.26 | 854.15 | 846.09 | 838.34 |
| 40 | 926.51 | 916.33 | 906.43 | 896.97 | 887.63 | 878.71 | 870.05 | 861.61 | 853.49 | 845.40 | 837.72 |
| 41 | 926.30 | 916.12 | 906.25 | 896.74 | 887.44 | 878.57 | 869.95 | - | 853.22 | 845.22 | 837.55 |
| 42 | 925.88 | 915.81 | 905.90 | 896.41 | 887.15 | 878.16 | 869.51 | 861.04 | 852.80 | 844.97 | 837.29 |
| 43 | 925.69 | 915.54 | 905.69 | 896.10 | 886.88 | 877.98 | 869.25 | 860.85 | 852.63 | 945.12 | 837.04 |
| 44 | 925.07 | 914.89 | 904.99 | 895.54 | 886.21 | 877.38 | 868.63 | 860.25 | 852.06 | 844.28 | 836.47 |
| 45 | 924.73 | 914.54 | 904.69 | 895.23 | 886.14 | 877.15 | 868.41 | 860.08 | - | 843.98 | 836.26 |
| 46 | 924.29 | 914.12 | 904.40 | 894.99 | 885.77 | 876.83 | 868.09 | 859.74 | 851.59 | 843.77 | 835.96 |
| 47 | 924.14 | 913.96 | 904.12 | 894.75 | 885.54 | 876.62 | 867.92 | - | 851.41 | - | 835.86 |

Table VII‑1 Simulated CFO (MHz) with 700fF ANT cap (after PEX) with different MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE / MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE (column) and MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE/MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE (row) configurations

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Power Oscillator Frequency (MHz) | | | | | | | | | | |
| **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| 0 | 913.25 | 903.38 | 894.06 | 884.81 | 876.00 | 867.36 | 858.97 | 850.80 | 842.88 | 835.32 | 827.78 |
| 1 | 912.95 | 903.17 | 893.81 | 884.65 | 875.79 | 867.12 | 858.93 | 850.68 | 842.81 | 835.05 | 827.01 |
| 2 | 912.52 | 902.77 | 893.46 | 884.20 | 875.42 | 866.76 | 858.45 | 850.32 | 842.40 | 834.77 | 827.36 |
| 3 | 912.41 | 902.53 | 893.39 | 883.99 | 875.24 | 866.77 | 858.33 | 850.26 | 842.31 | 834.60 | 827.10 |
| 4 | 911.58 | 901.95 | 892.57 | 883.45 | 874.66 | 865.95 | 857.66 | 849.54 | 841.71 | 834.02 | 826.59 |
| 5 | 911.41 | 901.65 | 892.30 | 883.23 | 874.43 | 865.82 | 857.51 | 849.38 | 841.54 | 833.85 | 826.40 |
| 6 | 910.93 | 901.40 | 892.04 | 883.04 | 874.23 | 865.61 | 857.31 | 849.12 | 841.31 | 833.69 | 826.15 |
| 7 | 910.75 | 901.11 | 891.90 | 882.68 | 873.89 | 865.31 | 857.05 | 848.87 | 841.00 | 833.42 | 826.25 |
| 8 | 909.80 | 900.18 | 890.84 | 881.78 | 872.99 | 864.40 | 856.13 | 848.06 | 840.30 | 832.70 | 825.27 |
| 9 | 909.51 | 900.11 | 890.79 | 881.61 | 872.71 | 864.23 | 856.07 | 847.89 | 840.03 | 832.63 | 825.06 |
| 10 | 909.18 | 899.55 | 890.35 | 881.14 | 872.45 | 863.92 | 855.63 | 847.60 | 839.75 | 832.22 | 824.81 |
| 11 | 909.02 | 899.38 | 890.15 | 881.07 | 872.17 | 863.70 | 855.50 | 847.57 | 839.58 | 832.05 | 824.62 |
| 12 | 908.21 | 898.82 | 889.41 | 880.39 | 871.80 | 863.12 | 855.02 | 846.86 | 839.17 | 831.45 | 824.08 |
| 13 | 908.07 | 898.37 | 889.16 | 880.11 | 871.43 | 862.86 | 854.70 | 846.68 | 838.91 | 831.33 | 823.92 |
| 14 | 907.69 | 898.17 | 888.82 | 879.76 | 871.08 | 862.54 | 854.37 | 846.41 | 838.62 | 831.01 | 823.78 |
| 15 | 907.52 | 897.86 | 889.81 | 879.66 | 870.87 | 862.57 | 854.20 | 846.33 | - | 831.06 | 823.46 |
| 16 | 906.04 | 896.54 | 887.27 | 878.37 | 869.60 | 861.17 | 852.99 | 845.15 | 837.34 | 829.81 | 822.47 |
| 17 | 905.88 | 896.47 | 887.08 | 878.12 | 869.45 | 861.01 | 852.86 | 844.84 | 837.09 | 829.58 | 822.29 |
| 18 | 905.54 | 895.98 | 886.82 | 877.85 | 869.06 | 860.86 | 852.65 | 844.74 | 836.87 | 829.39 | 822.05 |
| 19 | 905.20 | 895.69 | 886.46 | 877.52 | 868.91 | 860.54 | 852.39 | 844.37 | 912.66 | 829.18 | 821.81 |
| 20 | 904.56 | 895.09 | 885.89 | 876.95 | 868.28 | 859.92 | 851.82 | 843.83 | 836.08 | 828.58 | 821.32 |
| 21 | 904.32 | 894.90 | 885.65 | 876.73 | 868.07 | 859.67 | - | 843.70 | 835.92 | 828.54 | 821.26 |
| 22 | 903.95 | 894.52 | 885.26 | 876.35 | 867.82 | 859.38 | 851.27 | 843.40 | 835.62 | 828.23 | 820.91 |
| 23 | 903.77 | 894.41 | 885.07 | 876.16 | 867.57 | 859.20 | 851.06 | - | 835.44 | 827.96 | 820.75 |
| 24 | 902.96 | 893.45 | 884.29 | 875.47 | 866.89 | 858.64 | 850.48 | 842.54 | 834.98 | 827.49 | 820.24 |
| 25 | 902.71 | 893.24 | 884.09 | 875.27 | 866.80 | 858.43 | 850.19 | 842.29 | 834.63 | 827.16 | 819.95 |
| 26 | 902.36 | 893.01 | 883.79 | 874.93 | 866.37 | 857.96 | 849.84 | 841.99 | 834.41 | 826.93 | 819.67 |
| 27 | 902.11 | 892.63 | 883.64 | 874.71 | 866.22 | 912.74 | 849.65 | 841.85 | 834.17 | 826.88 | 819.49 |
| 28 | 901.37 | 892.10 | 882.97 | 874.04 | 865.59 | 857.25 | 849.08 | 841.23 | 833.62 | 826.24 | 818.95 |
| 29 | 901.24 | 912.23 | 882.69 | 873.84 | 865.34 | 857.07 | 848.94 | 841.05 | 833.49 | 826.06 | 818.83 |
| 30 | 900.96 | 891.66 | 882.37 | 873.52 | 865.04 | 856.86 | 848.33 | 840.82 | 833.20 | 825.90 | 818.53 |
| 31 | 900.65 | 891.28 | 882.21 | - | 864.78 | 856.53 | 848.42 | 912.51 | 832.99 | 825.54 | 818.35 |
| 32 | 899.77 | 890.24 | - | 872.41 | 863.92 | 855.68 | 847.61 | 839.79 | 832.20 | 824.90 | 817.68 |
| 33 | 899.38 | 890.06 | 881.11 | 872.33 | 863.74 | 855.78 | 912.76 | 839.61 | 832.09 | 824.65 | 817.46 |
| 34 | 899.17 | 889.80 | 880.70 | 871.88 | 863.48 | 855.18 | 847.20 | 839.30 | 831.80 | 824.35 | 817.22 |
| 35 | 898.85 | 889.52 | 880.43 | 871.71 | 863.25 | 854.94 | 846.98 | 839.12 | 831.59 | 824.25 | 817.05 |
| 36 | 898.21 | 888.89 | 879.82 | 871.12 | 862.64 | 854.48 | 846.38 | 838.63 | 831.05 | 823.68 | 816.53 |
| 37 | 897.91 | 888.62 | 879.58 | 870.97 | 862.48 | 854.35 | 846.17 | 838.44 | 830.85 | 823.50 | 816.37 |
| 38 | 897.52 | 888.25 | 879.33 | 870.55 | 862.12 | 853.90 | 845.89 | 838.13 | 830.65 | 823.31 | 816.16 |
| 39 | 897.39 | 888.08 | - | 870.33 | 861.93 | 853.77 | 845.68 | 837.96 | 830.40 | 823.02 | 815.94 |
| 40 | 896.48 | 887.30 | 878.34 | 869.70 | 861.18 | 852.99 | 845.10 | 837.29 | 829.75 | 822.49 | 815.30 |
| 41 | 896.44 | 887.06 | 878.14 | 869.42 | 861.00 | 852.87 | 844.90 | - | 829.60 | 822.36 | 815.14 |
| 42 | 896.01 | 886.70 | 877.83 | 869.17 | 860.68 | 852.57 | 844.54 | 836.78 | 829.27 | 822.03 | 814.88 |
| 43 | 895.75 | 886.55 | 877.59 | 868.87 | 860.52 | 852.34 | 844.32 | 836.67 | 829.13 | - | 814.74 |
| 44 | 895.21 | 885.96 | 876.96 | 868.34 | 859.93 | 851.79 | 843.82 | 836.12 | 828.61 | 821.30 | 814.21 |
| 45 | 894.80 | 885.66 | 876.73 | 868.06 | 859.77 | 851.50 | 843.72 | 835.91 | - | 821.13 | 814.09 |
| 46 | 894.45 | 885.33 | 876.38 | 867.82 | 859.48 | 851.25 | 843.39 | 835.63 | 828.19 | 820.87 | 813.74 |
| 47 | 894.35 | 885.05 | 876.18 | 867.61 | 859.37 | 851.02 | 843.14 | - | 827.92 | - | 813.61 |

Table VII‑2 Simulated CFO (MHz) with 800fF ANT cap (after PEX) with different MRR\_TRX\_CAP\_ANTP\_TUNE\_COARSE / MRR\_TRX\_CAP\_ANTN\_TUNE\_COARSE (column) and MRR\_TRX\_CAP\_ANTP\_TUNE\_FINE/MRR\_TRX\_CAP\_ANTN\_TUNE\_FINE (row) configurations

## On-Chip Clock Generator Frequency Range

Following tables show simulated on-chip clock generator frequency depending on different tuning values (RO\_MIM and RO\_MOM). Simulation includes parasitic extraction.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| RO\_MIM  /RO\_MOM | Clock Freq.(kHz) | RO\_MIM  /RO\_MOM | Clock Freq.(kHz) | RO\_MIM  /RO\_MOM | Clock Freq.(kHz) | RO\_MIM  /RO\_MOM | Clock Freq.(kHz) |
| 0 | 339.2 | **32** | 276.6 | **64** | 233.8 | **96** | 202.5 |
| 1 | 334.6 | **33** | 273.6 | **65** | 231.7 | **97** | 200.9 |
| 2 | 329.3 | **34** | 270.0 | **66** | 229.1 | **98** | 198.9 |
| 3 | 325.9 | **35** | 267.8 | **67** | 227.5 | **99** | 197.7 |
| 4 | 321.0 | **36** | 264.4 | **68** | 225.1 | **100** | 195.9 |
| 5 | 316.9 | **37** | 261.7 | **69** | 223.1 | **101** | 194.4 |
| 6 | 312.9 | **38** | 259.0 | **70** | 221.1 | **102** | 192.9 |
| 7 | 309.9 | **39** | 256.9 | **71** | 219.6 | **103** | 191.8 |
| 8 | 304.8 | **40** | 253.4 | **72** | 217.0 | **104** | 189.8 |
| 9 | 301.1 | **41** | 250.8 | **73** | 215.1 | **105** | 188.3 |
| 10 | 296.8 | **42** | 247.8 | **74** | 213.0 | **106** | 186.7 |
| 11 | 294.1 | **43** | 246.0 | **75** | 211.6 | **107** | 185.6 |
| 12 | 290.1 | **44** | 243.2 | **76** | 209.5 | **108** | 184.0 |
| 13 | 286.8 | **45** | 240.9 | **77** | 207.8 | **109** | 182.7 |
| 14 | 283.6 | **46** | 238.6 | **78** | 206.1 | **110** | 181.4 |
| 15 | 281.1 | **47** | 236.9 | **79** | 204.8 | **111** | 180.4 |
| 16 | 276.6 | **48** | 233.8 | **80** | 202.4 | **112** | 178.6 |
| 17 | 273.6 | **49** | 231.6 | **81** | 200.8 | **113** | 177.3 |
| 18 | 270.0 | **50** | 229.0 | **82** | 198.9 | **114** | 175.8 |
| 19 | 267.8 | **51** | 227.4 | **83** | 197.6 | **115** | 174.9 |
| 20 | 264.4 | **52** | 225.0 | **84** | 195.8 | **116** | 173.4 |
| 21 | 261.7 | **53** | 223.0 | **85** | 194.3 | **117** | 172.3 |
| 22 | 259.0 | **54** | 221.0 | **86** | 192.8 | **118** | 171.1 |
| 23 | 256.9 | **55** | 219.6 | **87** | 191.7 | **119** | 170.2 |
| 24 | 253.5 | **56** | 217.1 | **88** | 189.8 | **120** | 168.7 |
| 25 | 250.9 | **57** | 215.2 | **89** | 188.4 | **121** | 167.6 |
| 26 | 248.0 | **58** | 213.0 | **90** | 186.7 | **122** | 166.2 |
| 27 | 246.1 | **59** | 211.6 | **91** | 185.6 | **123** | 165.4 |
| 28 | 243.3 | **60** | 209.5 | **92** | 184.0 | **124** | 164.1 |
| 29 | 241.0 | **61** | 207.8 | **93** | 182.7 | **125** | 163.1 |
| 30 | 238.7 | **62** | 206.1 | **94** | 181.4 | **126** | 162.0 |
| 31 | 237.0 | **63** | 204.8 | **95** | 180.4 | **127** | 161.2 |

Table VII‑3 Simulated SFO (kHz) with different RO\_MIM/RO\_MOM configurations

1. zhiyoong@umich.edu [↑](#footnote-ref-1)
2. seojeong@umich.edu [↑](#footnote-ref-2)
3. lxchuo@umich.edu [↑](#footnote-ref-3)
4. Leakage Power does not include power-gating [↑](#footnote-ref-4)
5. Leakage Power does not include power-gating [↑](#footnote-ref-5)