SONY

6.25-mm (Type 1/2.9) diagonal SPAD ToF Depth Sensor with signal-amplifying pixels

IMX459-AAMV-W

1. Description and Usage

The IMX459-AAMV-W is a 6.25-mm (Type 1/2.9) diagonal Single Photon Avalanche Diode (SPAD) ToF Depth Sensor with signal-amplifying pixels. By arraying the 597 × 168 number of SPADs and summing their outputs, the 3D distance images can be generated from the distance information, and it can be achieved a measurement distance of up to 300 m. The number of SPADs (size of a macro pixel) at the time of ranging operation can be adjusted according to the application. The ranging operation is operated by 1 GHz sampling, and the function of generating a histogram with ToF width of 2024 bin (2024 ns) and grayscale width of 12 bits and it can be detecting echo and peak of the emitted light from the result. Its ambient light elimination function ensures that it does not saturate even under sunlight and can achieve distance measurements with a high dynamic range. Its light emission timing control function is able to compensate for the delay in timing between laser emission and reception. Equipped with echo and peak detection functions, ranging data output modes, digital signal processing, and more, it is optimized to meet the performance and functionality required by LiDAR. Safety Mechanism (SM) functions required for automotive products are supported.
Applications: LiDAR for automotive

2. Features and Functions

- ◆ SPAD signal-amplifying pixels
- ◆ Number of effective SPAD
  - 597 (H) × 168 (V) approx. 100k SPAD
- ◆ CRA: 0 degrees
- ◆ Input frequencies: 16 MHz, 20 MHz, 24 MHz, 30 MHz
- ◆ External communication interfaces
  - I^2C communication
  - SPI communication
- ◆ Output interface
  - MIPI CSI-2 serial output (4 lanes/2 lanes)
- ◆ Readout modes
  - Line mode
  - Array mode
- ◆ Output formats
  - Ranging data output mode (RAW12, ToF width: 2024 bins, gray scale width: 12 bits)
  - Echo output mode (RAW12, ToF width: 2024 bins, gray scale width: 12 bits)
  - Histogram output mode (RAW12, ToF width: 2024 bins, gray scale width: 12 bits)
- ◆ Variable pixel size, region of interest (ROI) function
- ◆ Ambient light monitor function
  - Ambient light count width: 22 bits
- ◆ Emission timing control function
- ◆ Histogram generation function
- ◆ Echo and peak detection functions
- ◆ AEC-Q100 Grade 2 qualified
- ◆ ESD rank
  - HBM (Grade 2): Classification 2
  - CDM (Grade 2): Classification C4B

3. Device Structure

◆ SPAD ToF Depth Sensor
◆ Image size: Diagonal 6.25 mm (Type 1/2.9)
◆ SPAD unit cell size: 10.08 μm (H) × 10.08 μm (V)
◆ Element size: 3 (H) × 3 (V) SPAD
◆ Number of physical active SPAD*1: 600 (H) × 189 (V) approx. 110k SPAD
◆ Number of effective SPAD: 597 (H) × 168 (V) approx. 100k SPAD
◆ Substrate material: Silicon

*1 Including non-effective pixels and monitor pixels

4. Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
SPAD breakdown voltage power supply	VOP*1	- 26	+ 0.3	V	—
SPAD excess voltage power supply	Vex*2	- 0.3	4.0	V	—
Digital power supply	VDDD*3	- 0.3	1.5	V	—
Analog power supply	VDDA*4	- 0.3	4.0	V	—
I/O power supply	VDDIO*5	- 0.3	2.5	V	—

5. Recommended Drive Conditions

Table 5-1 Recommended Drive Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SPAD breakdown voltage power supply	VOP*1	- 24.5	- 20.5	- 17	V	—
SPAD excess voltage power supply	Vex*2	3.15	3.3	3.6	V	—
Digital power supply	VDDD*3	1.05	1.1	1.2	V	—
Analog power supply	VDDA*4	3.15	3.3	3.45	V	—
I/O power supply	VDDIO*5	1.7	1.8	1.9	V	—
Operating temperature	Topr	Ta = - 40 to + 105 Tj = - 40 to + 125			℃	—
Storage temperature	Tstg	Ta = - 40 to + 125			℃	—

*1 VOP: VRLD
*2 Vex: VDDHPF
*3 VDDD: VDDLSC, VDDLPL1, VDDLPL2, VDDLIF
*4 VDDA: VDDHAN
*5 VDDIO: VDDMIO, VDDMIF

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Automotive-0.0.2

7. Contents

8. Optical Center

Fig. 8-1 shows Optical Center (Top View).
In the figure, the A1.pin is located at the bottom right.

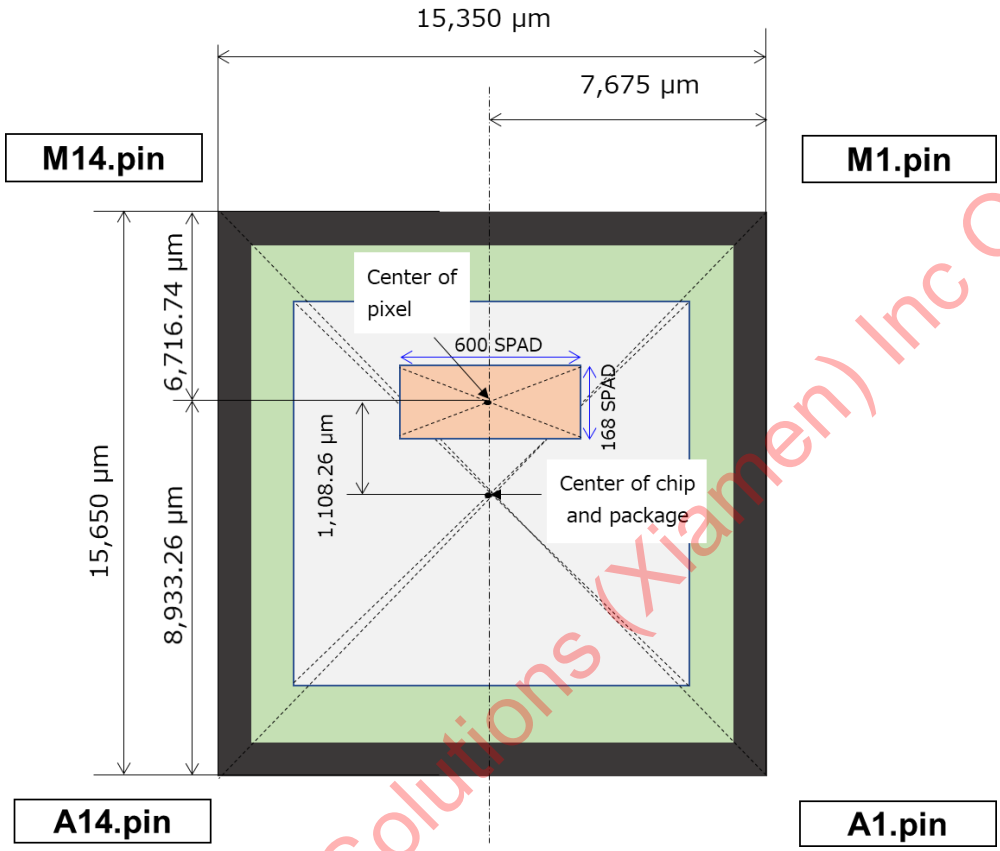


Fig. 8-1 Optical Center (Top View)[*1]

[*1] The chip center and package center match.
(The pixel center and package center is unmatch.)

9. SPAD Configuration

Fig. 9-1 shows SPAD Configuration.
In the figure, the A1.pin is located at the bottom right.

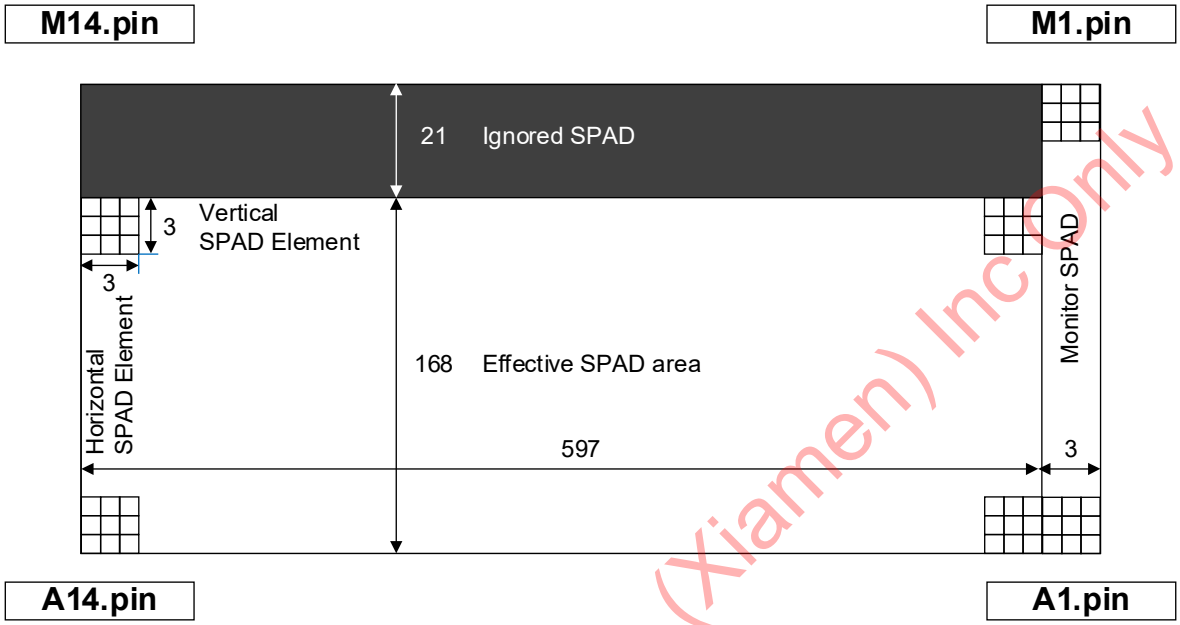


Fig. 9-1 SPAD Configuration

10. Block Diagram

Fig. 10-1 shows Block Diagram.

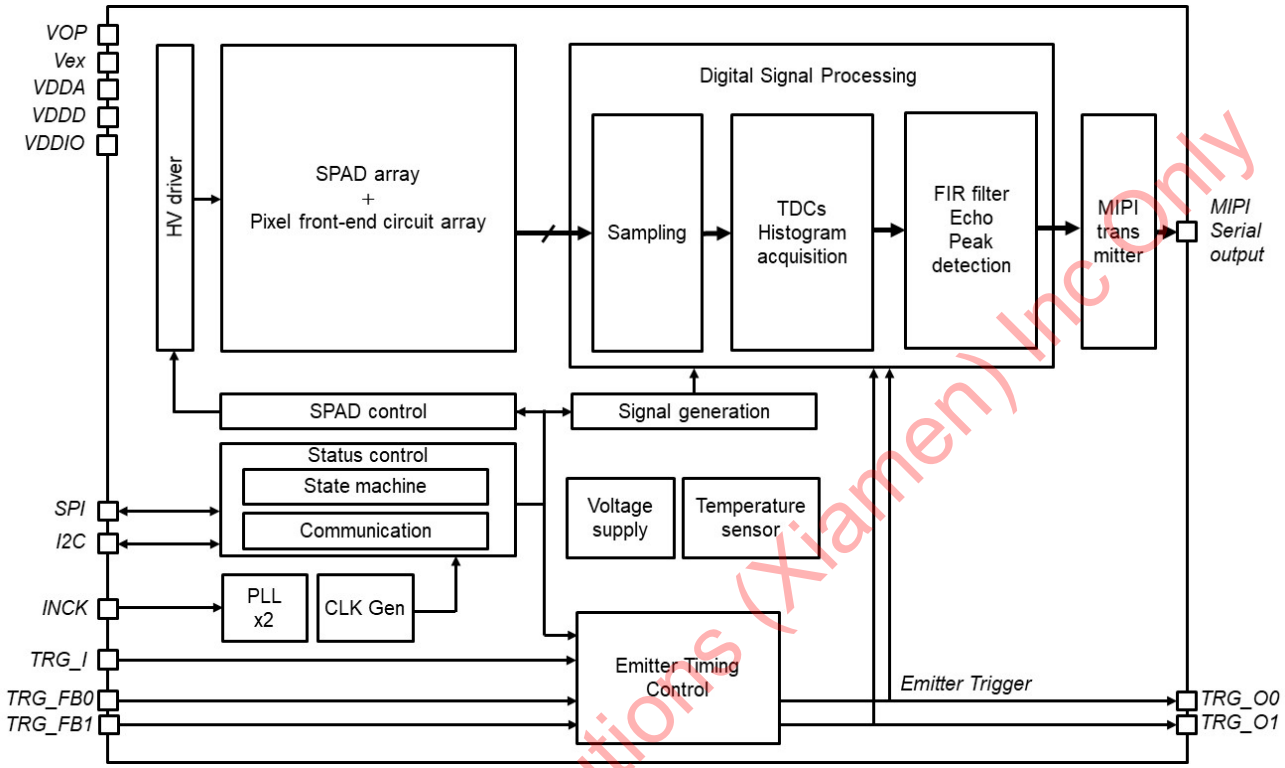
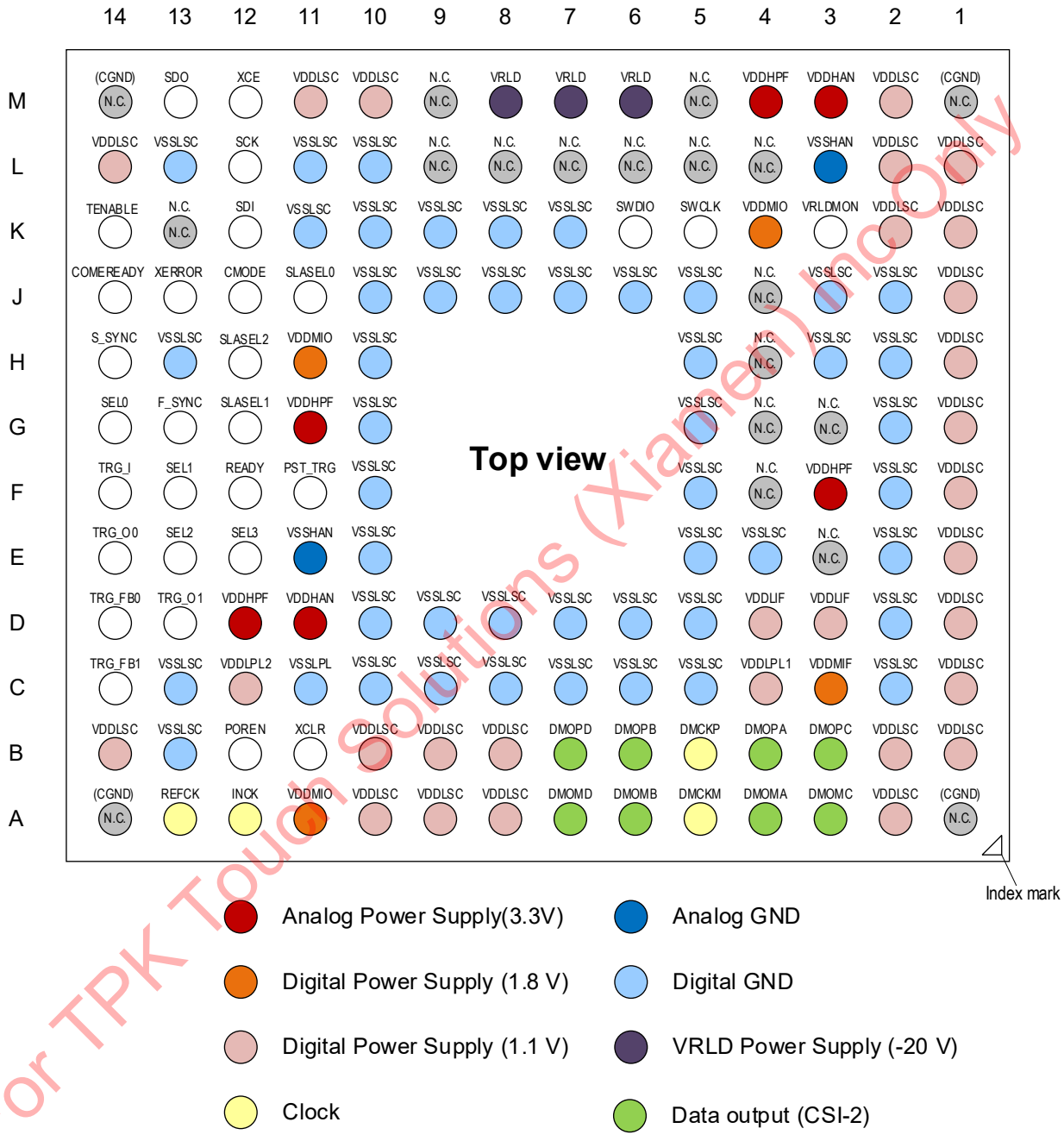


Fig. 10-1 Block Diagram

11. Pin Configuration

Fig. 11-1 shows Pin Configuration (Top View).
In the figure, the Index mark of A1.pin is located at the bottom right.



* The N.C. pin marked (CGND) can be connected to GND. N.C. pins not listed here must be left OPEN.

Fig. 11-1 Pin Configuration (Top View)

12. Pin Description

Table 12-1 List of Pins

No.	Pin No.	I/O	Analog /Digital	Symbol	Pin Description
1	A1	—	—	N.C.	Leave OPEN or connect to GND
2	A2	Power	Digital	VDDLSC	1.1 V power supply
3	A3	Output	Digital	DMOMC	MIPI CSI-2 data lane 3
4	A4	Output	Digital	DMOMA	MIPI CSI-2 data lane 1
5	A5	Output	Digital	DMCKM	MIPI CSI-2 clock lane
6	A6	Output	Digital	DMOMB	MIPI CSI-2 data lane 2
7	A7	Output	Digital	DMOMD	MIPI CSI-2 data lane 4
8	A8	Power	Digital	VDDLSC	1.1 V power supply
9	A9	Power	Digital	VDDLSC	1.1 V power supply
10	A10	Power	Digital	VDDLSC	1.1 V power supply
11	A11	Power	Digital	VDDMIO	1.8 V power supply
12	A12	Input	Digital	INCK	Master clock input
13	A13	Input	Digital	REFCK	Reference clock input
14	A14	—	—	N.C.	Leave OPEN or connect to GND
15	B1	Power	Digital	VDDLSC	1.1 V power supply
16	B2	Power	Digital	VDDLSC	1.1 V power supply
17	B3	Output	Digital	DMOPC	MIPI CSI-2 data lane 3
18	B4	Output	Digital	DMOPA	MIPI CSI-2 data lane 1
19	B5	Output	Digital	DMCKP	MIPI CSI-2 clock lane
20	B6	Output	Digital	DMOPB	MIPI CSI-2 data lane 2
21	B7	Output	Digital	DMOPD	MIPI CSI-2 data lane 4
22	B8	Power	Digital	VDDLSC	1.1 V power supply
23	B9	Power	Digital	VDDLSC	1.1 V power supply
24	B10	Power	Digital	VDDLSC	1.1 V power supply
25	B11	Input	Digital	XCLR	System Reset (Active Low)
26	B12	Input	Digital	POREN	Power supply monitor circuit enable input
27	B13	GND	Digital	VSSLSC	1.1 V GND
28	B14	Power	Digital	VDDLSC	1.1 V power supply
29	C1	Power	Digital	VDDLSC	1.1 V power supply
30	C2	GND	Digital	VSSLSC	1.1 V GND
31	C3	Power	Digital	VDDMIF	1.8 V power supply
32	C4	Power	Digital	VDDLPL1	1.1 V power supply
33	C5	GND	Digital	VSSLSC	1.1 V GND
34	C6	GND	Digital	VSSLSC	1.1 V GND
35	C7	GND	Digital	VSSLSC	1.1 V GND
36	C8	GND	Digital	VSSLSC	1.1 V GND
37	C9	GND	Digital	VSSLSC	1.1 V GND
38	C10	GND	Digital	VSSLSC	1.1 V GND
39	C11	GND	Digital	VSSLPL	1.1 V GND
40	C12	Power	Digital	VDDLPL2	1.1 V power supply
41	C13	GND	Digital	VSSLSC	1.1 V GND
42	C14	Input	Digital	TRG_FB1	Emission trigger feedback input 1
43	D1	Power	Digital	VDDLSC	1.1 V power supply
44	D2	GND	Digital	VSSLSC	1.1 V GND
45	D3	Power	Digital	VDDLIF	1.1 V power supply
46	D4	Power	Digital	VDDLIF	1.1 V power supply
47	D5	GND	Digital	VSSLSC	1.1 V GND
48	D6	GND	Digital	VSSLSC	1.1 V GND
49	D7	GND	Digital	VSSLSC	1.1 V GND
50	D8	GND	Digital	VSSLSC	1.1 V GND

No.	Pin No.	I/O	Analog /Digital	Symbol	Pin Description
51	D9	GND	Digital	VSSLSC	1.1 V GND
52	D10	GND	Digital	VSSLSC	1.1 V GND
53	D11	Power	Analog	VDDHAN	3.3 V power supply
54	D12	Power	Analog	VDDHPF	3.3 V power supply
55	D13	Output	Digital	TRG_O1	Emission trigger output 1
56	D14	Input	Digital	TRG_FB0	Emission trigger feedback input 0
57	E1	Power	Digital	VDDLSC	1.1 V power supply
58	E2	GND	Digital	VSSLSC	1.1 V GND
59	E3	—	—	N.C.	Leave OPEN
60	E4	GND	Digital	VSSLSC	1.1 V GND
61	E5	GND	Digital	VSSLSC	1.1 V GND
62	E10	GND	Digital	VSSLSC	1.1 V GND
63	E11	GND	Analog	VSSHAN	3.3 V GND
64	E12	Input	Digital	SEL3	Effective pixel area select signal input 3
65	E13	Input	Digital	SEL2	Effective pixel area select signal input 2
66	E14	Output	Digital	TRG_O0	Emission trigger output 0
67	F1	Power	Digital	VDDLSC	1.1 V power supply
68	F2	GND	Digital	VSSLSC	1.1 V GND
69	F3	Power	Analog	VDDHPF	3.3 V power supply
70	F4	—	—	N.C.	Leave OPEN
71	F5	GND	Digital	VSSLSC	1.1 V GND
72	F10	GND	Digital	VSSLSC	1.1 V GND
73	F11	I/O	Digital	PST_TRG	Get ambient light timing signal I/O
74	F12	Output	Digital	READY	IC available signal output
75	F13	Input	Digital	SEL1	Effective pixel area select signal input 1
76	F14	I/O	Digital	TRG_I	Emission trigger I/O
77	G1	Power	Digital	VDDLSC	1.1 V power supply
78	G2	GND	Digital	VSSLSC	1.1 V GND
79	G3	—	—	N.C.	Leave OPEN
80	G4	—	—	N.C.	Leave OPEN
81	G5	GND	Digital	VSSLSC	1.1 V GND
82	G10	GND	Digital	VSSLSC	1.1 V GND
83	G11	Power	Analog	VDDHPF	3.3 V power supply
84	G12	Input	Digital	SLASEL1	I^2C slave address select signal 1
85	G13	I/O	Digital	F_SYNC	Frame synchronization signal I/O
86	G14	Input	Digital	SEL0	Effective pixel area select signal input 0
87	H1	Power	Digital	VDDLSC	1.1 V power supply
88	H2	GND	Digital	VSSLSC	1.1 V GND
89	H3	GND	Digital	VSSLSC	1.1 V GND
90	H4	—	—	N.C.	Leave OPEN
91	H5	GND	Digital	VSSLSC	1.1 V GND
92	H10	GND	Digital	VSSLSC	1.1 V GND
93	H11	Power	Digital	VDDMIO	1.8 V power supply
94	H12	Input	Digital	SLASEL2	I^2C slave address select signal 2
95	H13	GND	Digital	VSSLSC	1.1 V GND
96	H14	I/O	Digital	S_SYNC	Slot synchronization signal I/O
97	J1	Power	Digital	VDDLSC	1.1 V power supply
98	J2	GND	Digital	VSSLSC	1.1 V GND
99	J3	GND	Digital	VSSLSC	1.1 V GND
100	J4	—	—	N.C.	Leave OPEN
101	J5	GND	Digital	VSSLSC	1.1 V GND
102	J6	GND	Digital	VSSLSC	1.1 V GND
103	J7	GND	Digital	VSSLSC	1.1 V GND
104	J8	GND	Digital	VSSLSC	1.1 V GND

No.	Pin No.	I/O	Analog /Digital	Symbol	Pin Description
105	J9	GND	Digital	VSSLSC	1.1 V GND
106	J10	GND	Digital	VSSLSC	1.1 V GND
107	J11	Input	Digital	SLASEL0	I^2C slave address select signal 0
108	J12	Input	Digital	CMODE	Communication I/F switching input
109	J13	Output	Digital	XERROR	External reset request signal output
110	J14	Output	Digital	COMREADY	Communication period notification output
111	K1	Power	Digital	VDDLSC	1.1 V power supply
112	K2	Power	Digital	VDDLSC	1.1 V power supply
113	K3	Input	Analog	VRLDMON	VRLD monitor input
114	K4	Power	Digital	VDDMIO	1.8 V power supply
115	K5	Input	Digital	SWCLK	Serial Wire clock input
116	K6	I/O	Digital	SWDIO	Serial Wire data I/O
117	K7	GND	Digital	VSSLSC	1.1 V GND
118	K8	GND	Digital	VSSLSC	1.1 V GND
119	K9	GND	Digital	VSSLSC	1.1 V GND
120	K10	GND	Digital	VSSLSC	1.1 V GND
121	K11	GND	Digital	VSSLSC	1.1 V GND
122	K12	I/O	Digital	SDI	I^2C/SPI communication data I/O
123	K13	—	—	N.C.	Leave OPEN
124	K14	Input	Digital	TENABLE	Test enable input
125	L1	Power	Digital	VDDLSC	1.1 V power supply
126	L2	Power	Digital	VDDLSC	1.1 V power supply
127	L3	GND	Analog	VSSHAN	3.3 V GND
128	L4	—	—	N.C.	Leave OPEN
129	L5	—	—	N.C.	Leave OPEN
130	L6	—	—	N.C.	Leave OPEN
131	L7	—	—	N.C.	Leave OPEN
132	L8	—	—	N.C.	Leave OPEN
133	L9	—	—	N.C.	Leave OPEN
134	L10	GND	Digital	VSSLSC	1.1 V GND
135	L11	GND	Digital	VSSLSC	1.1 V GND
136	L12	I/O	Digital	SCK	I^2C/SPI communication clock I/O
137	L13	GND	Digital	VSSLSC	1.1 V GND
138	L14	Power	Digital	VDDLSC	1.1 V power supply
139	M1	—	—	N.C.	Leave OPEN or connect to GND
140	M2	Power	Digital	VDDLSC	1.1 V power supply
141	M3	Power	Analog	VDDHAN	3.3 V power supply
142	M4	Power	Analog	VDDHPF	3.3 V power supply
143	M5	—	—	N.C.	Leave OPEN
144	M6	Power	Analog	VRLD	SPAD anode potential
145	M7	Power	Analog	VRLD	SPAD anode potential
146	M8	Power	Analog	VRLD	SPAD anode potential
147	M9	—	—	N.C.	Leave OPEN
148	M10	Power	Digital	VDDLSC	1.1 V power supply
149	M11	Power	Digital	VDDLSC	1.1 V power supply
150	M12	Input	Digital	XCE	Serial communication data for SPI communication enable input
151	M13	Output	Digital	SDO	Serial communication data for SPI communication output
152	M14	—	—	N.C.	Leave OPEN or connect to GND

13. Electrical Characteristics

13.1. DC Characteristics

Table 13-1 DC Characteristics

Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital input voltage	INCK, REFCK CMODE SCK, SDI SLASEL0 SLASEL1 SLASEL2 F_SYNC, S_SYNC PST_TRG TRG_FB0 TRG_FB1 TRG_I SEL0, SEL1 SEL2, SEL3 PORENSWCLK, SWDIO TENABLE XCE	VIH	—	0.75 × VDDIO	—	—	V
		VIL	—	—	—	0.25 × VDDIO	V
	XCLR	VIH	—	1.35	—	—	V
		VIL	—	—	—	0.27	V
Digital output voltage	XERROR, READY COMREADY SCK, SDI, SDO F_SYNC, S_SYNC PST_TRG, TRG_I TRG_O0, TRG_O1 SWDIO	VOH	—	VDDIO - 0.2	—	—	V
		VOL	—	—	—	0.2	V
Digital output current		IOH	VOH = VDDIO - 0.2	4.0*1	—	—	mA
		IOL	VOL = 0.2	4.0*1	—	—	mA

*1 IOH and IOL conform to the drivability setting value. The values in the table are the default settings.

13.2. AC Characteristics

13.2.1. Master Clock (INCK)

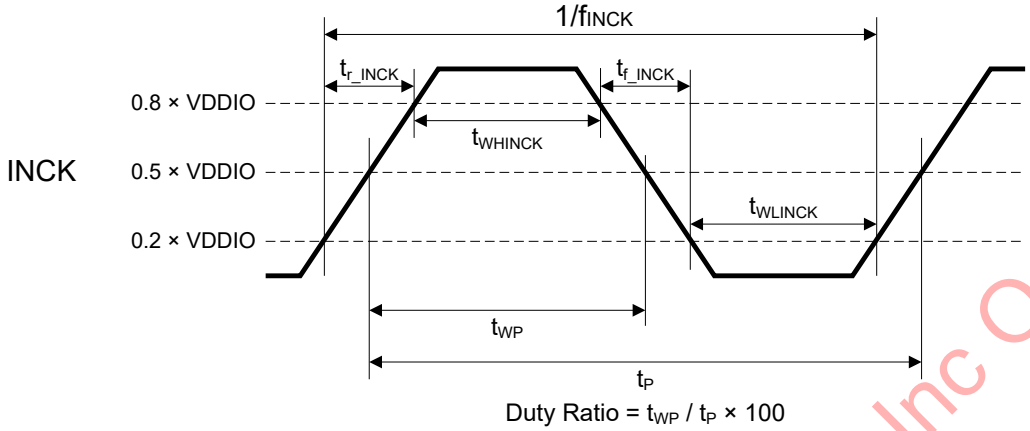


Fig. 13-1 INCK Waveform Schematic Diagram

Table 13-2 Input Clock Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	16	20	30	MHz	f_{INCK}= 16,20,24,30 MHz (Intermediate values not allowed)
INCK clock accuracy	—	- 150	—	+ 150	ppm	Accuracy of the quartz crystal resonator of about ±50 ppm is recommended because it affects ranging accuracy.
INCK Low level pulse width	f_{WLINCK}	15	—	—	ns	Voltage conditions: 0.2 × VDDIO
INCK High level pulse width	f_{WHINCK}	15	—	—	ns	Voltage conditions: 0.8 × VDDIO
INCK clock duty	—	45	50	55	%	Defined by 0.5 × VDDIO
INCK rise time	t_{r_INCK}	—	—	5	ns	0.2 × VDDIO→0.8 × VDDIO
INCK fall time	t_{f_INCK}	—	—	5	ns	0.8 × VDDIO→0.2 × VDDIO

13.2.2. Reference Clock (REFCK)

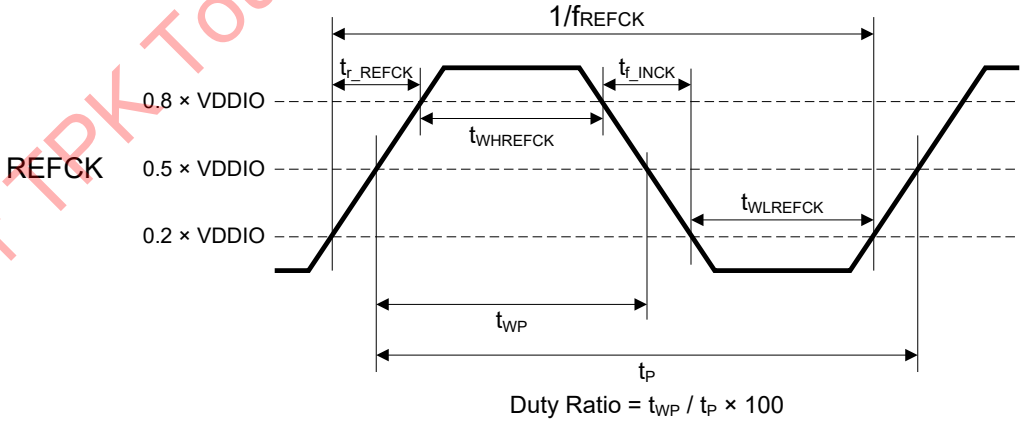


Fig. 13-2 REFCK Waveform Schematic Diagram

Table 13-3 REFCK Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
REFCK clock frequency	f_{REFCK}	16	f_{INCK}	30	MHz	Input same frequency as INCK for REFCK
REFCK Low level pulse	$f_{WLREFCK}$	15	—	—	ns	Voltage conditions: 0.2 × VDDIO

width						
REFCK High level pulse width	$f_{WHREFCK}$	15	—	—	ns	Voltage conditions: 0.8 × VDDIO
REFCK clock duty	—	45	50	55	%	Defined by 0.5 × VDDIO
REFCK rise time	t_{r_REFCK}	—	—	5	ns	0.2 × VDDIO→0.8 × VDDIO
REFCK fall time	t_{f_REFCK}	—	—	5	ns	0.8 × VDDIO→0.2 × VDDIO

13.2.3. System Reset (XCLR)

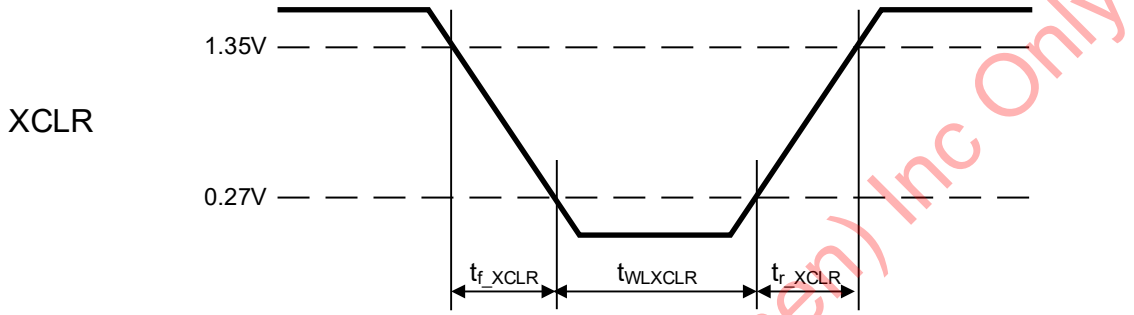


Fig. 13-3 XCLR Waveform Schematic Diagram

Table 13-4 XCLR Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	1000	—	—	ns	Voltage conditions: 0.27 V
XCLR rise time	t_{r_XCLR}	—	—	100	ns	0.27 V→1.35 V
XCLR fall time	t_{f_XCLR}	—	—	100	ns	1.35 V→0.27 V

13.2.4. Get Ambient Light Timing Signal (PST_TRG)

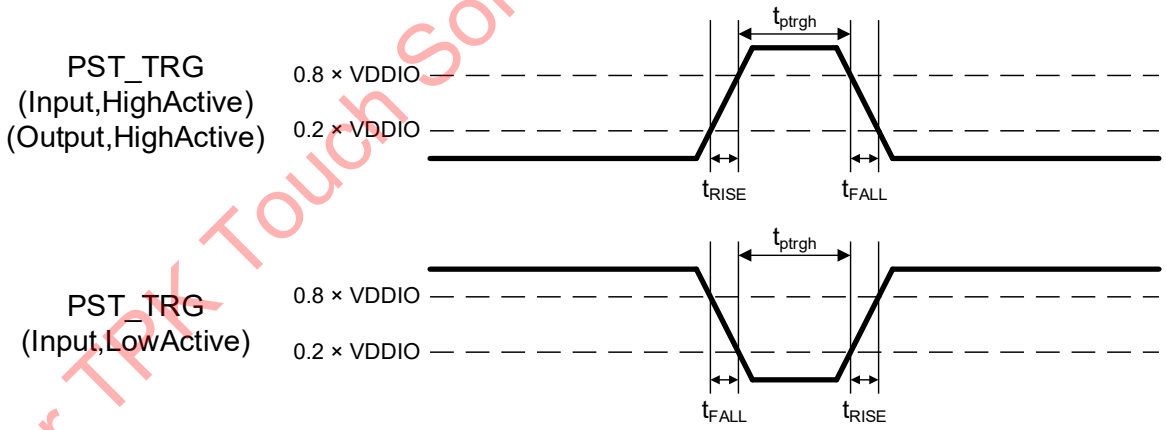


Fig. 13-4 PST_TRG Waveform Schematic Diagram

Table 13-5 PST_TRG Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
PST_TRG High level pulse width	t_{ptrgh}	100	—	—	ns	Voltage conditions: 0.8 × VDDIO
PST_TRG signal rise time (When PST_TRG signal is output)	t_{RISE}	—	—	100	ns	0.2 × VDDIO→0.8 × VDDIO
PST_TRG signal fall time (When PST_TRG signal is output)	t_{FALL}	—	—	100	ns	0.8 × VDDIO→0.2 × VDDIO

Table 13-6 PST_TRG Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
PST_TRG High level pulse width	t_{ptrgh}	16	64	1000	ns	Voltage conditions: 0.8 × VDDIO
PST_TRG signal rise time (When PST_TRG signal is output)	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
PST_TRG signal fall time (When PST_TRG signal is output)	t_{FALL}	—	—	1.6	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.5. Effective Pixel Area Select Signal / Emission Trigger Input Signal (SEL/TRG_I)

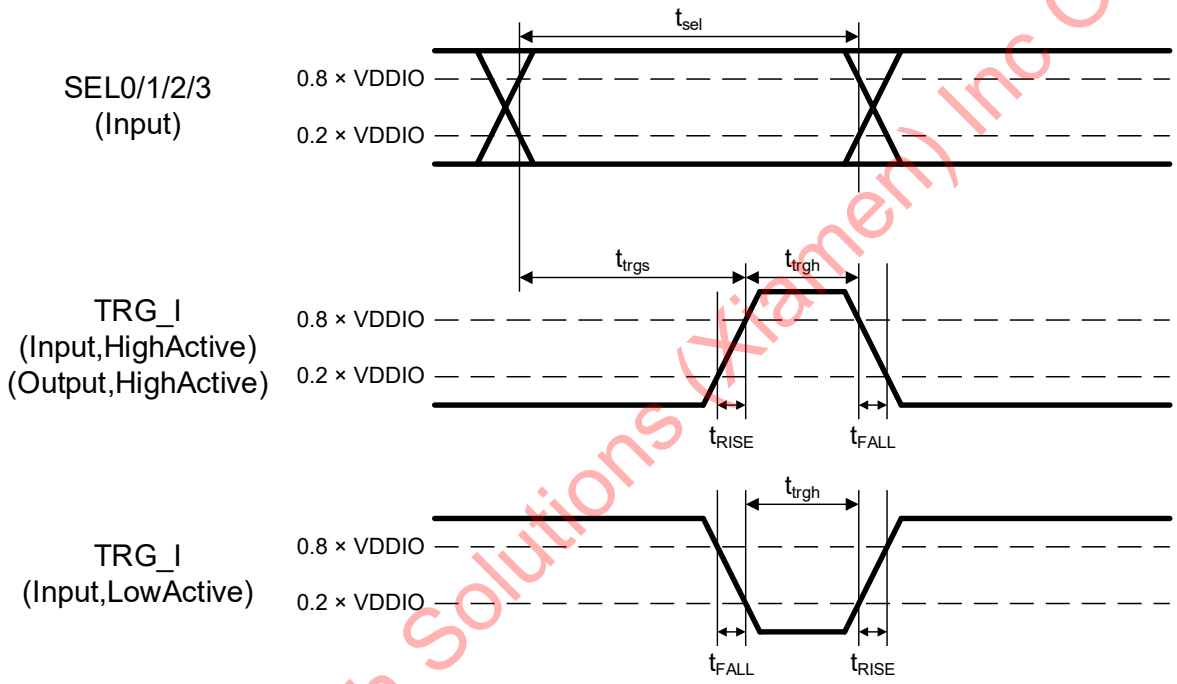


Fig. 13-5 SEL0/1/2/3, TRG_I Waveform Schematic Diagram

Table 13-7 SEL and TRG_I Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SEL pulse width	t_{sel}	125	—	—	ns	Voltage conditions: 0.2, 0.8×VDDIO
Emission trigger input setup time	t_{trgs}	25	—	—	ns	Voltage conditions: 0.2, 0.8×VDDIO
Emission trigger pulse width	t_{trgh}	100	—	—	ns	Voltage conditions: 0.8 × VDDIO
Emission trigger rise time (when emission trigger is output)	t_{RISE}	—	—	100	ns	0.2 × VDDIO→0.8 × VDDIO
Emission trigger fall time (when emission trigger is output)	t_{FALL}	—	—	100	ns	0.8 × VDDIO→0.2 × VDDIO

Table 13-8 TRG_I Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Emission trigger pulse width	t_{trgh}	16	64	1000	ns	Voltage conditions: 0.8 × VDDIO
Emission trigger rise time (when emission trigger is output)	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
Emission trigger fall time (when emission trigger is output)	t_{FALL}	—	—	1.6	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.6. Emission Trigger Feedback Signal (TRG_FB0/1)

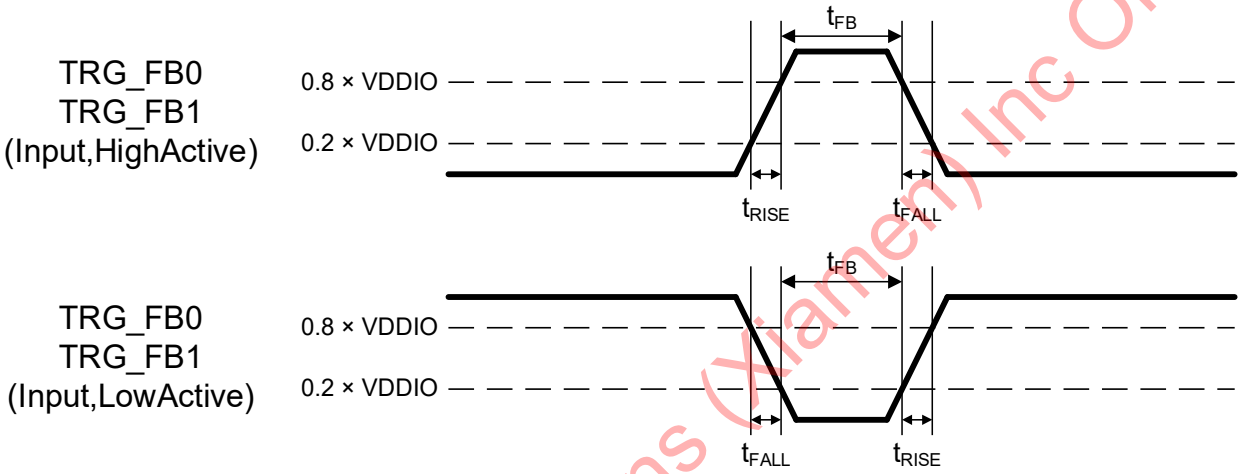


Fig. 13-6 TRG_FB0/1 Waveform Schematic Diagram

Table 13-9 TRG_FB0/1 Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Trigger feedback signal pulse width	t_{FB}	4	5	—	ns	Voltage conditions: 0.8 × VDDIO
Trigger feedback signal rise time	t_{RISE}	—	—	100	ns	0.2 × VDDIO→0.8 × VDDIO
Trigger feedback signal fall time	t_{FALL}	—	—	100	ns	0.8 × VDDIO→0.2 × VDDIO

13.2.7. Emission Trigger Output Signal (TRG_O0/1)

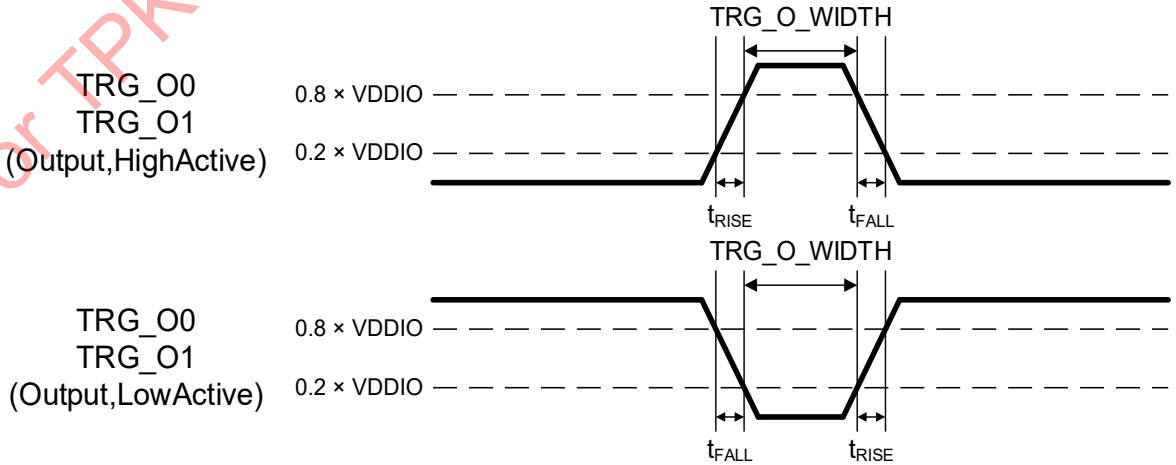


Fig. 13-7 TRG_O0/1 Waveform Schematic Diagram

Table 13-10 TRG_O0/1 Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
TRG_O0/1 signal pulse width	TRG_O_WIDTH	16	100	1000	ns	The standard value is the default value
TRG_O0/1 signal rise time	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
TRG_O0/1 signal fall time	t_{FALL}	—	—	1.7	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.8. Frame Synchronization Signal / Slot Synchronization Signal (F_SYNC/ S_SYNC)

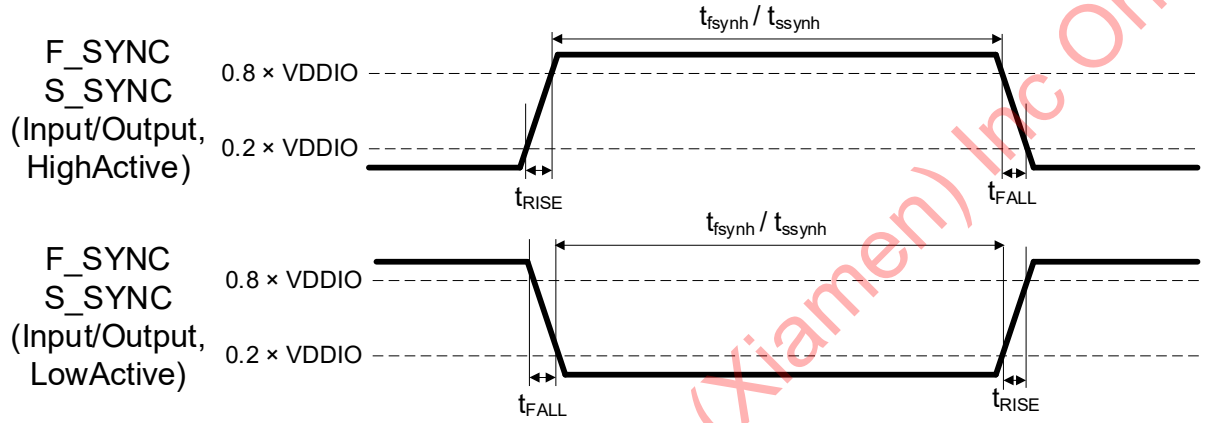


Fig. 13-8 F_SYNC / S_SYNC Waveform Schematic Diagram

Table 13-11 F_SYNC/S_SYNC Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
F_SYNC pulse width	t_{fsynh}	8	—	998	ms	—
S_SYNC pulse width	t_{ssynh}	40	—	—	μs	—
F_SYNC/S_SYNC signal Rise time (when synchronization signal is output)	t_{RISE}	—	—	100	ns	0.2 × VDDIO→0.8 × VDDIO
F_SYNC/S_SYNC signal Fall time (when synchronization signal is output)	t_{FALL}	—	—	100	ns	0.8 × VDDIO→0.2 × VDDIO

Table 13-12 F_SYNC/S_SYNC Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
F_SYNC pulse width	t_{fsynh}	1	7.992	998	ms	—
S_SYNC pulse width	t_{ssynh}	40	48	1000	μs	—
F_SYNC/S_SYNC signal Rise time (when synchronization signal is output)	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
F_SYNC/S_SYNC signal Fall time (when synchronization signal is output)	t_{FALL}	—	—	1.6	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.9. IC Available Signal/Communication Period Notification (READY/COMREADY)

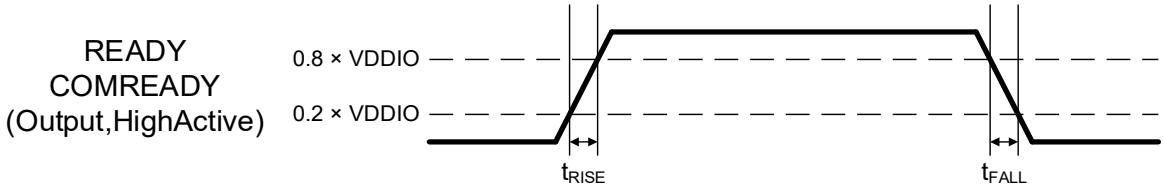


Fig. 13-9 READY / COMREADY Waveform Schematic Diagram

Table 13-13 READY/COMREADY Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
READY/COMREADY signal Rise time	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
READY/COMREADY signal Fall time	t_{FALL}	—	—	1.6	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.10. External Reset Request Signal (XERROR)

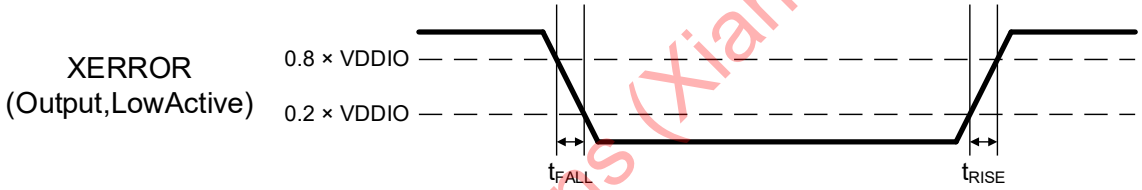


Fig. 13-10 XERROR Waveform Schematic Diagram

Table 13-14 XERROR Output Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XERROR signal Rise time	t_{RISE}	—	—	1.8	ns	0.2 × VDDIO→0.8 × VDDIO Output load capacitance: 20 pF
XERROR signal Fall time	t_{FALL}	—	—	1.6	ns	0.8 × VDDIO→0.2 × VDDIO Output load capacitance: 20 pF

13.2.11. Serial Communication

I²C communication

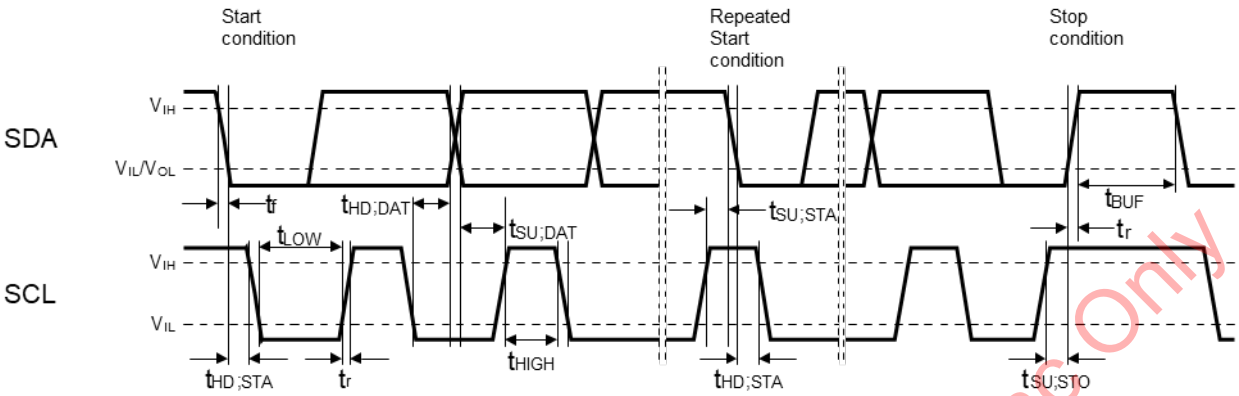


Fig. 13-11 I²C Communication Waveform Schematic Diagram

Table 13-15 I²C Communication Operating Specifications

Item	Symbol	Fast mode		Unit	Remarks
		Min.	Max.		
Low level input voltage	V_{IL}	-0.5	0.3 × VDDIO	V	—
High level input voltage	V_{IH}	0.7 × VDDIO	VDDIO max +0.5	V	—
Low level output voltage	V_{OL}	0	0.2 × VDDIO	V	VDDIO < 2 V, Sink 3 mA
Output fall time	t_{of}	—	250	ns	Load 10 pF to 400 pF, 0.7 × VDDIO → 0.3 × VDDIO
Input current	Ii	-10	10	μA	0.1 × VDDIO → 0.9 × VDDIO
SCL and SDA input capacitance	Ci	—	10	pF	—

Table 13-16 I²C Communication AC Timing

Item	Symbol	Fast mode			Unit	Remarks
		Min.	Typ.	Max.		
SCL clock frequency	f_{SCL}	—	400	—	kHz	Only FastMode is supported
Hold time (Start condition, Repeated Start Condition)	$t_{HD;STA}$	0.6	—	—	μs	—
SCL clock Low period	t_{LOW}	1.3	—	—	μs	—
SCL clock High period	t_{HIGH}	0.6	—	—	μs	—
Setup time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs	—
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs	—
Data setup time	$t_{SU;DAT}$	100	—	—	ns	—
SDA and SCL rise time	t_r	—	—	300	ns	—
SDA and SCL fall time	t_f	—	—	300	ns	—
Setup time (Stop condition)	$t_{SU;STO}$	0.6	—	—	μs	—
Bus free time between Stop condition and Start condition	t_{BUF}	1.3	—	—	μs	—

SPI communication

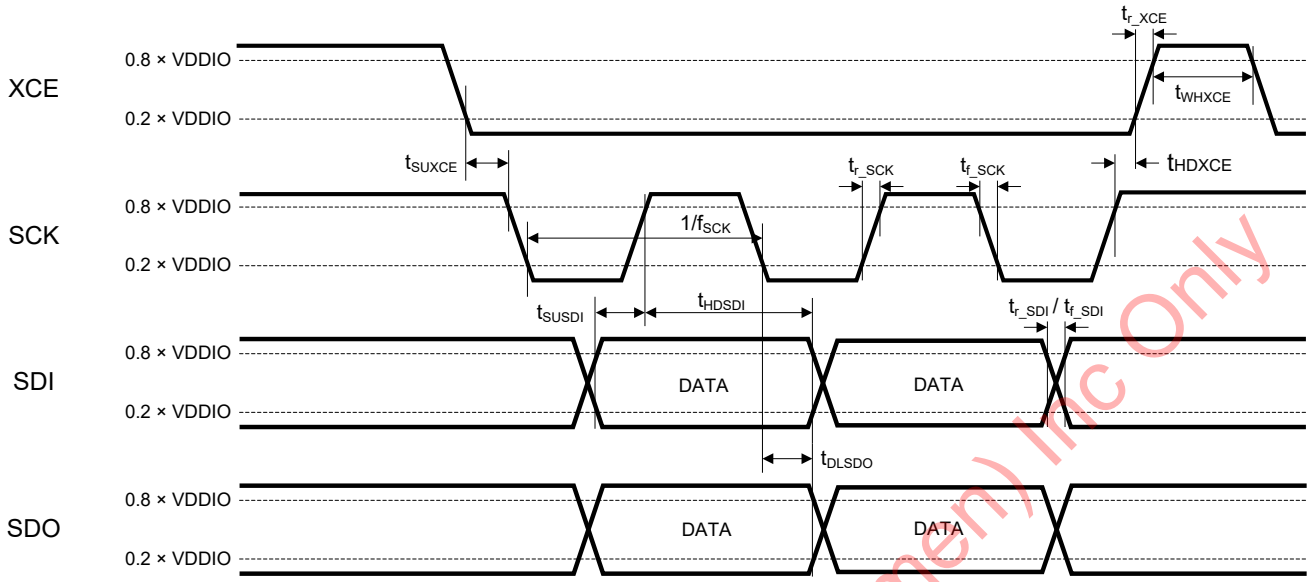


Fig. 13-12 SPI Communication Waveform Schematic Diagram

Table 13-17 SPI Communication AC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	f_{INCK} / 2*1	MHz	—
XCE input setup time	t_{SUXCE}	20	—	—	ns	Voltage conditions: 0.2,0.8 × VDDIO
XCE input hold time	t_{HDXCE}	20	—	—	ns	Voltage conditions: 0.2,0.8 × VDDIO
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	Voltage conditions: 0.8 × VDDIO
SDI input setup time	t_{SUSDI}	10	—	—	ns	Voltage conditions: 0.2,0.8 × VDDIO
SDI input hold time	t_{HDSDI}	10	—	—	ns	Voltage conditions: 0.8 × VDDIO
SDO output hold time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF Voltage conditions: 0.2,0.8 × VDDIO
XCE rise time	t_{r_XCE}	—	—	100	ns	0.2 × VDDIO → 0.8 × VDDIO
XCE fall time	t_{f_XCE}	—	—	100	ns	0.8 × VDDIO → 0.2 × VDDIO
SCK rise time	t_{r_SCK}	—	—	100	ns	0.2 × VDDIO → 0.8 × VDDIO
SCK fall time	t_{f_SCK}	—	—	100	ns	0.8 × VDDIO → 0.2 × VDDIO
SDI rise time	t_{r_SDI}	—	—	100	ns	0.2 × VDDIO → 0.8 × VDDIO
SDI fall time	t_{f_SDI}	—	—	100	ns	0.8 × VDDIO → 0.2 × VDDIO

*1 The maximum value varies according to the input INCK frequency.

13.3 Current Consumption

The prerequisites for the average operating current are as follows:

- Readout: Line modes
- Pixel size: 1 (H) × 4(V) element = 3 (H) × 12 (V) SPAD
- Number of horizontal pixels: 192 pixels
- F_SYNC cycle: 100 ms
- S_SYNC cycle: 125 µs
- Number of slots: 784 times
- Number of TRG_I: 20 times
- Frame rate: 10 frame/s
- SPAD activation rate: 10 MHz
- Output data mode: Ranging; Output data rate: 800 Mbps/lane
- Number of lanes: 4 lanes
- SPAD On period : 1.000 µs
- LD divisions: 4 divisions
- Power supply: Standard VDDD = 1.1 V, VDDA = 3.3 V, VDDIO = 1.8 V, Vex = 3.3 V, VOP = Optimal value
  Maximum VDDD = 1.15 V, VDDA = 3.4 V, VDDIO = 1.9 V, Vex = 3.4 V, VOP = Optimal value
- Temperature: Standard 85 ℃, Maximum 125 ℃

Table 13-18 Current Consumption

Item		Symbol	Typ.	Max.	Unit
Average operating current (Frame average)	SPAD breakdown voltage power supply	IVOP_A*1	1.7	6.0	mA
	SPAD excess voltage power supply	IVex_A*2	2.7	10.0	mA
	Digital power supply	IVDDD_A*3	320	598	mA
	Analog power supply	IVDDA_A*4	2.6	3.2	mA
	I/O power supply	IVDDIO_A*5	2.8	3.6	mA
Peak operating current	SPAD breakdown voltage power supply	IVOP_P*1	64.7	236	mA
	SPAD excess voltage power supply	IVex_P*2	151	672	mA
	Digital power supply	IVDDD_P*3	1643	3401	mA
	Analog power supply	IVDDA_P*4	2.6	6.4	mA
	I/O power supply	IVDDIO_P*5	2.8	7.2	mA
Standby operating current*6	SPAD breakdown voltage power supply*7	IVOP_STB*1	0	3.0	mA
	SPAD excess voltage power supply	IVex_STB*2	0	0.3	mA
	Digital power supply	IVDDD_STB*3	19	400	mA
	Analog power supply	IVDDA_STB*4	0	0.1	mA
	I/O power supply	IVDDIO_STB*5	0	0.1	mA

*1 VOP: VRLD
*2 Vex: VDDHPF
*3 VDDD: VDDLSC, VDDLPL1, VDDLPL2, VDDLIF
*4 VDDA: VDDHAN
*5 VDDIO: VDDMIO, VDDMIF
*6 XCLR = 0 V
*7 VRLD = 0 V

The above current consumption is a reference value. If these prerequisites are to be changed, use the voltage power

supply with a current consumption not exceeding the maximum value.
The array mode has a similar current value as the line mode if the activation rate is equivalent to that of the line mode.

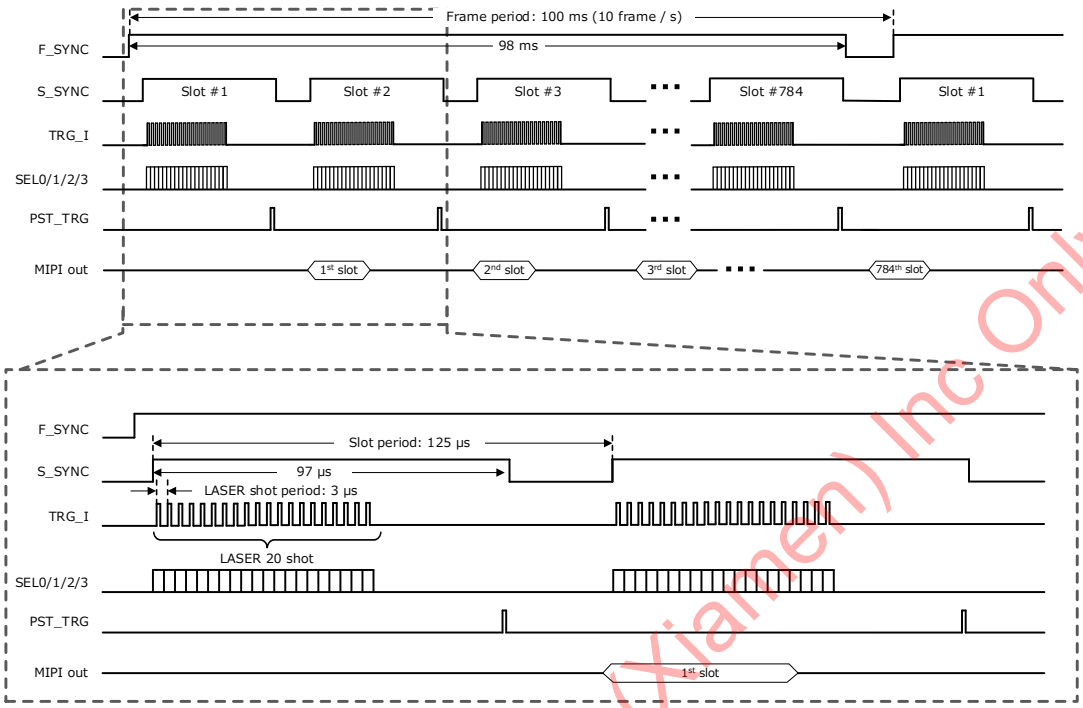
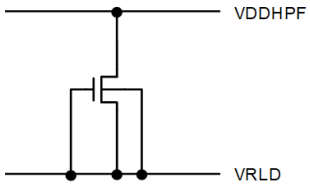
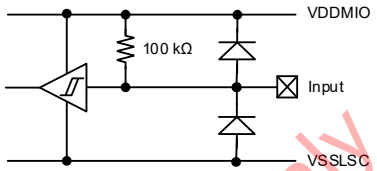
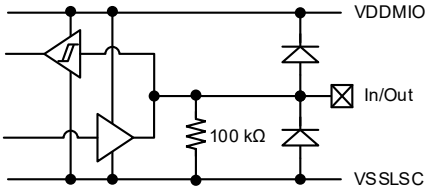
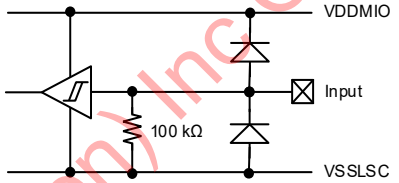
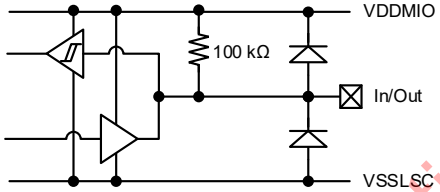
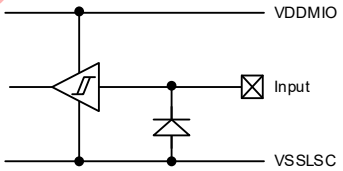
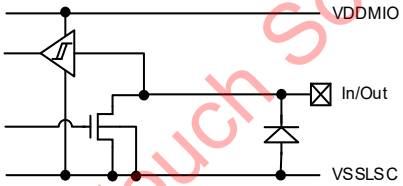
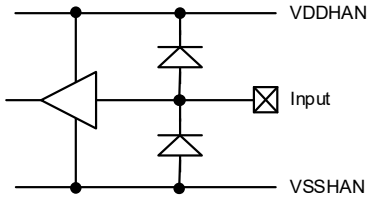
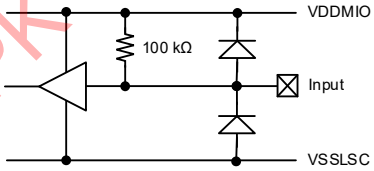
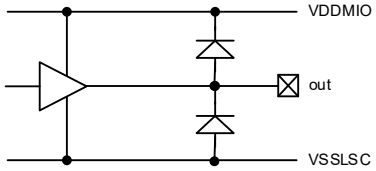
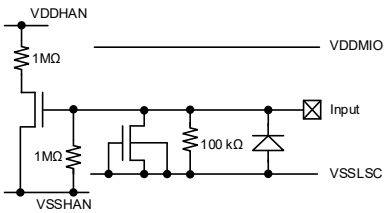
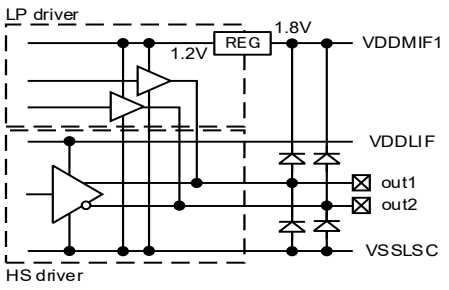


Fig. 13-13 Timing Chart Diagram of Current Consumption Conditions

14. Input/Output Equivalent Circuits

Table 14-1 Input/Output Pins Equivalent Circuits

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
VRLD		SWCLK XCE	
PST_TRG TRG_I TRG_FB0 TRG_FB1 F_SYNC S_SYNC		TENABLE CMODE SEL0 SEL1 SEL2 SEL3 SLASEL0 SLASEL1 SLASEL2	
SWDIO		INCK REFCK	
SCK SDI		VRLDMON	
POREN		SDO READY COMREADY XERROR TRG_O0 TRG_O1	
XCLR		DMOPA DMOPB DMOPC DMOPD DMOMA DMOMB DMOMC DMOMD DMCKP DMCKM	

15. Characteristics

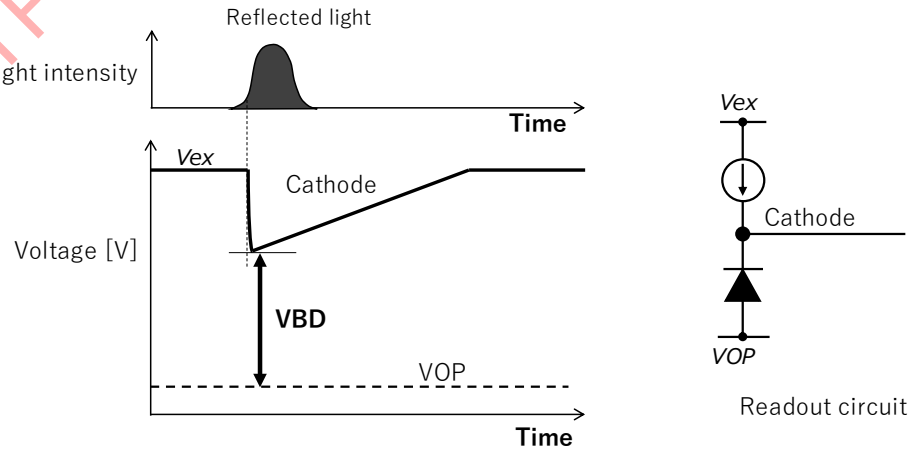
Table 15-1 List of Characteristics

Laser wavelength (λ = 905 nm)

Item	Symbol	Conditions			Characteristics			Unit	Remarks
		Power supply	Temperature [℃]	SPAD/ Element	Min.	Typ.	Max.		
Breakdown voltage (*3)	VBD	Typ.(*2)	- 40 to 125	Element	- 24.5	(- 22.5)	- 17	V	—
Breakdown voltage Temperature-dependent	VBD /Tj	Typ.(*2)	- 40 to 125	Element	—	(- 25) *1	—	mV/℃	—
Dark count rate	DCR	Typ.(*2)	- 40 to 125	Element	—	(3.5k)	6 M	cps	Average per SPAD
Photon Detection Efficiency	PDE	Typ.(*2)	- 40 to 125	Element	10	(24)	—	%	Average per SPAD
Dead time (Pulse width, Most frequent)	DT	Typ.(*2)	85	Element	—	(9)	11.5	ns	Average per SPAD
Dead time (Pulse width, Accumulation 99%)	DT2	Typ.(*2)	85	Element	—	(15)	(20)	ns	Average per SPAD
After-pulse probability	APP	Typ.(*2)	- 15	Element	—	—	(5)	%	Average per SPAD
Crosstalk probability between SPAD	XT	Typ.(*2)	85	SPAD	—	(0.75)	—	%	—
SPAD output jitter (FWHM)	Jitter	Typ.(*2)	85	SPAD	—	(300)	—	ps	—
Inter-element output skew (all pixels)	—	Typ.(*2)	- 40 to 125	Element	—	—	1.45	ns	Identical H direction Between p-p
Incident angle characteristics	CRA	90 % sensitivity relative to 0° λ = 905 nm			—	—	20	deg	—

Values in parentheses are for reference only

*1 Linear approximation from - 40 °C to 125 °C
*2 VDDD = 1.1 V, VDDA = 3.3 V, VDDIO = 1.8 V, Vex = 3.3 V, VOP = Optimal voltage
*3 Breakdown voltage (VBD) means the avalanche voltage of SPAD, and is defined as the difference between the bottom level of the cathode and VOP when SPAD reacts, as shown in Fig. 15-1



Quench・Recharge waveform

Fig. 15-1 SPAD quench recharge waveform and readout circuit

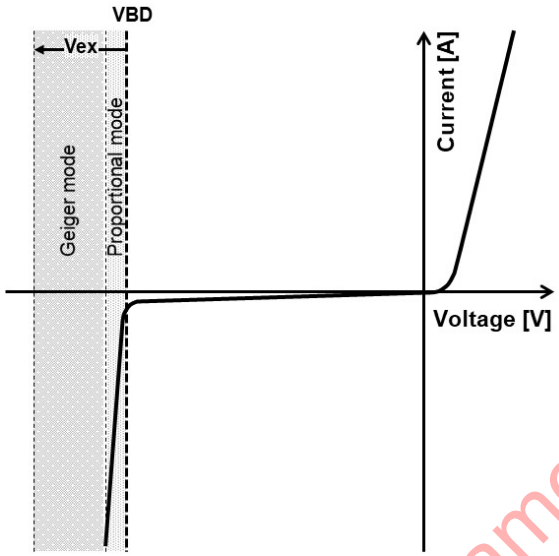
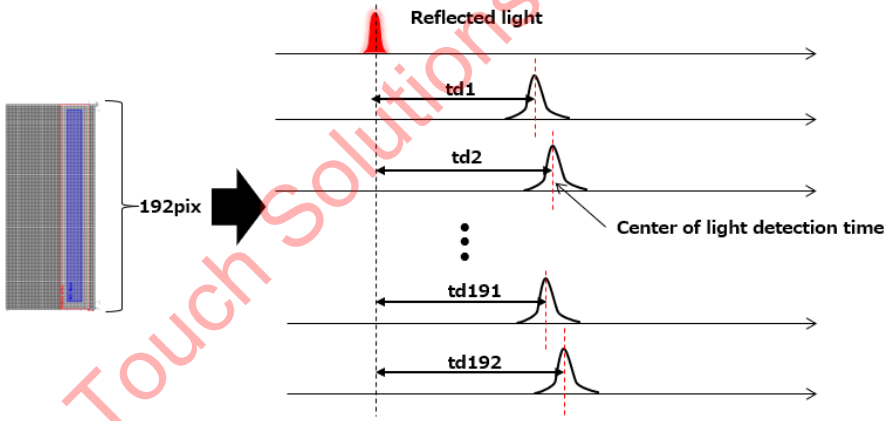


Fig. 15-2 Schematic Diagram of SPAD Breakdown Voltage VBD (Diode I-V Characteristics)



Inter-element output skew=td_max – td_min

td_max : Maximum light detection time in 192 pixels
td_min : Minimum light detection time in 192 pixels

Fig. 15-3 Inter-element output skew (all pixels) Defined

16. Example of Spectral Sensitivity Characteristics

(Vex = 3.3 V / Tj = 40 ℃)

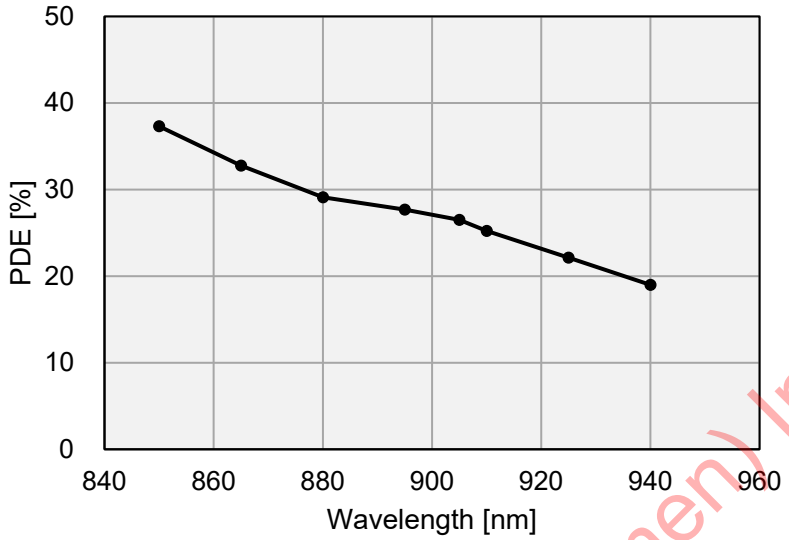


Fig. 16-1 Example of Spectral Sensitivity Characteristics

17. Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by SPI communication and I²C communication. See the Application Note for the addresses, setting values, and communication protocol to be set.

17.1. Selecting the Communication System

The communication system is specified by the CMODE pin. Establish the CMODE pin status before canceling the system reset.
(Do not switch this pin status during operation.) The CMODE pin can also be left open. In this case I²C communication is selected.

Table 17-1 List of Available Communication Systems

Pin name	Pin No.	Pin processing	Communication system	Remarks
CMODE	J12	Fixed to Low or Open	I²C communication	High: VDDIO
		Fixed to High	SPI communication	Low: GND

17.2. Description of Register Communication (I²C Communication)

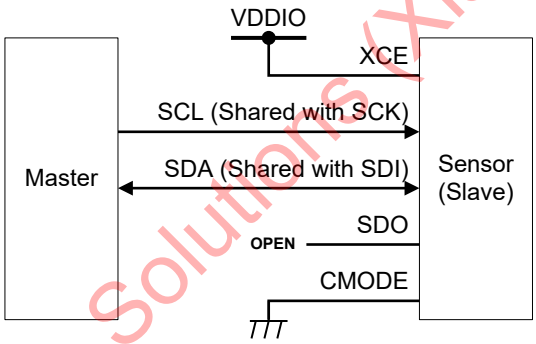


Fig. 17-1 Serial Communication Pin Connections (I²C Communication)

Table 17-2 Description of 17 I²C Communication Pins

Pin name	Pin No.	Remarks
SCL (Shared with SCK)	L12	Serial communication clock input
SDA (Shared with SDI)	K12	Serial communication data I/O
SLASEL2	H12	Slave address selection input
SLASEL1	G12	Slave address selection input
SLASEL0	J11	Slave address selection input

Table 17-3 Supported 17 I²C Communication Modes

Mode	Support	Communication speed
Standard mode	Non-Supported	100 kbps
Fast mode	Supported	400 kbps
Fast mode plus	Non-Supported	1 Mbps

17.2.1. Slave Address

The slave address of the sensor is specified by the SLASEL2, SLASEL1 and SLASEL0 pins. Establish the SLASEL2, SLASEL1 and SLASEL0 pin statuses before canceling the system reset. (Do not switch this pin status during operation.)

Table 17-4 List of Available Slave Addresses

Pin processing L: Low (GND or Open) / H: High (VDDIO)			Slave address								
SLASEL2	SLASEL1	SLASEL0	HEX	MSB	-						LSB
L	L	L	0x1A	0	0	1	1	0	1	0	R/W
L	L	H	0x1B	0	0	1	1	0	1	1	
L	H	L	0x1C	0	0	1	1	1	0	0	
L	H	H	0x1D	0	0	1	1	1	0	1	
H	L	L	0x10	0	0	1	0	0	0	0	
H	L	H	0x20	0	1	0	0	0	0	0	
H	H	L	0x36	0	1	1	0	1	1	0	
H	H	H	0x37	0	1	1	0	1	1	1	

Table 17-5 R/W Transfer Direction

R/W bit	Transfer direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

17.3. Description of Register Setting (SPI Communication)

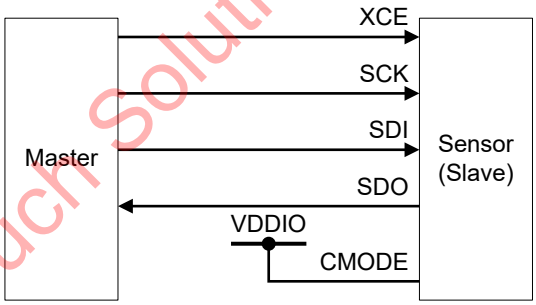


Fig. 17-2 Serial Communication Pin Connections (SPI Communication)

Table 17-6 Description of SPI Communication Pins

Pin name	Pin No.	Remarks
XCE	M12	Serial communication enable input
SCK	L12	Serial communication clock input
SDI	K12	Serial communication data input
SDO	M13	Serial communication data output

When selecting SPI communication clip the SLASEL0/1/2 pin on GND

18. Output Interface

18.1. Description

This section describes the ranging data output modes supported by this sensor.

The following readout modes are supported.

- Line mode max. 21(V) × 576(H) SPAD
- Array mode max. 6(V) × 576(H) SPAD

The following output modes are supported.

- MIPI CSI-2 serial data output 4 Lane, RAW12
- MIPI CSI-2 serial data output 2 Lane, RAW12

18.2. MIPI Transmitter

This section describes the CSI-2 output pins (DMOPA to DMOPD, DMOMA to DMOMD, DMCKP, DMCKM).

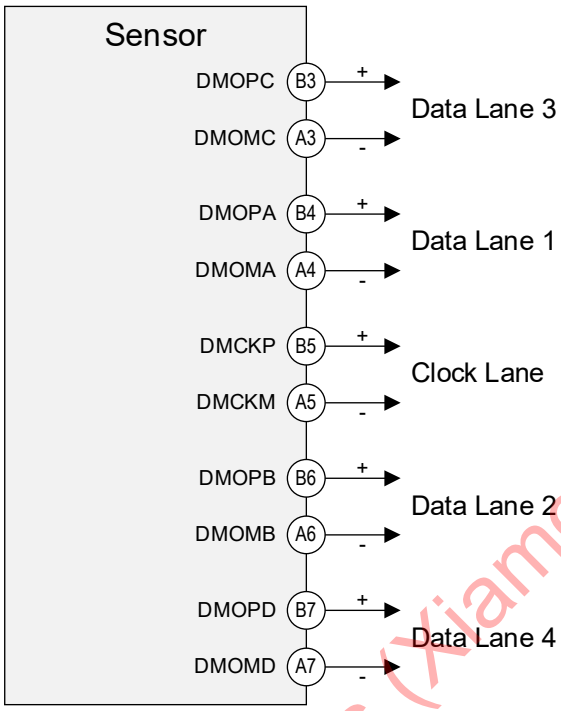


Fig. 18-1 Relationship between Pin Name and MIPI Output Lane

The pixel signals are output on the CSI-2 high-speed serial interface.
Refer to the following MIPI standards.

- MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

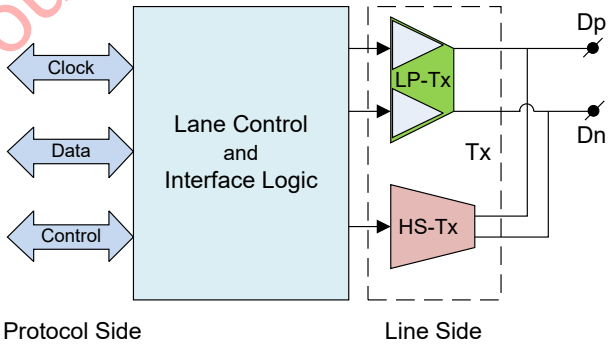


Fig. 18-2 Universal Lane Module Functions

18.3. Frame Format

Each line of each frame is output in the same manner as the CSI-2 General Frame Format. The settings in each packet header are described below. The MIPI output is output as one frame not in F_SYNC units but in slot units (S_SYNC units).

Table 18-1 DATA Type

Header [5:0]	Name	Description
0x00	Frame Start Code	FS line output
0x01	Frame End Code	FE line output
0x2C	RAW12	RAW12 output (Active area)
0x12	Embedded Data	Embedded line output
0x30	Statistics Data	Statistics line output
0x31	Ambient Data	Ambient line output

18.4. Frame Structure

The figure below shows the frame configuration.

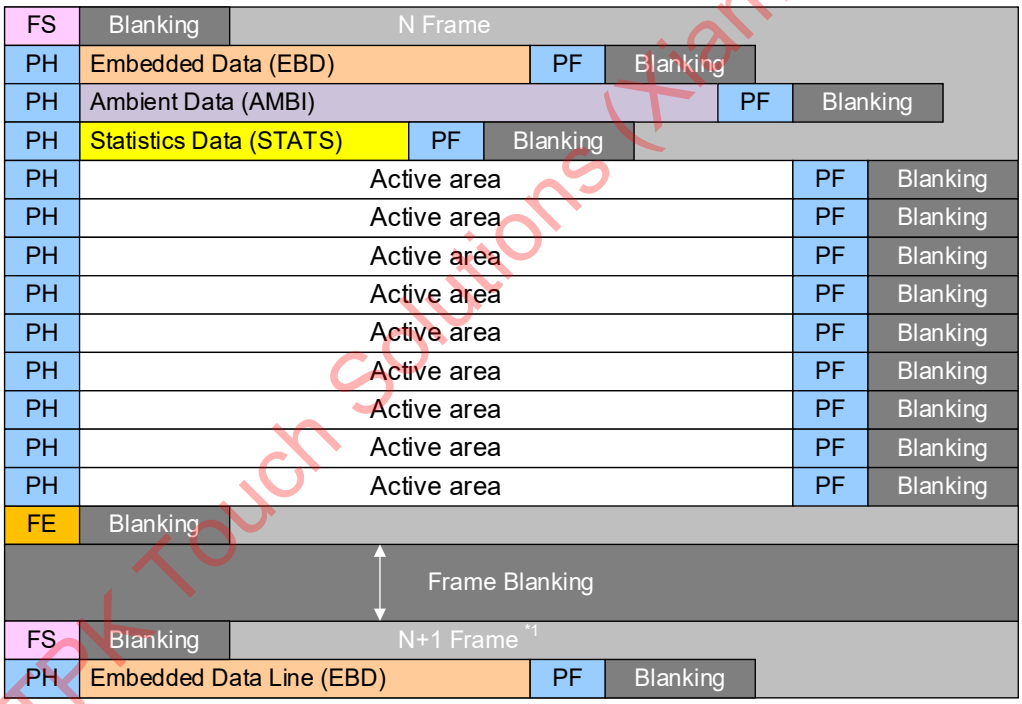


Fig. 18-3 Output Frame Configuration

*1 “N + 1 Frame” means the next slot data.

18.5. CSI-2 Output Format

The output format of this sensor supports the following modes:

- MIPI CSI-2 serial data output 4 Lane, RAW12
- MIPI CSI-2 serial data output 2 Lane, RAW12

The ranging data is output as CSI-2. DMOPA and DMOMA are called the data signals for data lane 1, DMOPB and DMOMB for data lane 2, DMOPC and DMOMC for data lane 3, and DMOPD and DMOMD for data lane 4. In addition, the clock signal is output from DMCKP and DMCKM.
In 2-lane output drive mode, the data is output from data lane 1 and data lane 2.
In 4-lane output drive mode, the data is output from data lane 1, data lane 2, data lane 3 and data lane 4.

An example of RAW12 output is shown below.

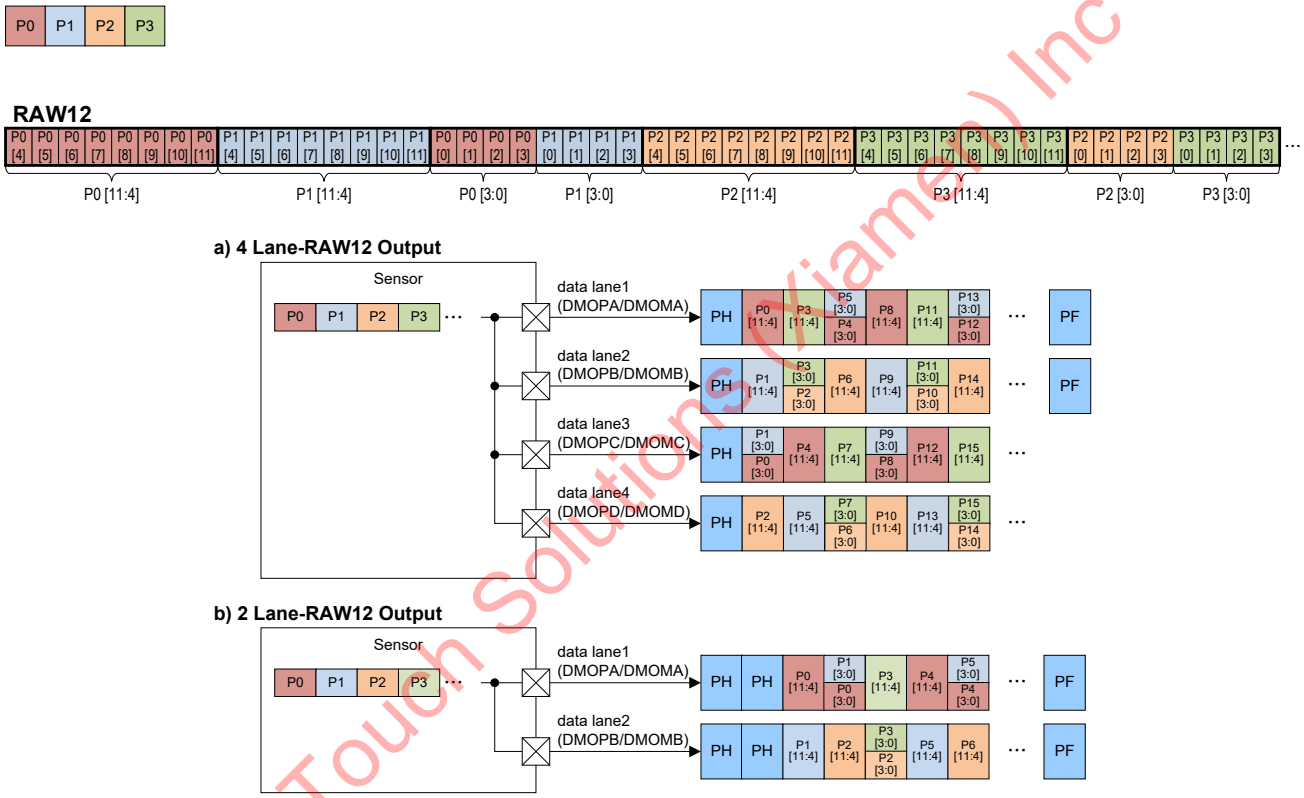


Fig. 18-4 Example of RAW12 Output

19. Operating Modes

19.1. Description

This section describes the ranging data output modes supported by this sensor.

The following operating modes are supported.

- ◆Ranging mode
- ◆Echo mode
- ◆Histogram mode

The minimum slot rates supported in ranging mode are shown below. However, the values noted below are for the MIPI 2 Gbps/lane, 4 lanes use case.

Table 19-1 List of Operating Modes (Ranging Mode)

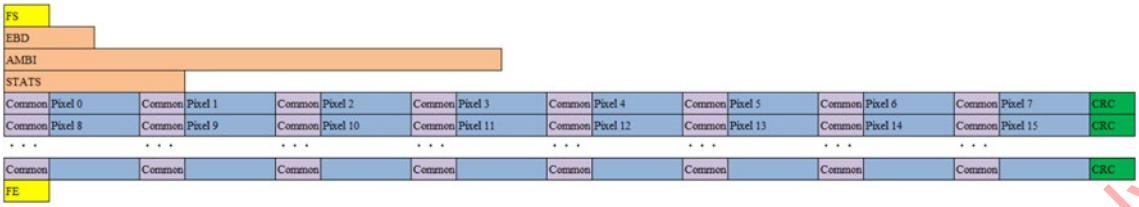
Number of pixels	One Pixel configuration (H × V SPAD)	SPAD on period	TDC	Up Sample	Ranging possible distance	Ranging resolution	Minimum slot rate	Remarks
192 pixels	3 × N	1.000 µs	1 GHz	× 1, × 2coarse	150 m	15 cm	50 µs	Output data needs to be reduced
96 pixels	6 × N	2.024 µs			303 m		50 µs	
48 pixels	12 × N	2.024 µs			303 m		50 µs	
192 pixels	3 × N	2.000 µs	0.5 GHz	× 1, × 2coarse	300 m	30 cm	50 µs	Output data needs to be reduced
96 pixels	6 × N	2.024 µs			303 m		50 µs	
48 pixels	12 × N	2.024 µs			303 m		50 µs	

Prerequisites: Ranging mode, MIPI 2 Gbps/lane, 4 lanes
N = 1 to 21

19.2. Data output Format

The detailed output formats and data in ranging mode, echo mode and histogram mode are described below.

19.2.1. Ranging Mode



*Pixel packing can be selected from 1/4/8/12/16.

Fig. 19-1 Output Format (Ranging Mode)

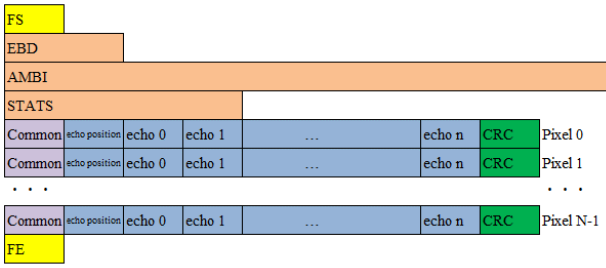
Table 19-2 Detailed Ranging Mode Data

Pixel No.	Pixel information	Echo No.	Output data	Bit accuracy	Bit assignment	Number of bits	On/Off register name
0	Common information	-	Pixel No.	U12	[11:0]	12	G_OUTPUT_HEAD_0
			Echo detection threshold	U12	[11:0]	12	
			Echo judgment threshold 1	U12	[11:0]	12	G_OUTPUT_HEAD_1
			Echo judgment threshold 2	U12	[11:0]	12	
			Bn	U8	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_2
			SUM_Bi	U12	[11:0]	12	
			REF maximum signal strength	U8	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_3
			REF maximum position	U12	[11:0]	12	
			Long-distance maximum signal strength	U8	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_4
			MAX_Bi	U8	{4'b0, [7:0]}	12	
	Individual information	1	Peak signal strength	U12	[11:0]	12	G_OUTPUT_RANGE_PEAK
			Peak position	U12	[11:0]	12	
			Half width start position (integer)	U12	[11:0]	12	G_OUTPUT_RANGE_HALF
			Half width start position (decimal)	U4	{8'b0, [3:0]}	12	
			Half width end position (integer)	U12	[11:0]	12	
			Half width end position (decimal)	U4	{8'b0, [3:0]}	12	
			Echo start position	U12	[11:0]	12	G_OUTPUT_RANGE_ECHO
			Echo end position	U12	[11:0]	12	
			Valley minimum signal strength	U12	[11:0]	12	G_OUTPUT_RANGE_OTHER
			Long-distance peak position	U12	[11:0]	12	
			Peak minimum signal strength	U12	[11:0]	12	G_OUTPUT_RANGE_FLAG
			Various flags [11:8] Echo number [7:6]Reserved [5] Peak value detected multiple times, [4] Last split peak, [3] First split peak, [2] End position error, [1] Start position error, [0] Echo valid	U12	[11:0]	12	
		・・・	・・・		・・・		
		10	Peak signal strength	U12	[11:0]	12	
			・・・		・・・		
			Various flags [11:8] Echo number [7:6]Reserved [5] Peak value detected multiple times, [4] Last split peak, [3] First split peak, [2] End position error, [1] Start position error, [0] Echo valid	U12	[11:0]	12	
	CRC	-	CRC (when packed, only the last pixel of a line is output)	U16	{4'b0,CRC[7:0]}	12	-
		-			{4'b0,CRC[15:8]}	12	-
1		・・・	・・・		・・・		
2		・・・	・・・		・・・		
・・・		・・・	・・・		・・・		
N-1		・・・	・・・		・・・		

N=48,96,192 *Can set the number of echoes per pixel with G_OUTPUT_NUM_ECHO

Detailed ranging mode data

19.2.2. Echo Mode



*Pixel packing can be selected from 1/4/8/12/16.

Fig. 19-2 Output Format (Echo Mode)

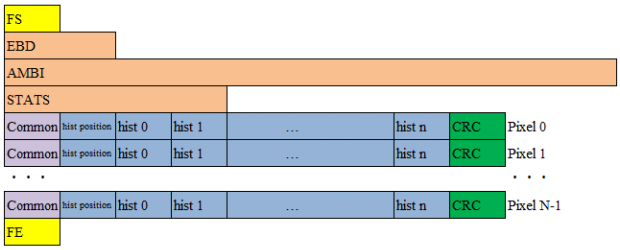
Table 19-3 Detailed Echo Mode Data

Pixel No.	Pixel information	Echo No.	Output data	Bit accuracy	Bit assignment	Number of bits	On/Off register name
0	Common information	-	Pixel No.	U12	[11:0]	12	G_OUTPUT_HEAD_0
			Echo detection threshold	U12	[11:0]	12	
			Echo judgment threshold 1	U12	[11:0]	12	G_OUTPUT_HEAD_1
			Echo judgment threshold 2	U12	[11:0]	12	
			Bn	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_2
			SUM_Bi	U12	[11:0]	12	
			REF maximum signal strength	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_3
			REF maximum position	U12	[11:0]	12	
			Long-distance maximum signal strength	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_4
			MAX_Bi	U8	{4'b0, [7:0]}	12	
	Individual information	1	Echo start position	U12	[11:0]	12	
			Echo end position	U12	[11:0]	12	
			Echo (start+0)	U12	[11:0]	12	
			Echo (start+1)	U12	[11:0]	12	
			· · ·		· · ·		
			Echo (end-1)	U12	[11:0]	12	
			Echo (end-0)	U12	[11:0]	12	
		· · ·	· · ·		· · ·		
		· · ·	· · ·		· · ·		
		· · ·	· · ·		· · ·		
		10	Echo start position	U12	[11:0]	12	
			Echo end position	U12	[11:0]	12	
			Echo (start+0)	U12	[11:0]	12	
			Echo (start+1)	U12	[11:0]	12	
			· · ·		· · ·		
			Echo (end-1)	U12	[11:0]	12	
			Echo (end-0)	U12	[11:0]	12	
	CRC	-	CRC (when packed, only the last pixel of a line is output)	U16	{4'b0,CRC[7:0]}	12	-
		-			{4'b0,CRC[15:8]}	12	-
1		· · ·	· · ·		· · ·		
2		· · ·	· · ·		· · ·		
· · ·		· · ·	· · ·		· · ·		
N-1		· · ·	· · ·		· · ·		

N=48,96,192 When G_OUTPUT_NUMBIN_MODE = 0, the number of output echoes per pixel can be set in G_OUTPUT_NUM_ECHO

Detailed echo mode data

19.2.3. Histogram Mode



*Pixel packing can be selected from 1/4/8/12/16

Fig. 19-3 Output Format (Histogram Mode)

Table 19-4 Detailed Histogram Mode Data

Pixel No.	Pixel information	Echo No.	Output data	Bit accuracy	Bit assignment	Number of bits	On/Off register name
0	Common information	-	Pixel No.	U12	[11:0]	12	G_OUTPUT_HEAD_0
			Echo detection threshold	U12	[11:0]	12	
			Echo judgment threshold 1	U12	[11:0]	12	G_OUTPUT_HEAD_1
			Echo judgment threshold 2	U12	[11:0]	12	
			Bn	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_2
			SUM_Bi	U12	[11:0]	12	
			REF maximum signal strength	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_3
			REF maximum position	U12	[11:0]	12	
			Long-distance maximum signal strength	U12	{4'b0, [7:0]}	12	G_OUTPUT_HEAD_4
			MAX_Bi	U8	{4'b0, [7:0]}	12	
	Individual information	-	Histogram start position	U12	[11:0]	12	G_OUTPUT_HIST_TIMEINFO
			Histogram end position	U12	[11:0]	12	
			Histogram (start+0)	U12	[11:0]	12	
			Histogram (start+1)	U12	[11:0]	12	
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・		
			・・・		・・・	12	
			Histogram (end-1)	U12	[11:0]	12	
			Histogram (end-0)	U12	[11:0]	12	
	CRC	-	CRC (when packed, only the last pixel of a line is output)	U16	{4'b0,CRC[7:0]}	12	-
		-			{4'b0,CRC[15:8]}	12	-
1		・・・	・・・				
2		・・・	・・・				
・・・		・・・	・・・				
N-1		・・・	・・・				

N=48,96,192 *Set output bin with B_STRM_HIST_TIME_START/B_STRM_HIST_TIME_END

Detailed histogram mode data

20. Example of Peripheral Circuits

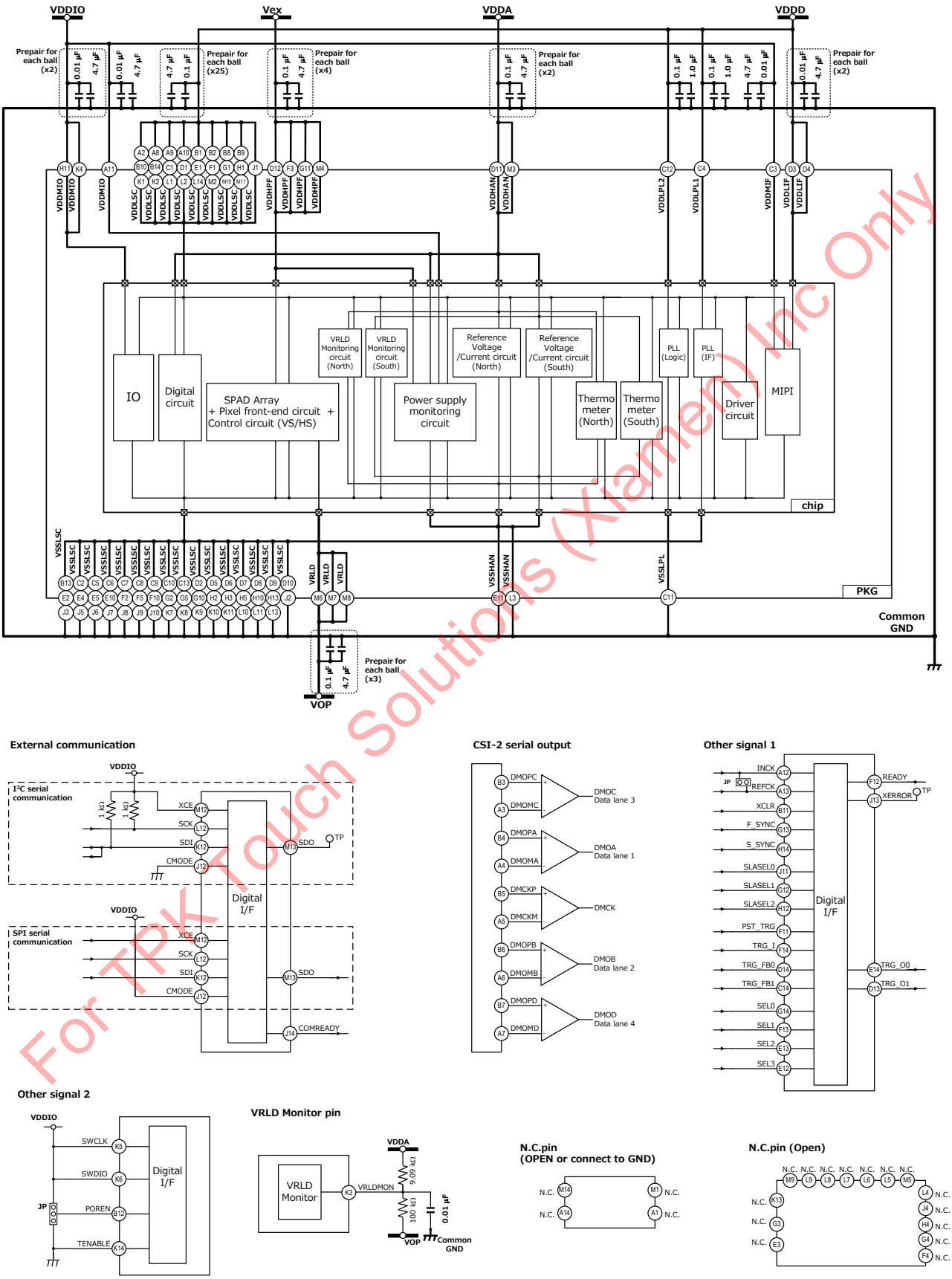


Fig. 20-1 Example of Peripheral Circuits

The power supply smoothing capacitors of 1.0 µF or more connected to the same power supply in the figure,the number of capacitors can be reduced on the assumption that the total capacity value of the capacitors does not decrease.(For example, when bundling the 4.7 µF capacitors for two pins, 4.7 µF × 2 = 9.4 µF, so select a larger value such as 10 µF, etc.).

Capacitors below 0.1 µF in the figure are required to remove high frequency noise, so it is not recommended to reduce or combine them.
A large number of capacitors are mounted, so the recommended size is 0603. However, when selecting the ceramic capacitors to be used, select the components and sizes in consideration of the relationship between the actually applied DC voltages and the actual capacitance values.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third-party and other right due to same.

21. Power-On/Off

21.1. Power-on/off Sequence

The VDDD, VDDA, VDDIO and Vex power supply On/Off sequences order do not matter. the slew rate restriction described below should be observed with regards to the rise from 0 V to the supply voltages (0 % to 100 %) during power-on. There are restrictions on the order of VOP On/Off sequences.
Refer to the Application Note for sequence details. The potential difference between Vex and VOP during Vex start-up should be the SPAD breakdown voltage or less. (*1).

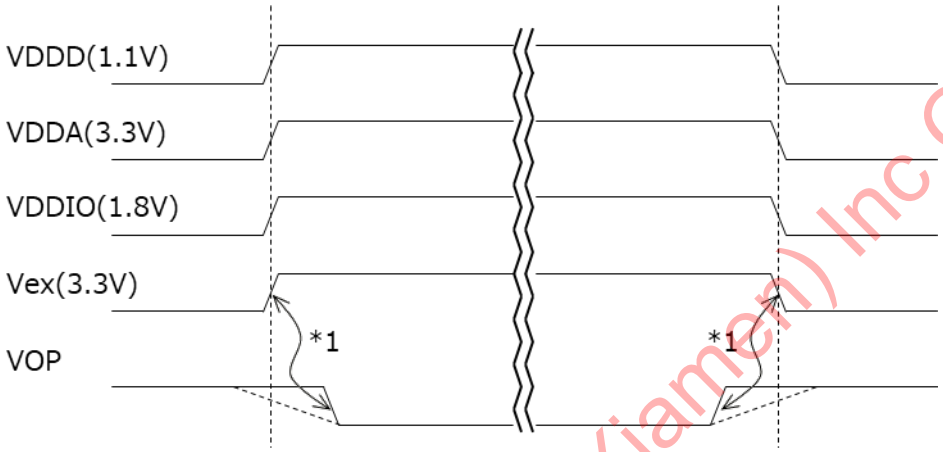


Fig. 21-1 Power-On/Off Sequences

21.2. Slew Rate during Power-On

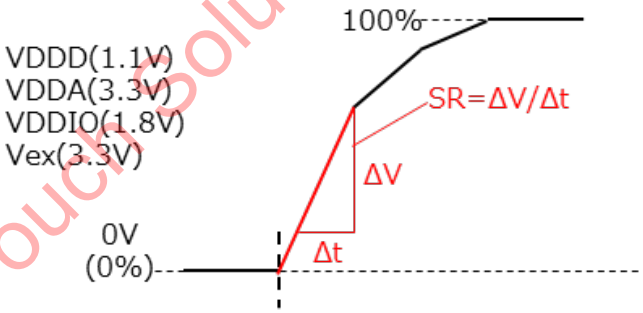


Fig. 21-2 Slew Rate

Table 21-1 Slew Rate

Item	Symbol	Power supply	Min.	Typ.	Max.	Unit	Remarks
Slew rate	SR	VDDD	—	—	25	mV/μs	—
		VDDA	—	—	25	mV/μs	—
		VDDIO	—	—	25	mV/μs	—
		Vex	—	—	25	mV/μs	—

22. Special Note on DCR White Pixel Standards

22.1. Description

After shipment inspection, pixels of the SPAD ToF Depth Sensor may be damaged by radiation effects such as cosmic rays, resulting in dark count rate (DCR) white pixel in images (hereinafter referred to as “DCR white pixel occurrences”).
Under the current state of science and technology, it is impossible to prevent such phenomena from occurring by means of the SPAD ToF Depth Sensor alone.
When using a SPAD ToF Depth Sensor, we recommend that you consider measures to deal with DCR white pixel occurrences, such as setting quality assurance standards for DCR white pixel.
If, within three (3) months after delivery to your company (but only before installation into your product), characteristics of DCR in a SPAD ToF Depth Sensor delivered to your company by Sony Semiconductor Solutions Corporation. or its distributors (collectively, "the Seller") exceeds DCR white pixel standard (Refer to table15-1), the Seller will replace the SPAD ToF Depth Sensor free of charge. Please note that we are unable to extend this support to products that have undergone processing after delivery to your company, products that have been incorporated into your company's products, products that have been shipped from your company to a third party in any form, or products delivered from the Seller to your company more than three months prior.
Except for this offer of free replacement by the Seller, Sony Semiconductor Solutions Corporation. and its distributors assume no responsibility for any DCR white pixel occurrences. Except for this offer of free replacement, any problems arising from DCR white pixel occurrences shall be resolved at your responsibility and expense.

[Reference] Number of DCR white pixel occurrences per year

Below is the data on the projected annual number of DCR white pixel occurrences in buildings 124 m above sea level in Kumamoto Prefecture, Japan.
We recommend that you consider setting quality assurance standards that correspond to the annual number DCR white pixel occurrences.
This data is an estimated number of occurrences calculated according to the structure and electrical characteristics of each device based on past field tests. This data is provided for your reference only and does not constitute part of the SPAD ToF Depth Sensor specification.

Annual occurrence of DCR white pixel: 1.35 (Tj = 85 °C, element units)

Note 1: Indicates the number of DCR white pixel occurrences per year of inactivity.

Note 2: The annual number of DCR white pixel occurrences varies depending on the environment of the SPAD ToF Depth Sensor storage location (altitude, geomagnetic latitude, structure of the building, etc.) and the time of year (influence of solar activity). In addition, statistical errors must be considered.
This data should therefore be understood as an example of experimental data at a specific time and in a specific environment.

Note 3: This data must not be misinterpreted as a guarantee of the upper limit on the number of DCR white pixel occurrences per year.

23. Marking

23.1. Alignment mark

Fig. 23-1 shows Alignment mark.

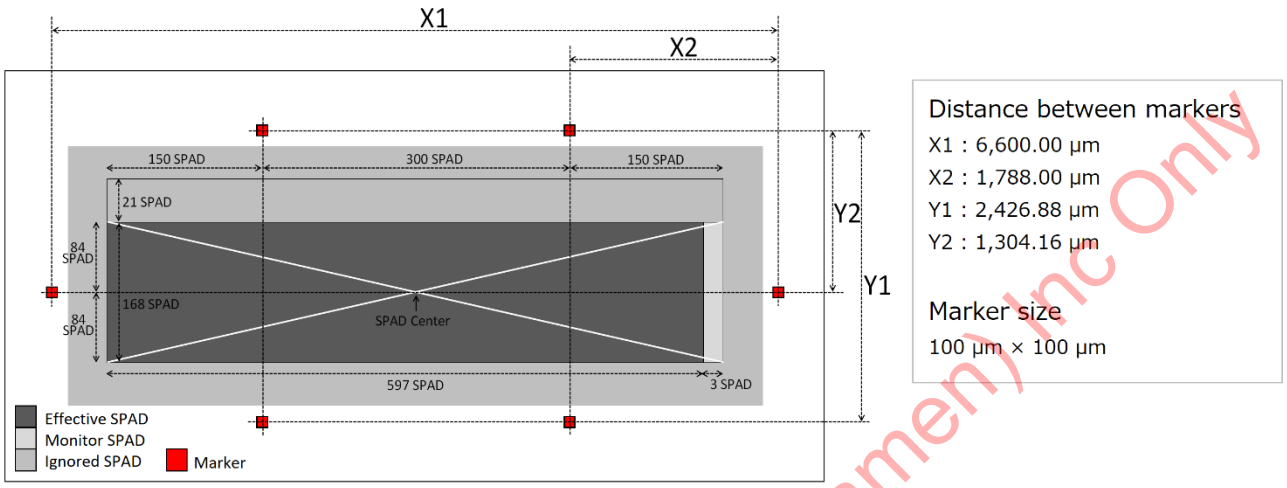


Fig. 23-1 Alignment mark

total 6 markers are placed, 2 on the top and 2 on the bottom and 1 on the left and right with respect to the center of pixel.
The top and bottom positions of the markers are placed one above and one below the 150SPAD positions from both the left and right sides in the horizontal direction (597 SPAD).
The left and right positions of the markers are placed one above and one below the 84SPAD positions from both the top and bottom sides in the vertical direction (168 SPAD).

23.2. Mark on the back of the chip

Fig. 23-2 shows Mark on the back of the chip (Bottom View).
In the figure, the A1.pin is located at the top left.

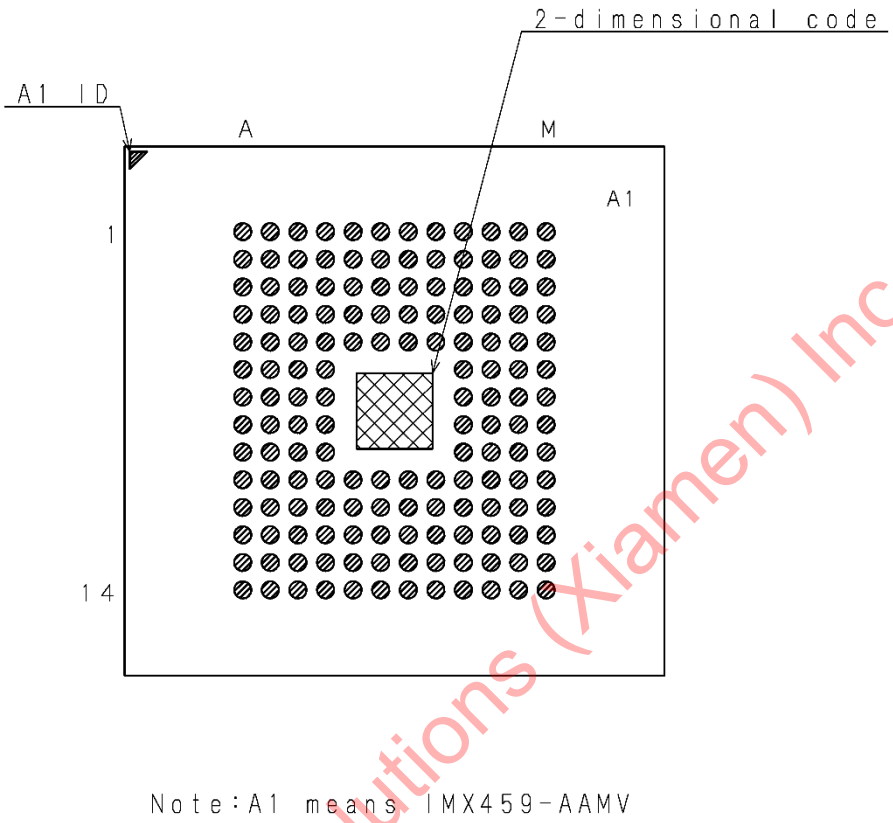


Fig. 23-2 Mark on the back of the chip (Bottom View)

Refer to "8. Optical Center" for the positional relationship between the PKG center and the pixel center.

24. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

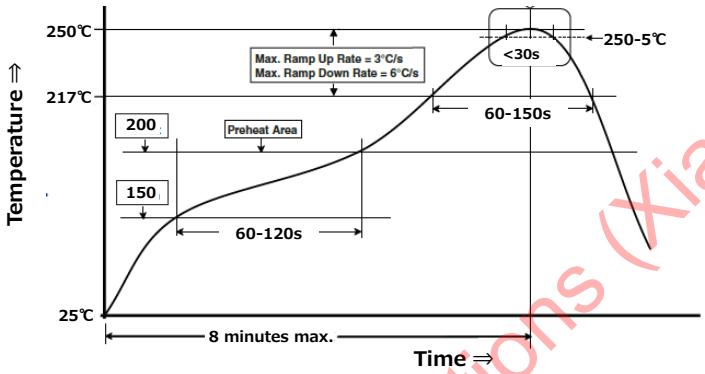
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering (*In conformance with J-STD-020E)

Profile Feature	Profile
Preheat Temperature Min.	150℃
Preheat Temperature Max.	200℃
Preheat Time from 150 to 200℃	60-120 seconds
Ramp-up rate 217 to 250℃	3℃ / second max.
Liquidus temperature	217℃
Time maintained above 217℃	60-150 seconds
Peak package body temperature	250℃
Time within 5℃ of the peak temperature	<30 seconds
Ramp-down rate 250 to 217℃	6℃ / second max.
Time 25℃ to peak temperature	8 minutes max.



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 250 °C.

(b) Perform the reflow soldering maximum three times.

(c) Finish reflow soldering within 168 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 60 % RH or less after unsealing the package.

(d) If more than 168 h have elapsed since the degassed packing was unsealed, perform once at 125 °C for 24 h. Perform baking within one month.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods.

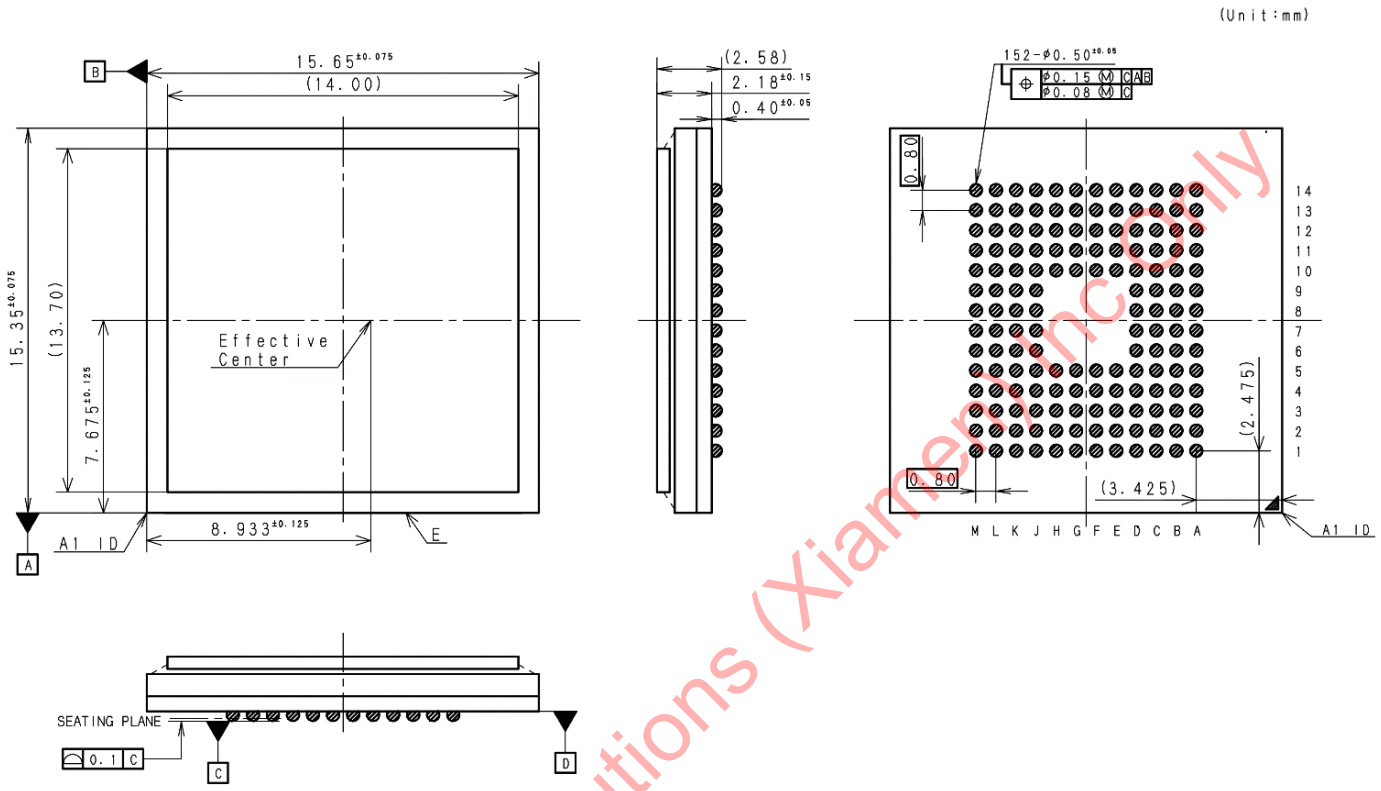
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

25. Package Outline

Fig. 25-1 shows Package Outline.
In the package diagram (Top View) on the left, A1.pin is located at the bottom left.
In the package diagram (Bottom View) on the right, A1.pin is located at the bottom right.



1) The rotation angle of the effective image area relative to "E" is ±1°
2) The height from the bottom "D" to the effective image area is 1.245±0.1
3) The tilt of the effective image area relative to the bottom "D" is less than 0.05
4) The thickness of the seal glass is 0.5
5) Solder Ball Material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)
6) Glass : Both sides AR coat

PACKAGE STRUCTURE

CLASSIFICATION	BGA
TREATMENT MATERIAL	Sn-3.0 Ag-0.5Cu
PIN NUMBER	152Pin
PACKAGE WEIGHT(Typ.)	0.95g
DRAWNG NUMBER	AS-C115(E)

Fig. 25-1 Package Outline

Refer to "8. Optical Center" for the positional relationship between the PKG center and the pixel center.

26. Open Source Software License

27. Revision History

Date	Revision	Chapter	Description
2020/5/1	0.001	-	Initial version
2020/6/18	0.003	11	Pin Configuration described
		12	VSSLPL1 removed from examples in 12. Pin Description Modes after merging VSSLPL1 -> VSSLSC
		19	VSSLPL1 removed from examples in 19. Operating Modes after merging VSSLPL1 -> VSSLSC
		23	Package Outline updated
2020/11/26	0.004	8	8. Optical Center updated
		9	9. SPAD Configuration updated
		10	10. Block Diagram Update
		13.2	13.2.4 to 7 Low Active waveforms added (PST_TRG, SEL/TRG_I, TRG_FB, TRG_O)
			13.2.8 to 11 Newly added (F_SYNC/S_SYNC, COMREADY/READY, XERROR, STOUT0/1)
		13.3	13.3. Current Consumption Update
		15	15. Characteristics updated
		16	16. Example of Spectral Sensitivity Characteristics added
		22	22. Special Note on DCR Defect Standards added
		23	Package Outline updated
2021/12/22	0.005	—	Title Renamed SPAD depth sensor to SPAD ToF Depth Sensor
		1	1. Description and Usage Renamed SPAD depth sensor to SPAD ToF Depth Sensor
		3	3. Device Structure Renamed SPAD depth sensor to SPAD ToF Depth Sensor
		13.1	DC Characteristics XCLR is changed
		13.2.1 to 13.2.12	Changed chapters 13.1.1. - 13.1.12. from chapter 13.2.1. - chapter 13.2.12.
		13.3	Current consumption is updated
		15	Definition of VBD is added
			Table15-1 List of Characteristics is updated
		18.1	Array mode max 21V→6V
		19.1	Table 19-1 Minimum slot rate is changed
		22.1.	22.1. Description Renamed SPAD depth sensor to SPAD ToF Depth Sensor
		23.1	Alignment mark is added
		24	Notes on Handing is updated
		25	25. Package Outline updated
2022/7/8	0.006	1	1. Description and Usage is updated.
		4	Absolute Maximum Ratings is updated (-24.5V to -26.0V)
		5	Recommended device conditions VDDD 1.0V to 1.05V
		6	Description updated
		8	8. Optical Center updated
		12	12. Pin Description is updated
		13.2.2	REFCK clock frequency is corrected.
		13.2.3	XCLR Threshold level is updated
			Tr/Tf Max value is changed (5ns to 100ns)
		13.2.12	Table 13-17 I^2C Communication AC Timing is updated
		13.3	Current consumption is updated
		15	Table 15-1 List of Characteristics is updated
			Fig. 15-1 SPAD quench recharge waveform and readout circuit is updated
		17.2	Table 17-6 Description of SPI Communication Pins is updated
		19.1	Table 19-1 List of Operating Modes (Ranging Mode) is updated
		19.2.1	Fig. 19-1 Output Format (Ranging Mode) is updated
		19.2.2	Fig. 19-2 Output Format (Echo Mode) is updated
		19.2.3	Fig. 19-3 Output Format (Histogram Mode) is updated
		20	Fig. 20-1 Example of Peripheral Circuits is updated

		22	22. Special Note on DCR Defect Standards is updated
		23.1	Fig. 23-1 Alignment mark is updated
		23.2	Fig. 23-2 Mark on the back of the chip (Bottom View) is updated
		25	Fig. 25-1 Package Outline is updated
2023/04/28	1.0.0	13.3	Array mode description is added
		15	Table 15 1 List of Characteristics is updated
		15	Fig15-3 Inter-element output skew (all pixels) added
		18.5	Fig18-4 is updated
		19.1	Table 19-1 x2 fine row deletion
		22.1	22.Special Note on DCR white pixel Standards is updated
2023/08/17	1.0.1	7	Chapter and Page number is updated
		11	Table 11-1 Pin Position is updated
		12	Table 12-1 List of Pins is updated
		13.2.11	SPAD Test Monitor Output (STOUT0/STOUT1) Chapter is deleted
		14	Table 14-1 Input/Output Pins Equivalent Circuits is updated
		20	Fig. 20-1 is updated
		-	Page number updated Chapter number updated Fig number updated Table number updated
2023/11/29	1.0.2	8	Fig. 11 1 Pin Configuration (Top View) is updated
		36	Fig. 19 2 Output Format (Echo Mode) is updated
		37	Fig. 19 3 Output Format (Histogram Mode) is updated
		46	Fig. 25 1 Package Outline is updated