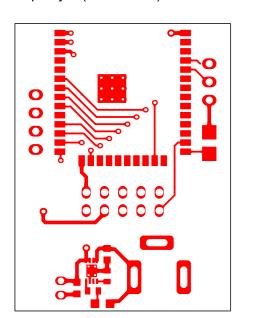
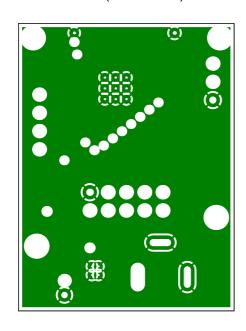
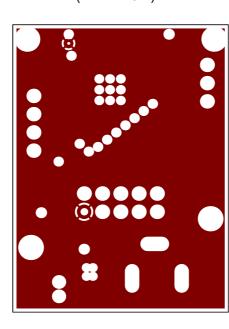
Top Layer (Scale 1.9:1)



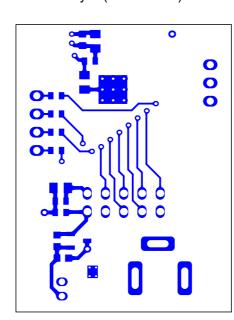
GroundPlane (Scale 1.9:1)



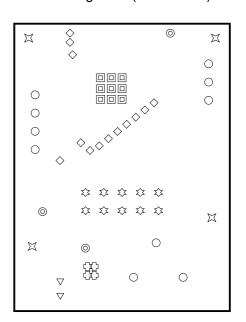
VccPlane (Scale 1.9:1)



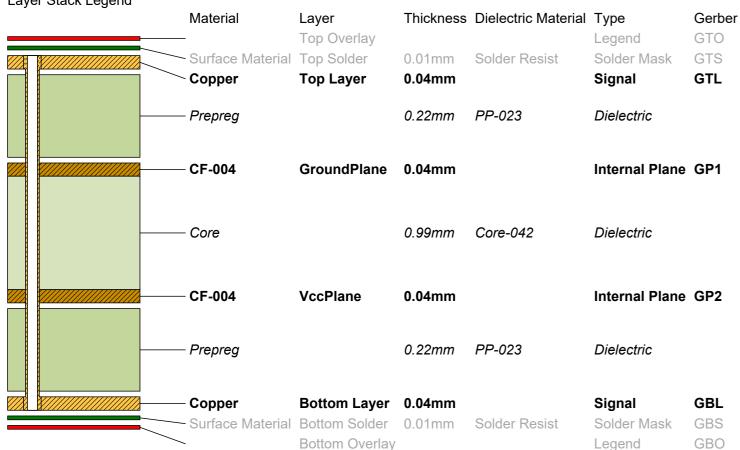
Bottom Layer (Scale 1.9:1)



Drill Drawing View (Scale 1.9:1)



Layer Stack Legend



Total thickness: 1.59mm

Drill Table

	Symbol	Count	Hole Size	Plated	Hole Tolerance
	¢	4	0.25mm	Plated	
		9	0.30mm	Plated	
	\Diamond	13	0.38mm	Plated	
	0	3	0.51mm	Plated	
	∇	2	0.90mm	Plated	
ı	0	10	1.00mm	Plated	
	₿	10	1.02mm	Plated	
	Ħ	4	2.50mm	Plated	
		55 Total			

TECNOLOGIA

	WF TECNOLOGIA	Revisão	Data	Responsável	Histórico
	Natan Figueiredo +55 41 99558-4388	R00	17/02/202	Natan MF	=HIST01
	eng.figueiredo@gmail.com				=HIST02
GIA	Projeto Motherboard Bracelet				=HIST03
	Elaboração Roger Aprovação Marlio Layout Natan Figueiredo				
	Código Revisão R00 Folha 1/1				=HIST04
	Data 4/4/2024 Horário 2:35 AM Tamanho A3				
	Arquivo Y:\GIT\WF_Tecnologia\Roger_Lakoski_Mestrado\RL_Motherboard_Bra	celet\Moth	erboard_Bra	celet_Fabricati	ion.PCBDwf