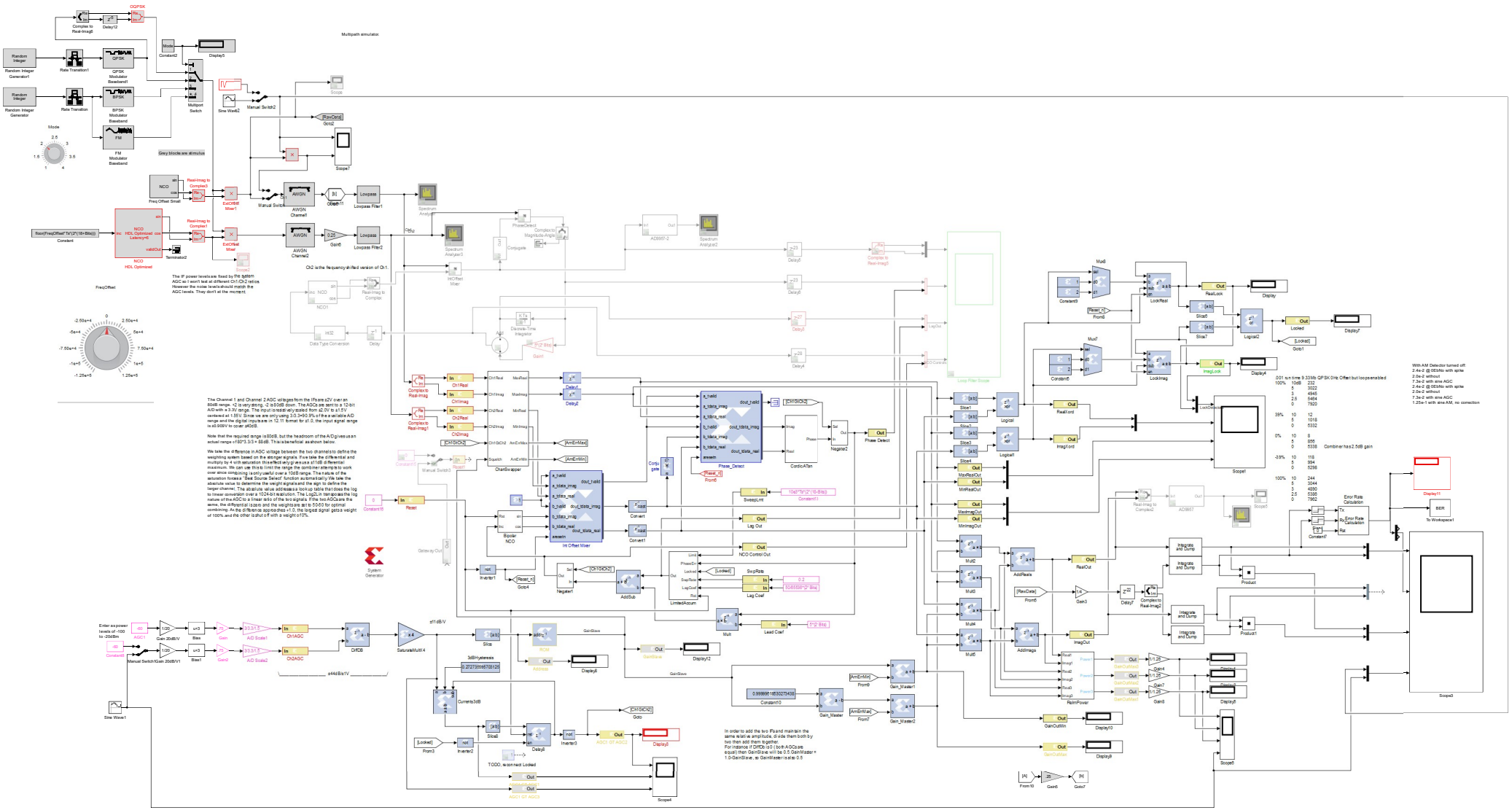
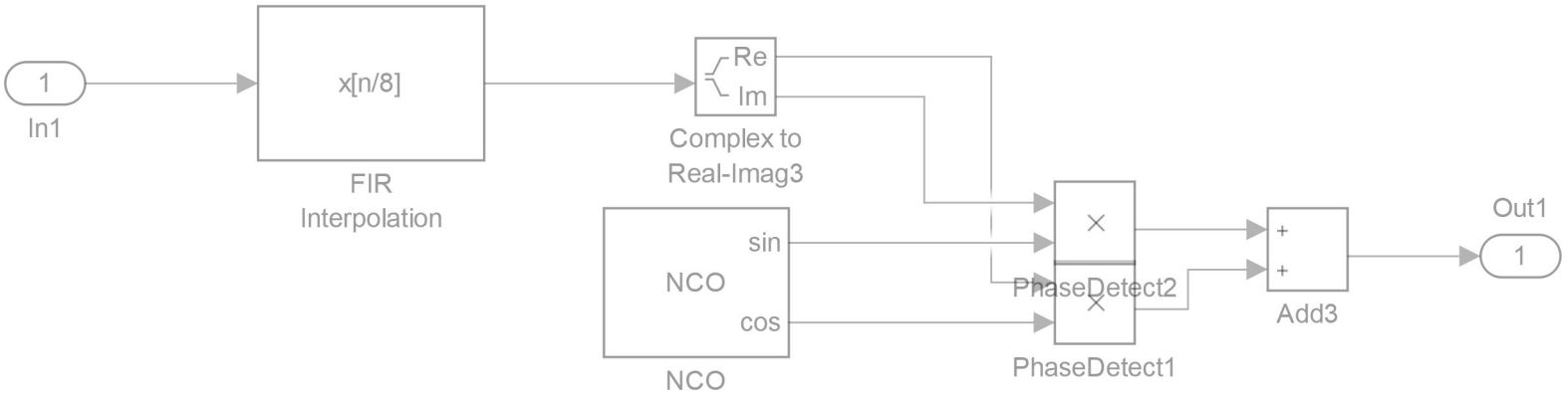
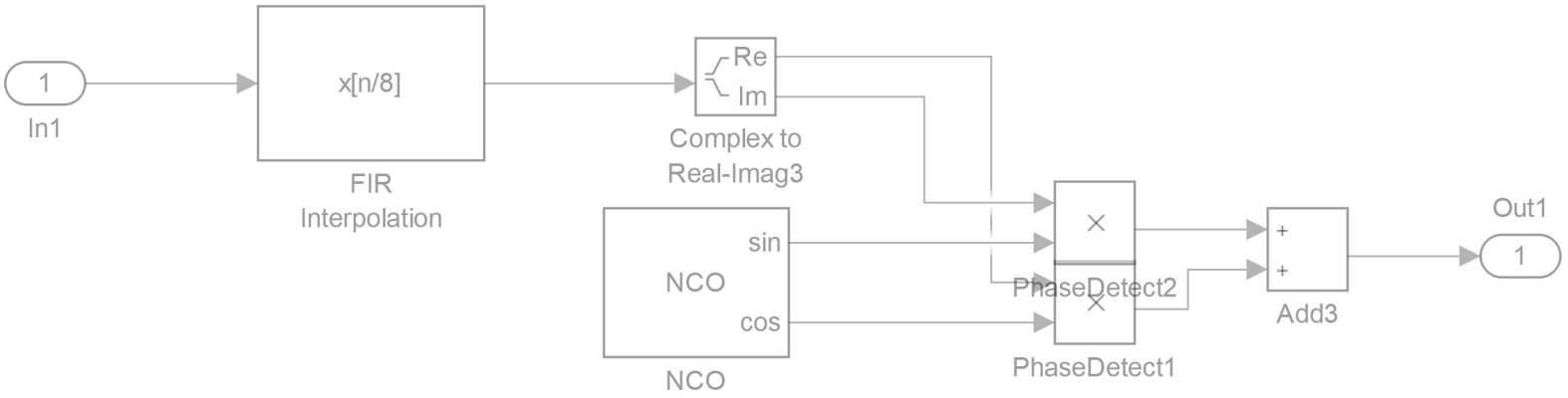
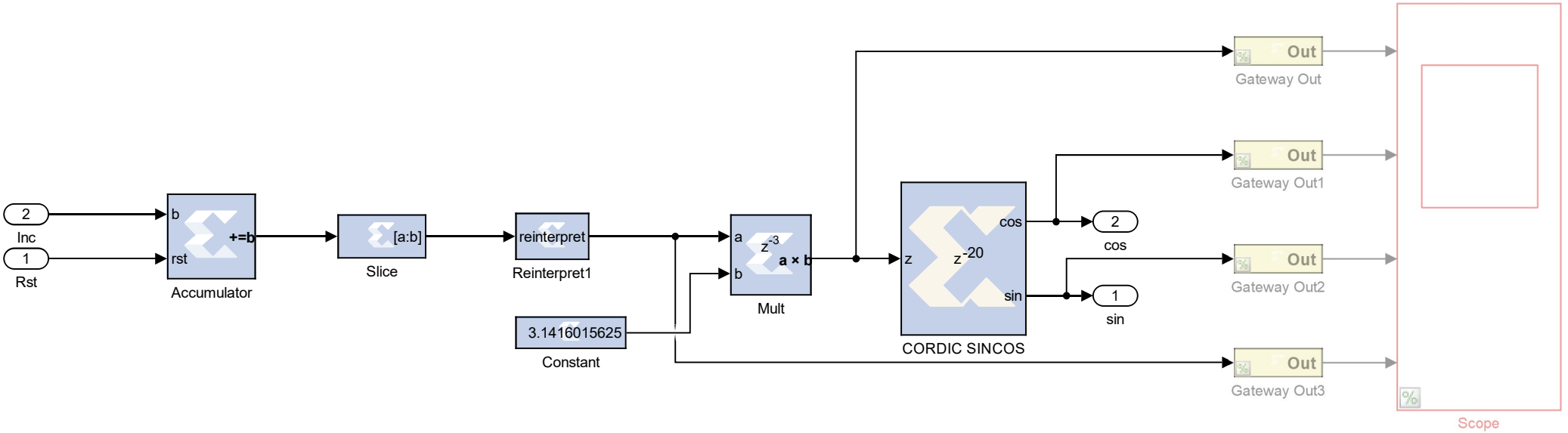
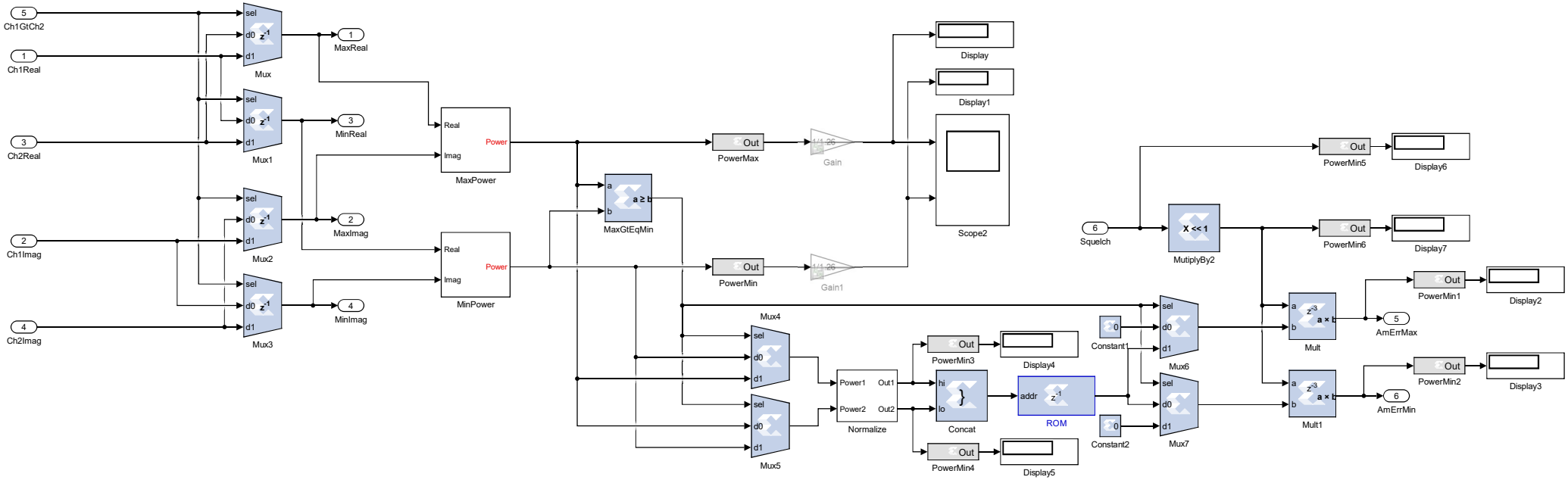


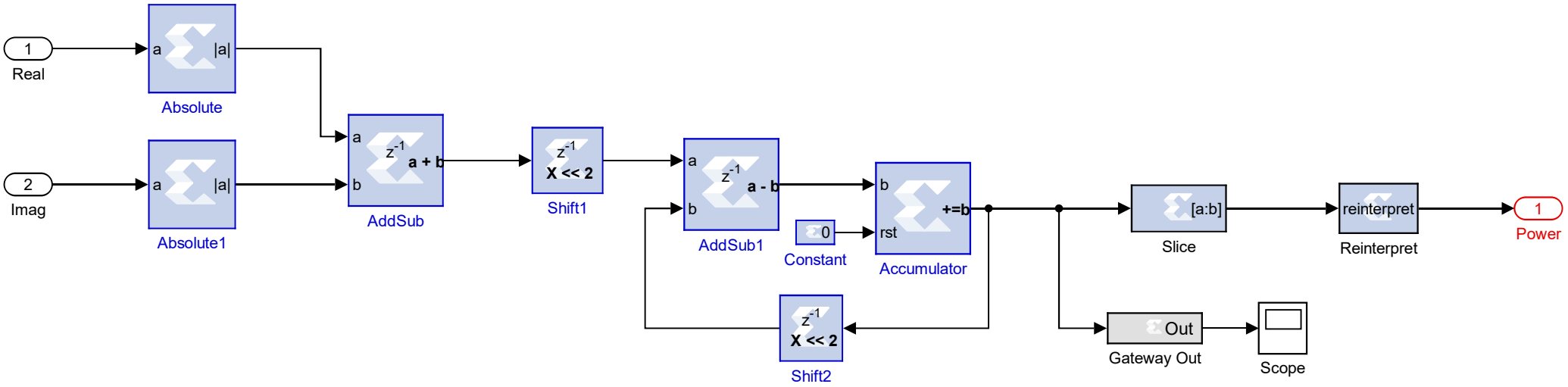
Multipath simulator
Grey blocks are stimulus
Ch2 is the frequency shifted version of Ch1.
The IF power levels are fixed by the system AGC so I won't test at different Ch1/Ch2 ratios. However the noise levels should match the AGC levels. They don't at the moment.
The Channel 1 and Channel 2 AGC voltages from the IFsave s2V over an 80dB range. +2 is very strong, -2 is 80dB down. The AGCs are sent to a 12-bit A/D with a 3.3V range. The input is resistively scaled from ±2.0V to ±1.5V centered at 1.55V. Since we are only using 3/3.3=90.9% of the available A/D range and the digital inputs are in 12.11 format for ±1.0, the input signal range is ±0.909V to cover ±40dB.
Note that the required range is 80dB, but the headroom of the A/D gives us an actual range of 80*3.3/3 = 88dB. This is beneficial as shown below.
We take the difference in AGC voltage between the two channels to define the weighting system based on the stronger signals. If we take the differential and multiply by 4 with saturation this effect only gives us a ±1dB differential maximum. We can use this to limit the range the combiner attempts to work over since combining is only useful over a 10dB range. The nature of the saturation forces a "Best Source Select" function automatically. We take the absolute value to determine the weight signals and the sign to define the larger channel. The absolute value addresses a look-up table that does the log to linear conversion over a 1024-bit resolution. The Log2Lin transposes the log nature of the AGC to a linear ratio of the two signals. If the two AGCs are the same, the differential is zero and the weights are set to 50/50 for optimal combining. As the difference approaches +1.0, the largest signal gets a weight of 100% and the other is shut off with a weight of 0%.
In order to add the two IFs and maintain the same relative amplitude, divide them both by two then add them together.
For instance if DifDb is 0 (both AGCs are equal) then GainSlave will be 0.5 GainMaster = 1.0-GainSlave, so GainMaster is also 0.5
With AM Detector turned off:
2.4e-2 @ 0EbNo with spike
2.0e-2 without
7.3e-2 with sine AGC
2.4e-2 @ 0EbNo with spike
2.0e-2 without
7.3e-2 with sine AGC
1.25e-1 with sine AM, no correction
Combiner has 2.5dB gain

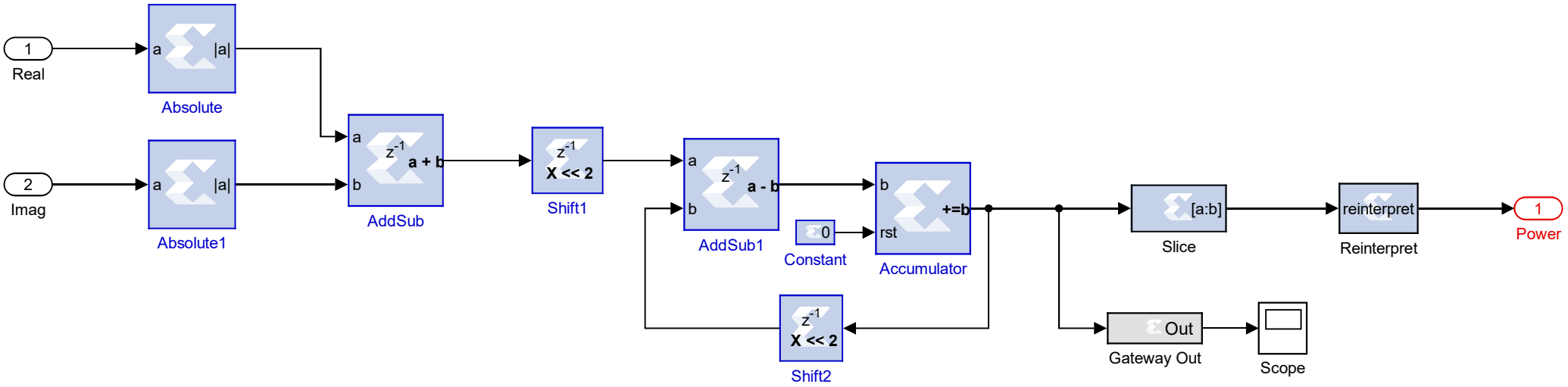

1
In1
x[n/8]
FIR
Interpolation
Re
Im
Complex to
Real-Imag3
sin
NCO
cos
NCO
PhaseDetect2
PhaseDetect1
Add3
Out1
1

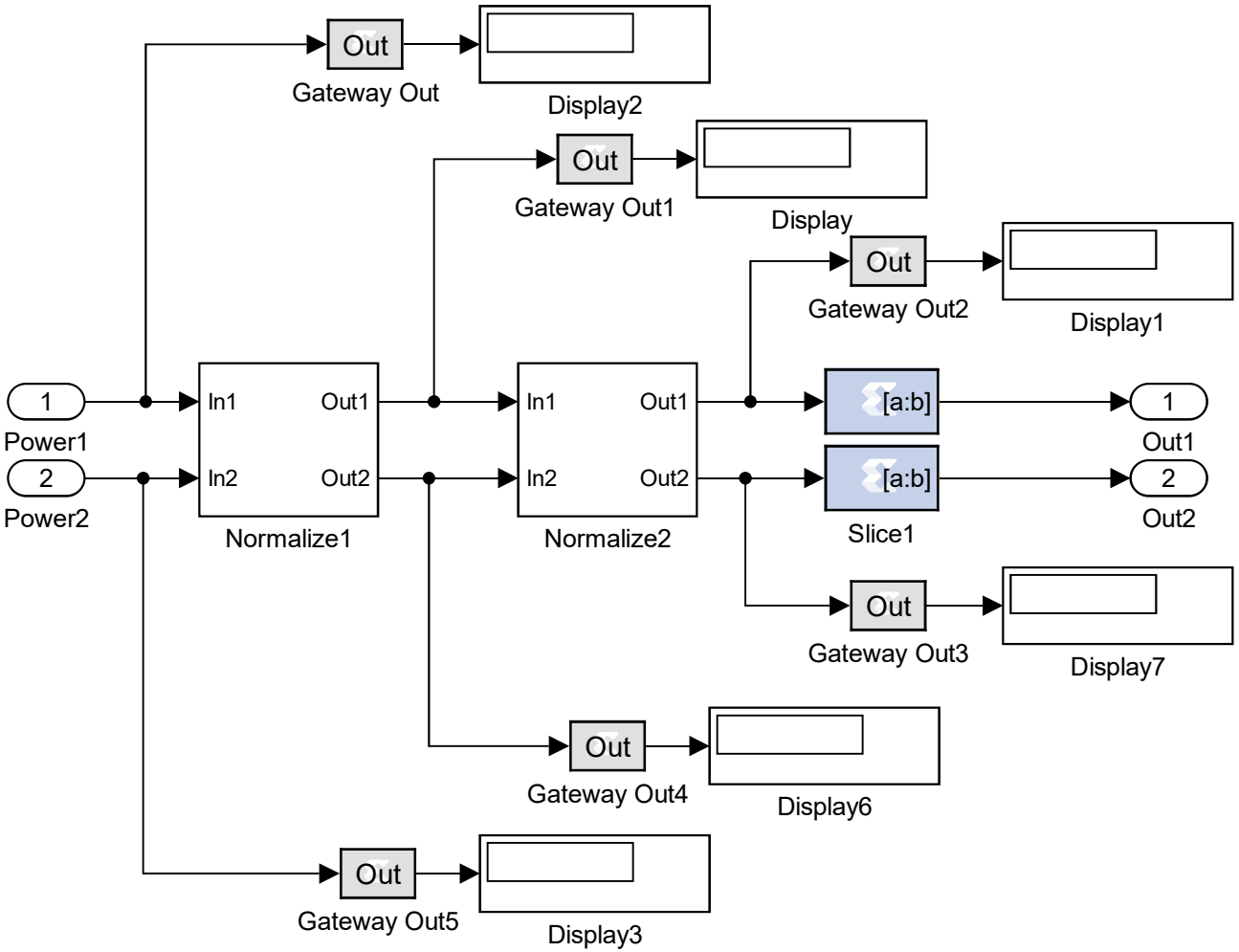

1
In1
x[n/8]
FIR
Interpolation
Re
Im
Complex to
Real-Imag3
sin
NCO
cos
NCO
PhaseDetect2
PhaseDetect1
Add3
Out1
1

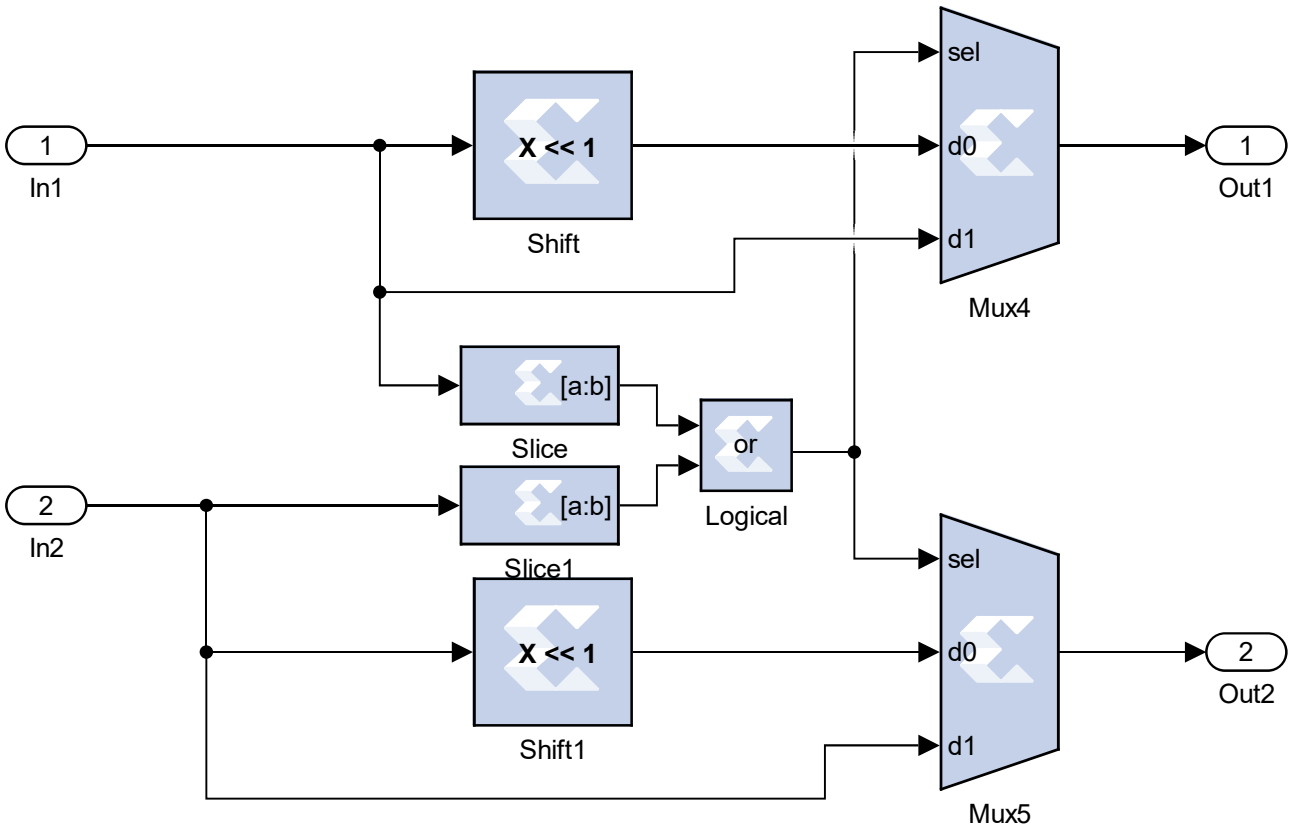

2
Inc
1
Rst
b
rst
+=b
Accumulator
[a:b]
Slice
reinterpret
Reinterpret1
3.1416015625
Constant
a
b
z-3
a × b
Mult
z
z-20
cos
sin
CORDIC SINCOS
2
cos
1
sin
Out
Gateway Out
Out
Gateway Out1
Out
Gateway Out2
Out
Gateway Out3
Scope

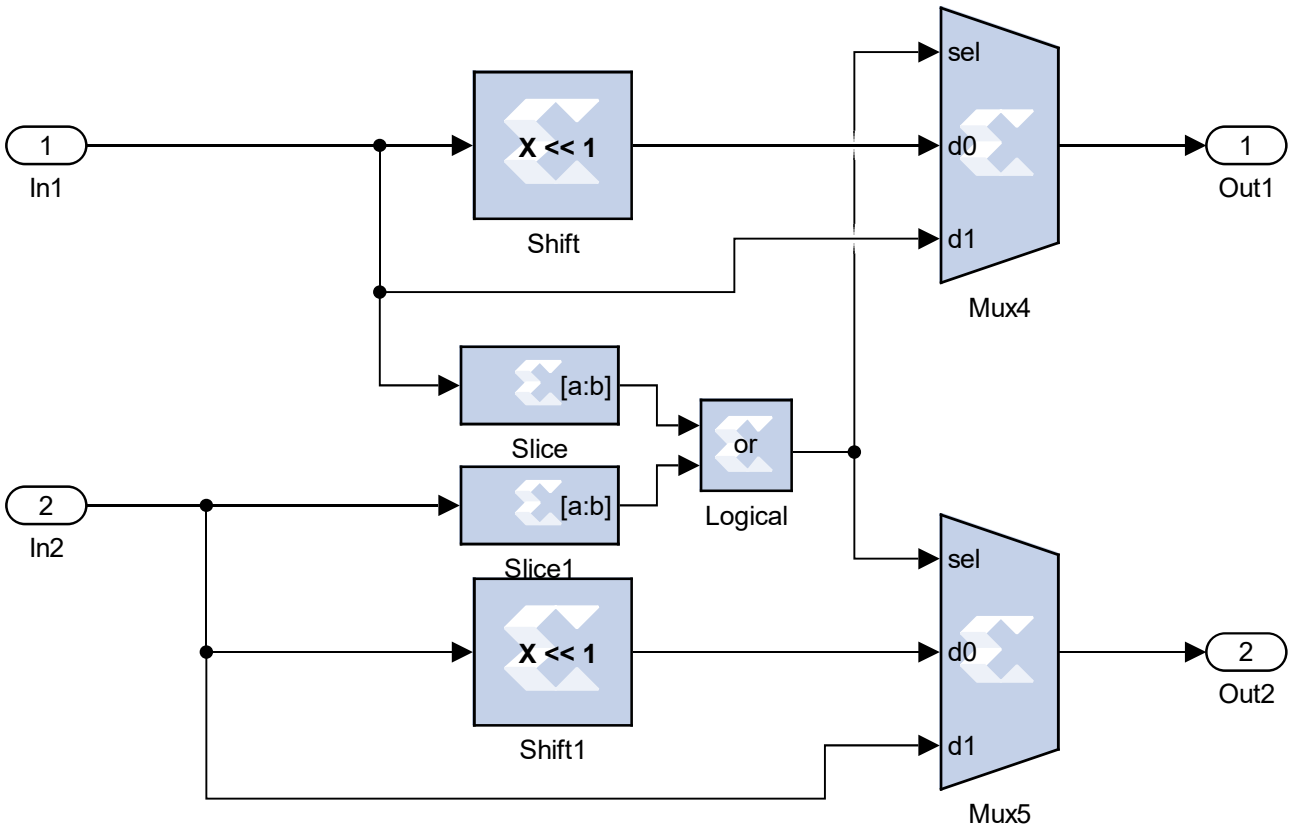

5
Ch1GtCh2
1
Ch1Real
3
Ch2Real
2
Ch1Imag
4
Ch2Imag
sel
d0
d1
Mux
Mux1
Mux2
Mux3
1
MaxReal
3
MinReal
2
MaxImag
4
MinImag
Real
Imag
Power
MaxPower
MinPower
a
b
a ≥ b
MaxGtEqMin
Out
PowerMax
PowerMin
Gain
Gain1
Display
Display1
Scope2
Mux4
Mux5
Power1
Power2
Out1
Out2
Normalize
PowerMin3
PowerMin4
Display4
Display5
hi
lo
Concat
addr
ROM
0
Constant1
Constant2
Mux6
Mux7
6
Squelch
X << 1
MutiplyBy2
PowerMin5
PowerMin6
PowerMin1
PowerMin2
Display6
Display7
Display2
Display3
Mult
Mult1
5
AmErrMax
6
AmErrMin

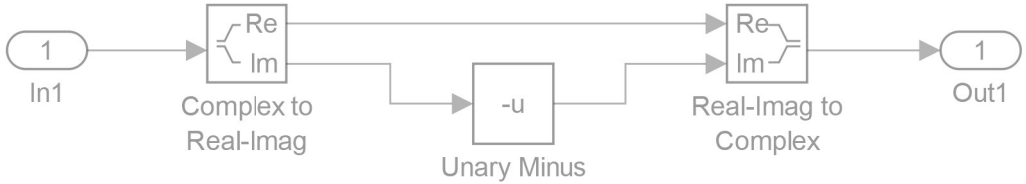

1
Real
a
|a|
Absolute
2
Imag
a
|a|
Absolute1
a
b
z-1
a + b
AddSub
z-1
X << 2
Shift1
a
b
z-1
a - b
AddSub1
0
Constant
b
rst
+=b
Accumulator
z-1
X << 2
Shift2
[a:b]
Slice
reinterpret
Reinterpret
1
Power
Out
Gateway Out
Scope


1
Real
a
|a|
Absolute
2
Imag
a
|a|
Absolute1
a
b
z-1
a + b
AddSub
z-1
X << 2
Shift1
a
b
z-1
a - b
AddSub1
0
Constant
b
rst
+=b
Accumulator
z-1
X << 2
Shift2
[a:b]
Slice
reinterpret
Reinterpret
1
Power
Out
Gateway Out
Scope

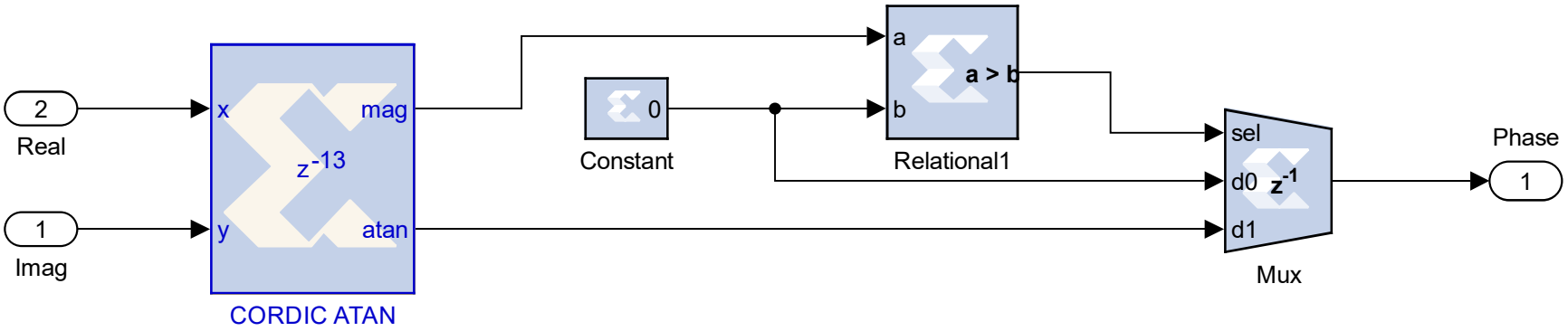

Out
Gateway Out
Display2
Out
Gateway Out1
Display
Out
Gateway Out2
Display1
1
Power1
2
Power2
In1
In2
Out1
Out2
Normalize1
In1
In2
Out1
Out2
Normalize2
[a:b]
[a:b]
Slice1
1
Out1
2
Out2
Out
Gateway Out3
Display7
Out
Gateway Out4
Display6
Out
Gateway Out5
Display3

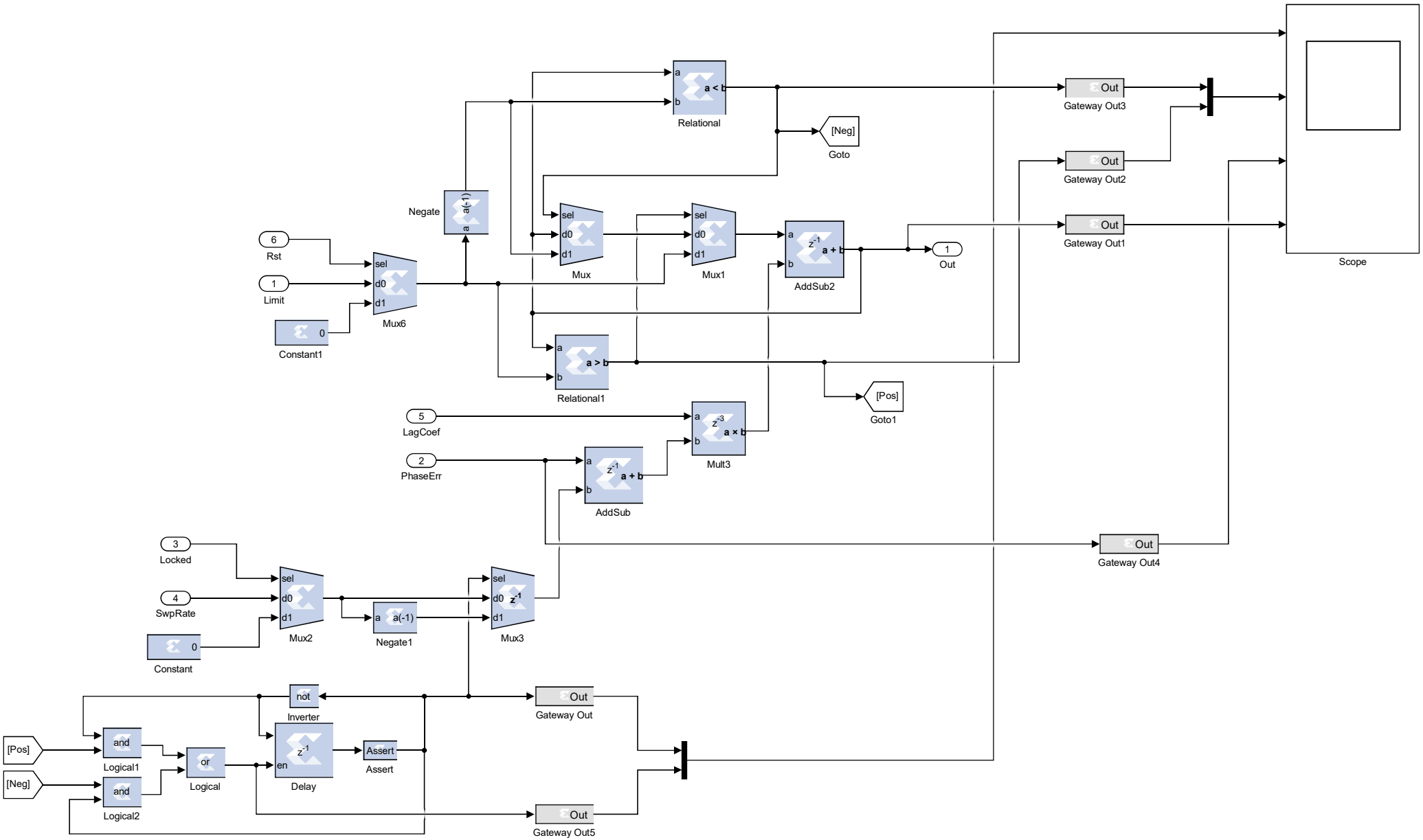

1
In1
X << 1
Shift
sel
d0
d1
Mux4
1
Out1
[a:b]
Slice
or
Logical
2
In2
[a:b]
Slice1
X << 1
Shift1
sel
d0
d1
Mux5
2
Out2

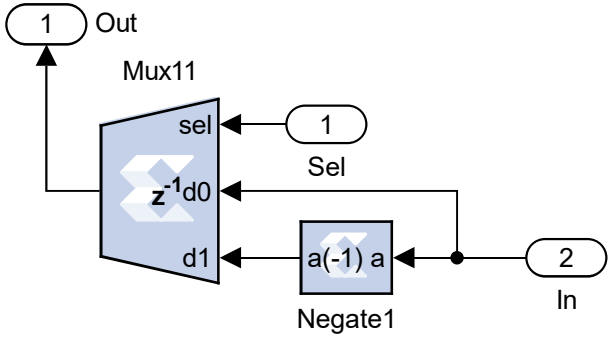

1
In1
X << 1
Shift
sel
d0
d1
Mux4
1
Out1
[a:b]
Slice
or
Logical
2
In2
[a:b]
Slice1
X << 1
Shift1
sel
d0
d1
Mux5
2
Out2

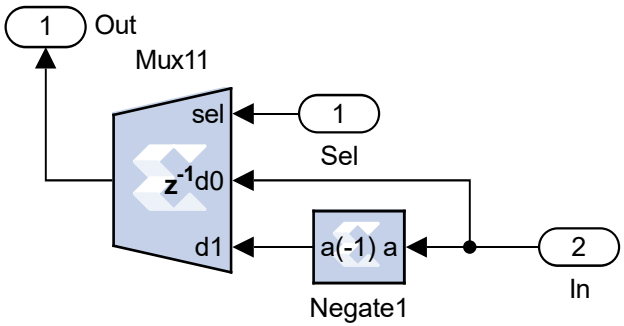

1
In1
Re
Im
Complex to
Real-Imag
-u
Unary Minus
Re
Im
Real-Imag to
Complex
1
Out1

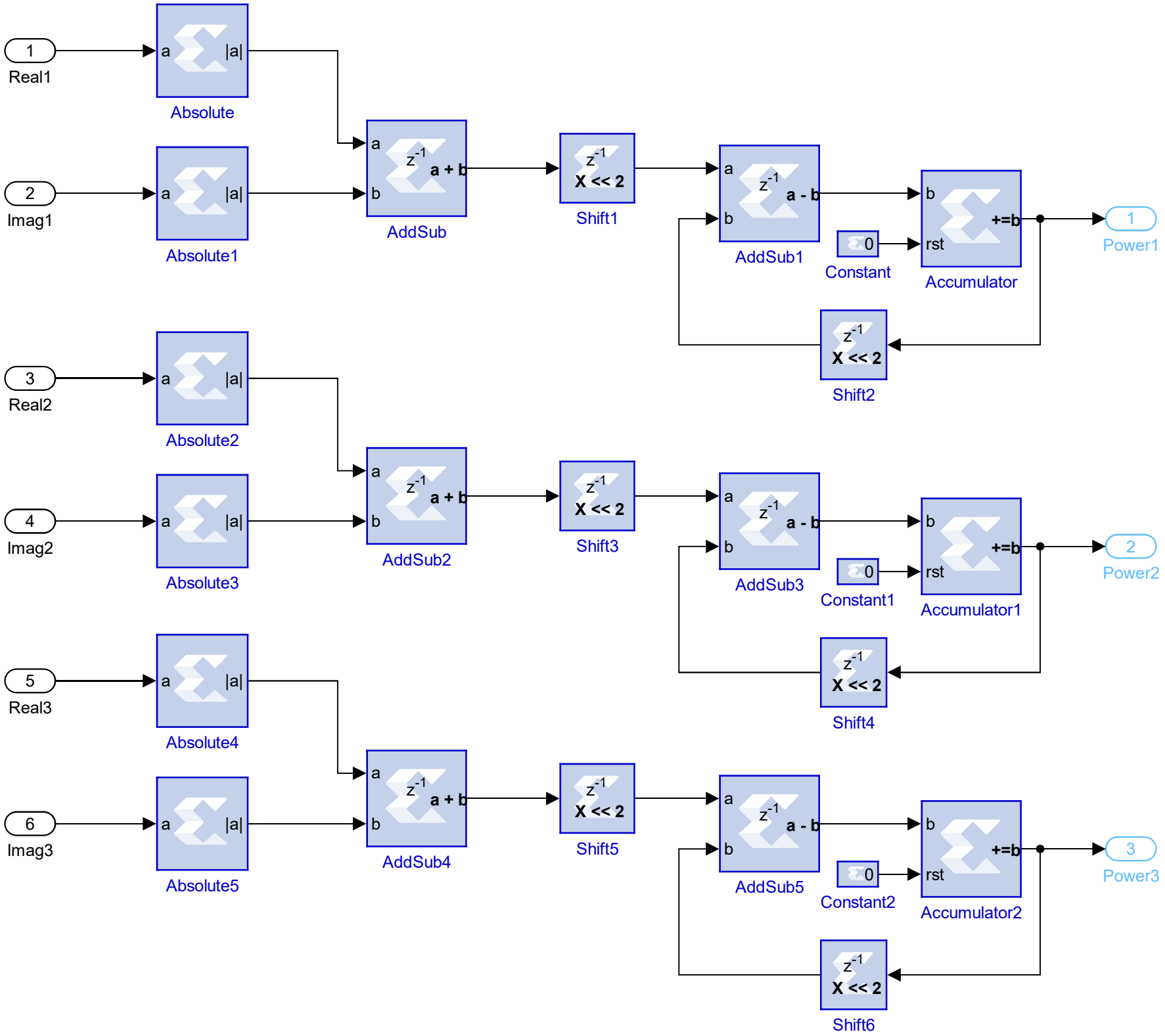
If Real=Imag=0, the Cordic goes to 180°, not 0.




Relational
Goto
[Neg]
Gateway Out3
Gateway Out2
Gateway Out1
Scope
Negate
Mux
Mux1
AddSub2
Out
6
Rst
1
Limit
Mux6
Constant1
Relational1
[Pos]
Goto1
5
LagCoef
2
PhaseErr
Mult3
AddSub
Gateway Out4
3
Locked
4
SwpRate
Mux2
Negate1
Mux3
Constant
not
Inverter
Gateway Out
[Pos]
[Neg]
Logical1
Logical2
Logical
Delay
Assert
Gateway Out5


1
Out
Mux11
sel
1
Sel
z-1d0
d1
a(-1) a
2
In
Negate1


1
Out
Mux11
sel
1
Sel
z-1d0
d1
a(-1) a
2
In
Negate1


1
Real1
a
|a|
Absolute
2
Imag1
Absolute1
a
b
z-1
a + b
AddSub
z-1
X << 2
Shift1
a - b
AddSub1
0
Constant
b
rst
+=b
Accumulator
1
Power1
z-1
X << 2
Shift2
3
Real2
Absolute2
4
Imag2
Absolute3
AddSub2
Shift3
AddSub3
Constant1
Accumulator1
2
Power2
Shift4
5
Real3
Absolute4
6
Imag3
Absolute5
AddSub4
Shift5
AddSub5
Constant2
Accumulator2
3
Power3
Shift6