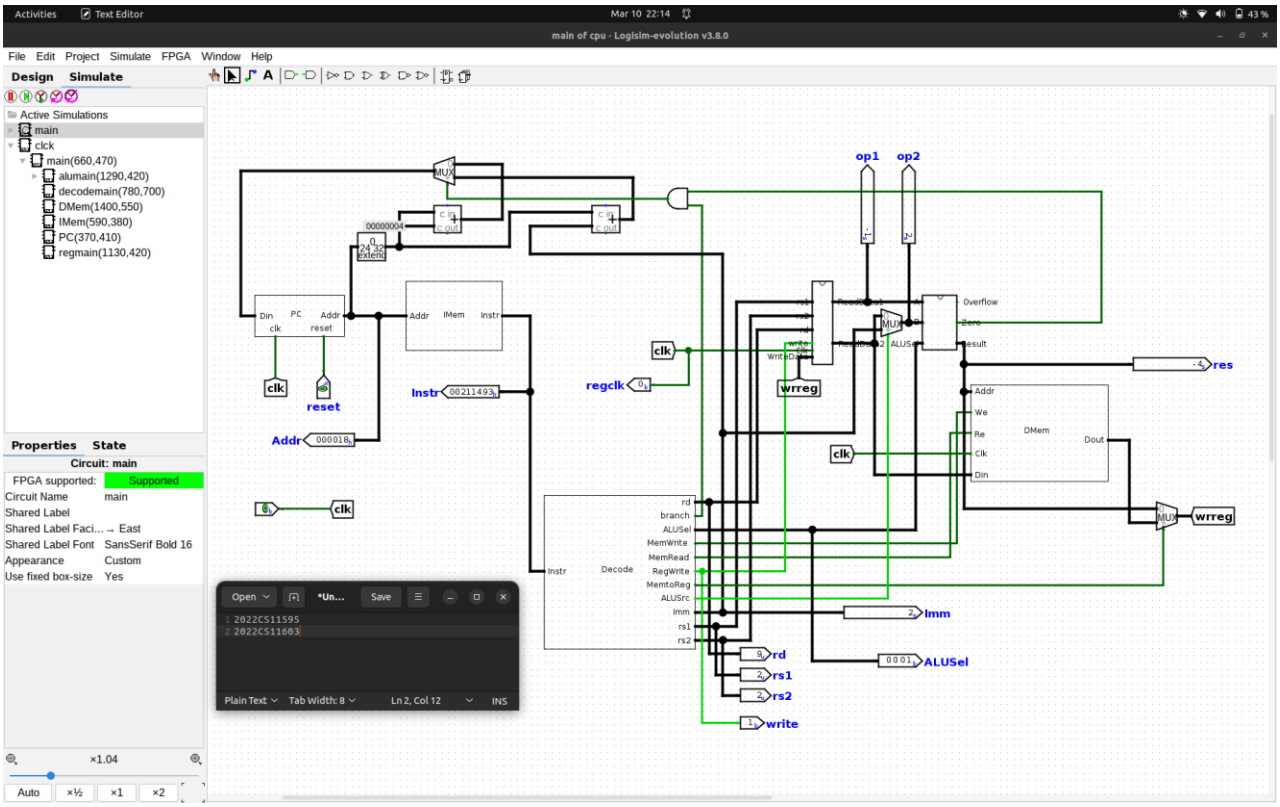
Processor – Part 4

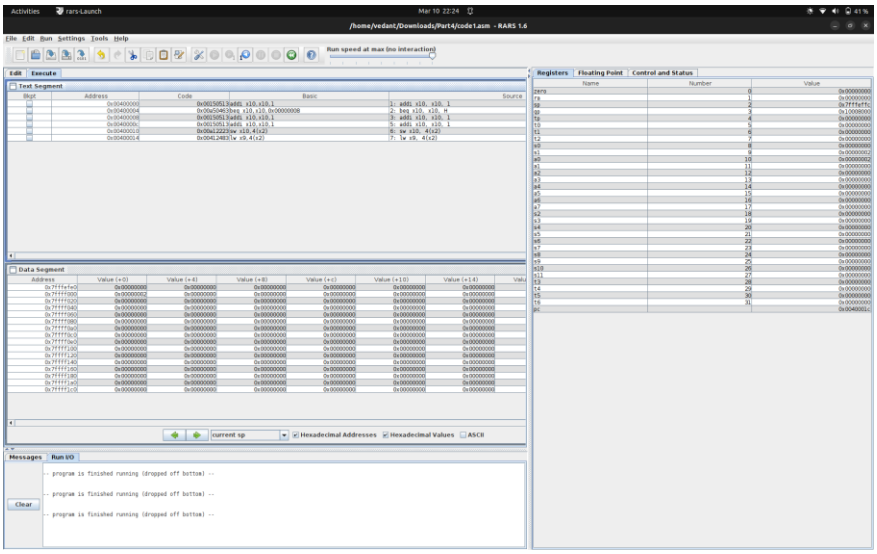
Single-cycle CPU

We tested our processor on 2 codes written on RARS 1.6 in RISC-V assembly.

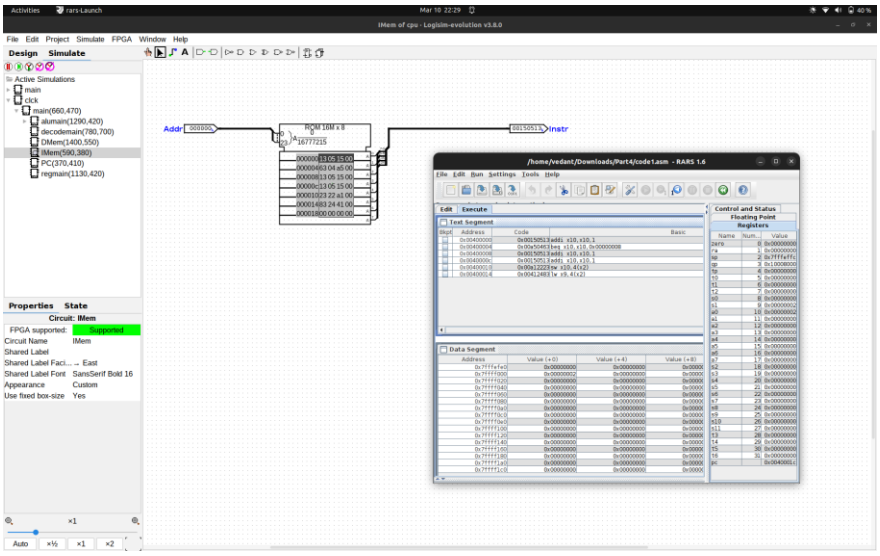
Top-level View of the CPU:



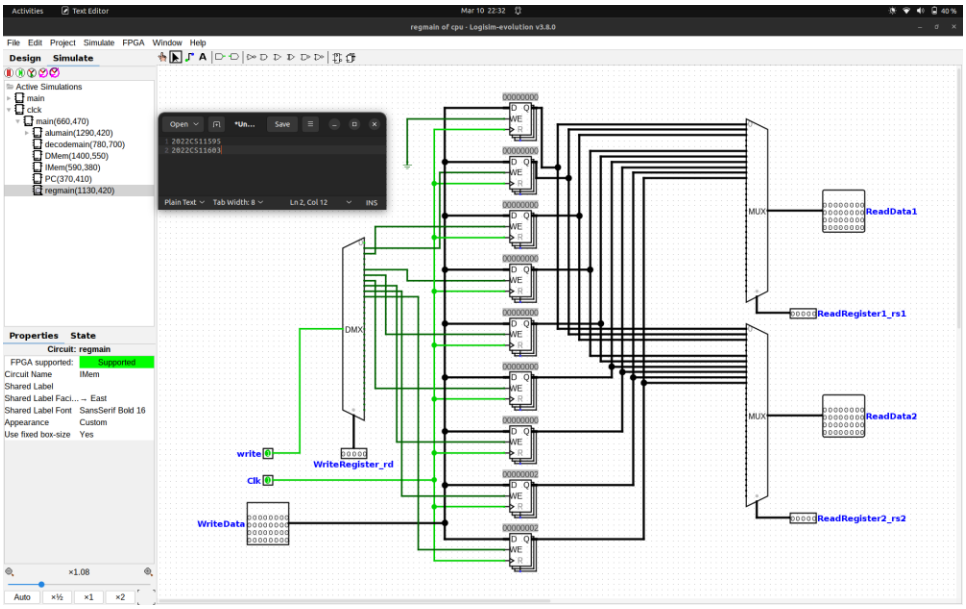
Code 1:



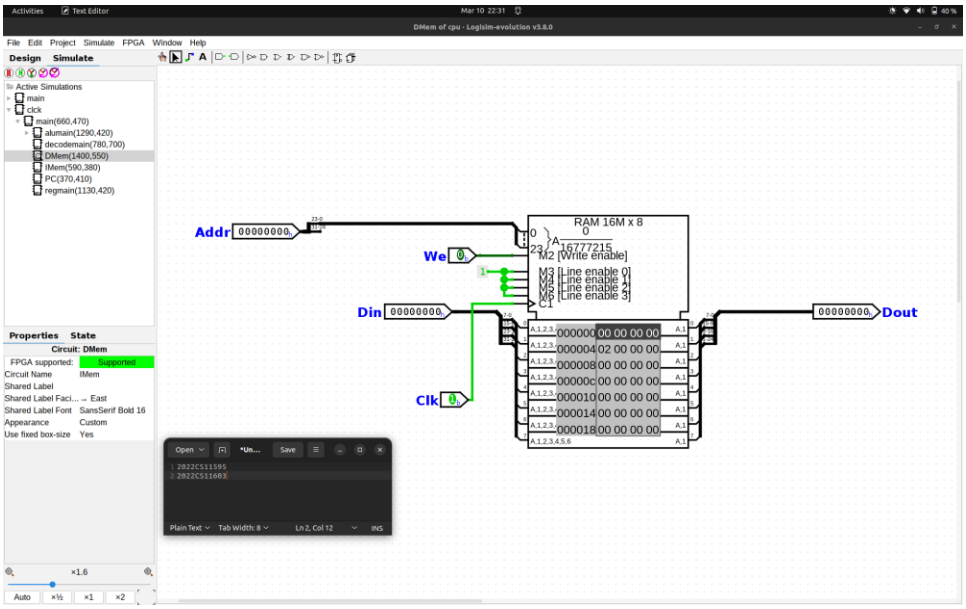
The machine code we fed into IMem:



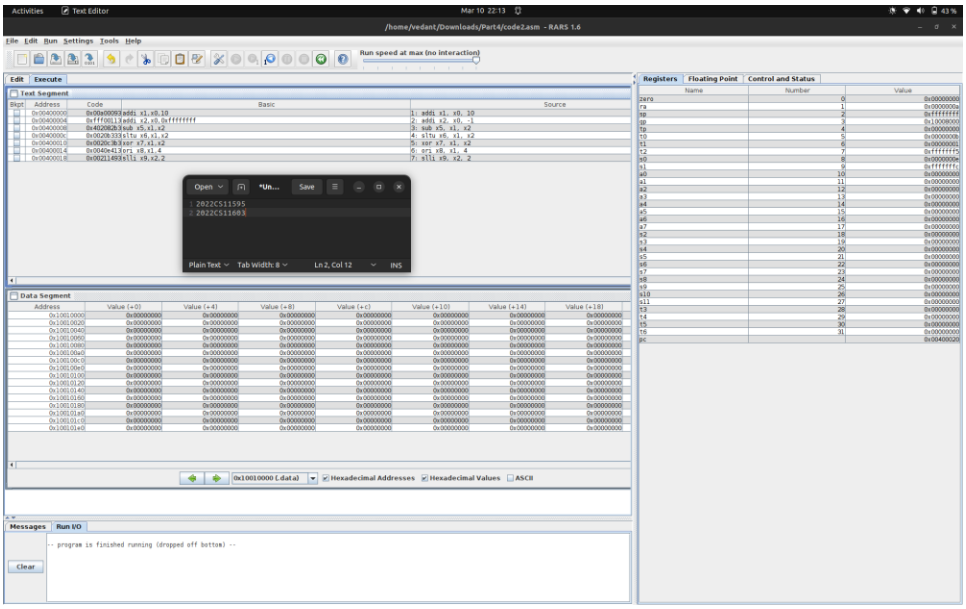
Register file of CPU after execution:



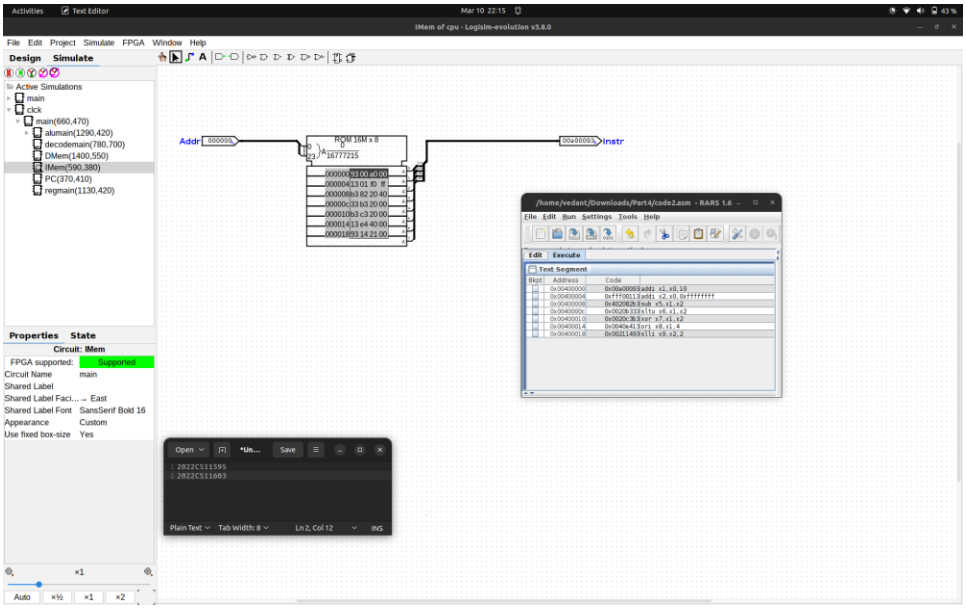
DMem of CPU after execution:



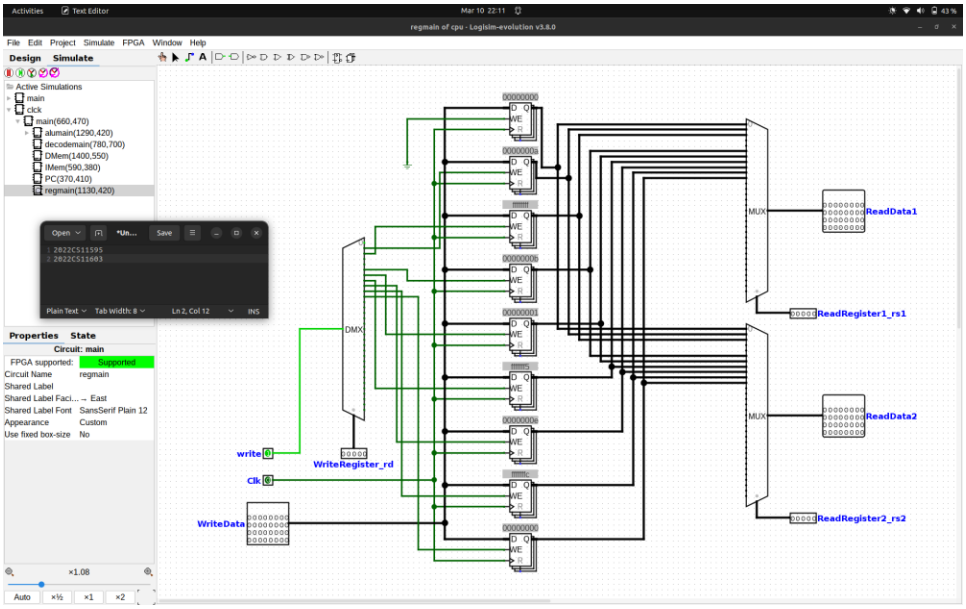
Code 2:



The machine code we fed into IMem:



Register file of CPU after execution:



Thus, we can see that the register file and DMem of CPU matches with the registers and memory in RARS in both cases.