Lecture 6: 8086/8088 Pins and Work Modes

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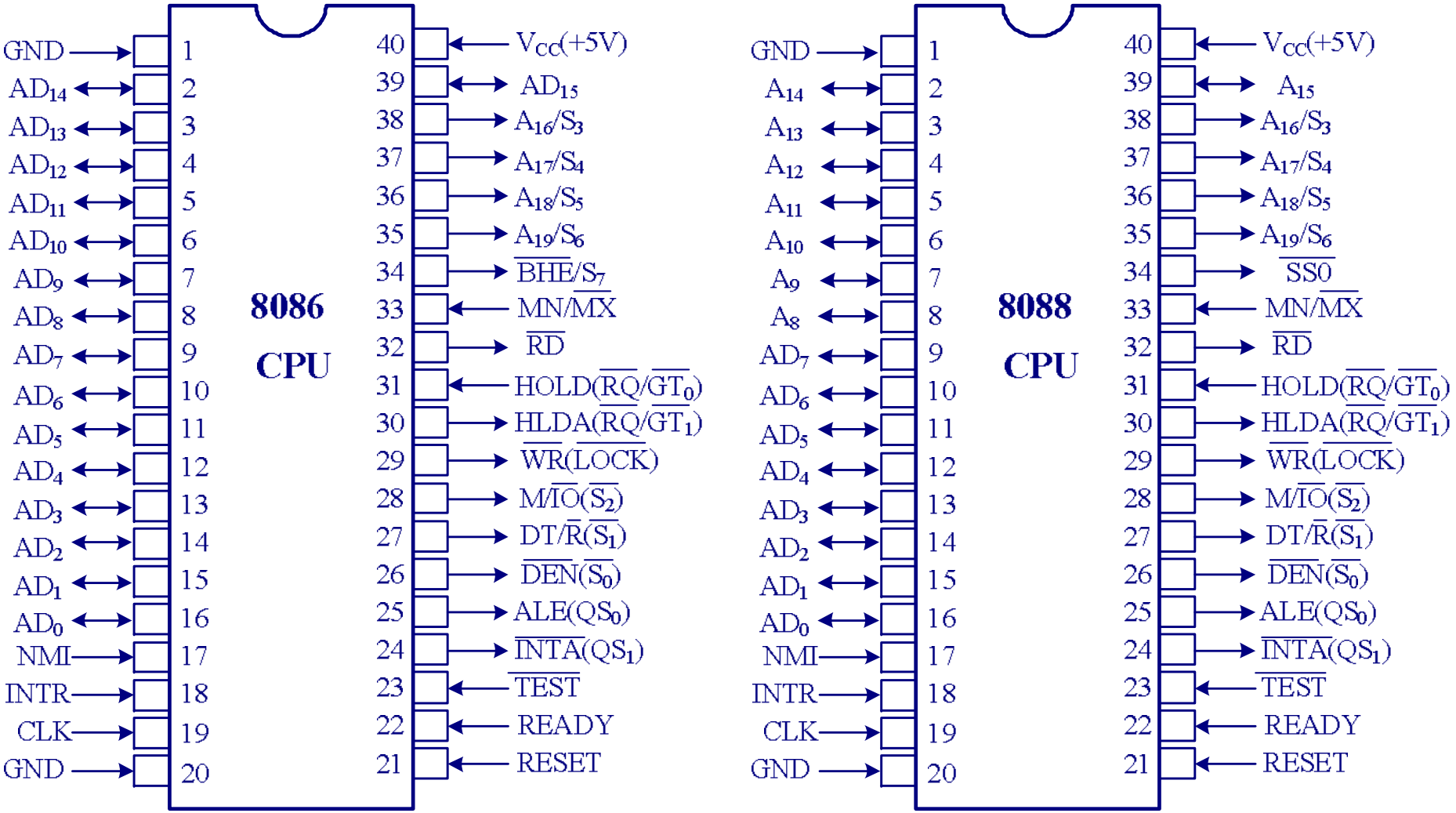
The 80x86 IBM PC and Compatible Computers

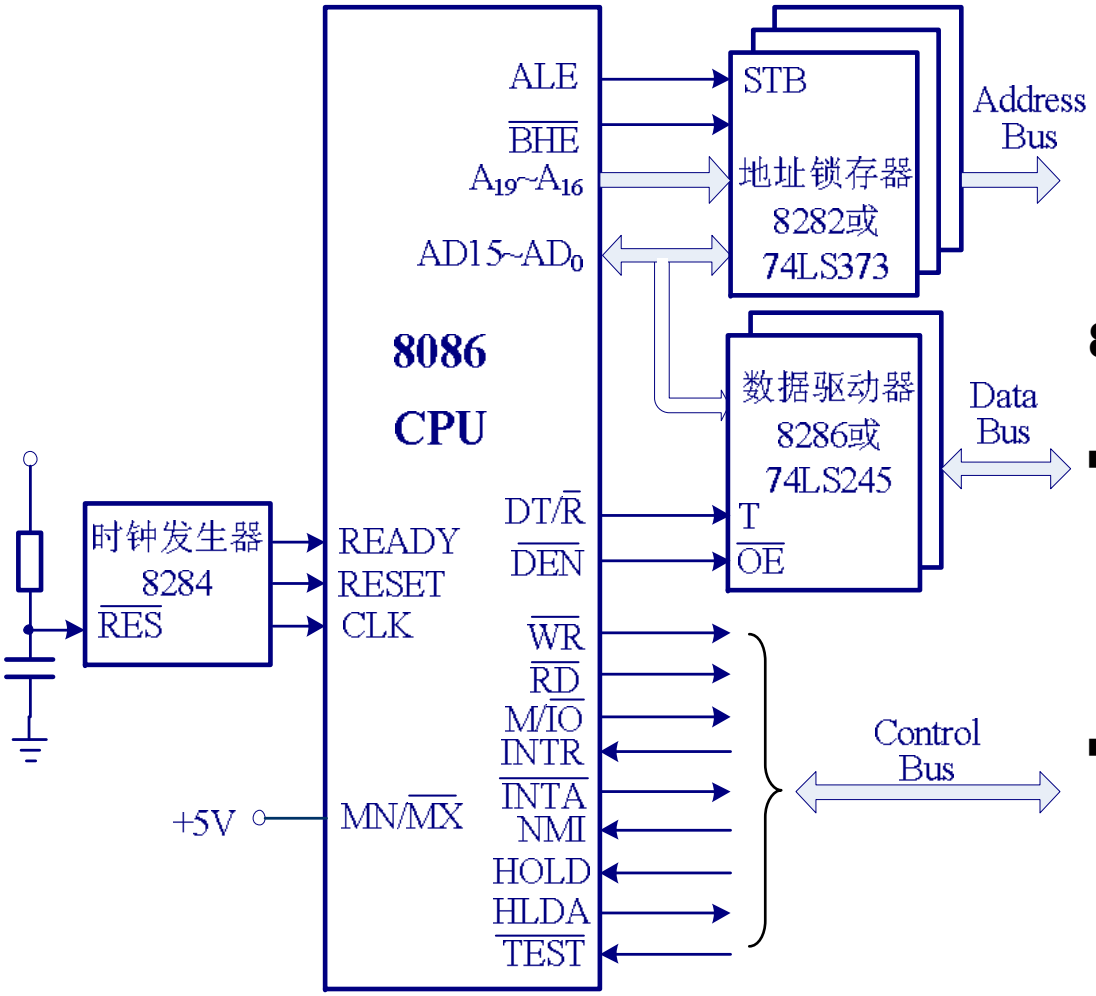
Chapter 9.1

8088 Microprocessor

8086/8088 Pins



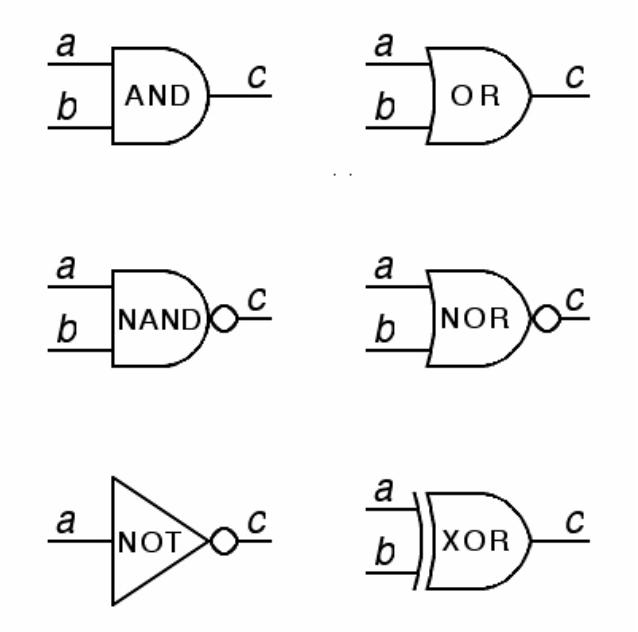
Minimum Mode



8086/88's two work modes:

- Minimum mode : $MN/\overline{MX}=1$
  - Single CPU;
  - Control signals from the CPU
- Maximum mode : $MN/\overline{MX}=0$
  - Multiple CPUs(8086+8087)
  - 8288 control chip supports

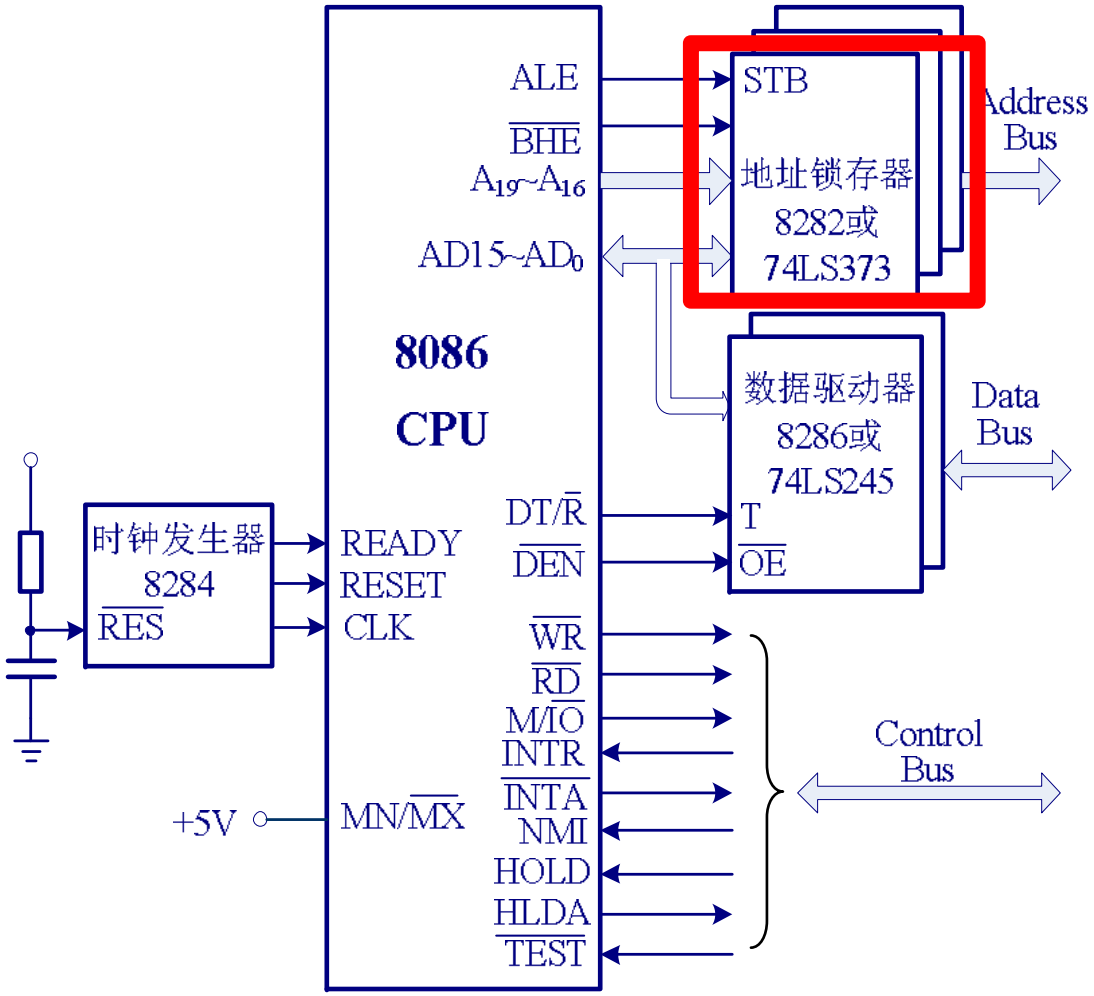
Remember CMOS Gates?

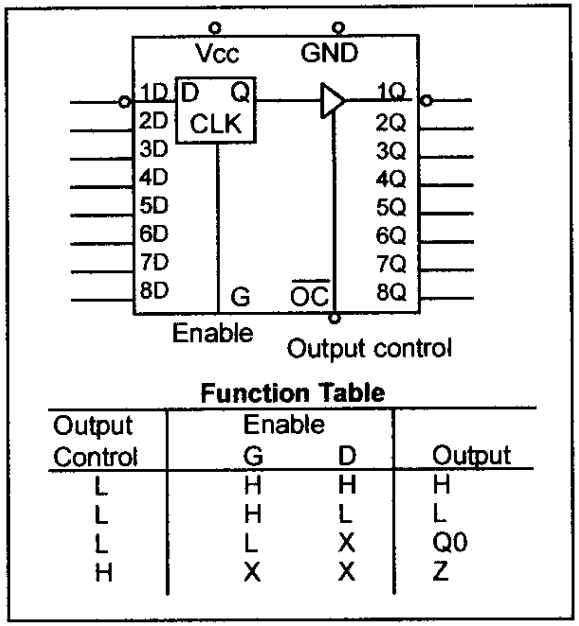


inputs		the output c					
a	b	AND $a\,b$	OR $a+b$	NAND $\overline{a\,b}$	NOR $\overline{a+b}$	NOT $\overline{a}$	XOR $a \oplus b$
0	0	0	0	1	1	1	0
0	1	0	1	1	0		1
1	0	0	1	1	0	0	1
1	1	1	1	0	0		0

Boolean logic operations

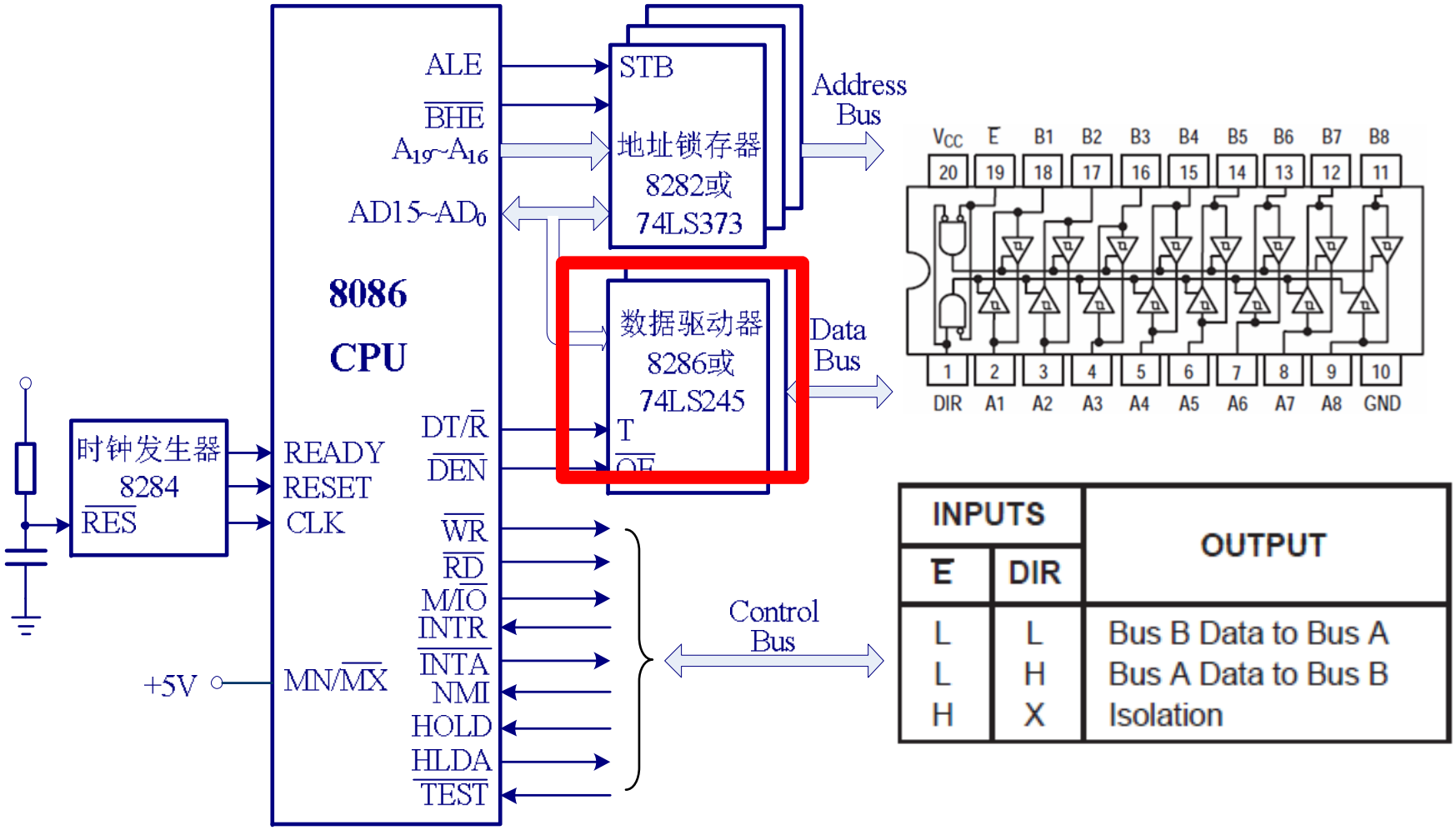
Address/Data Demultiplexing & Address latching





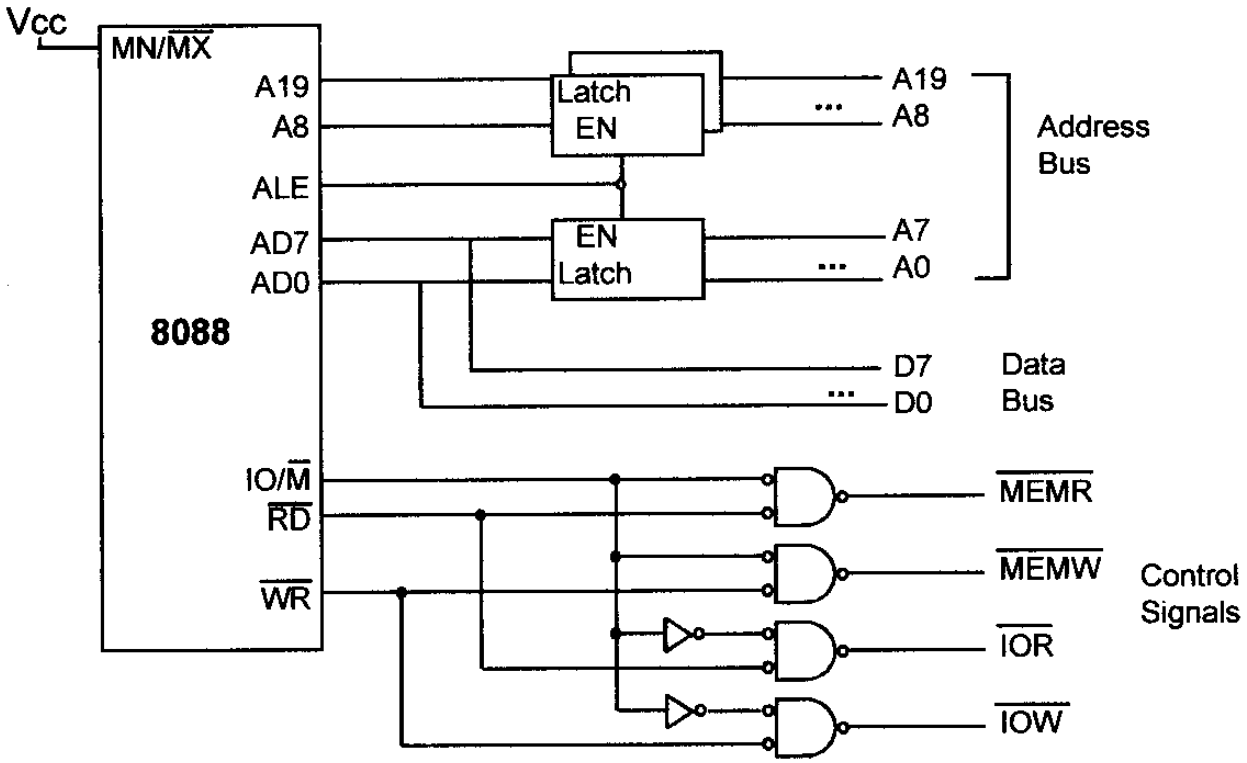
74LS373 D Latch

Data Bus Transceiver



INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

Memory/IO Control Signals



Other Control Signals

- **MN/~MX:** Minimum mode (high level), Maximum mode (low level)
- **~RD:** output signal, CPU is reading from memory/IO
- **READY:** input signal, memory/IO is ready for data transfer
- **INTR:** input signal, interrupt request from 8259 interrupt controller, maskable by clearing the IF
- **NMI:** input signal, non-maskable interrupt, CPU is interrupted after finishing the current instruction; cannot be masked by software
- **INTA:** output signal, interrupt ack
- **~BHE:** output signal, ~BHE=0, AD8-AD15; ~BHE=1, AD0-AD7

Other Control Signals

- **HOLD:** input signal, hold the bus request
- **HLDA:** output signal, hold request ack
- **RESET:** input signal, reset the CPU

8086/88 Memory/IO Timing