Resistive Network System for Neural Network Computation

Section L4A
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Agenda

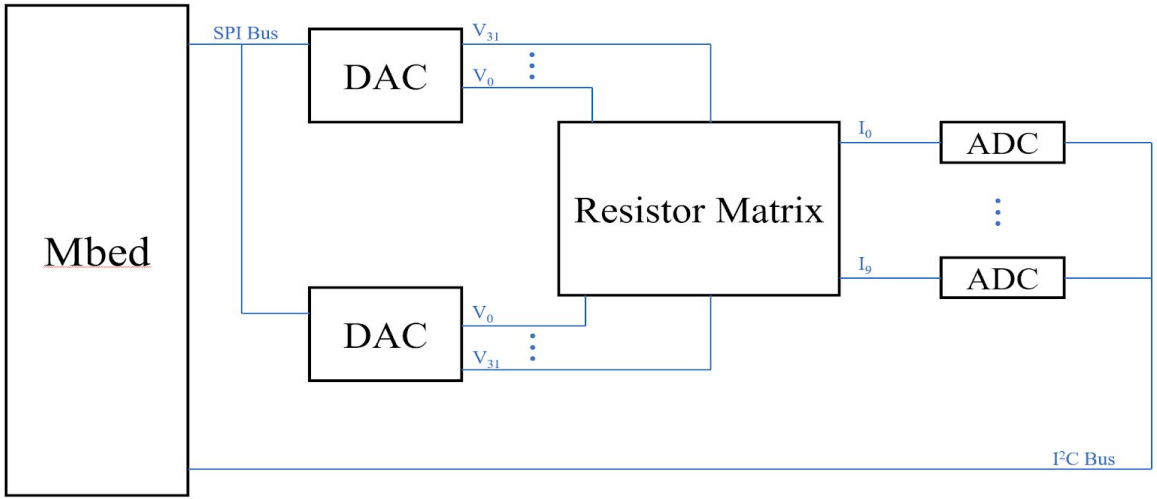
- **Overview**
- Key specifications
- Expected Outcomes

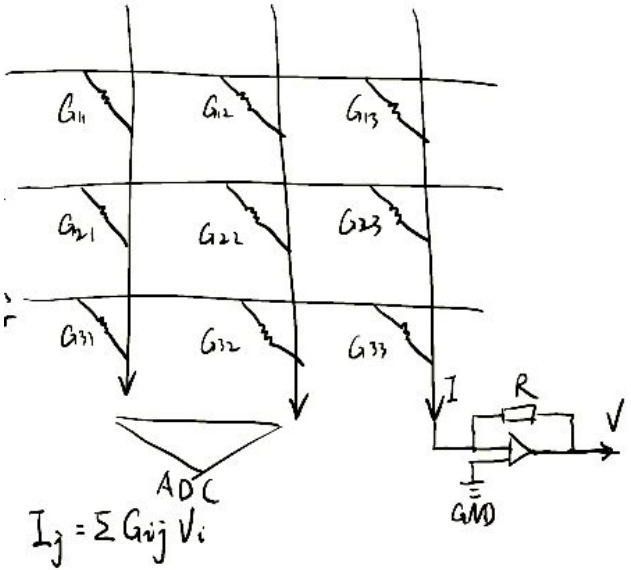
Objective

The team will design and prototype a resistor network system that emulates the floating point multiplication operations that are essential to neural network computation. A microcontroller unit (MCU) will take in images of handwritten digits, convert the pixel data into corresponding voltage levels, and feed them into the resistor network.

The resistor network, which consists of arrays of resistors with different resistance representing the weights of the nodes, will convert the voltage levels into different current levels, which are then converted back into voltage values. The microcontroller will then read the current output of the resistor network and determine which digits the original inputs represent.

System Layout





Computation Distribution

- Convolution, dropout & maxpool layers -> performed on MCU
- Computation of one fully-connected layer of size [64, 10] will take advantage of the resistive network
- MCU will also perform softmax operations and make corresponding classification decisions

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Target Resistive Network Specification

Item	Specification
Detection Accuracy	≥ 97%
Output Nodes	10
Input Nodes	64
Hidden Layer Number	1

Proposed Resistor Specs

Item	Specification
Quantization Level	5
Resistor Range	1000Ω - 5000Ω
Resistor Mounting	Through Hole

Proposed Digital-to-Analog Specs

Item	Specification
Analog Input Pin Number	≥ 10
Analog Output Pin Number	≥ 64
Power Supply	5V
ADC Resolution	8 bits
Interfaces	USB or Serial, I^2C, SPI
RAM	≥ 8K bytes

Proposed Analog-to-Digital Converter Specs

Item	Specification
Resolution	≥ 8 bits
Voltage Range	0mV-100mV
Interfaces	I2C

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Expected Functional Procedures

- Data will be pre-loaded into the Microcontroller (MCU).
- The MCU will be connected to the resistive network—consisting of 640 commercially available resistors—by DAC converters, where it sends the analog voltage values.
- The MCU will generate inputs and feed that into the resistive network. In our case, the inputs are an encoded matrix of size 8-by-8
- After passing through the trained resistive network, the data will be read by the MCU from the ADC converters connected to the network.
- The output data will be collected and buffered to the PC. The data will be visualized and analyzed by the user and compared to the target output to evaluate the performance.

Notes

1. Since the MCU now takes over the computation of other layers, the input size is no longer required to preserve enough information of the original image data. This is a desired attribute for quick prototyping.
2. In order to decrease the total power consumption of the system, resistor values are increased by an order of magnitude (in the range of thousands of Ohms).
3. The op amp + resistor translation of the current makes the ADC range flexible, as long as the resolution meets the component specification.

Thank you!