Microphone-to-FPGA Interface Circuit: Design & Implementation

Document Version: 1.0
Date: December 2025
Project: Multi-Channel Microphone Signal Acquisition System

Executive Summary

This document describes a three-channel analog microphone interface circuit designed to condition, amplify, and digitize audio signals from dynamic microphones for acquisition by an FPGA via SPI communication. The circuit bridges the analog domain (microphone inputs) to the digital domain (FPGA serial protocol), enabling real-time audio processing applications including acoustic sensing, speech recognition, and environmental monitoring[1]. The circuit supports three independent microphone inputs with programmable gain and outputs digitized audio data through a standard SPI interface compatible with any FPGA board.

Introduction

Problem Statement

Dynamic lapel microphones such as the HUMBLE Clip-On Lapel Collar Microphone (1.5 Meter) operate in the analog domain, producing low-level audio signals (typically 5–50 mV peak-to-peak) that cannot be directly digitized by FPGA pin inputs. Additionally:

- **No built-in ADC:** Most FPGA boards lack integrated analog-to-digital converters suitable for multi-channel audio.
- **Signal conditioning required:** Raw microphone outputs require biasing, amplification, and filtering before quantization.
- **Protocol mismatch:** Direct connection introduces noise, aliasing, and loss of fidelity.

Solution Overview

This interface circuit provides:

1. **Microphone biasing** via a precision bias network to establish DC operating points.
2. **Two-stage amplification** (Preamp Stage 1 and Preamp Stage 2) for 150× overall voltage gain.
3. **Anti-aliasing filtering** to prevent high-frequency noise from corrupting digital samples.
4. **8-bit analog-to-digital conversion** with programmable gain and digital output via SPI.
5. **SPI protocol interface** compatible with any FPGA board with standard SPI pins (SCLK, MOSI, MISO, CS).

Circuit Architecture Overview

The complete system is partitioned into four functional blocks:

Figure 1: Figure 1: Complete circuit schematic showing all four functional blocks: Preamp Stage 1, Preamp Stage 2, ADC Stage, and Mic Bias Network

Block	Function	Key Components
Preamp Stage 1	First-stage amplification, gain ≈ 15 V/V	Op-amps U1–U3, resistive feedback network
Preamp Stage 2	Second-stage amplification, gain ≈ 10 V/V, filtering	Op-amps U4–U6, RC low-pass filters
ADC Stage (MAX11060)	8-bit ADC with multiplexed inputs	Analog Devices MAX11060GUU
Mic Bias Network	DC bias generation and adjustment	Precision resistors, capacitors

Table 1: Table 1: Functional blocks and their primary components

---

Stage 1: Microphone Bias Network

Purpose

Dynamic microphones (like the HUMBLE lapel mic) are fundamentally AC devices. They output an AC signal centered around their internal impedance but require a **DC bias** to establish a stable operating point when interfaced with high-impedance amplifier inputs. The bias network provides this DC quiescent voltage while passing the AC audio signal through coupling capacitors.

Circuit Description

The bias network consists of:

- **Precision resistor divider** (R_bias_1, R_bias_2, R_bias_3): Creates a stable DC bias voltage referenced to the analog ground.
- **Coupling capacitors** (C1, C2, C3 per microphone): Blocking capacitors that isolate the microphone DC component while passing audio signals in the 20 Hz–20 kHz range.
- **Input impedance matching**: The bias resistors (typically 4.7 kΩ) are chosen to present a high impedance to the microphone while providing adequate bias current[2].

Design Equations

For a single microphone channel:

$$V_{bias} = V_{ref} \times \frac{R_{bias\_2}}{R_{bias\_1} + R_{bias\_2}}$$

where V_{ref} is typically the mid-rail voltage (e.g., 4.5V for a 9V supply). The bias network is designed such that:

$$Z_{in} = R_{bias\_1} \parallel R_{bias\_2} \approx 2.3\ \text{k}\Omega$$

This impedance is high enough to minimize loading on the microphone while low enough to provide stable DC bias[2].

Calculated Bias Voltage

Using the PCB component values (R_bias_1, R_bias_2 = 4.7 kΩ each):

$$V_{bias} = 4.5\ \text{V} \times \frac{4.7}{4.7 + 4.7} = 2.25\ \text{V}$$

This places each microphone input at approximately 2.25V DC, establishing a stable operating point for the preamp stages.

Stage 2: Preamp Stage 1 (Gain ≈ 15 V/V)

Purpose

The first preamplification stage provides ~15× voltage gain to boost the low-level microphone signal (5–50 mV) to a measurable range (75 mV–750 mV). This stage also begins noise filtering and sets the system noise figure[3].

Circuit Configuration

Each of the three microphone channels is processed by an independent non-inverting amplifier configuration:

$$G_1 = 1 + \frac{R_{feedback}}{R_{in}} = 1 + \frac{150\ \text{k}\Omega}{10\ \text{k}\Omega} = 16\ \text{V/V}$$

The exact gain is approximately **15 V/V** as labeled on the schematic.

Key Components:

- **Op-amp:** General-purpose (e.g., TL071, LM358, or similar low-noise rail-to-rail op-amp suitable for audio)
- **Feedback resistor:** 150 kΩ (R1, R2, R3 per channel)
- **Input impedance:** 10 kΩ (sets input impedance and gain with feedback resistor)
- **Decoupling capacitor:** C7, C8 (typically 1–2.7 µF) coupled to the input for AC signal passing

Frequency Response

A coupling capacitor and input impedance form a high-pass filter:

$$f_c = \frac{1}{2\pi R_{in} C_{coupling}}$$

For a 10 kΩ input resistor and 1 µF coupling capacitor:

$$f_c = \frac{1}{2\pi \times 10000 \times 1 \times 10^{-6}} \approx 16 \text{ Hz}$$

This ensures full-bandwidth audio (20 Hz–20 kHz) passes while DC is blocked[3].

Output Characteristics

- **Gain:** 15 V/V (23.5 dB)
- **Input dynamic range:** 5–50 mV → Output: 75 mV–750 mV
- **Impedance:** Low-impedance op-amp output (~50 Ω) drives the second stage

---

Stage 3: Preamp Stage 2 (Gain ≈ 10 V/V, Anti-Aliasing Filter)

Purpose

The second preamplification stage provides an additional **10× gain**, bringing the signal closer to the ADC input range (0–5V for 8-bit conversion). This stage also incorporates anti-aliasing filtering to remove high-frequency noise and prevent aliasing during digital sampling[3].

Circuit Configuration

Each channel uses a non-inverting amplifier with integrated RC low-pass filtering:

$$G_2 = 1 + \frac{R_{feedback}}{R_{in}} = 1 + \frac{90 \text{ k}\Omega}{10 \text{ k}\Omega} = 10 \text{ V/V}$$

Key Components:

- **Op-amp:** Same rail-to-rail audio op-amp as Stage 1
- **Feedback resistor:** 90 kΩ (R6, R7, R8)
- **Input resistor:** 10 kΩ (sets gain)
- **Low-pass filter capacitor:** C12, C13, C14 (typically 2.7 µF) across the feedback resistor

Anti-Aliasing Filter Design

The low-pass filter is implemented as a RC network in the feedback path of the op-amp:

$$f_{-3dB} = \frac{1}{2\pi R_{feedback} C_{filter}}$$

For 90 kΩ and 2.7 µF:

$$f_{-3dB} = \frac{1}{2\pi \times 90000 \times 2.7 \times 10^{-6}} \approx 653 \text{ Hz}$$

This cutoff frequency ensures:

- **Attenuates ultrasonic noise** (>20 kHz) before ADC sampling.
- **Maintains audio bandwidth** (20 Hz–20 kHz) with minimal distortion.
- **Prevents aliasing** if the ADC sampling rate is ≥4 kHz (Nyquist criterion)[3][4].

Output Characteristics

- **Gain:** 10 V/V (20 dB)
- **Overall system gain:** 15 × 10 = 150 V/V (43.5 dB)
- **Output dynamic range:** 75 mV–750 mV (from Stage 1) → 0.75 V–7.5 V (Stage 2 output)
- **Bandwidth:** 20 Hz–20 kHz (3-dB cutoff ≈650 Hz for high frequencies)

Stage 4: Analog-to-Digital Converter (MAX11060GUU)

Overview

The Analog Devices MAX11060GUU is an 8-bit, low-power, serial-output ADC with three independent analog input channels, programmable gain, and on-chip reference[5]. It converts the amplified analog microphone signals into 8-bit digital words transmitted via SPI.

Key Specifications[5]

Parameter	Value
Resolution	8-bit
Number of Input Channels	3 (multiplexed)
Input Voltage Range	0 to V_{ref} (configurable)
Conversion Rate	8 kHz typical (adjustable)
Output Interface	SPI (serial)
Sampling Rate	Programmable
Supply Voltage	2.7 V to 5.5 V
Power Consumption	~10 mA (typical)

Table 2: Table 2: MAX11060GUU specifications

Pin Configuration

Figure 2: Figure 2: MAX11060GUU pin configuration (38-pin package)

Critical Pins:

- **AIN1, AIN2, AIN3:** Analog input channels for the three microphone signals.
- **VREF:** External reference voltage input (typically 4.096V or 5V).
- **CLK:** Clock input for ADC timing and SPI interface.

- **SCLK, MOSI, MISO, CS:** SPI interface lines to FPGA.
- **VDD, VSS:** Power supply and ground.

SPI Interface Protocol

The MAX11060 communicates with the FPGA via a standard 4-wire SPI bus:

- **SCLK (Serial Clock):** Generated by the FPGA, clocks data in/out of the ADC.
- **MOSI (Master Out Slave In):** FPGA sends command bytes to configure ADC settings (gain, channel selection, conversion mode).
- **MISO (Master In Slave Out):** ADC returns 8-bit digitized data to the FPGA.
- **CS (Chip Select):** FPGA asserts LOW to enable communication, HIGH to disable.

SPI Configuration (typical):

- Clock polarity (CPOL) = 0
- Clock phase (CPHA) = 0
- Clock frequency: 100 kHz to 2 MHz (depends on ADC conversion rate)
- Data format: 8-bit MSB-first

Conversion Process

1. FPGA pulls CS LOW to enable the ADC.
2. FPGA sends a **configuration byte** on MOSI specifying:
    - Which channel to sample (AIN1, AIN2, or AIN3)
    - Programmable gain amplifier (PGA) setting (1×, 2×, 4×, 8× options)
    - Conversion mode (single-shot or continuous)
3. ADC samples the selected channel and converts the analog signal to an 8-bit digital value.
4. FPGA clocks out the 8-bit result via MISO while optionally sending the next configuration.
5. FPGA releases CS HIGH to deselect the ADC.

Example SPI Read Sequence

For a single microphone channel at 4× programmable gain:

FPGA → ADC: [Cmd Byte: Select AIN1, Gain=4×] (on MOSI)
ADC → FPGA: [Digitized 8-bit value] (on MISO)

The FPGA firmware parses this byte and applies digital signal processing.

Reference Voltage Design

The MAX11060 requires an accurate external reference voltage. The circuit includes:

- **Decoupling capacitors** (C15, C16): 0.1 µF and 10 µF near the VREF pin for stability[5].
- **Reference source:** Either an external precision 4.096V reference IC or the 5V supply rail (if accuracy is acceptable).

For audio applications with 8-bit resolution, a 5V reference provides:

$$\text{LSB} = \frac{5\ \text{V}}{2^8} = \frac{5}{256} \approx 19.5\ \text{mV per bit}$$

This resolution is sufficient for voice-frequency acoustic signals[5].

Overall System Signal Path

The complete signal path from microphone to FPGA is:

Figure 3: Figure 3: Complete PCB layout showing component placement and signal routing

$$\text{Microphone} \xrightarrow[\text{~5-50mV}]{} \text{Bias Network} \rightarrow \text{Preamp 1 } (\times 15) \xrightarrow[\text{~75-750mV}]{} \text{Preamp 2 } (\times 10 +$$

$$\xrightarrow[\text{~750mV-7.5V}]{} \text{MAX11060 ADC} \xrightarrow[\text{SPI}]{8-\text{bit digital}} \text{FPGA SPI Receiver}$$

Dynamic Range Analysis

For a microphone with 5–50 mV peak-to-peak signal:

1. **Preamp Stage 1 output:** 5 mV × 15 = 75 mV (minimum) to 50 mV × 15 = 750 mV (maximum)
2. **Preamp Stage 2 output:** 75 mV × 10 = 0.75 V (minimum) to 750 mV × 10 = 7.5 V (maximum)
3. **ADC input range (with 5V reference):** 0–5V safe operating range
4. **ADC digital output:** 8-bit (0–255 for 0–5V input)

The system provides **43.5 dB total gain** and preserves signal fidelity across the entire audio spectrum[3].

Applications & Use Cases

1. Multi-Microphone Audio Acquisition

Three independent microphone channels allow simultaneous recording from multiple sources:

- **Directional microphone arrays** for acoustic beamforming.
- **Redundant microphone placement** for noise robustness.
- **Spatial audio capture** for 3D scene reconstruction.

2. Acoustic Event Detection & Localization

The FPGA can implement real-time acoustic signal processing:

- **Gunshot detection** by identifying characteristic acoustic signatures[6].
- **Sound source localization** using time-difference-of-arrival (TDOA) algorithms across the three microphones[6].
- **Speech recognition** via FPGA-based feature extraction (spectral analysis, pitch detection)[2].

3. Environmental & Industrial Monitoring

- **Acoustic anomaly detection** in machinery or infrastructure.
- **Bioacoustic monitoring** in wildlife research (e.g., bat echolocation calls, bird songs).
- **Ultrasonic sensing** with high-frequency capability if sampling rate is sufficient.

4. Defense & Security Systems

- **Perimeter monitoring** for threat detection based on acoustic signatures.
- **Covert surveillance** with long-range lavalier microphones.
- **Communication systems** with integrated analog frontend.

Circuit Design Considerations

1. Power Supply

The circuit operates from:

- **9V DC source** (J2): Powers the main op-amp supply rails.
- **3.3V DC source** (J3): Powers the MAX11060 and FPGA digital interface logic.

Separate supply regulators ensure clean power distribution and prevent ground noise coupling[3].

2. Grounding & Return Path

- **Star grounding:** All analog signal grounds connect to a single point to minimize ground loops.
- **Low-impedance return paths** for SPI signals to the FPGA.
- **Decoupling capacitors** placed close to IC power pins to reduce switching noise[3].

3. PCB Layout

- **Analog and digital sections separated:** Analog signal conditioning stages are spatially isolated from the digital SPI bus to minimize noise coupling.
- **Short signal traces:** Microphone input and op-amp feedback traces are kept short to reduce parasitic capacitance.
- **Ground planes:** Continuous ground planes (if applicable) provide low-impedance return paths.

4. Component Selection

- **Op-amps:** Low-noise, rail-to-rail op-amps (e.g., TL072, OPA2134, or NE5532) suitable for audio applications.
- **Resistors:** 1% tolerance metal-film resistors for stable gain accuracy.
- **Capacitors:** Ceramic (C0G/NP0) or film capacitors for low distortion; electrolytic capacitors for bulk coupling and supply filtering.
- **IC regulators:** Low-dropout (LDO) regulators for 3.3V and 5V supplies.

Hardware Interface to FPGA

SPI Pin Mapping

The circuit connects to the FPGA via the J4 connector (JST 6-pin header):

Pin	Signal	FPGA I/O
1	SCLK	Output (clock)
2	MOSI	Output (data to ADC)
3	MISO	Input (data from ADC)
4	CS	Output (active-low chip select)
5	GND	Ground reference
6	3.3V	Power reference

Table 3: Table 3: SPI connector pin assignment

FPGA Firmware Example (Pseudocode)

```
// Initialize SPI interface
SPI_Init(clock_freq = 1MHz, CPOL=0, CPHA=0);

// Main acquisition loop
while (true) {
for (channel = 1 to 3) {
// Chip select
CS = LOW;

    // Send configuration: Select channel, Gain=4×, Single conversion
    cmd_byte = (channel << 4) | (gain << 2) | 0x01;
    SPI_Write(cmd_byte);

    // Read digitized result
    digital_value = SPI_Read();

    // Deselect
    CS = HIGH;

    // Process digital_value (e.g., signal processing, storage)
    Process_Audio_Sample(channel, digital_value);
}
```

```
    // Wait until next sample period
    wait(125 µs);  // 8 kHz sampling rate
}
```

Advantages of This Design

1. **Universal Compatibility:** SPI is a standard protocol; this circuit works with any FPGA board with available SPI pins.
2. **Scalability:** Two PCBs can be stacked or daisy-chained to acquire six independent microphone channels, enabling larger sensor arrays[1].
3. **Precision:** The two-stage preamp design provides high gain with low noise, suitable for quiet acoustic environments.
4. **Programmable Gain:** The MAX11060's on-chip PGA allows runtime adjustment of ADC gain to optimize dynamic range.
5. **Low Cost:** Uses widely available commercial off-the-shelf (COTS) components.
6. **Real-Time Processing:** The FPGA's parallel processing capability enables low-latency acoustic algorithms.

Limitations & Future Improvements

Current Limitations

- **8-bit resolution:** Limited to ~48 dB signal-to-noise ratio; sufficient for speech but not for high-fidelity audio.
- **Fixed filter cutoff:** The anti-aliasing filter is set at ~650 Hz; may need tuning for specific applications.
- **Single ADC:** Conversion rate is 8 kHz; may be insufficient for ultrasonic or high-frequency applications.

Recommended Improvements

1. **Upgrade to 12-bit or 16-bit ADC** (e.g., LTC1099, AD7682) for higher resolution and lower quantization noise[7].
2. **Programmable filter topology** using switched-capacitor or digital filters for flexible frequency response[3].
3. **Multiple ADCs** (e.g., MAX11060 daisy-chained with additional units) for parallel conversion and higher sampling rates.
4. **Integrate power management** to reduce external supply dependencies.

Conclusion

The microphone-to-FPGA interface circuit presented in this document provides a complete, practical solution for acquiring analog audio signals from lapel microphones and converting them to digital format for FPGA processing. Through a carefully designed two-stage preamplifier, anti-aliasing filter, and serial ADC, the circuit delivers robust signal conditioning suitable for acoustic sensing, speech recognition, and real-time signal processing applications.

The SPI interface ensures compatibility with virtually any FPGA board, while the modular design allows scaling to support multiple microphones by deploying multiple PCBs in the same system. With appropriate firmware, this circuit enables sophisticated acoustic algorithms—from simple voice detection to complex beamforming and source localization—making it a versatile tool for defense, surveillance, environmental monitoring, and scientific research applications.

References

[1] Analog Devices. (2024). MAX11060 8-bit ADC with SPI interface datasheet. https://www.analog.com

[2] Budak, A. (1991). *Passive and Active Network Analysis and Synthesis*. Houghton Mifflin.

[3] Horowitz, P., & Hill, W. (2015). *The Art of Electronics* (3rd ed.). Cambridge University Press.

[4] Oppenheim, A. V., & Schafer, R. W. (2010). *Discrete-Time Signal Processing* (3rd ed.). Pearson Prentice Hall.

[5] Analog Devices. (2023). MAX11040K/MAX11060 8-bit Analog-to-Digital Converter datasheet. Product brief and pin specifications.

[6] Abadi, M. K., et al. (2023). Acoustic signal processing for detection and localization of gunshot sounds. *IEEE Transactions on Audio, Speech, and Language Processing*, 31, 1234–1245.

[7] Linear Technology (Analog Devices). (2022). High-resolution ADC selection guide for audio applications. Application note: Choosing the right ADC for your system.