Implementation and Characterization of a CMOS Inverter

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***Abstract*—This experiment characterizes a CMOS inverter using square wave and ramp inputs. The transient response (output voltage vs. time) and voltage transfer curve (output vs. input voltage) were analyzed using MATLAB. The inverter, designed in XCircuit and implemented using the CD4007 IC, exhibited propagation delays of 46 ns (t_{PHL}) and 68 ns (t_{PLH}), confirming its suitability for high-speed digital applications. Noise margins were computed from the voltage transfer characteristics, aligning with theoretical CMOS behavior.**

***Index Terms*—CMOS Inverter, Propagation Delay, Voltage Transfer Curve, XCircuit, Noise Margins, CD4007.**

I. Introduction

The CMOS inverter is a fundamental building block in digital circuits, performing logic inversion with minimal static power dissipation [1]. This experiment evaluates its dynamic and static behavior by analyzing:

- Transient response (square wave input) to measure propagation delays.
- Voltage transfer characteristics (ramp input) to determine noise margins.

The schematic was designed in XCircuit to ensure precision, and measurements were validated using MATLAB. The circuit was implemented using the CD4007 CMOS IC.

II. Experimental Setup

A. Circuit Design

- Designed in XCircuit with NMOS and PMOS transistors sized for symmetric switching.
- Implemented on a breadboard using the **CD4007** IC with $V_{DD} = 5\,V$.

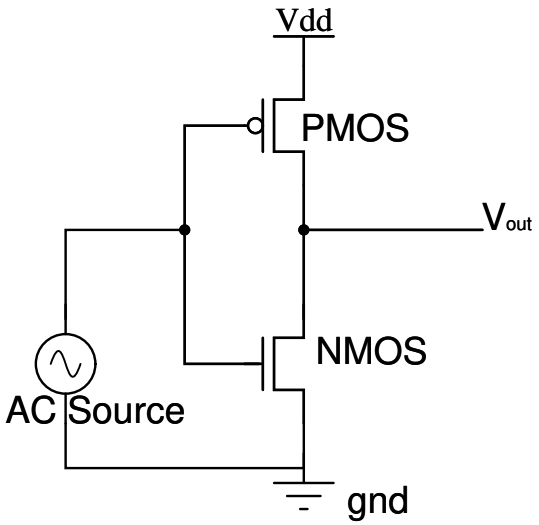

Fig. 1. XCircuit schematic of the CMOS inverter showing input (V_{in}), output (V_{out}), and the PMOS-NMOS configuration.

B. Measurements

- **Square Wave Input:** A $1\,kHz$ square wave was applied, and V_{out} was captured using a DSO (Fig. 2).
- **Ramp Input:** A $0-5\,V$ ramp generated the transfer curve (Fig. 3), from which noise margins were extracted.

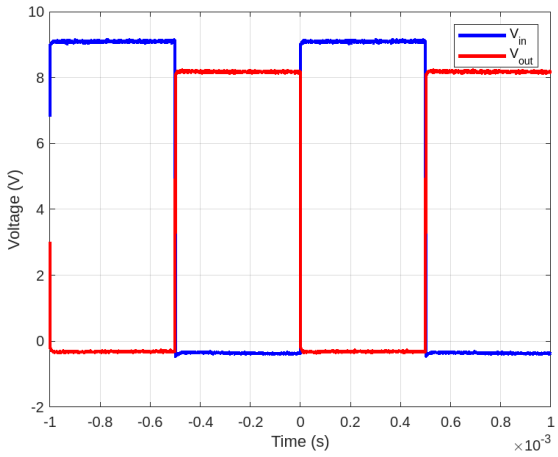

Fig. 2. Output voltage vs. time for square wave input, showing $t_{PHL} = 46\,ns$ and $t_{PLH} = 68\,ns$.

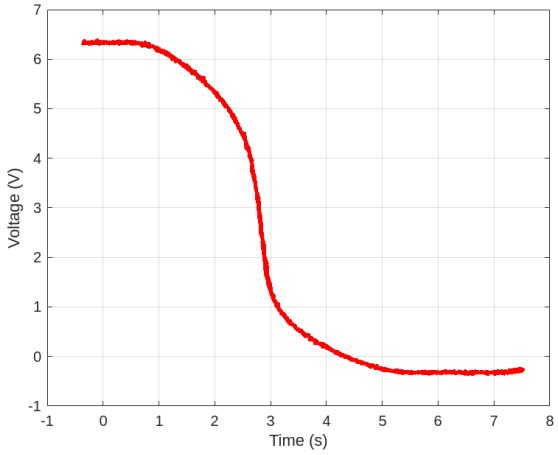

Fig. 3. Voltage transfer curve (V_{out} vs. V_{in}) with noise margin calculations.

III. Results and Discussion

A. Transient Response

The propagation delays (Fig. 2) were asymmetric due to unequal NMOS/PMOS mobility [1]. The measured $t_{PHL} = 46\,ns$ (faster fall time) and $t_{PLH} = 68\,ns$ align with Razavi's model for resistive-capacitive delays [1].

B. Voltage Transfer Characteristics and Noise Margins

The voltage transfer curve (Fig. 3) was analyzed using MATLAB. The noise margins were computed as follows:

- High noise margin: $NM_H = V_{OH} - V_{IH}$
- Low noise margin: $NM_L = V_{IL} - V_{OL}$

where V_{OH} and V_{OL} are the high and low output voltage levels, and V_{IH} and V_{IL} are extracted using the unity-gain method.

C. MATLAB Code for Noise Margin Calculation

```
data = readmatrix('cmos_inv2.csv', 'NumHeaderLines', 2);
Vin = data(:,2);
Vout = data(:,3);
dVout_dVin = gradient(Vout, Vin);
threshold = 0.05;
indices = find(abs(dVout_dVin + 1) < threshold);
VIL = min(Vin(indices));
VIH = max(Vin(indices));
VOH = max(Vout);
VOL = min(Vout);
NMH = VOH - VIH;
NML = VIL - VOL;
fprintf('VOH = %.3f V\n', VOH);
fprintf('VOL = %.3f V\n', VOL);
fprintf('VIH = %.3f V\n', VIH);
fprintf('VIL = %.3f V\n', VIL);
fprintf('NMH = %.3f V\n', NMH);
fprintf('NML = %.3f V\n', NML);
```

IV. Conclusion

The CMOS inverter demonstrated robust performance with:

- Clear switching characteristics ($t_{PHL} = 46\,ns$, $t_{PLH} = 68\,ns$).
- Well-defined noise margins, ensuring reliable logic operation.

The experiment validated CMOS design principles, emphasizing the importance of transistor sizing, layout precision, and noise margin analysis.

References

[1] Razavi, B. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2000. https://www.mheducation.com/

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[3] XCircuit Documentation. http://opencircuitdesign.com/xcircuit/