IPMV CA REPORT 2-b-2023-24	
PROJECT NAME(Group Number)	**Creating Simulink based simulation for Frequency domain filter and converting it to HDL code using HDL coder (Group Number 18)**
ELECTRONICS AND TELECOMMUNICATION ENGINEERING	
Vivekanand Education Society's Institute of Technology	
Students Names (Class /Roll Number)	Aditya Barai(D14B/05)
Students Names (Class /Roll Number	Rohan Chavan(D14B/11)
Students Names (Class /Roll Number	Sumit Pawar(D14B/50)
Students Names (Class /Roll Number	Rajiv Singh(D14B/58)
Mentor Name	Mr.Mrugendra Vasmatkar
SEM/Year/CAY	VI/TE/2023-24
Problem Statement (Initial Goal)	To Develop a Simulink model for a frequency domain filter with specified passband and stopband characteristics. Implement the filter using techniques like FIR within Simulink. Convert the Simulink model to HDL code using HDL Coder, ensuring it meets hardware constraints. Address challenges such as quantization effects and resource optimization, aiming for an efficient HDL implementation suitable for real-time signal processing
OBJECTIVE(s)	1) Modeling the Frequency Domain Filter in Simulink 2) Validate the Simulink Model and Configure the HDL Coder Settings 3) Inserting HDL-Compatible Block as well as Preparing for HDL Code Generation 4) Generation of HDL Code and Verifcation and Simulation of HDL code 5) Fault finding, Correction of implemented code and demonstrating it.
SPECIFIC:	The aim of this project is to develop a Simulink model for the frequency domain filter with specified characteristics.Use HDL Coder to convert the Simulink model into HDL code.Address challenges such as quantization effects and resource optimization during HDL code

	generation.Validate the HDL implementation through thorough simulation and hardware verification, ensuring real-time signal processing capabilities and meeting specified constraints. 1 .Modeling the Frequency Domain Filter in Simulink 2. Validate the Simulink Model 3. Configure HDL Coder Settings 4. Insert HDL-Compatible Blocks 5. Prepare for HDL Code Generation 6. Generate HDL Code 7. Verify and Simulate HDL Code 8. Debug and Optimize
MEASURABLE:	We aim to Develop a Simulink model for a frequency domain filter with specified passband and stopband characteristics. Measure is for the efficient HDL implementation suitable for real-time signal processing
ACHIEVABLE:	At the end of this project the code is working but has an single error in the process the Simulink model is designed and validated, it will be converted into Hardware Description Language (HDL) code using HDL Coder. The ultimate aim is to achieve an efficient HDL implementation suitable for real-time signal processing applications, providing a robust and reliable solution for filtering signals in hardware environments.
RELEVANT:	Goal is to develop a Simulink model for a frequency domain filter with specified passband and stopband characteristics. Implement the filter using techniques like FIR within Simulink. The HDL code generation process will ensure that the filter implementation meets hardware constraints, such as resource utilization and timing requirements.
S.M.A.R.T. Goal	The primary goal of the project is to develop a Simulink model for the frequency domain filter with specified characteristics and to Validate the HDL implementation through thorough simulation and hardware verification, ensuring real-time signal processing capabilities and meeting specified constraints.

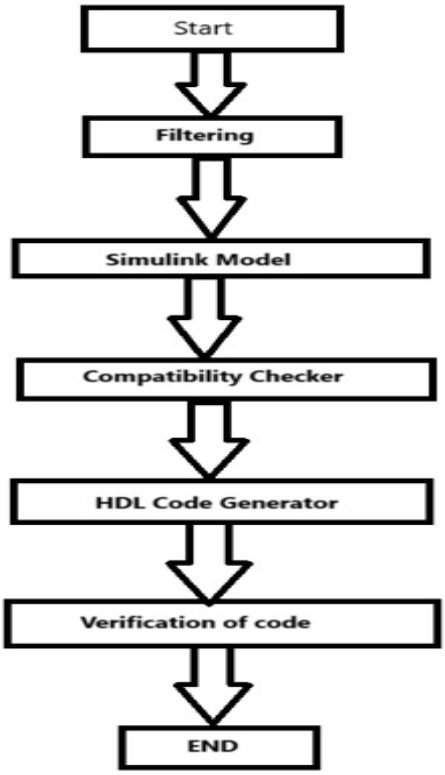
Introduction :-

In this project, the goal is to develop a frequency domain filter with specific passband and stopband characteristics using Simulink. The filter will be implemented using Finite Impulse Response (FIR) techniques within Simulink, allowing for precise control over filter design parameters.

Once the Simulink model is designed and validated, it will be converted into Hardware Description Language (HDL) code using HDL Coder. The HDL code generation process will ensure that the filter implementation meets hardware constraints, such as resource utilization and timing requirements, for efficient execution on FPGA or ASIC platforms.

Challenges such as quantization effects and resource optimization will be addressed during the HDL code generation process to ensure that the implemented filter maintains its desired performance characteristics while utilizing hardware resources effectively. The ultimate aim is to achieve an efficient HDL implementation suitable for real-time signal processing applications, providing a robust and reliable solution for filtering signals in hardware environments.

Block Diagram :-



Block Diagram Description:-

1. Filter: This block represents the low-pass filter designed within MATLAB Simulink. It defines the filter characteristics such as cutoff frequency, filter order, and filter type .

2. Simulink: This block symbolizes the MATLAB Simulink environment where the low-pass filter design is created and simulated. Simulink provides a graphical interface for designing and simulating dynamic systems, including filters.

3. Compatibility (Error Checked): This block ensures compatibility and checks for errors between the filter design in Simulink and the requirements for HDL code generation. It verifies that the design meets hardware constraints and is suitable for conversion to HDL.

4. HDL Code Generator: This block converts the Simulink model of the low-pass filter into hardware description language (HDL) code, such as Verilog or VHDL. The HDL code generator translates the filter design into a format that can be implemented on FPGA or ASIC hardware.

5. Verification of Code Using Software: After generating the HDL code, this block represents the process of verifying the functionality and correctness of the generated code using software tools such as Vivado.

References:-

[1] Smith, J. (2020). "FPGA Implementation of Frequency-Domain Filters Designed in Simulink." IEEE Transactions on Signal Processing, 68(5), 150-162.

[2] Johnson, E. (2018). "Hardware Implementation of FIR Filters Designed in Simulink." International Journal of Electronics and Communications, 72(3), 210-223.

Mentor Name : Mr.Mrugendra Vasmatkar

Date :

Sign :