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-- File Name: hdlsrc/hdlcoder_dspprogfir0x2810x29/coeffs_registers.vhd
-- Created: 2024-03-30 07:59:21
--
-- Generated by MATLAB 24.1, HDL Coder 24.1, and Simulink 24.1
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--
-- Module: coeffs_registers
-- Source Path: hdlcoder_dspprogfir0x2810x29/Programmable FIR via
Registers/coeffs_registers
-- Hierarchy Level: 1
-- Model version: 10.0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
USE work.Programmable_FIR_via_Registers_pkg.ALL;
ENTITY coeffs_registers IS
 PORT( clk                               :   IN    std_logic;
       reset                             :   IN    std_logic;
       enb                               :   IN    std_logic;
       coeffs_in                         :   IN    std_logic_vector(13 DOWNTO
0);  -- sfix14_En13
       write_address                     :   IN    std_logic_vector(7 DOWNTO
0);  -- uint8
       write_enable                      :   IN    std_logic;
       coeffs_out                        :   OUT
vector_of_std_logic_vector14(0 TO 42)  -- sfix14_En13 [43]
       );
END coeffs_registers;
ARCHITECTURE rtl OF coeffs_registers IS
 -- Signals
 SIGNAL coeffs_in_signed                 : signed(13 DOWNTO 0);  -- sfix14_En13
 SIGNAL write_address_unsigned           : unsigned(7 DOWNTO 0);  -- uint8
 SIGNAL coeffs_regs                      : vector_of_signed14(0 TO 42);  --
sfix14_En13 [43]
 SIGNAL coeffs_assigned                  : vector_of_signed14(0 TO 42);  --
sfix14_En13 [43]
 SIGNAL coeffs_regs_ectrl                : vector_of_signed14(0 TO 42);  --
sfix14_En13 [43]
BEGIN
 coeffs_in_signed <= signed(coeffs_in);
 write_address_unsigned <= unsigned(write_address);
 coeffs_assignment_output : PROCESS (coeffs_in_signed, coeffs_regs,
write_address_unsigned)
```

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    VARIABLE cast : vector_of_unsigned8(0 TO 42);
  BEGIN
    FOR i IN 0 TO 42 LOOP
      cast(i) := unsigned(to_signed(i, 32)(7 DOWNTO 0));
      IF write_address_unsigned = cast(i) THEN
        coeffs_assigned(i) <= coeffs_in_signed;
      ELSE
        coeffs_assigned(i) <= coeffs_regs(i);
      END IF;
    END LOOP;
  END PROCESS coeffs_assignment_output;
   coeffs_regs_ectrl <= coeffs_regs WHEN write_enable = '0' ELSE
      coeffs_assigned;
  coeffs_regs_lowered_process : PROCESS (clk, reset)
  BEGIN
    IF reset = '1' THEN
      coeffs_regs <= (OTHERS => to_signed(16#0000#, 14));
    ELSIF clk'EVENT AND clk = '1' THEN
      IF enb = '1' THEN
        coeffs_regs <= coeffs_regs_ectrl;
      END IF;
    END IF;
  END PROCESS coeffs_regs_lowered_process;
  outputgen: FOR k IN 0 TO 42 GENERATE
    coeffs_out(k) <= std_logic_vector(coeffs_regs(k));
  END GENERATE;
END rtl;
```