EE 6313 Advanced Microprocessors
Fall 2020 Project 2

1 Overview

The goal of this project is to determine the best architecture for a cache controller that interfaces to a 16-bit microprocessor that is used for signal processing. While the microprocessor is general purpose in design and performs a number of functions, it is desired to speed up certain signal processing functions, such as those calculating the eigenvalues and eigenvectors of a system.

2 Detailed Requirements

You are given the task of determining the architecture of a cache memory to speed up a microprocessor system. After the program being executed was profiled, the largest hit in performance was seen in functions called choldc() and cholsl() which operate on a 256x256 symmetric matrix of single-precision real floating numbers.

The code for function choldc() and cholsl() are available from Numerical Recipes in C at http://www.nrbook.com/a/bookcpdf.php/bookcpdf/bookcpdf/c2-9.pdf, pg 97-8).

The goal is to determine the best architecture for the 128 KiB cache. The three degrees of freedom in the design are n-way set associativity, burst length, and write strategy (write-back or write-through). Assume that the data bus is limited to 32 bits in width.

Your project should seek to allow 4GiB of memory (1 Gi x 32 bit) to be interfaced and the cache should be limited to 128 KiB in size.

By adding extra code to the Cholesky functions as shown in class, it is possible to determine exactly how memory is accessed.

The metric being used to evaluate the best performance is the total access time required to run the choldc() followed by the cholsl() routine, including the time required to flush the pipeline after the least-squares solution is computed. You may assume that the cache is empty before the decomposition routine is called. The values in the matrix to be used will be discussed in class.

Please use the assumption that the miss penalty is 60 ns (for first memory access) and 17ns for subsequent accesses in the same SDRAM word line and the cache hit time is 1 ns.

Please calculate the performance as a function of set size (n-way), number of cache lines, block size, and write strategy (write-back allocate, write-through allocate, and write-through non-allocate). Determine which 3 configurations result in the best performance. At a minimum, n-way associativity of 1, 2, 4, 8, and 16 and burst lengths of 1, 2, 4, and 8 should be evaluated for all 3 write strategies (60 permutations).

3 Deadlines

Project is due on date specified in the syllabus. You may work in teams of one or two members. All members of the team shall participate equally and be prepared to answer any question about the project to avoid a deduction in points. Each member of the team will be graded independently, although only one report is needed.

Have fun!