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Assignment 1

1a. Performance in instructions per second for processor 1 (P1) = Clock Rate/CPI

$= 3 \times 10^9 / 1.5$

$= 2 \times 10^9$ instructions per second

Performance in instructions per second for processor 2 (P2) = Clock Rate/CPI

$= 2.5 \times 10^9 / 1.0$

$= 2.5 \times 10^9$ instructions per second

Performance in instructions per second for processor 3 (P3) = Clock Rate/CPI

$= 4 \times 10^9 / 2.0$

$= 2 \times 10^9$ instructions per second

Hence, Processor 2 (P2) has the best performance in terms of instructions per second.

1b. We know that, CPU Time for P1 = (Instruction Count (I.C.) x CPI)/Clock Rate

$10 = (\text{I.C.} \times 1.5)/3 \times 10^9$

I.C. = 20×10^9 Instructions

Clock Cycles for P1= I.C. x CPI

$= 20 \times 10^9 \times 1.5$

$= 30 \times 10^9$ Clock Cycles

CPU Time for P2 = (Instruction Count (I.C.) x CPI)/Clock Rate

$10 = (\text{I.C.} \times 1.0)/2.5 \times 10^9$

I.C. = 25×10^9 Instructions

Clock Cycles for P2= I.C. x CPI

$= 25 \times 10^9 \times 1.0$

$= 25 \times 10^9$ Clock Cycles

CPU Time for P2 = (Instruction Count (I.C.) x CPI)/Clock Rate

$10 = (\text{I.C.} \times 2.0)/4.0 \times 10^9$

I.C. = 20×10^9 Instructions

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Clock Cycles for P2= I.C. x CPI

= 20 x 10^9 x 2.0

= 40 x 10^9 Clock Cycles

1c. Now, the execution time is to be reduced by 30% which leads to increase in the CPI by 10%.

To achieve this, the clock rate should be changed, which is calculated below

For Processor 1,

0.7 x CPU Time for P1 = (I.C. x 1.65)/ Clock Rate $_{new}$ .....(1)

Old CPU Time for P1 = (I.C. x 1.5)/3 x 10^9 .....(2)

Taking Ratio of above two equations,

Clock Rate $_{new}$ = 4.714 GHz

For Processor 2,

0.7 x CPU Time for P2 = (I.C. x 1.1)/ Clock Rate $_{new}$ .....(1)

Old CPU Time for P2 = (I.C. x 1.0)/2.5 x 10^9 .....(2)

Taking Ratio of above two equations,

Clock Rate $_{new}$ = 3.928 GHz

For Processor 3,

0.7 x CPU Time for P3 = (I.C. x 2.2)/ Clock Rate $_{new}$ .....(1)

Old CPU Time for P3 = (I.C. x 2.0)/4 x 10^9 .....(2)

Taking Ratio of above two equations,

Clock Rate $_{new}$ = 6.285GHz

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2.

Compilers	A	B
I.C.	1.0E9	1.2E9
CPU Time	1.1s	1.5s

2a. Clock Cycle Time = 1ns

Average CPI for Compiler A = CPU Time/(Clock Cycle Time x I.C.)

= 1.1/(1 x 10^9 x 1ns)

= 1.1

Average CPI for Compiler B = CPU Time/(Clock Cycle Time x I.C.)

= 1.5/(1.2 x 10^9 x 1ns)

= 1.25

2b. Now, CPU Time $_A$/CPU Time $_B$ = (I.C. x CPI x Cycle Time of A)/(I.C. x CPI x Cycle Time of B)

= (1.2 x 10^9 x 1.25 x Cycle Time of A)/(1 x 10^9 x 1.1 x Cycle Time of B)

Since the Compilers are same even though the Processors are different, the CPI would be the same. Also, the CPU Time for both processors are same.

Hence, Cycle Time of A/Cycle Time of B = (1.2 x 10^9 x 1.25)/(1.0 x 10^9 x 1.1)

= 1.36

Hence, Clock Rate of B/Clock Rate of A = 1.36

Hence, Clock Rate of Complier B is 1.36 times faster than Clock Rate of Compiler A

2c. New Compiler I.C. = 6.0E8 and New Compiler CPI (Average) = 1.1 and Clock Cycle time = 1ns

Execution time of new Compiler = I.C. x Average CPI x Clock Cycle Time

= 6.0 x 10^8 x 1.1 x 1 x10^{-9} = 0.66s

Execution Time of Compiler A = I.C. x Average CPI x Clock Cycle Time

= 1.0 x 10^9 x 1.1 x 1 x10^{-9} = 1.1s

Execution Time of Compiler B = I.C. x Average CPI x Clock Cycle Time

= 1.2 x 10^9 x 1.25 x 1 x 10^{-9}= 1.5s

Since the Execution Time of new Compiler is less then Compiler A and Compiler B, hence new Compiler is faster than both the Compilers A and B.

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Speedup of new Compiler w.r.t. compiler A =

Execution Time of new Compiler/Execution Time of Compiler A = 0.66/1.1 = 0.6

Speedup of new Compiler w.r.t. compiler B =

Execution Time of new Compiler/Execution Time of Compiler B = 0.66/1.5 = 0.44

Hence, the speedup in terms of execution time of new compiler with respect to compiler A is 0.6 and with respect to compiler B is 0.44.

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3. The Pentium 4 Prescott processor, has a clock rate of 3.6 GHz and voltage of 1.25 V. It consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, had a clock rate of 3.4 GHz and voltage of 0.9 V. It consumed 30 W of static power and 40 W of dynamic power.

Dynamic Power = $C \times Vdd^2 \times f$

Static Power = $Vdd \times I$

Total Power = Dynamic Power + Static Power

3a. For Pentium 4 Prescott processor,

$90 = C \times 1.25^2 \times 3.6 \times 10^9$

$C =$ 16nF

For Core i5 Ivy Bridge,

$40 = C \times 0.9^2 \times 3.4 \times 10^9$

$C =$ 14.52nF

3b. For Pentium 4 Prescott processor,

The static power consumption is 10W

% of static power in total power is (10 x100)/100 = 10%

Ratio of Static power to Dynamic ratio = 10:90 =1:9 = 0.11

For Core i5 Ivy Bridge,

The static power consumption is 30W

% of static power in total power is (30 x100)/70 = 42.86%

Ratio of Static power to Dynamic ratio = 30:40 =3/4 = 0.75

3c. Now, total dissipated power is to be reduced by 10%

For Pentium 4 Prescott processor,

I = 10/1.25 = 8A

Total Power/ 0.9 x Total Power = $(C \times Vdd_{old}^2 \times f + Vdd_{old} \times I)/(C \times Vdd_{new}^2 \times f + Vdd_{new} \times I)$

$100/90 = (16nF \times 1.25^2 \times 3.6GHz + 1.25 \times 8)/(16nF \times Vdd_{new}^2 \times 3.6GHz + Vdd_{new} \times 8)$

Solving,

$Vdd_{new} =$ 1.18V

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Hence, the voltage is reduced by 0.07V from 1.25V to 1.18V.

For Core i5 Ivy Bridge,

I = 30/0.9 = 33.33A

Total Power/ 0.9 x Total Power = $(C \times Vdd_{old}^2 \times f + Vdd_{old} \times I)/(C \times Vdd_{new}^2 \times f + Vdd_{new} \times I)$

$1/0.9 = (14.52nF \times 0.9^2 \times 3.4GHz + 0.9 \times 33.33)/(14.52nF \times Vdd_{new}^2 \times 3.4GHz + Vdd_{new} \times 33.33)$

Solving,

Vdd_{new} = 0.84V

Hence, the voltage is reduced by 0.06V from 0.9V to 0.84V

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4. Total Time = 250s

FP instructions time = 70s

L/S instructions time = 85s

Branch instructions time = 40s

INT instructions time = 55s

4a. Time for FP operations is reduced by 20%

Hence FP instructions time = 0.8 x 70 = 56s

Hence Total time = 236s

Reduction in Total time is 14s i.e. by 5.6%

4b. Total Time is reduced by 20%

Hence Total Time = 0.8 x 250 = 200s

Hence time for INT instructions = 200 – 70 - 85 – 40 = 5s

Reduction in time for INT instructions is 50s (from 55s to 5s) i.e. by 90.91%

4c. If the Total time is reduced by 20%,

The total time = 200s

Original time was 250s

If the time were to reduce from 250s to 200s and all instruction time except the branch instruction time was supposed to be kept the same, the summation excluding the branch instruction time would be 85 + 70 + 55 = 210. So even if we keep the time for branch instruction time to be zero the total time required is at least 210s.

So, the total time cannot be reduced by 20% by reducing only the time for branch instructions.

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5. Execution Time = 100s

Overhead Time = 4s

We know that, Execution Time = Computing Time/No. of Processors + Overhead Time

For Number of processors = 1

Computing Time = Execution Time – Overhead Time

= 100 – 4 = 96s

Now,

No. of Processors	Execution Time	Speedup relative to a single processor	Ratio of Actual speedup to Ideal speedup
2.000	100/002 + 4 = 54.0	100 – 54.0 = 46.00	54.0/50.0 = 1.08
4.000	100/004 + 4 = 29.0	100 – 29.0 = 71.00	29.0/25.0 = 1.16
8.000	100/008 + 4 = 16.5	100 – 16.5 = 83.50	16.5/12.5 = 1.32
16.00	100/016 + 4 = 10.25	100 – 10.25 = 89.75	10.25/6.25 = 1.64
32.00	100/032 + 4 = 7.125	100 – 7.125 = 92.875	7.125/3.125 = 2.28
64.00	100/064 + 4 = 5.562	100 – 5.562 = 94.438	5.562/1.562 = 3.56
128.0	100/128 + 4 = 4.781	100 – 4.78 = 95.219	4.781/0.781 = 6.129

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6. Wafer 1:

Wafer Diameter = 15cm

Cost = 12

No. of Dies = 84

Defects per area = 0.020 defects/cm^2

Wafer 2:

Wafer Diameter = 20cm

Cost = 15

No. of Dies = 100

Defects per area = 0.031 defects/cm^2

6a. For Wafer 1

Yield = $1/(1+ (\text{defects per area} \times \text{Die Area}/2))^2$

= $1/(1+ (0.020 \times ((3.14 \times 7.5^2)/84)/2))^2$

= 0.9592

For Wafer 2

Yield = $1/(1+ (\text{defects per area} \times \text{Die Area}/2))^2$

= $1/(1+ (0.031 \times ((3.14 \times 10^2)/100)/2))^2$

= 0.9093

6b. For Wafer 1,

Cost per die = cost per wafer/(Dies per wafer x yield)

= 12/(84 x 0.9592)

= 0.149

For Wafer 2,

Cost per die = cost per wafer/(Dies per wafer x yield)

= 15/(100 x 0.9093)

= 0.165

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6c. Dies per wafer Increase by 10% and defects per area increases by 15%

We know that, Die Area = Wafer Area/Dies per wafer

For Wafer 1,

Die Area (new) = 3.14 x 7.5 x7.5/(1.1 x 84)

= $1.91cm^2$

Yield(new) = $1/(1+(1.15 \times 0.020 \times 1.91/2))^2$

= 0.9574

For Wafer 2,

Die Area (new) = 3.14 x 10 x10/(1.1 x 100)

= $2.85cm^2$

Yield(new) = $1/(1+(1.15 \times 0.031 \times 2.85/2))^2$

= 0.9072

6d. For Yield of 0.92 and Die area $200mm^2$ i.e. $2cm^2$, the defects per area can be calculated by the Yield formula,

Yield = $1/(1+ (\text{defects per area} \times \text{Die Area}/2))^2$

$0.92 = 1/(1 + (\text{defects per Area} \times 2/2))^2$

Solving we get,

Defects per area = 0.042 defects/cm^2

For Yield of 0.95 and Die area $200mm^2$ i.e. $2cm^2$, the defects per area can be calculated by the Yield formula,

Yield = $1/(1+ (\text{defects per area} \times \text{Die Area}/2))^2$

$0.95 = 1/(1 + (\text{defects per Area} \times 2/2))^2$

Solving we get,

Defects per area = 0.026 defects/cm^2