ECE 452: Computer Organization and Design
Spring 2017

Homework 1: Computer Abstractions and Technology

Assigned: 24 Jan 2017
Due: 2 Feb 2017

Instructions:

- Please submit your assignment solutions via Canvas in a word or pdf file.
- Some questions might not have a clearly correct or wrong answer. In such cases, grading is based on your arguments and reasoning for arriving at a solution.

Q1 (30 points) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.

a. **(10 points)** Which processor has the highest performance in terms of instructions per second?
b. **(10 points)** If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. **(10 points)** We are trying to reduce the execution time by 30% but this leads to an increase of 10% in the CPI. What clock rate should we have to get this time reduction?

Q2 (30 points) Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

a. **(10 points)** Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
b. **(10 points)** Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?
c. **(10 points)** A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

Q3 (40 points) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

a. **(10 points)** For each processor find the average capacitive loads.
b. **(10 points)** Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.
c. **(20 points)** If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: static power is defined as the product of voltage and leakage current.

Q4 (30 points) Expecting to improve the overall performance of a computer by improving only one aspect of the computer is a common pitfall. Consider a computer running a program that requires 250 s, with 70 s spent executing FP instructions, 85 s executed L/S instructions, and 40 s spent executing branch instructions.

a. **(10 points)** By how much is the total time reduced if the time for FP operations is reduced by 20%?
b. **(10 points)** By how much is the time for INT operations reduced if the total time is reduced by 20%?
c. **(10 points)** Can the total time can be reduced by 20% by reducing only the time for branch instructions?

Q5 (25 points) When a program is adapted to run on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for locked critical sections and/or to send data from one processor to another. Assume a program requires t = 100 s of execution time on one processor. When run p processors, each processor requires t/p s, as well as an additional 4 s of overhead, irrespective of the number of processors. Compute the per-processor execution time for 2, 4, 8, 16, 32, 64, and 128 processors. For each case, list the corresponding speedup relative to a single processor and the ratio between actual speedup versus ideal speedup (speedup if there was no overhead).

Q6 (45 points) Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.

a. **(10 points)** Find the yield for both wafers.
b. **(10 points)** Find the cost per die for both wafers.
c. **(10 points)** If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.
d. **(15 points)** Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.