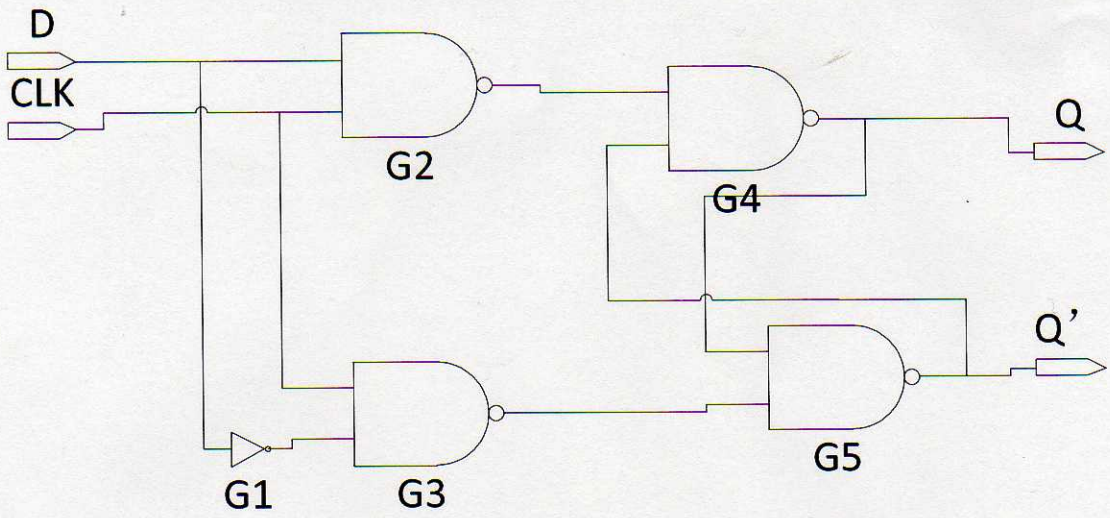
HW10



Q1, The circuit diagram above is a D-FF, analysis the circuit and draw its symbol, the symbol must illustrate correctly the triggering mechanism and its polarity.

positive level triggered D-FF

Q2, Use the same D-FF, determine its setup time, hold time, and FF delay in terms of gate delays(i.e., tG1, tG2, ⋯). Draw the time diagram. (Hint, ask yourself which time point on the clock signal should the setup time and hold time be referenced to?)

$t_{su} = t_{G1} + t_{G3} + t_{G5} + t_{G4}$

$t_{hold} = \max(t_{G2}, t_{G3})$