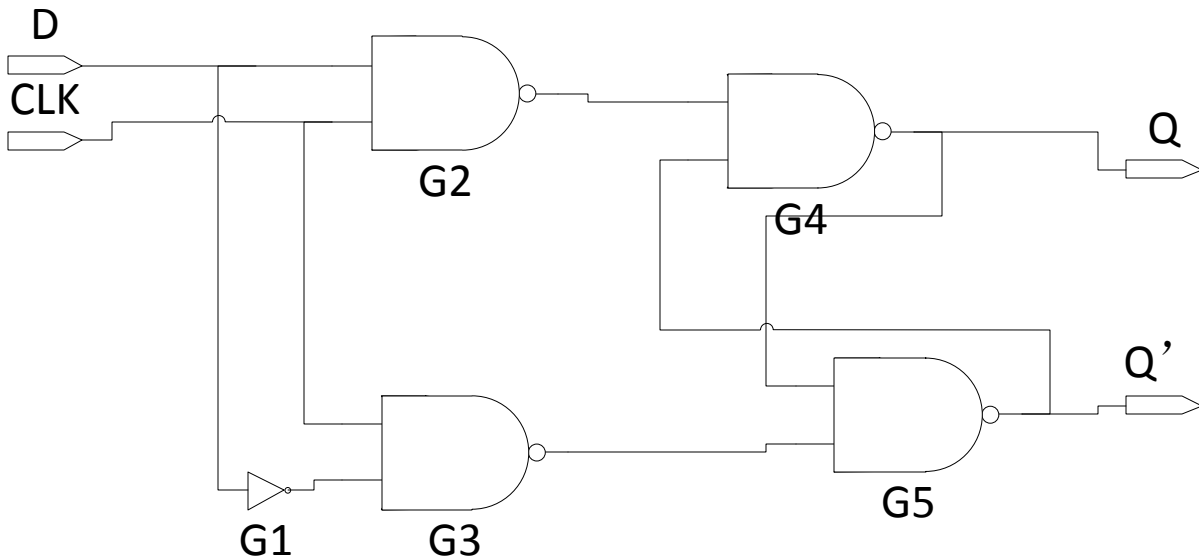


# HW10



Q1, The circuit diagram above is a D-FF, analysis the circuit and draw its symbol, the symbol must illustrate correctly the triggering mechanism and its polarity.

Q2, Use the same D-FF, Determine its setup time, hold time, and FF delay in terms of gate delays (i.e.,  $t_{G1}$ ,  $t_{G2}$ , ...). Draw the time diagram. (Hint, ask yourself which time point on the clock signal should the setup time and hold time be referenced to?)