EE451
Homework - #11

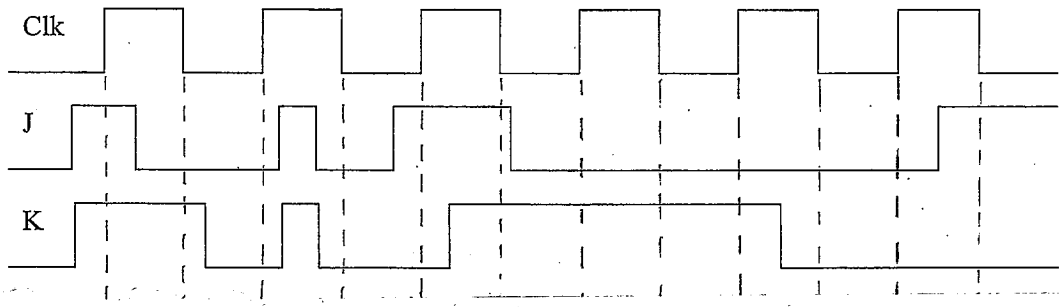
Q1. The basic functionality of a D flip-flop (FF) can be implemented with a J-K FF by connecting the input D to J and D' to K.

a) Show that this is true by comparing the characteristic equations for a D FF and JK FF.
b) Draw a timing diagram for clock, D and outputs Qp, Qn, Qms that illustrates the difference in input/output behavior of a positive edge triggered D FF, negative edge triggered D FF and a master slave D FF (implemented from a JK master-slave FF). Include some transitions on D while the clock is asserted.

Q2. Given the input and clock transitions (in the figure below), draw the waveforms for the output of a JK FF assuming;

a) it is a master-slave FF
b) it is a positive edge triggered FF
c) it is a negative edge triggered FF

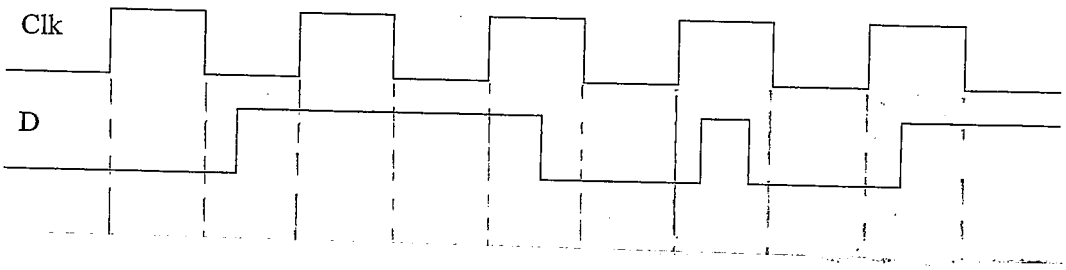
You may assume 0 setup, hold and propagation times and the initial state of the FF is 0.



Q3. Given the input and clock transitions (in the figure below), draw the waveforms for the output of a D device assuming;

a) it is a negative edge triggered FF
b) it is a master-slave FF
c) it is a positive edge triggered FF
d) it is a clocked latch

You may assume 0 setup, hold and propagation times.



Q4. Match the following five circuit diagrams with the phrase that best describes it from the following list:

1) clocked RS latch
2) clocked D latch
3) master-slave RS FF
4) +ve edge trig RS FF
5) –ve edge trig RS FF
6) master-slave D FF
7) +ve edge trig D FF
8) +ve edge trig D FF
9) master-slave T FF
10) +ve edge trig T FF
11) –ve edge trig T FF
12) master-slave JK FF
13) +ve edge trig JK FF
14) –ve edge trig JK FF