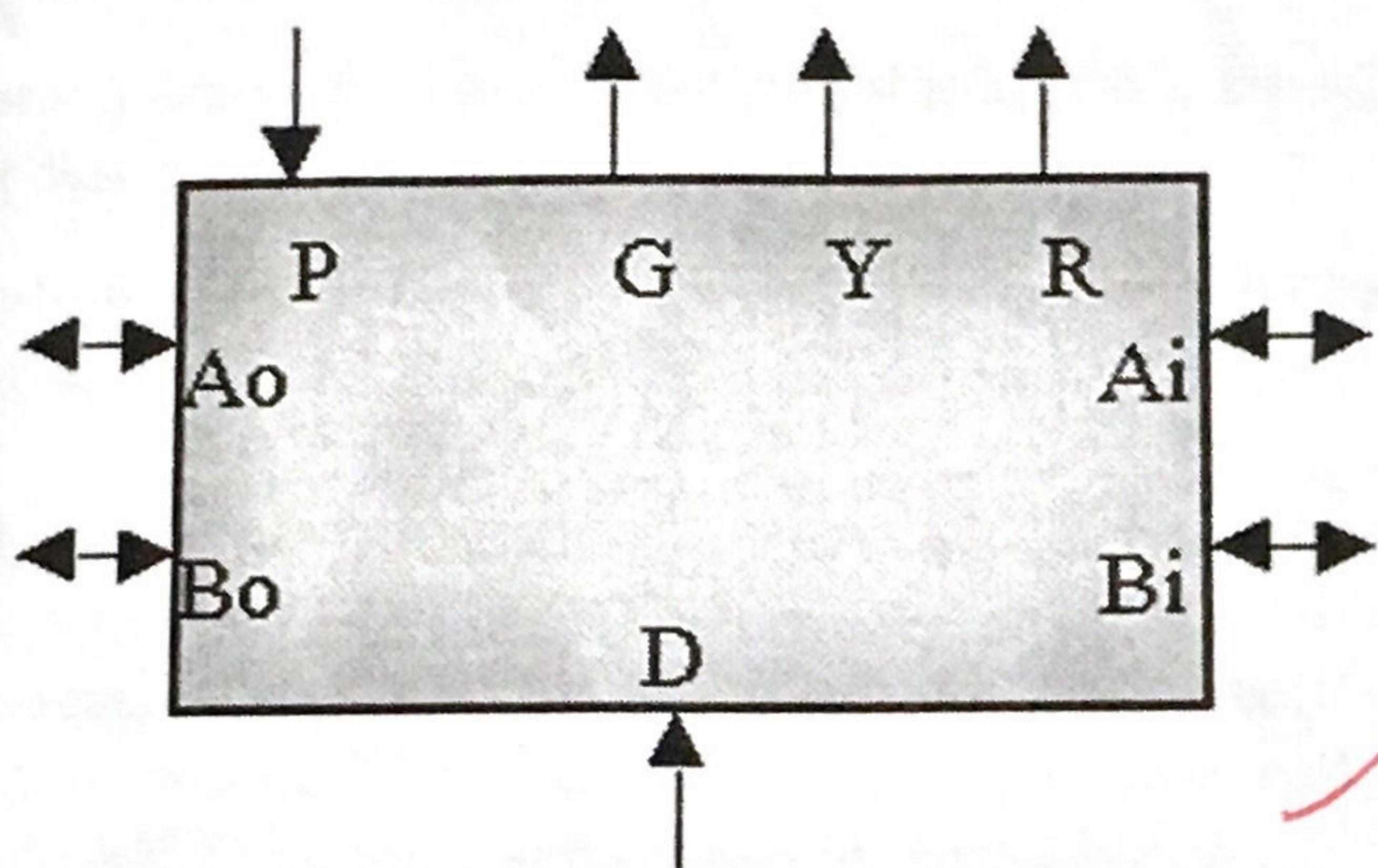


Lab Report 3

100

Goal: The objective of this lab was to design a control logic block for a subway station using Cadence.

Function: Each section of tracks in a subway station has a sensor to determine whether there is a train in that section and a signal with red, yellow, and green lights. We want the light in the track section to show red if there is a train in the track section in the very next station in the direction the train is traveling, yellow if there is no train in the track section in the very next station but the section after that is occupied, and green otherwise. We need to design a control module shown below:



Tracks allow trains move both ways from left to right and vice versa. The input D indicates the direction allowed at the time. When it is 1, the left-to-right direction is allowed; when it is 0, the right-to-left direction is allowed. The outputs G, Y, and R should be 1 to light the green, yellow, and red signals, respectively. The input P is 1 if there is a train in this section (subway station). The signals Ai, Bi, Ao and Bo are signal used to communicate from/to the station to the right and from/to the station to the left. The signals Ai and Bi are received/sent from/to the section to the right of the station, and signals Ao and Bo are received/sent from/to the section to the left of the station.

Inputs: Ai, Bi, Ao, Bo: Inputs from the neighboring subway stations.
P: Sensor input to indicate existence of a train on the track.
D: Track direction input.

Outputs: G, Y, R: Light control signals for green, yellow, and red lights, respectively.
Ai, Bi, Ao, Bo: Output signals for the neighboring stations.

Steps:

- Made truth table and logic design for the station controller and signal lights shown in the pre-lab attached behind.
- Started making a schematic for a subway station controller in cadence.
- Ai, Bi, Ao, Bo, are the I/O pins. D and P are the input pins and G, Y, R are the output pins.

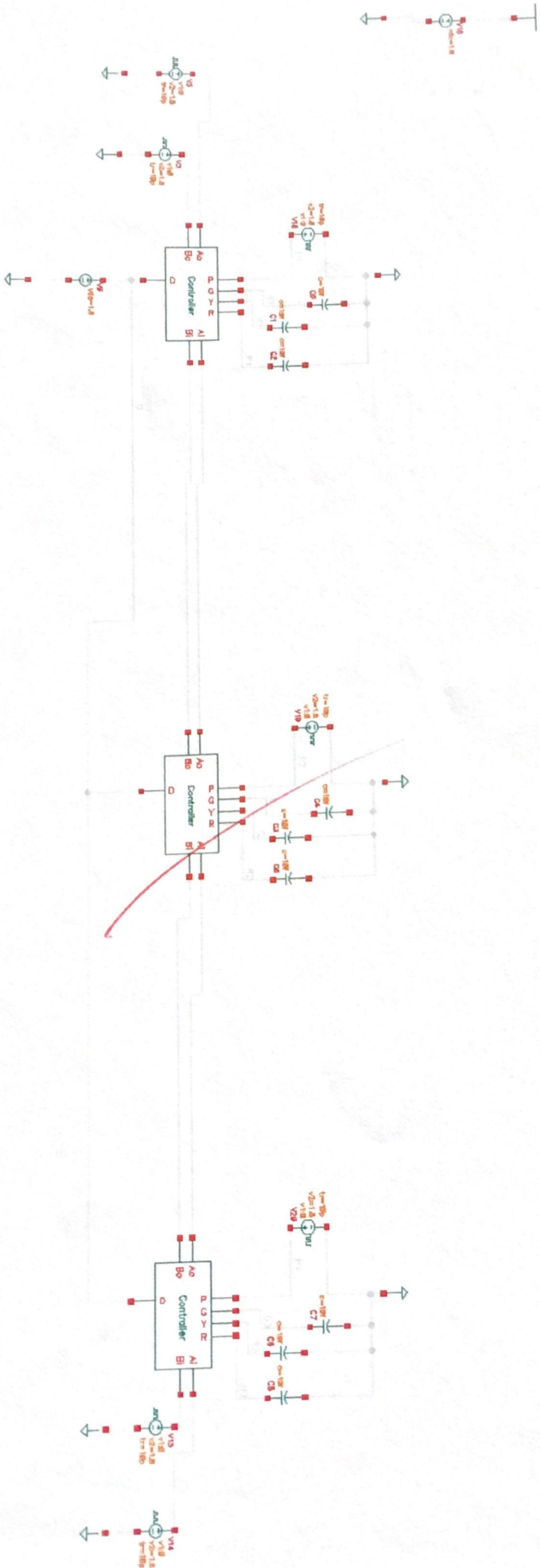
4. Since we only have two wires we need tri-state buffers which are enabled by D which is the direction pin and it guides the direction of flow of information and also states when Ai, Bi, Ao, Bo act as input or output ports.
5. P is basically a sensor which give the position of the train at a particular station. It is given as a input to tri-state buffers and according to D, the direction of flow P is decided i.e. whether it goes to Ai or Ao.
6. Finally, 3 instances of such station controllers are cascaded and simulated and the output is displayed on the graph which is attached below.


Conclusion: A subway design controller was made which guides the path of the train and tell that whether there is a train at the next station or a station after that. During this lab we came across static zero and static one timing hazards. Basically static hazards are timing hazards in which if one input changes, the output changes momentarily before it stabilizes to its correct value.

Static-1 hazard: In this, if the output is 1, and if the input changes the output goes to zero for a short time and then again settles on 1.

Static-0 hazard: In this, if the output is 0, and if the input changes the output shows a positive spike i.e. it goes to one momentarily before settling down to 0.


These hazards are usually due to NOT gate and to avoid this we can insert another (additional) delay to the circuit. This then eliminates the static hazard or eliminate the hazard by inserting more logic to counteract the effects. In other words, glitches happen when a changing input spans separate K-map encirclements. The solution to this is to add redundant K-map encirclements to ensure that all single-bit changes are covered by same block. To eliminate static-1 hazard use SOP form and to avoid static-0 hazard use POS form. But adding extra circuitry increases the cost and size of the circuit while removing the errors. Hence it is basically a trade-off between performance and cost and size of the circuit.






Transient Response

D = 0 Right to Left

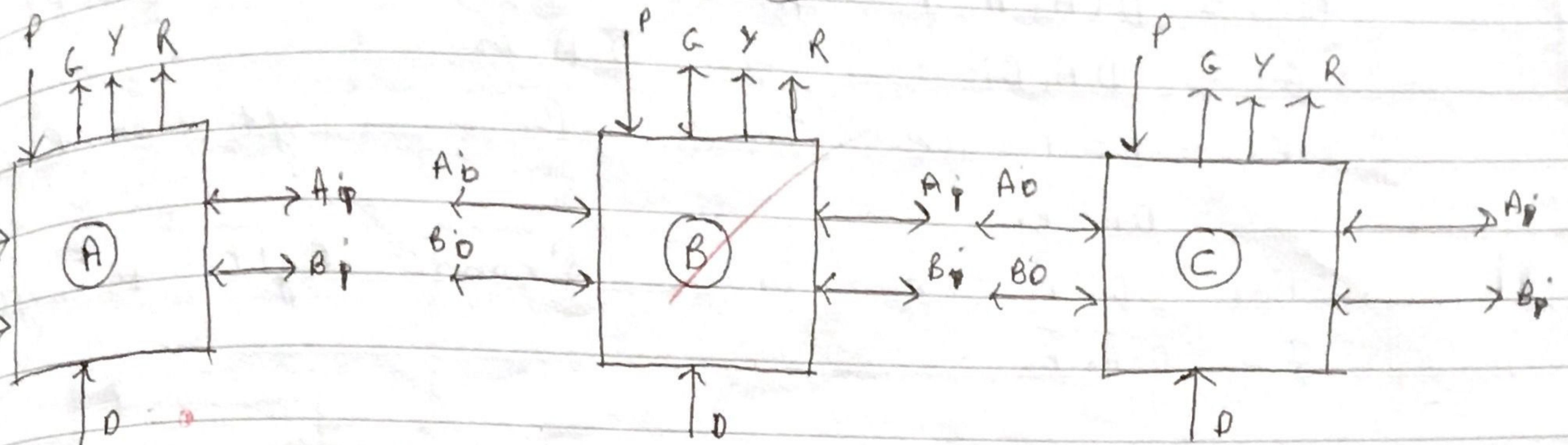


Transient Response

$D=1$ Left to Right



Pre Lab 3



$D = 1$ (Right to Left) (Left to Right)

Inputs			Outputs						
A_{i1}	B_{i1}	P	G	Y	R	A_{o1}	B_{o1}		
0	0	0	1	0	0	0	0		
0	1	0	0	1	0	0	0		
1	0	0	0	0	1	0	*		
1	1	0	0	0	1	0	*		
0	0	1	1	0	0	*	*		
0	1	1	0	1	0	*	*		
1	0	1	0	0	1	*	*		
1	1	1	0	0	1	*	*		

$D = 0$ (Right to Left)

Inputs			Outputs						
A_{i1}	B_{i1}	P	G	Y	R	A_{o1}	B_{o1}		
0	0	0	1	0	0	0	*		
0	1	0	0	1	0	0	*		
1	0	0	0	0	1	0	*		
1	1	0	0	0	1	0	*		
0	0	1	1	0	0	*	*		
0	1	1	0	1	0	*	*		
1	0	1	0	0	1	*	*		
1	1	1	0	0	1	*	*		

$$G = D(\bar{A}; \bar{B}_i \bar{P} + \bar{A}_i \bar{B}_i P) + \bar{D}(\bar{A}_o \bar{B}_o \bar{P} + \bar{A}_o \bar{B}_o P)$$

$$\therefore G = D\bar{A}; \bar{B}_i + \bar{D}\bar{A}_o \bar{B}_o$$

\therefore For $D=1$ i.e. Train from Left to Right

$$G = D\bar{A}; \bar{B}_i$$

\therefore For $D=0$ i.e. Train from Right to Left

$$G = \bar{D}\bar{A}_o \bar{B}_o$$

$$Y = D(\bar{A}; \bar{B}_i \bar{P} + \bar{A}_i B_i P) + \bar{D}(\bar{A}_o B_o \bar{P} + \bar{A}_o B_o P)$$

$$\therefore Y = D\bar{A}; B_i + \bar{D}\bar{A}_o B_o$$

\therefore For $D=1$ i.e. Train from Left to Right

$$Y = D\bar{A}; B_i$$

\therefore For $D=0$ i.e. Train from Right to Left

$$Y = \bar{D}\bar{A}_o B_o$$

$$R = D(A; \bar{B}_i \bar{P} + A_i \bar{B}_i P + A_i B_i \bar{P} + A_i B_i P) + \bar{D}(A_o \bar{B}_o \bar{P} + A_o \bar{B}_o P + A_o B_o \bar{P} + A_o B_o P)$$

$$\therefore R = DA_i + \bar{D}A_o$$

\therefore For $D=1$ i.e. Train from Left to Right

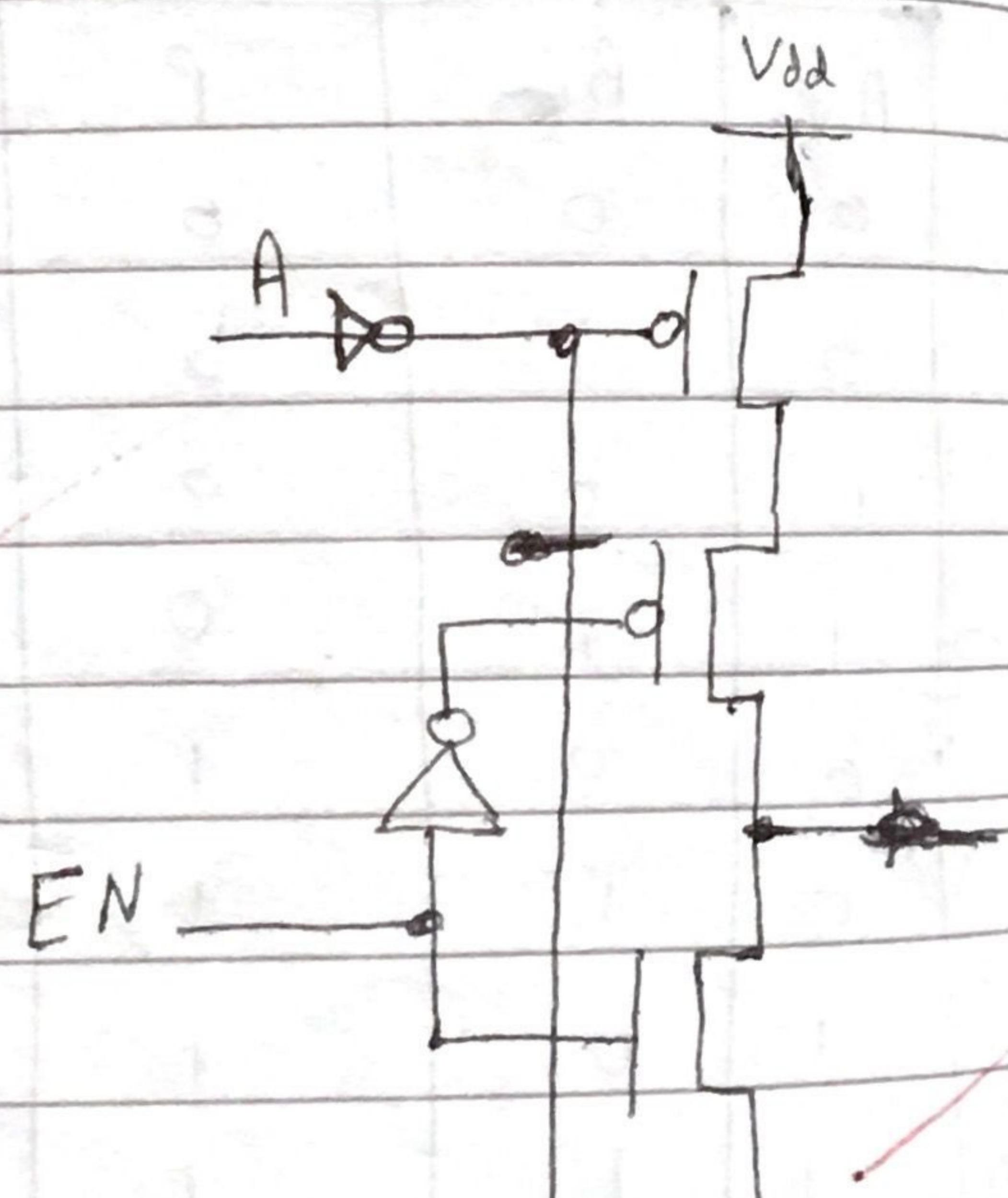
$$R = DA_i$$

\therefore For $D=0$ i.e. Train from Right to Left

$$R = \bar{D}A_o$$

* Tri-state Buffer Truth Table.

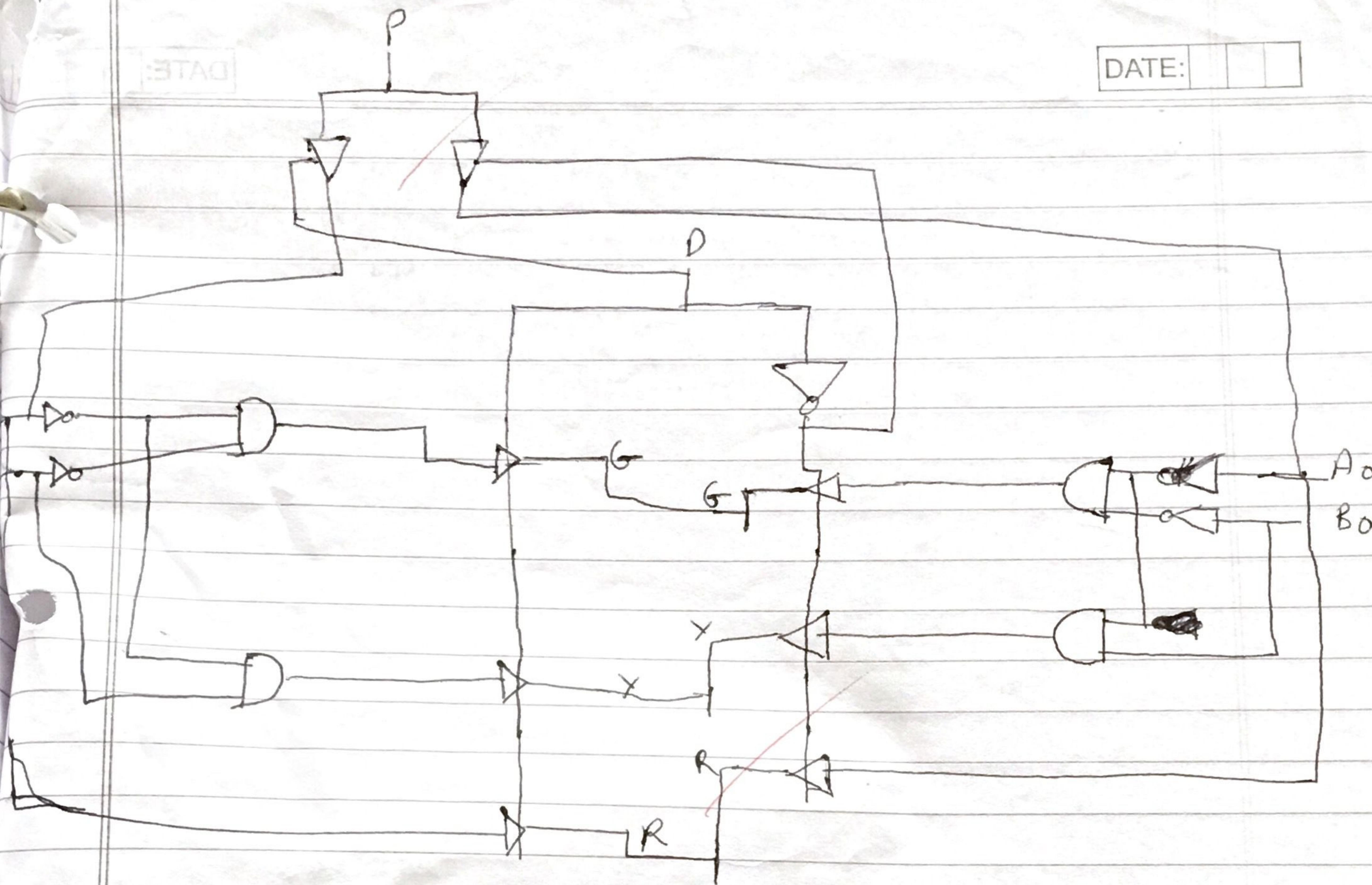
Enable	I/P	O/P
0	0	Z
0	1	Z
1	0	0
1	1	1



Non-Inverting Tristate
Buffer
(Active High)

DATE:

DATE: _____



subway station schematic

~~BB~~ 9/28/16