Lab Report 1

- **Goal:** The goal of this lab project was to design a 3-bit ALU using Cadence. The purpose of this ALU was to perform 4 functions viz. Addition, Subtraction, Ex-OR, Left Shift.

- **Steps:** To achieve this goal, we started by making a pre-lab (attached behind), which included Truth Table of 1-bit ALU, which we simplified to get logic equation using Karnaugh's Map. The 1-bit ALU that I designed had 2 function select inputs fun_sel0 and fun_sel1. According to the inputs values to these ports, the function of ALU would be selected. In my case 00 corresponds to Addition, 01 to Subtraction, 10- Ex-OR and 11 to Left Shift. The 3 input bits to the ALU were c_{in}, a, b and the output bits were S, C_{out}. According to the simplified equation the Gate Level Schematic was built to carry out the functions of ALU.
  To perform this experiment in Cadence, we used divide and conquer approach. We divided the circuit into parts, developed the circuits in those parts and ultimately combined to get the result of 3 bit ALU. We started off by making logic gates viz. AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. Using these gates, we made 1-bit ALU, and then by using these 1-bit ALU slices we built a circuit for 3-bit ALU which contained 15 inputs and 6 outputs.

- **Conclusion:** This Lab made me familiar with Linux environment and how to use Cadence for making hardware design. Basically it thought me a hierarchal approach towards designing the hardware. This Lab answered an important question that what is Hierarchal design method and what are its benefits?

  - In Practical or industrial hardware design, we deal with millions of transistors and gates. So if there is any error in one particular part while designing, it makes nearly impossible to debug it and almost months of your work is wasted. To avoid this, we design systems in hierarchal manner i.e. we divide the systems into many small parts so debugging becomes easy and we can build a circuit in a more efficient manner.
  - The benefits of hierarchal design are:
    1. Reduces circuit complexity, such as in our lab, instead of using transistors for making the 1-bit ALU, we first made logic gates using the transistors, and then using these logic gates to make 1-bit ALU, using which we ultimately made 3-bit ALU. By using this approach, it certainly reduced the circuit complexity to a great extent.
    2. Also using hierarchal design approach, we are able to reuse the design. In our case we made logic gates design which we used 1-bit ALU and then using these 1-bit ALU we implemented a 3-bit ALU, which was the goal of this Lab.