Lab Report 6

Goal: The objective of this lab is to learn simple sequential logic circuit design. The circuit we designed is a 3-bit grey code counter using D-FFs. The counting sequence for grey code is 000, 001, 011, 010, 110, 111, 101, 100. Use D-FFs to implement the counter.

Specifications:

Inputs: Clock signal, D input of the FF

Outputs: 3bit Grey code outputs

Steps: (Refer prelab)

1. Designed a D-FF using universal logic gates,

1. Designed a state transition table for the grey code counter.

2. Made state transition table and truth table.

3. Designed a combinational logic circuit for D-input of the FF using the truth table and Boolean equations.

4. Provided the clock input to the FF and simulated the circuit in Cadence.

Conclusion:

This lab thought us how to design sequential logic circuit. It gave us the brief overview of what is finite state machine? What are the advantages of using FSM? How to design a Finite State Machine?

Questions:

1. What is Moore Finite State Machine (FSM)?

-> A Moore FSM's is a state machine whose outputs depends only on the present state. It consists of 6 parameters:

1. Finite set of states (S)

2. Start state (S_0)

3. Input alphabets (∑)

4. Output alphabets (π)

5. Transition Function (T): S*∑ -> S

6. An Output function (G): S -> π

2. What is Mealy FSM?

-> A Mealy FSM's is a state machine whose outputs depends on both its present state and present inputs. It consists of 6 parameters:

1. Finite set of states (S)

2. Start state (S_0)

3. Input alphabets (∑)

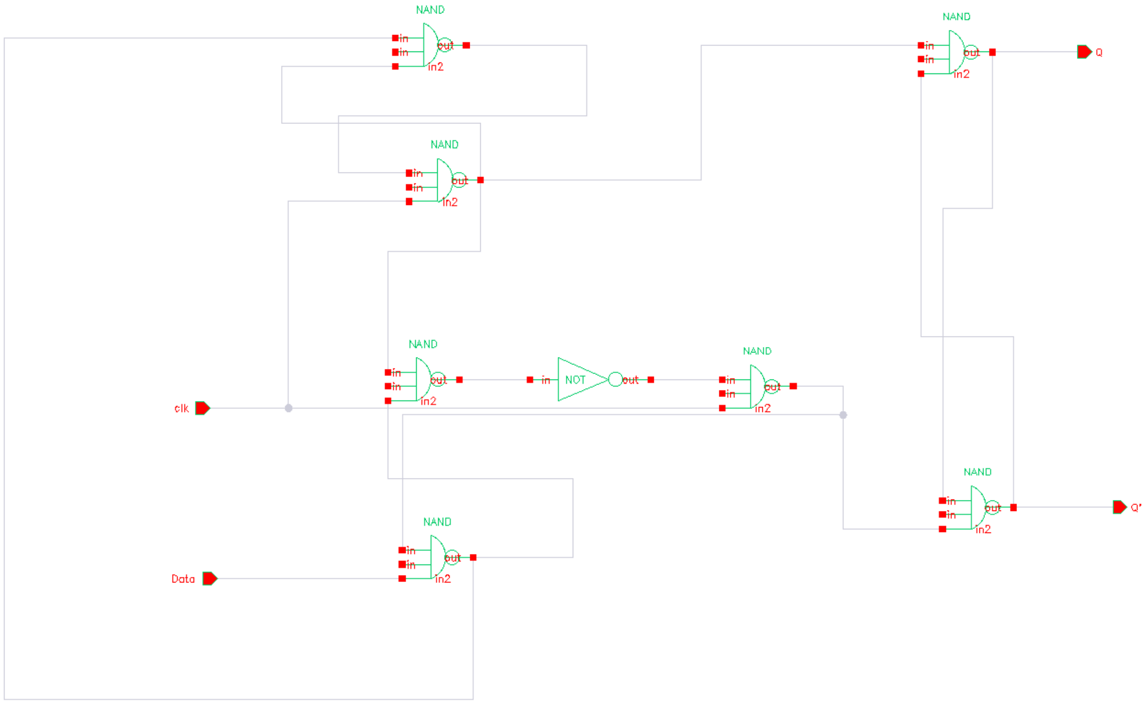
4. Output alphabets (π)

5. Transition Function (T): S*∑ -> S

6. An Output function (G): S -> π

Comparison:

A Mealy FSM has fewer number of states and hence is faster but it is not as reliable as Moore. Mealy reacts faster to inputs as compared to Moore. In fact, the output of Mealy changes as soon there is change in the input but the output of Moore changes when there is an edge triggered depending whether it's a positive edge trigger or negative edge triggered.


NAND
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in
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NAND
in
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in2
NAND
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in
out
in2
Q
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in
in
out
in2
in
NOT
out
NAND
in
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clk
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Q'
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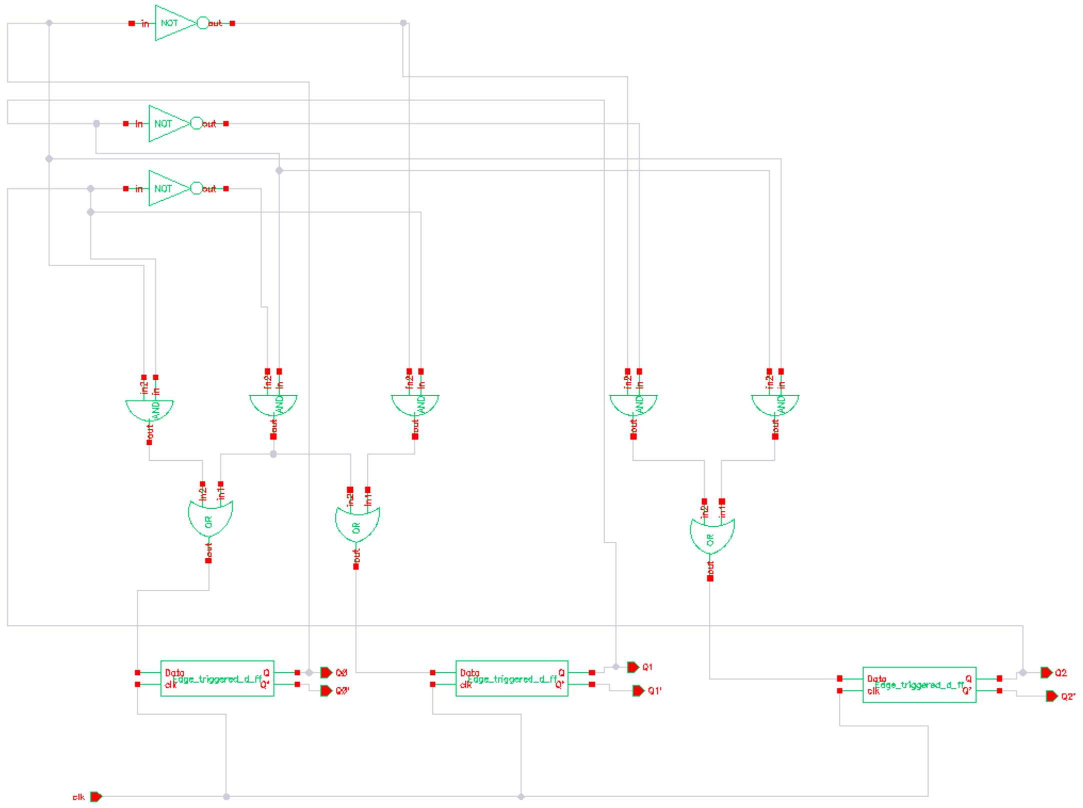
in2
Data


in
NOT
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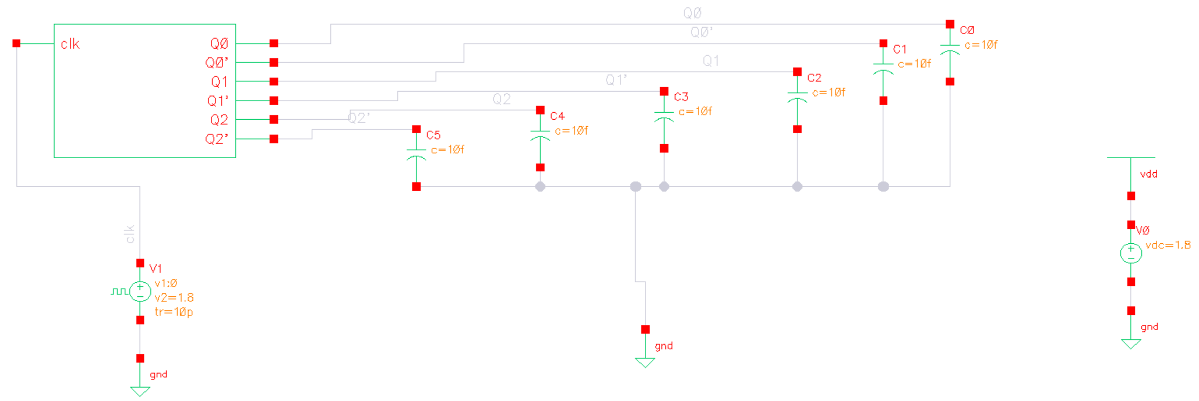
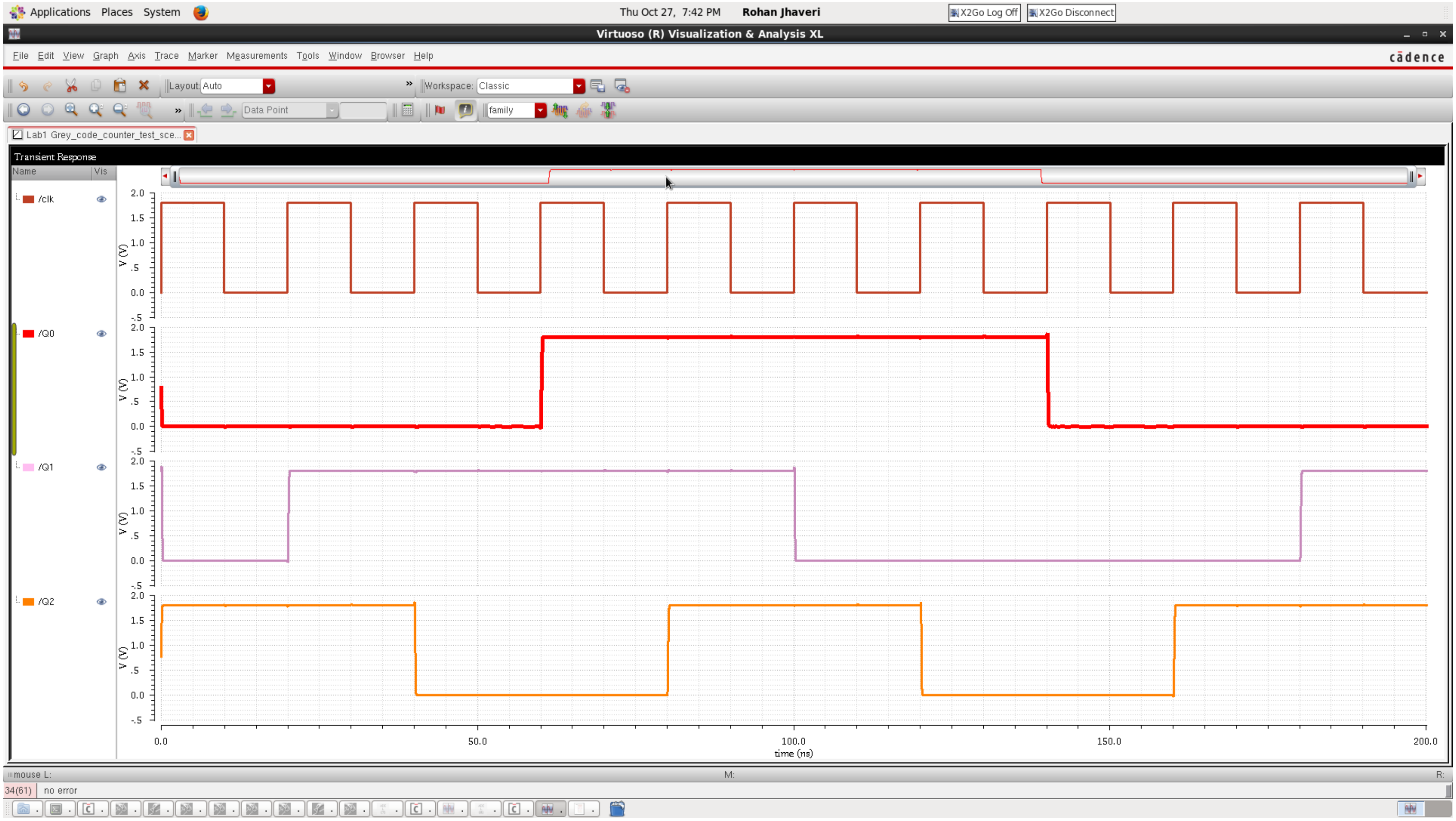
AND
out
in2
in1
OR
out
in2
in1
OR
out
in2
in1
OR
out
Data
clk
Edge_triggered_d_ff
Q
Q'
Q0
Q0'
Data
clk
Edge_triggered_d_ff
Q
Q'
Q1
Q1'
Data
clk
Edge_triggered_d_ff
Q
Q'
Q2
Q2'
clk



clk
QØ
QØ'
Q1
Q1'
Q2
Q2'
QØ
QØ'
Q1
Q1'
Q2
Q2'
CØ
c=1Øf
C1
c=1Øf
C2
c=1Øf
C3
c=1Øf
C4
c=1Øf
C5
c=1Øf
clk
V1
v1:Ø
v2=1.8
tr=1Øp
gnd
gnd
vdd
VØ
vdc=1.8
gnd



Virtuoso (R) Visualization & Analysis XL

Thu Oct 27, 7:42 PM Rohan Jhaveri

Layout: Auto

Workspace: Classic

Lab1 Grey_code_counter_test_sce...

Transient Response

34(61) no error